Microchip

27LV256

256K (32K x 8) Low-Voltage CMOS EPROM

FEATURES

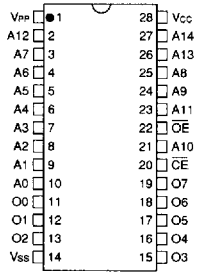
- Wide voltage range 3.0V to 5.5V
- High speed performance
  —200ns access time available at 3.0V
- CMOS Technology for low power consumption
  —8mA Active current at 3.0V
  —20mA Active current at 5.5V
  —100µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- High speed "Express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  —28-pin Dual-in-line package
  —32-pin PLCC package
  —28-pin SOIC package
  —28-pin TSOP package
  —Tape and reel
- Available for the following temperature ranges:
  —Commercial: 0° C to 70° C
  —Industrial: -40° C to 85° C

DESCRIPTION

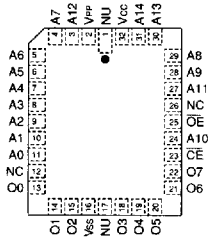
The Microchip Technology Inc. 27LV256 is a low-voltage (3.0 volt) CMOS EPROM designed for battery powered applications. The device is organized as a 32K x 8 (32K-Byte) non-volatile memory product. The 27LV256 consumes only 8mA maximum of active current during a 3.0 volt read operation, thereby improving battery performance. This device is designed for very low-voltage applications where conventional 5.0 volt only EPROMS can not be used. Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 200ns at 3.0 volts. This device allows systems designers the ability to use low voltage non-volatile memory with today's low-voltage microprocessors and peripherals in battery powered applications.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

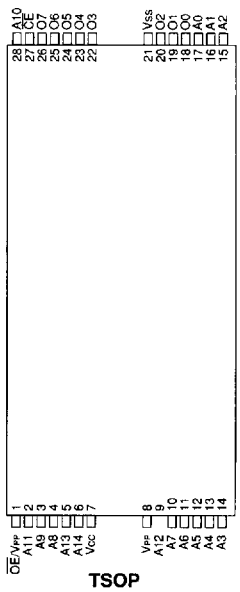
PIN CONFIGURATIONS
Top View



DIP/SOIC



PLCC/LCC



TSOP

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PIN FUNCTION TABLE	
Name	**Function**
A0 - A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V or +3V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14.0V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC + 1.0V
Storage temperature ..... -65° C to 150° C
Ambient temp. with power applied ..... -65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = 3.0V to 5.0V unless otherwise specified
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage	all		ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb= 25° C; f = 1MHz
Power Supply Current, Active	C I	TTL input TTL input	ICC1 ICC2		20 @ 5.0V 8 @ 3.0V 25 @ 5.0V 10 @ 3.0V	mA mA mA mA	VCC = 5.5V; VPP = VCC; f = 1MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I all	TTL input TTL input CMOS input	ICC(S)		1 @ 3.0V 2 @ 3.0V 100 @ 3.0V	mA mA µA	 $\overline{CE}$ = VCC ±0.2V

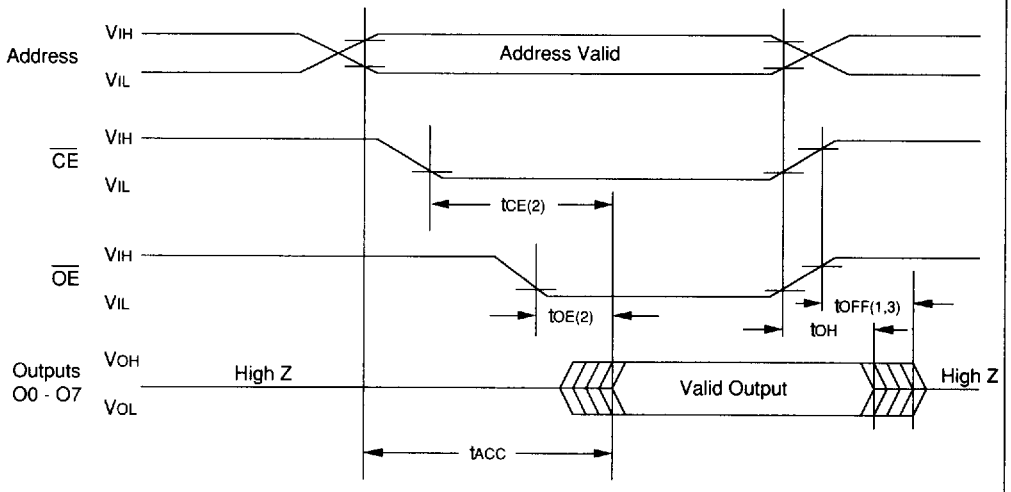
* Parts: C = Commercial Temperature Range; I = Industrial Temperature Range
Notes: (1) Active current increases 5 mA per MHz up to operating frequency for all temperature ranges.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C

Parameter	Sym	27LV256-20		27LV256-25		27LV256-30		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC		200		250		300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE		200		250		300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE		100		125		125	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	50	0	50	0	50	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	tOH	0		0		0		ns	

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

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PROGRAMMING
DC Characteristics

Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400µA I_{OL} = 2.1mA
V_{CC} Current, program & verify		I_{CC2}		20	mA	Note 1
V_{PP} Current, program		I_{PP2}		25	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

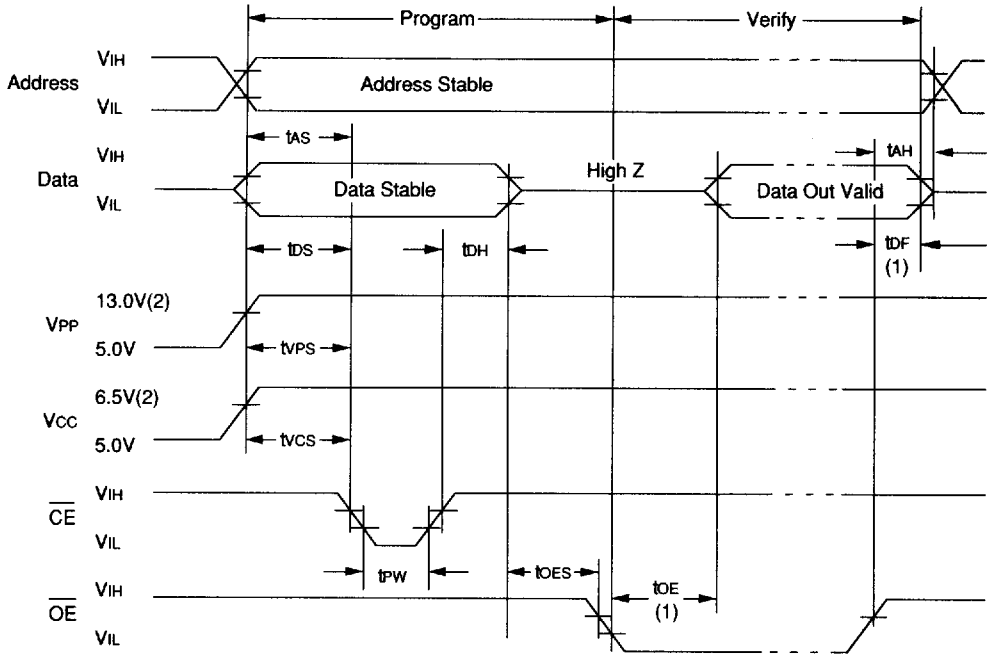
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4 V and V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V
Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100µsec ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5 V ±0.25 V, VPP = VH = 13.0 V ±0.25 V for express algorithm

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

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Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high.

Programming Mode

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to proper voltage,
b) V_{PP} is brought to proper V_H level,
c) The $\overline{OE}$ pin is high and
d) the $\overline{CE}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low-going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) The $\overline{CE}$ pin is high and
d) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data, although address and data will be available on their input pins.

Identity Mode

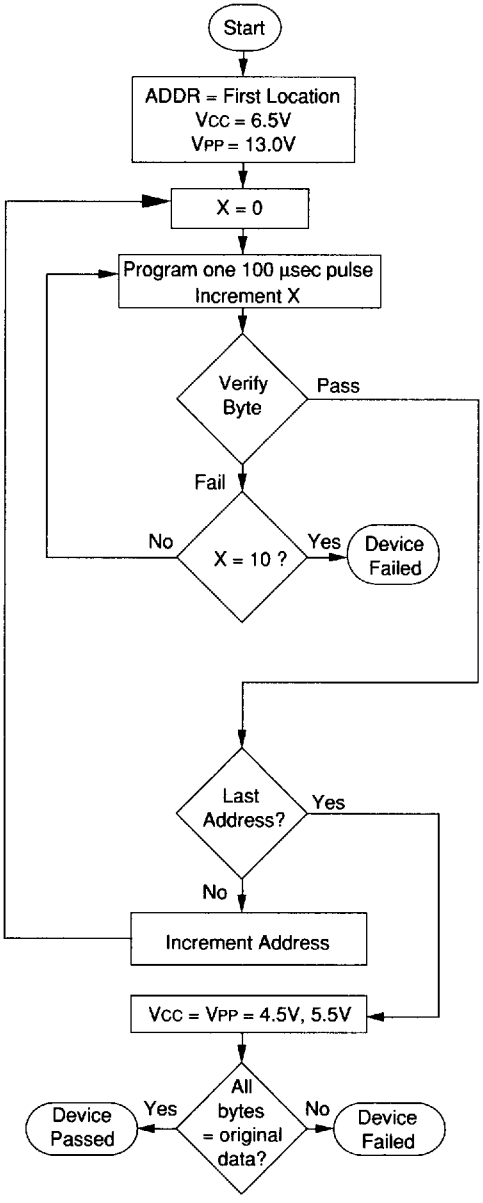
In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access either of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	0	1	1	0	0	8C

* Code subject to change.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27LV256 - 25 I / P

Package:	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	J	Ceramic DIP
	K	Ceramic Leadless Chip Carrier
	TS	Plastic Thin Small Outline (TSOP)
Temperature Range:	-	0° C to 70° C
	I	-40° C to 85° C
Access Time:	20	200 nsec
	25	250 nsec
	30	300 nsec
Device:	27LV256	256K (32K x 8) Low Voltage CMOS EPROM