Revision History

- Jan 11 , 2000

  Rev - B Added More Detailed Dimension Information Of PCB , Full Data sheet Changed to new format.

- May 05 , 1999

  Rev - A Datasheet released.

128M Bytes (16M x 72) DRAM 168Pin DIMM With ECC based on 16M x 4

General Description

The UG516W724(8)4HK(S)G is a 16,7774,216 bits by 72 EDO DRAM module with ECC . The UG516W724(8)4HK(S)G is assembled using 18 pcs of 16Mx4 4K\8K refresh DRAMs in 32-pin SOJ/TSOP package,and 2 pcs ABT163244 buffers in 240mil package mounted on a 168-pin buffered printed circuit board.

Features

- Single 3.3 +/- 0.3V power supply
- Extended data out mode
- CAS-before-RAS Refresh capability
- RAS-only and Hidden Refresh capability
- 4096 \ 8192 refresh cycles every 64 \ 128 ms
- 12/12 \ 13/11 Addressing (Row / Column)
- LVTTL compatible inputs and output
- Buffered input except RAS and DQ
- New JEDEC standard pinout & Buffered PDpin
- PCB:Height (1250mil),double sided component

Pin Assignment

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	OE2	86	DQ36	128	NC
3	DQ1	45	RAS2	87	DQ37	129	RAS3
4	DQ2	46	CAS4	88	DQ38	130	CAS5
5	DQ3	47	NC	89	DQ39	131	NC
6	VCC	48	WE2	90	VCC	132	PDE
7	DQ4	49	VCC	91	DQ40	133	VCC
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	VCC	101	DQ49	143	VCC
18	VCC	60	DQ24	102	VCC	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	NC	106	DQ53	148	NC
23	VSS	65	DQ25	107	VSS	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	VCC	68	VSS	110	VCC	152	VSS
27	WE0	69	DQ28	111	NC	153	DQ64
28	CAS0	70	DQ29	112	CAS1	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ66
30	RAS0	72	DQ31	114	RAS1	156	DQ67
31	OE0	73	VCC	115	NC	157	VCC
32	VSS	74	DQ32	116	VSS	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	A12	81	PD5	123	NC	165	PD6
40	VCC	82	PD7	124	VCC	166	PD8
41	NC	83	ID0	125	NC	167	ID1
42	NC	84	VCC	126	B0	168	VCC

Absolute Maximum Ratings

• Voltage Relative to GND	-1.0 to +4.6 V
• Operating Temperature	0 to +70°C
• Storage Temperature	-55° to +150°C
• Short-circuit Output Current	50mA
• Power Dissipation	18.0 W

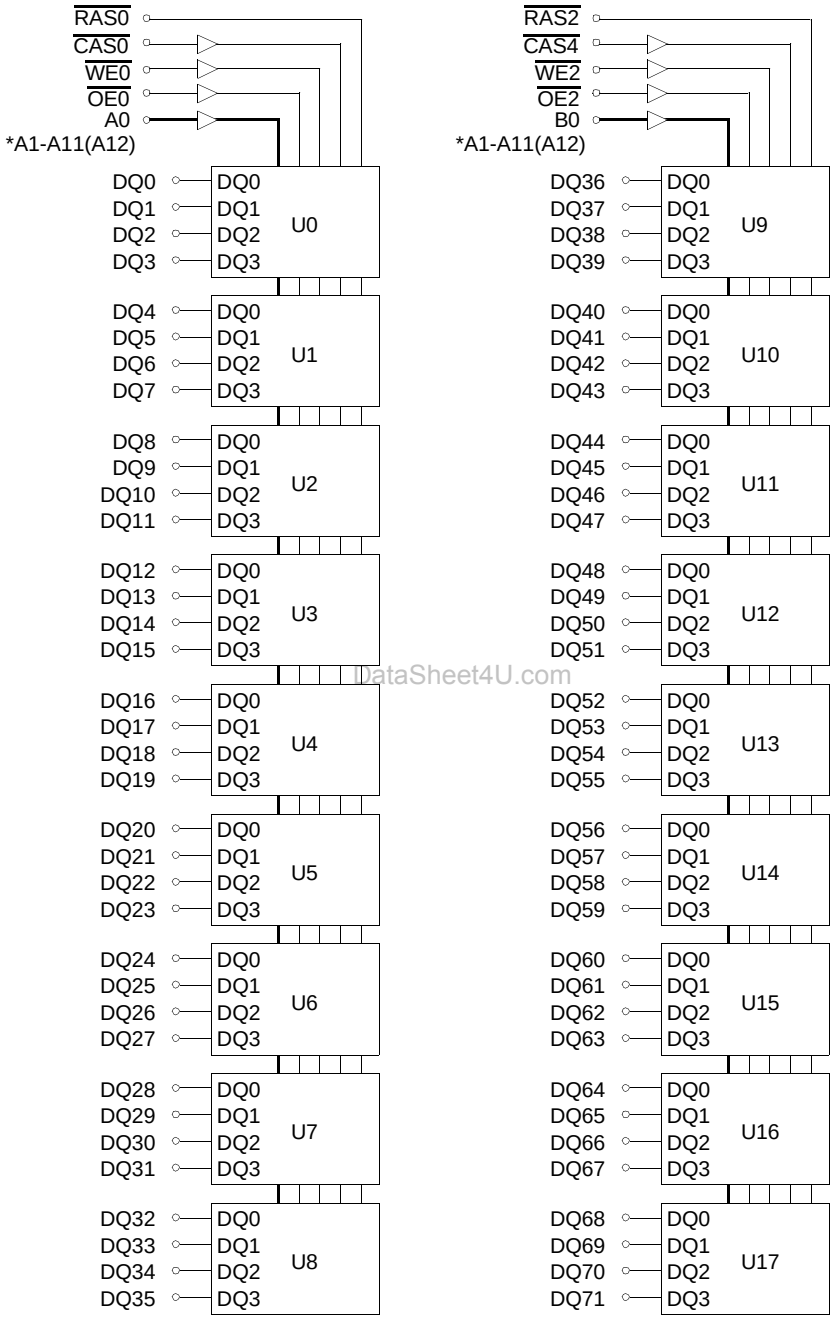
Part Identification

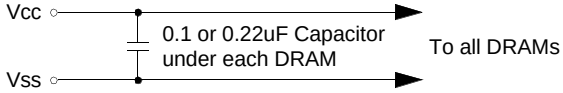
Part number	Packages	Ref.cycle
UG516W7244HKG	SOJ	4K
UG516W7244HSG	TSOP	4K
UG516W7284HKG	SOJ	8K
UG516W7284HSG	TSOP	8K

Pin Names

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref)
A0, B0, A1 - A12	Address Input(8K ref)
DQ0 - DQ71	Data In/Out
WE0 , WE2	Read/Write Enable
OE0, OE2	Output Enable
RAS0 ~ RAS3	Row Address Strobe
CAS0, 1,4,5	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
PDE	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 , 1	ID bit

Functional Block Diagram

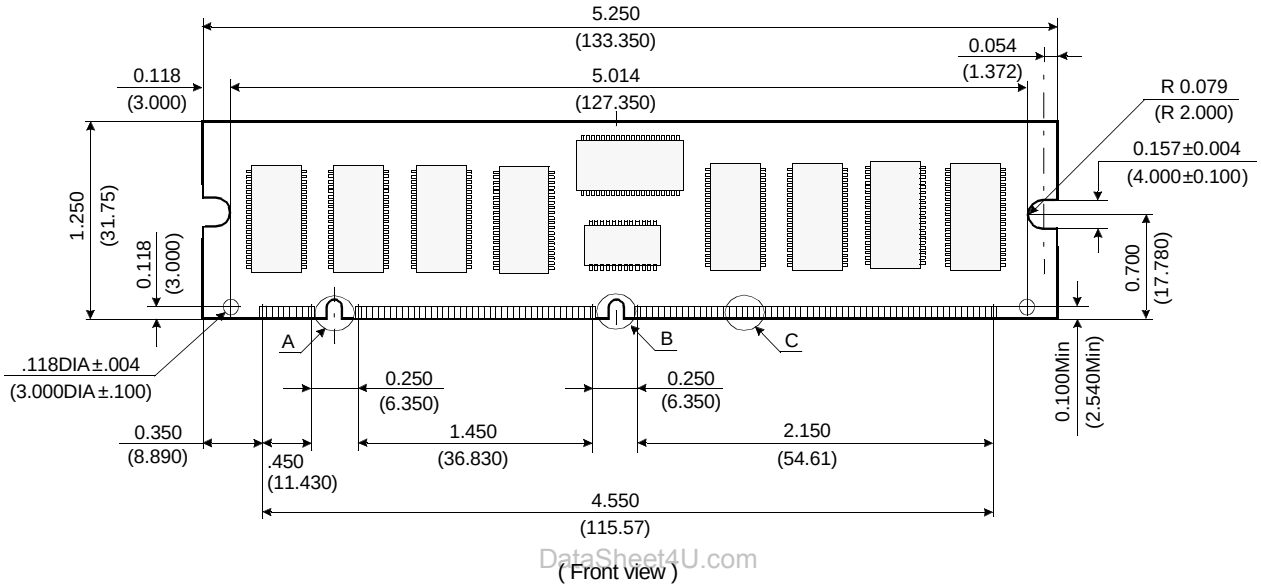




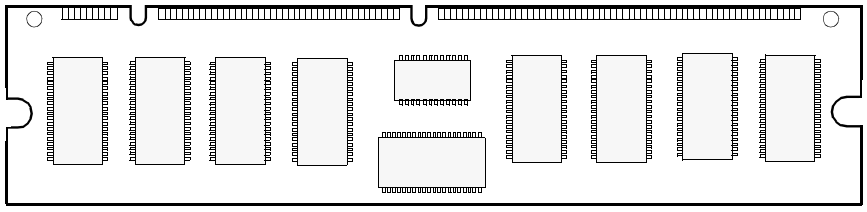
*A12 is used for 8K ref. only.

Physical Dimension

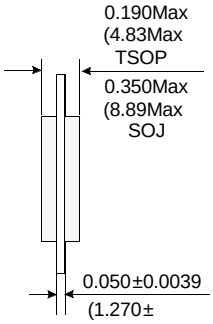
168 Pin DIMM Module

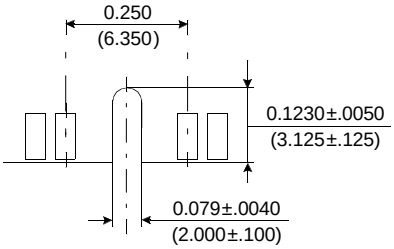


(Front view)

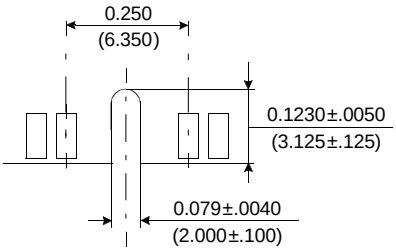


(Back view)

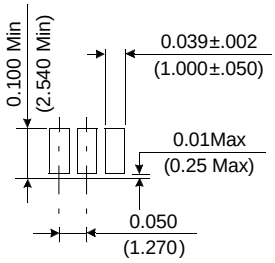




Detail A



Detail B



Detail C

Tolerances : ± .005(.13) unless otherwise specified

Units : Inches (millimeters)

The following information is based on Micron component P/N MT4C16M4H9(G3) only .

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on any pin relative V SS	VIN, VOUT	-1.0 to +4.6	V
Voltage on VCC supply relative to V SS	VCC	-1.0 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	18	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for in tended periods may affect device reliability.

Recommended Operating Conditions

(Voltage referenced to V SS, TA = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	3.0	3.3	3.6	V
Ground	VSS	0	0	0	V
Input High Voltage	VIH	2.0	-	VCC+0.3	V
Input Low Voltage	VIL	-0.3	-	0.8	V

DC And Operating Characteristics

(Recommended operating conditions unless otherwise noted)

Symbol	Speed	UG516W7284HK(S)G		UG516W7244HK(S)G		Unit
		Min	Max	Min	Max	
ICC1	-5	-	2080	-	2720	mA
	-6	-	1920	-	2560	mA
ICC2	ALL	-	16	-	16	mA
ICC3	-5	-	2400	-	2400	mA
	-6	-	1920	-	1920	mA
ICC4	-5	-	2080	-	2720	mA
	-6	-	1920	-	2560	mA
ICC5	ALL	-	8	-	8	mA
ICC6	-5	-	2560	-	2560	mA
	-6	-	2400	-	2400	mA
II(L)	ALL	-36	36	-36	36	uA
IO(L)		-5	5	-5	5	uA
VOH	ALL	2.4	-	2.4	-	V
VOL		-	0.4	-	0.4	V

ICC1 : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @ tRC=min)

ICC2 : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=VIH)

ICC3 : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=VIH, $\overline{RAS}$ cycling @tRC=min)

ICC4 : Extended Data Out Mode Current * ($\overline{RAS}$=VIL, $\overline{CAS}$ cycling : tHPC=min)

ICC5 : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=VCC-0.2V)

ICC6 : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min)

I(IL) : Input Leakage Current (Any input 0 ≤ VIN ≤VCC+0.3V, all other pins not under test=0 V)

I(OL) : Output Leakage Current(Data Out is disabled, 0V ≤ VOUT ≤VCC)

VOH : Output High Voltage Level (I OH = -2mA)

VOL : Output Low Voltage Level (I OL = 2mA)

* NOTE : ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In I CC1 and ICC3, address can be changed maximum once while $\overline{RAS}$=VIL. In ICC4, address can be changed maximum once within one EDO mode cycle time, tHPC.

Capacitance (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0 , A1 - A12]	C_{IN1}	-	80	pF
Input capacitance[$\overline{WE0}$,$\overline{WE2}$,$\overline{OE0}$,$\overline{OE2}$]	C_{IN2}	-	56	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	35	pF
Input capacitance[$\overline{CAS0}$,1, 4, 5]	C_{IN4}	-	35	pF
Input/Output capacitance[DQ0-DQ71]	CDQ	-	10	pF

AC Characteristics (0° ≤T_A ≤70°C, V_{CC}=3.3V ± 0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading C_L=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	116		140		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5,13
Access time from column address	t_{AA}		25		30	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3,13
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	13
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	11		14		ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	9		12		ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	13
Row address set-up time	t_{ASR}	0		0		ns	13
Row address hold time	t_{RAH}	9		10		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8,13
Write command hold time	t_{WCH}	8		10		ns	7
Write command pulse width	t_{WP}	5		5		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	13
Data set-up time	t_{DS}	0		0		ns	
Data hold time	t_{DH}	8		10		ns	9,13
Refresh period (4K)	t_{REF}		64		64	ms	9,13
Refresh period (8K)	t_{REF}		128		128	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ dealy time	t_{CWD}	28		35		ns	7
$\overline{RAS}$ to $\overline{W}$ dealy time	t_{RWD}	67		79		ns	7,13

AC Characteristics (0°C ≤ TA ≤ 70°C, VCC=3.3V±0.3V. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	42		49		ns	7
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		10		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-write cycle time	t_{HPRWC}	47		56		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	125K	60	125K	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	8		10		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		10		ns	13
$\overline{OE}$ access time	t_{OEA}		12		15	ns	13
$\overline{OE}$ to data delay	t_{OED}	15		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	12	0	15	ns	13
$\overline{OE}$ command hold time	t_{OEH}	8		10		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		10		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	10		10		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. $t_{ASC} \geq 6$ns.

13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.