SINGLE SUPPLY QUAD PECL/TTL-TO-PECL

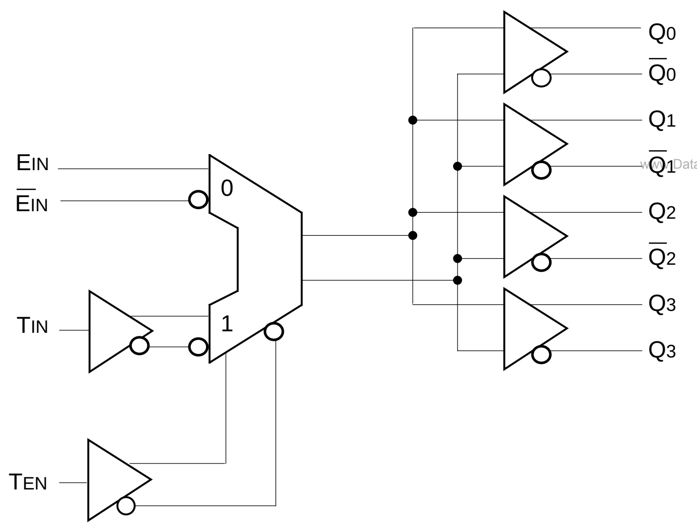
The Infinite Bandwidth Company™

ClockWorks™
SY100S815
FINAL

FEATURES

- **Quad PECL version of popular ECLinPS E111**
- **Low skew**
- **Guaranteed skew spec**
- **TTL enable input**
- **Selectable TTL or PECL clock input**
- **Single +5V supply**
- **Differential internal design**
- **PECL I/O fully compatible with industry standard**
- **Internal 75kΩ PECL input pull-down resistors**
- **Available in 16-pin SOIC package**

BLOCK DIAGRAM



PIN NAMES

Pin	Function
EIN, $\overline{\text{EIN}}$	Differential PECL Input Pair
TIN	TTL Input
TEN	TTL Input Enable
Q0, $\overline{\text{Q0}}$ – Q3, $\overline{\text{Q3}}$	Differential PECL Outputs
VCC	PECL VCC (+5.0V)
VEE	PECL Ground (0V)

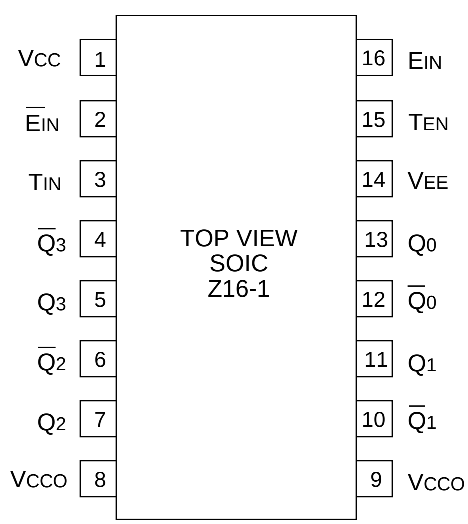
DESCRIPTION

The SY100S815 is a low skew 1-to-4 PECL differential driver designed for clock distribution in new, high-performance PECL systems. It accepts either a PECL clock input or a TTL input by using the TTL enable pin TEN. When the TTL enable pin is HIGH, the TTL input is enabled and the PECL input is disabled. When the enable pin is set LOW, the TTL input is disabled and the PECL input is enabled.

The device is specifically designed and produced for low skew. The interconnect scheme and metal layout are carefully optimized for minimal gate-to-gate skew within the device. Wafer characterization and process control ensure consistent distribution of propagation delay from lot to lot. Since the S815 shares a common set of "basic" processing with the other members of the ECLinPS family, wafer characterization at the point of device personalization allows for tighter control of parameters, including propagation delay.

To ensure that the skew specification is met, it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and, therefore, terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same VCCO as the pair(s) being used on that side) in order to maintain minimum skew.

PIN CONFIGURATION



Rev.: F Amendment: /0
Issue Date: October, 1998

TRUTH TABLE

T_{EN}	E_{IN}	T_{IN}	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = +5.0V \pm 5\%$

		$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	μA
V_{IH}	Input HIGH Voltage(1)	3.835	—	4.120	3.835	—	4.120	3.835	—	4.120	V
V_{IL}	Input LOW Voltage(1)	3.190	—	3.525	3.190	—	3.525	3.190	—	3.525	V
V_{OH}	Output HIGH Voltage(2)	V_{CC} –1025	V_{CC} –955	V_{CC} –870	V_{CC} –1025	V_{CC} –955	V_{CC} –870	V_{CC} –1025	V_{CC} –955	V_{CC} –870	mV
V_{OL}	Output LOW Voltage(2)	V_{CC} –1890	V_{CC} –1705	V_{CC} –1620	V_{CC} –1890	V_{CC} –1705	V_{CC} –1620	V_{CC} –1890	V_{CC} –1705	V_{CC} –1620	mV
I_{CC}	Power Supply(3) Current	—	53	65	—	53	65	—	60	74	mA

NOTES:

1. $V_{CC} = V_{CCO} = 5.0V$
2. $V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.) Loading with 50Ω to V_{CC} –2V.
3. All inputs and outputs open.

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = +5.0V \pm 5\%$

		$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V	
V_{IL}	Input LOW Voltage	—	—	0.8	—	—	0.8	—	—	0.8	V	
I_{IH}	Input HIGH Current(1),(2)	— —	— —	20 100	— —	— —	20 100	— —	— —	20 100	μA	
I_{IL}	Input LOW Current(3)	—	—	–0.6	—	—	–0.6	—	—	–0.6	mA	
V_{IK}	Input Clamp Voltage(4)	—	—	–1.2	—	—	–1.2	—	—	–1.2	V	

NOTES:

1. V_{IN}=2.7V
2. V_{IN}=5.0V
3. V_{IN}=0.5V
4. I_{IN}=-18mA

AC ELECTRICAL CHARACTERISTICS(1–6)

$V_{CC} = V_{CCO} = +5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay to Output(1) E_{IN} (differential)(2) E_{IN} (single-ended)(3) T_{IN}	 430 330 350	 — — —	 630 730 950	 430 330 350	 — — —	 630 730 950	 430 330 350	 — — —	 630 730 950	ps
t_{skew}	Within-Device skew(4)	—	25	50	—	25	50	—	25	50	ps
V_{PP}	Minimum PECL(5) Input Swing	250	—	—	250	—	—	250	—	—	mV
V_{CMR}	PECL Common(6) Mode Range	–1.6	—	–0.4	–1.6	—	–0.4	–1.6	—	–0.4	V
t_r t_f	Output Rise/Fall Times 20% to 80%	275	375	600	275	375	600	275	375	600	ps

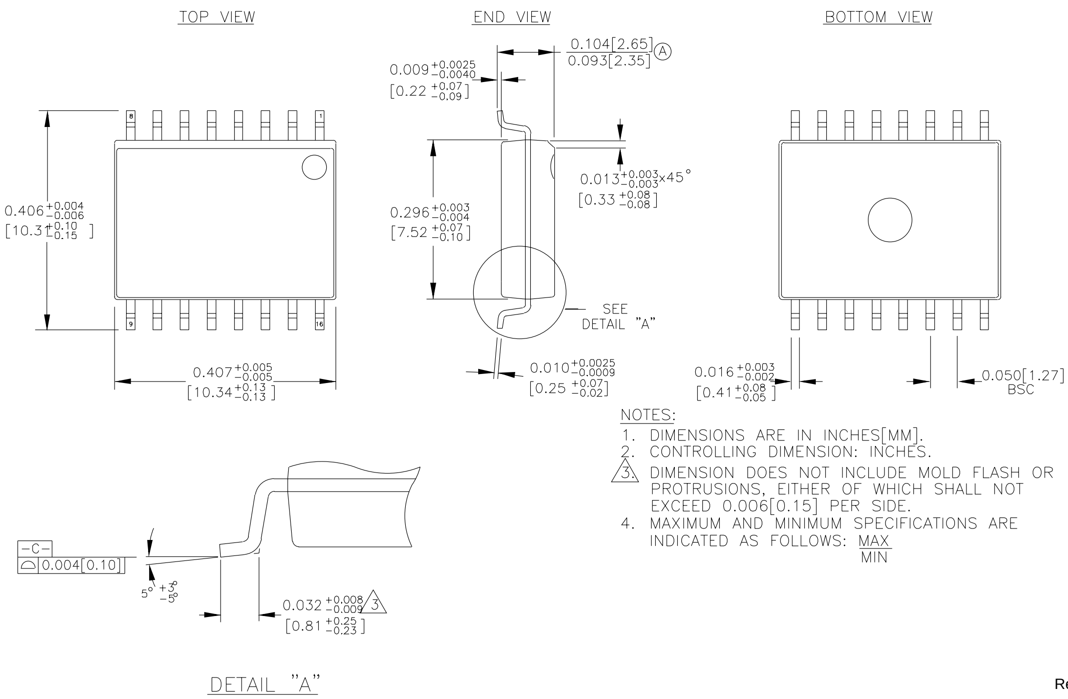
NOTES:

1. Part-to-part skew is defined as Max. — Min. value at the given temperature.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP} (min.) is AC limited for the S815, as a differential input as low as 50mV will still produce full PECL levels at the output.
6. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.).

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S815ZC	Z16-1	Commercial
SY100S815ZCTR	Z16-1	Commercial

16 LEAD SOIC .300" WIDE (Z16-1)



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