National Semiconductor

ADVANCED INFORMATION

54F/74F702
Read-Back Transceiver

General Description

The 'F702 is a byte wide readback transceiver with bidirectional controls. It is a buffered transceiver that features readback capabilities allowing previously latched data to be read back to the originating bus. These extra pathways are controlled with separate enables in order to allow independent operation of each side of the transceiver.

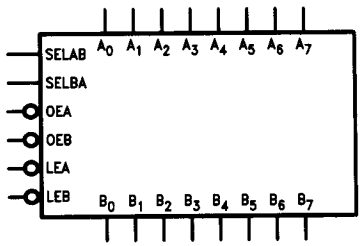
The Read-Back Transceiver can be used as a buffered interface between two busses. Data can be transmitted from A to B and temporarily stored in the B latch. Later, the data in the B latch can be accessed by the A bus in order to verify that the correct data is held by the B latch.

Bus integrity can be verified using the 'F702. Data from A is stored in the B latch. Later, the data is fed back to the A bus and compared to a matching word in the system. If the match is good, then the A bus is maintaining the correct state. The B bus can also be checked in the same manner.

Features

- Bi-directional control
- Allows feedback from latches to original data bus
- Allows independent operation of each side of the transceiver
- 300 Mil 24-pin slimline DIP

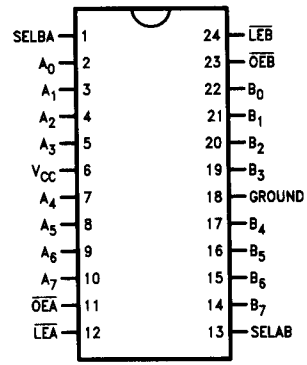
Logic Symbol



TL/F/9590–1

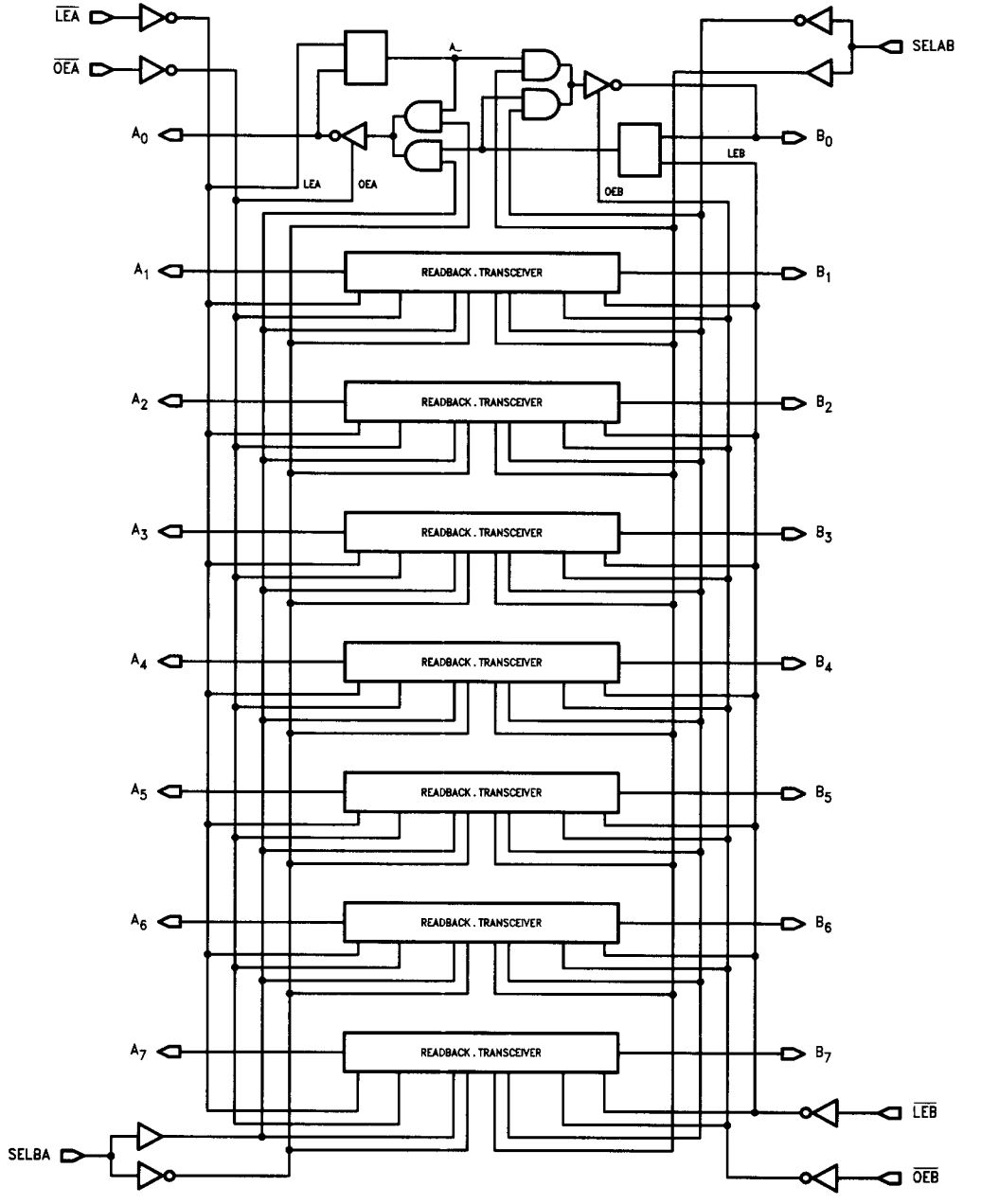
Connection Diagram

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9590–2

Functional Block Diagram



TL/F/9590–3