T-41-89

RS data

CMOS Compatible logic gate optoisolator

Stock number 301-741

The 301-741 is an optically coupled logic gate that combines a GaAsP LED and an integrated high gain photon detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides typically 0.1 mA of differential mode noise immunity and eliminates the potential for output signal chatter. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1,000 volts/μsec, equivalent to rejecting a 300 volt sinusoid at 1 MHz. Improved power supply rejection eliminates the need for special power supply bypassing precautions.

The electrical and switching characteristics of the 301-741 are guaranteed over the temperature range of 0°C to 85°C. The 301-741 is guaranteed to operate over a V_{CC} range of 4.5 volts to 20 volts. Low I_F and wide V_{CC} ranges allow compatibility with TTL, LSTTL, and CMOS logic. Low I_F and low I_{CC} result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a typical propagation delay of 160 nsec when a 120 pF peaking capacitor is used in parallel with the 1.1kΩ current limiting resistor.

The 301-741 is useful for isolating high speed logic interfaces, buffering of input and output lines and implementing isolated line receivers in high noise environments.

Absolute maximum ratings

(No derating required up to 70°C)

Storage temperature	−55°C to +125°C
Operating temperature	−40°C to +85°C[1]
Lead solder temperature	260°C for 10s (1.6mm below seating plane)
Average forward input current — I_F	10mA
Peak transient input current — I_F (≤1 μs pulse width, 300pps)	1A
Reverse input voltage	5V
Supply voltage — V_{CC}	0.0V min., 20V max.
Three state enable voltage — V_E	−0.5V min., 20V max.
Output voltage — V_O	−0.5V min., 20V max.
Total package power dissipation — P	210mW[1]
Average output current — I_O	25mA

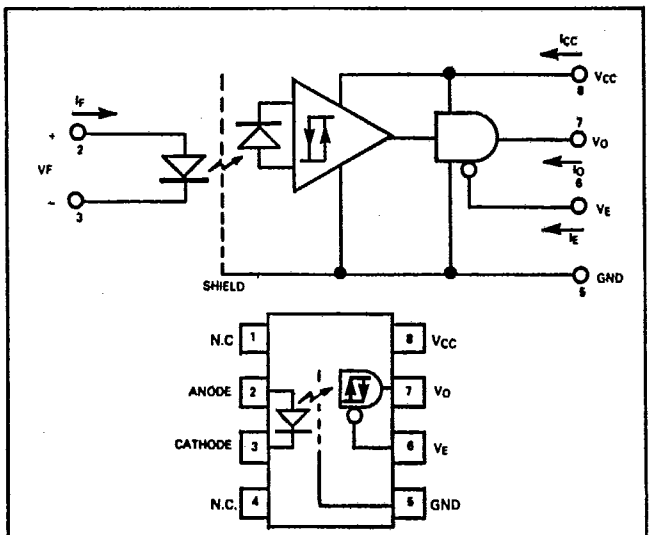
[1]. Derate total package power dissipation, P, linearly above 70°C free air temperature at a rate of 4.5mW/°C.

Features

- Compatible with LSTTL, TTL and CMOS logic
- 2.5 MBAUD guaranteed over temperature
- Low input current (1.6mA)
- Wide V_{CC} range (4.5 to 20 Volts)
- Three state output (no pullup resistor required)
- Guaranteed performance from 0°C to +85°C
- Internal shield for high common mode rejection

Applications

- Isolation of high speed logic systems
- Computer-peripheral interfaces
- Microprocessor system interfaces
- Ground loop elimination
- Pulse transformer replacement
- Isolated buss driver
- High speed line receiver



TRUTH TABLE

(Positive Logic)

Input	Enable	Output
H	H	Z
L	H	Z
H	L	H
L	L	L

5213

Electrical characteristics For 0°C ≤ T_A [1] ≤ 85°C, 4.5V ≤ V_{CC} ≤ 20V, 1.6mA ≤ $I_{F(ON)}$ ≤ 5mA, 0.0mA ≤ $I_{F(OFF)}$ ≤ 0.1mA. All typicals at T_A = 25°C, V_{CC} = 5V, $I_{F(ON)}$ = 3mA unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4mA (4 TTL Loads)		1	
Logic High Output Voltage	V_{OH}	2.4			Volts	I_{OH} = −2.6mA		2	
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	µA	V_O = 5.5V	I_F = 5mA		
				500	µA	V_O = 20V	V_{CC} = 4.5V		
Logic High Enable Voltage	V_{EH}	2.0			Volts				
Logic Low Enable Voltage	V_{EL}			0.8	Volts				
Logic High Enable Current	I_{EH}			20	µA	V_{EN} = 2.7V			
				100	µA	V_{EN} = 5.5V			
			.004	250	µA	V_{EN} = 20V			
Logic Low Enable Current	I_{EL}			−0.32	mA	V_{EN} = 0.4V			
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	V_{CC} = 5.5V	I_F = 0mA		
			5.25	7.5	mA	V_{CC} = 20V	V_E = Don't Care		
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	V_{CC} = 5.5V	I_F = 5mA,		
			3.1	6.0	mA	V_{CC} = 20V	V_E = Don't Care		
High Impedance State Output Current	I_{OZL}			−20	µA	V_O = 0.4V	V_{EN}=2V.I_F=5mA		
	I_{OZH}			20	µA	V_O = 2.4V	V_{EN} = 2V, I_F = 0		
				100	µA	V_O = 5.5V			
				500	µA	V_O = 20V			
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	V_O = V_{CC} = 5.5V	I_F = 0mA		2
		40			mA	V_O = V_{CC} = 20V			
Logic High Short Circuit Output Current	I_{OSH}	−10			mA	V_{CC} = 5.5V	I_F = 5mA V_O = GND		2
		−25			mA	V_{CC} = 20V			
Input Current Hysteresis	I_{HYS}		0.12		mA	V_{CC} = 5V		3	
Input Forward Voltage	V_F		1.5	1.70	Volts	I_F = 5mA, T_A = 25°C			
Input Reverse Breakdown Voltage	V_R	5			Volts	I_R = 10 µA at T_A = 25°C			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		−1.7		mV/°C	I_F = 5mA			
Input-Output Insulation Leakage Current	I_{I-O}			1	µA	V_{I-O} = 3000 VDC T_A = 25°C, t = 5s Relative Humidity = 45%			3
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 VDC			3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1MHz, V_{I-O} = 0 VDC			3
Input Capacitance	C_{IN}		90		pF	F= 1MHz, V_F = 0V, Pins 2 and 3			

Notes: 2. Duration of output short circuit time should not exceed 10ms.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Switching characteristics For 0°C ≤ T_A [1] ≤ 85°C, 4.5V ≤ V_{CC} ≤ 20V, 1.6mA ≤ $I_{F(ON)}$ ≤ 5mA, 0.0mA ≤ $I_{F(OFF)}$ ≤ 0.1mA. All typicals at T_A = 25°C, V_{CC} = 5V, $I_{F(ON)}$ = 3mA unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		210		ns	Without Peaking Capacitor	4.5	4.5
			160	400		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		170		ns	Without Peaking Capacitor	4.5	4.5
			115	400		With Peaking Capacitor		
Output Enable Time to Logic High	t_{PZH}		25		ns		7.9	
Output Enable Time to Logic Low	t_{PZL}		28		ns		7.8	
Output Disable Time from Logic High	t_{PHZ}		105		ns		7.9	
Output Disable Time from Logic Low	t_{PLZ}		60		ns		7.8	

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Output Rise Time (10-90%)	t_r		55		ns		4.6	
Output Fall Time (90-10%)	t_f		15		ns		4.6	
Logic High Common Mode Transient Immunity	CM_H	-1000	-10,000		V/μs	$T_A = 25°C$, $I_F = 1.6mA$		6
Logic Low Common Mode Transient Immunity	CM_L	1000	10,000		V/μs	$T_A = 25°C$, $I_F = 0$		6

Notes:

4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the output pulse.
5. When the peaking capacitor is omitted, propagation delay times may increase by 100ns.
6. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8V$). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0V$).

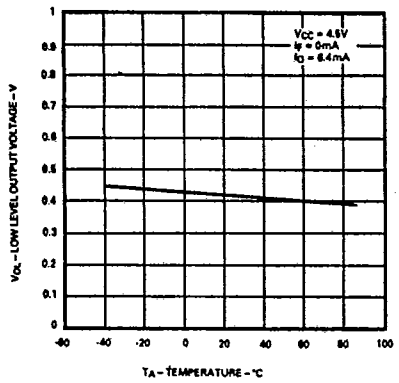


Figure 1 **Typical Logic Low Output Voltage vs. Temperature**

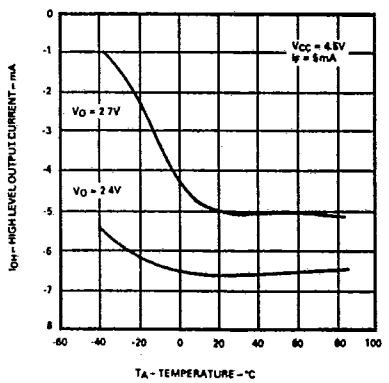


Figure 2 **Typical Logic High Output Current vs. Temperature**

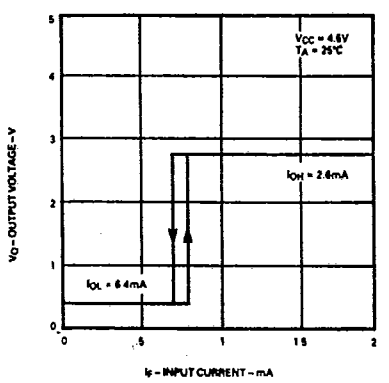


Figure 3 **Output Voltage vs. Forward Input Current**

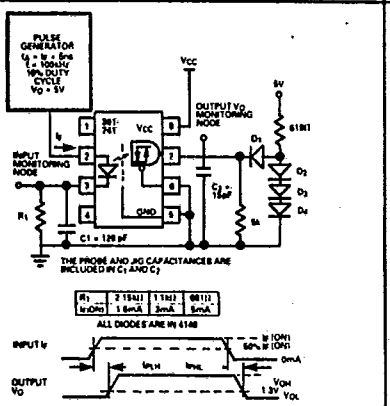


Figure 4 **Test Circuit for t_{PLH}, t_{PHL}, t_p and t_f**

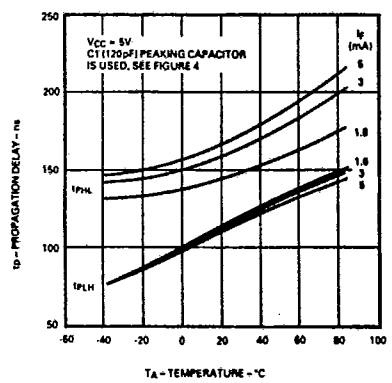


Figure 5 **Typical Propagation Delays vs. Temperature**

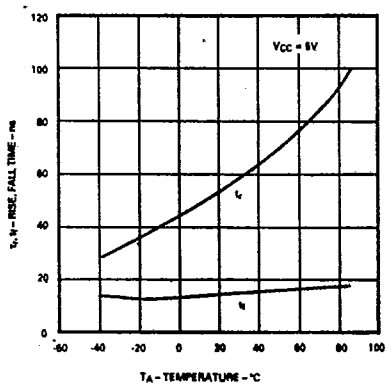


Figure 6 **Typical Rise, Fall Time vs. Temperature**

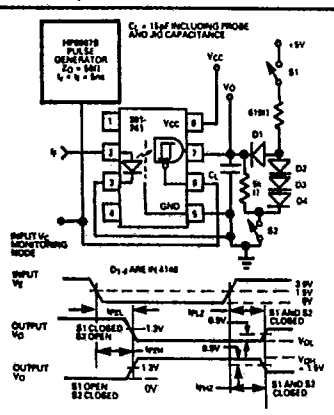


Figure 7 **Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}**

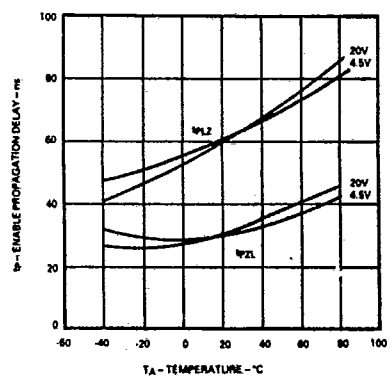


Figure 8 **Typical Logic Low Enable Propagation Delay vs. Temperature**

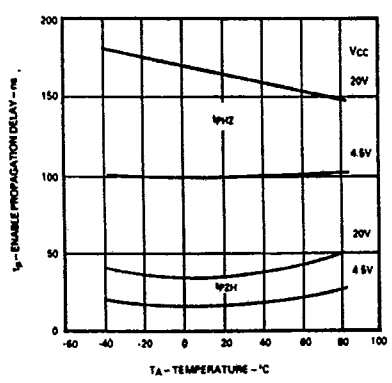
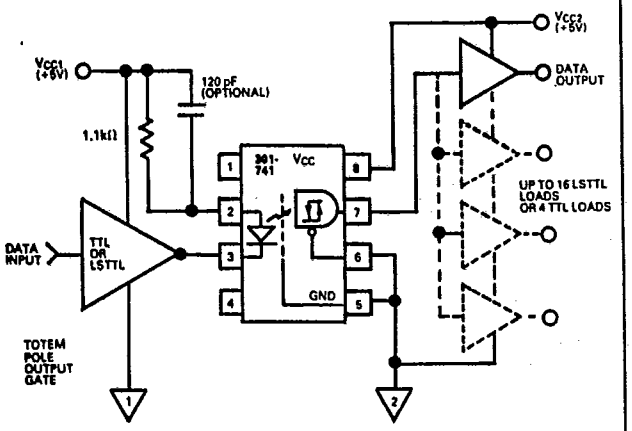


Figure 9 **Typical Logic High Enable Propagation Delay vs. Temperature**

RS data

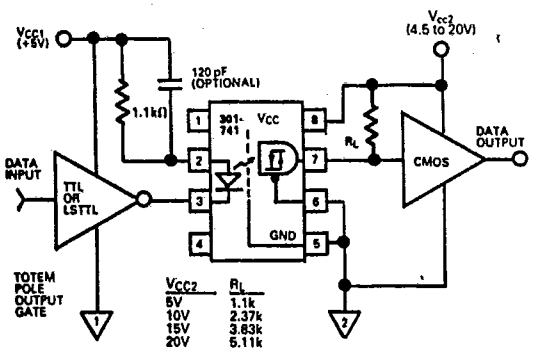
Recommended circuit design

Figure 10 **Recommended LSTTL to LSTTL Circuit**



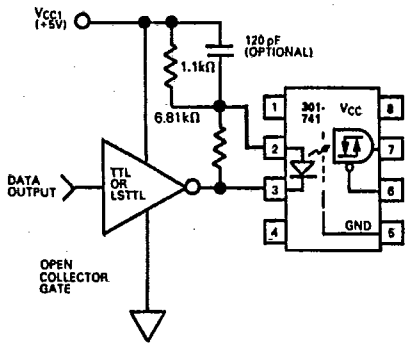
The 120pF capacitor may be omitted in applications where 500ns propagation delay is sufficient.

Figure 11 **LSTTL to CMOS Circuit**



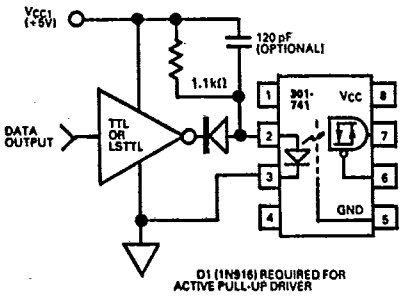
The 120pF capacitor may be omitted in applications where 500ns propagation delay is sufficient.

Figure 12 **Series LED Drive with Open Collector Gate (6.81kΩ Resistor Shunts I_{OH} from the LED)**



The 120pF capacitor may be omitted in applications where 500ns propagation delay is sufficient.

Figure 13 **Alternative LED Drive Circuit**



The 120pF capacitor may be omitted in applications where 500ns propagation delay is sufficient.