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SSI 32P3001
Pulse Detector with Programmable Filter

September 1994

DESCRIPTION

The SSI 32P3001 is a bipolar integrated circuit that provides all the data processing for detection and qualification of encoded read signals from a head preamplifier. This device can handle a NRZ data rate of 64 Mbit/s.

The SSI 32P3001 includes an AGC amplifier with AGC charge pump, a programmable 7-pole Bessel low pass filter, and a pulse qualification circuit. The device features a complete differential circuit architecture in the signal path, for high immunity to noise and power supply ripples.

For fast write-to-read recovery, the SSI 32P3001 allows the user to control the low input state and AGC Fast Recovery mode independently. The AGC action can also be disabled for embedded servo decoding or other processing needs.

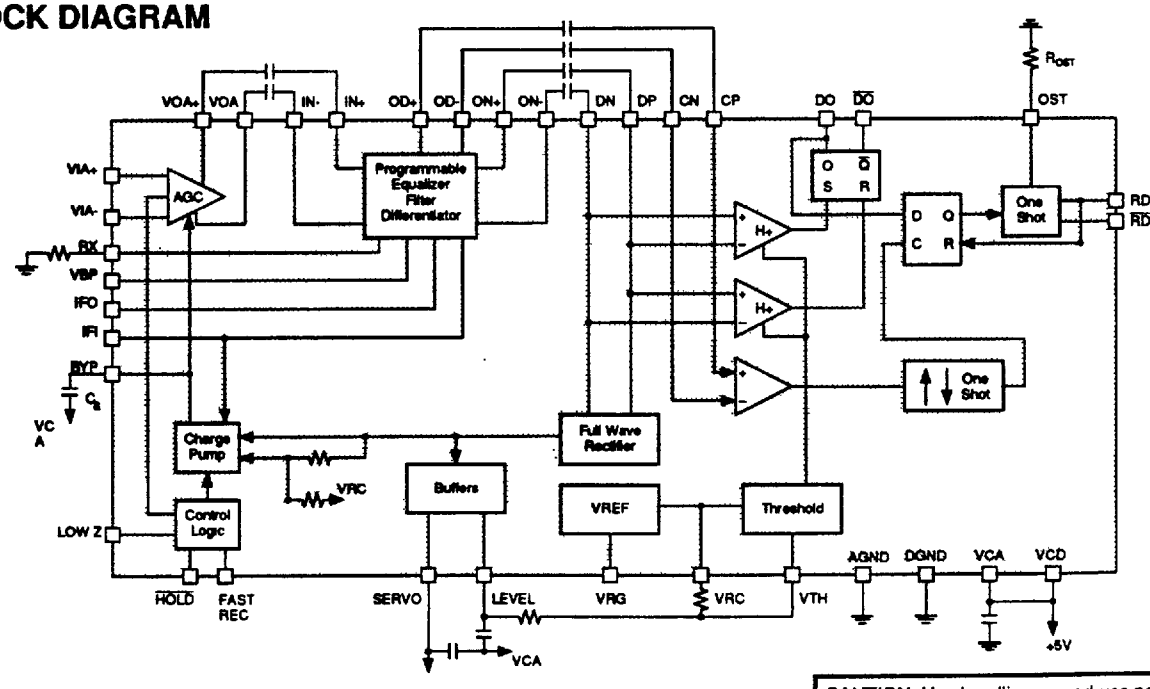
Ideal for constant density recording applications, the SSI 32P3001 low pass filter has a programmable 5-24 MHz bandwidth and 0 - 14 dB boost for pulse slimming. A time derivative of the read signal is also provided by the filter for time qualification in peak detection.

The SSI 32P3001 requires only a +5V power supply and is available in a 36-lead SOM package.

FEATURES

- **Compatible with 64 Mbit/s data rate operation**
- **Fast Attack/Decay modes for rapid AGC recovery**
- **Low Drift AGC hold, fast AGC recovery, and low AGC input impedance control signals**
- **Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components**
- **±0.6 ns filter group delay variation from 0.3 *fc* to *fc* = 24 MHz**
- **Alternating polarity qualification**
- **0.5 ns max pulse pairing**
- **+5V only operation**
- **36-lead SOM package**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32P3001 Pulse Detector is designed to support a 64 Mbit/s NRZ data rate. The signal processing circuits include a wide band variable gain amplifier, a dual-rate AGC charge pump, a programmable electronic filter, and a pulse qualifier.

AGC AMPLIFIER

The wide band AGC amplifier is to amplify the read signal from the read/write pre-amp to a signal level acceptable at the pulse qualifier. The AGC amplifier gain is an exponential function of the BYP voltage when referenced to VCA.

$$Av = Ao \exp[(\frac{V@BYP - Vr}{K})]$$

In a closed AGC loop, the sensitivity of Ao, Vr and K to typical process variations is irrelevant. The typical values of Ao, Vr and K are provided for references only, and not tested in production. Ao = 11, Vr = 3.6 and K = 0.22

AGC ACTIONS

The AGC loop is to maintain a constant DP/DN signal at the nominal level, ~1Vp-pd. The AGC actions are current charging and discharging the external BYP integrating capacitor. These AGC actions can be classified into the following categories:

AUTOMATIC

Slow Decay

When the DP/DN signal is below the nominal level, a slow decay current, ID, charges the BYP capacitor. The AGC amplifier gain is increased slowly. This slow decay current tracks with the bandwidth of the filter. ID = 0.0067 x IFI. At T = 27°C, the maximum ID is 4.0 µA when the filter cutoff frequency is 24 MHz.

Slow Attack

When the DP/DN signal exceeds the nominal level but is below 125% of the nominal level, a slow attack current, ICH, discharges the BYP capacitor. The AGC amplifier gain is decreased. The slow attack current is 30 times that of the slow decay current. Thus, for a given BYP capacitor, the slow attack response time is quicker than the slow decay response.

Fast Attack

When the DP/DN signal exceeds 125% of the nominal level, the device enters a Fast Attack mode. A fast attack current, ICHF, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered. The fast attack current is 6.4 times that of the slow attack current.

USER CONTROL

FAST REC

When FAST REC = TTL logic high, the SSI 32P3001 enters the Fast Recovery mode. Independent of the DP/DN signal level, a fast recovery current, IDF, charges the BYP capacitor. This fast recovery current magnitude is 20 times that of the slow decay current. The AGC amplifier gain is quickly raised. Meanwhile, all the above automatic AGC actions remain active.

$\overline{\text{HOLD}}$

When $\overline{\text{HOLD}}$ = TTL logic low, all the automatic AGC actions and the fast recovery action are suspended. The BYP capacitor voltage remains constant, except for leakage effects.

PROGRAMMABLE FILTER

The SSI 32P3001 includes a programmable low pass filter following the AGC amplifier for (1) 2X voltage gain from filter input to filter outputs, (2) noise limiting, (3) pulse slimming, and (4) provision of a time differentiated signal. The low pass filter is of a 7-pole 2-zero Bessel type. The filter's unboosted -3 dB bandwidth, defined as the cutoff frequency, is programmable from 5-24 MHz; the high frequency equalization is programmable from 0 - 14 dB at the cutoff frequency.

The filter input is ac-coupled from the AGC amplifier output. The filter's normal low pass output is ac-coupled to the data channel of the pulse qualifier. The differentiated low pass output is ac-coupled to the time channel of the pulse qualifier.

The normalized 7-pole 2-zero Bessel filter transfer function is given in figure 1.

The cutoff frequency, fc, is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current, IFO = 0.75 / RX, at T = 27°C. IFI should be made proportional to IFO for fc temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents by the following equation:

$$fc = 24 \cdot \frac{IFI}{IFO} \cdot \frac{1.25}{RX(k\Omega)} \cdot MHz$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc = 24 \cdot \frac{1.25}{RX(k\Omega)} \cdot MHz$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control fc of the Silicon Systems programmable filters. When the DACF, which has a 4X current gain from its reference to fullscale output, is used, 5 kΩ RX is used. The fc is then given by:

$$fc(MHz) = 24 \cdot \frac{F\_Code}{127}$$

where F_Code is a decimal code equivalent to the 7-bit input into the DACF.

The high frequency equalization is programmable with two pins: VRG and VBP. The VRG is a bandgap reference voltage, nominally equal to 2.33V. The voltage at the VBP pin determines the amount of high frequency boost at the cutoff frequency. The boost function is as the following:

$$Boost(dB) = 20\log_{10}\left[\left(Kb \cdot \frac{VBP}{VRG}\right) + 1\right]$$

$$Kb = 3.42 + 0.03 \cdot fci$$

where fci is the ideal cutoff frequency in MHz.

For a fixed boost setting, a resistor divider between VRG and ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VRG should be the reference voltage to the DAC. The DAC output voltage is then proportional to VRG. The DACS in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems' programmable filters.

When DACS is used, the boost relation then reduces to:

$$Boost(dB) = 20\log_{10}\left[\left(\frac{Kb \cdot S\_Code}{127}\right) + 1\right]$$

PULSE QUALIFICATION

The SSI 32P3001 validates each DP/DN peak by combination of level qualification and time qualification. In level qualification, a dual-comparator threshold detection eliminates errors due to low level additive noise. In time qualification, the filter's differentiated output is used to locate signal peaks.

LEVEL QUALIFICATION

The level qualification is performed by a dual comparator circuit. One comparator detects a positive peak by comparing the data signal with a positive threshold. The other comparator detects a negative peak by comparing the data signal with a negative threshold. Each comparator has a small hysteresis, 20% of the set threshold, to avoid false triggering by noise around the set threshold. Polarity check is added to ensure that the slope of two successive peaks is opposite in sign.

The SSI 32P3001 allows two ways of setting the thresholds: fixed threshold or DP/DN tracking threshold. Fixed threshold can be simply set by a DC voltage at the VTH pin, such as from a resistor divider from VCC to VRC (VCC is the +5V supply. VRC is the bandgap voltage referenced from VCC, i.e., VRC = VCC - VRG). The threshold at each comparator can be computed as: Hysteresis Gain • (VTH - VRC). The thresholds at the two comparators are of the same magnitude, but of opposite polarity. For high performance system applications, however, a fixed threshold is not recommended.

LEVEL QUALIFICATION (continued)

DP/DN tracking threshold has the advantages of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The threshold is designed as a percentage of the DP/DN peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider network, to the VTH pin. For a given divider network attenuation a, the equivalent input threshold, THR is:

THR = V_{IN} • LG • a • GHYS Vpd
For example if a = 0.5
V_{IN} = 1 Vp-pd = 500 mVpd

The equivalent input threshold is 290 mVpd or 58% of the input signal. While both the Level Gain and Hysteresis Gain bear a moderate tolerance due to typical process variation, they inversely track each other to yield a much tighter threshold accuracy in a closed loop.

While the external resistor divider ratio determines the qualification setting, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DP/DN peak, but large enough to provide a constant threshold after a long duration of input absence.

The Pulse Qualifier output is the pseudo-ECL differential output, RD and $\overline{RD}$. Corresponding to each validated peak of the DP/DN signal, a one-shot pulse occurs at the RD/$\overline{RD}$ output. The pulse width of the one-shot pulse is determined by a external resistor from the OST pin to ground.

Pulse Width (ns) = 0.16 • R_{OST}(kΩ) • [15.5 + Cs(pF)] - 2

R_{OST} = 2kΩ to 8kΩ, C_S = stray capacitance

DO and $\overline{DO}$ form the differential output as test points to examine the data input of the qualifier D flip-flop. Each is an open-emitter output requiring an external 5 kΩ resistor pull-down to ground. These outputs should be left unconnected during normal operation to reduce power dissipation.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
VIA+, VIA-	I	AGC Amplifier input pins.
IN+, IN-	I	Equalizer/filter input pins.
DP, DN	I	Data inputs to data comparators and fullwave rectifier.
CP, CN	I	Differentiated data inputs to the clock comparator.
VTH	I	Threshold level setting input for the data comparators.
FAST REC	I	TTL compatible input when high puts the charge pump in the Fast Decay mode.
LOW Z	I	TTL compatible input when high reduces the AGC amplifier input resistance.
$\overline{HOLD}$	I	TTL compatible input when low disables the AGC action by turning off the charge pump.
VOA+, VOA-	O	AGC amplifier output pins.
ON+, ON-	O	Equalizer/filter normal output pins. A 5 kΩ resistor pull-down resistor is required to monitor this output. The pins should be left open in normal operation to reduce power dissipation.
OD+, OD-	O	Equalizer/filter differentiated output pins.
DO, $\overline{DO}$	O	PECL compatible data comparator latch output pins.
RD, $\overline{RD}$	O	PECL compatible read data output pins.
LEVEL	O	Open NPN emitter output that provides a fullwave rectified signal for the VTH input. The signal is referenced to VRC.
SERVO	O	Open NPN emitter output that provides a fullwave rectified servo signal. The signal is referenced to VRC.

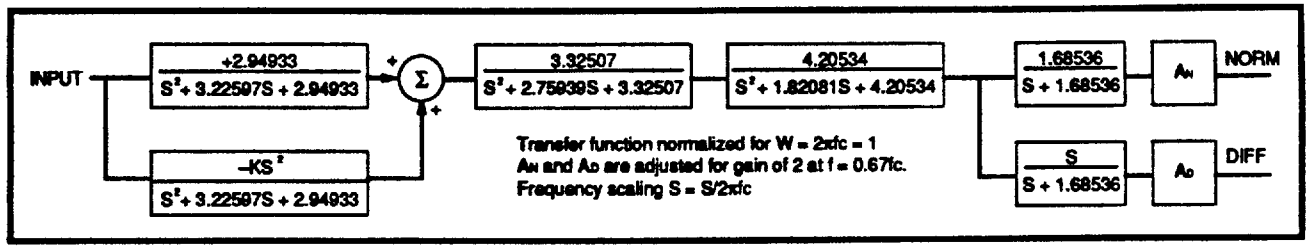


FIGURE 1: Bessel Filter Transfer Function

TABLE 1: Typical Change in f - 3 dB Point with Boost – $K = 2.94933\ (10^{\frac{BOOST\ (dB)}{20}} - 1)$

Boost (dB)	Gain @ fc (dB)	Gain @ peak (dB)	fPeak/fc	f - 3 dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.20	0.36
2	-1	0.00	no peak	1.47	0.76
3	0	0.15	0.62	1.74	1.22
4	1	1.00	1.08	1.96	1.73
5	2	2.12	1.24	2.13	2.30
6	3	3.35	1.24	2.28	2.94
7	4	4.56	1.39	2.42	3.65
8	5	5.82	1.39	2.54	4.46
9	6	7.04	1.39	2.66	5.36
10	7	8.24	1.39	2.77	6.38
11	8	9.41	1.39	2.88	7.52
12	9	10.55	1.39	2.98	8.79
13	10	11.70	1.55	3.08	10.22

Notes: 1. fc is the original programmed cutoff frequency with no boost.
2. f - 3 dB is the new -3 dB value with boost implemented.
3. $f$peak is the frequency where the magnitude peaks with boost implemented.

e.g., fc = 13 MHz when boost = 0 dB
if boost is programmed to 5 dB then f - 3 dB = 27.69 MHz
$f$peak = 16.12 MHz

PIN DESCRIPTION (continued)

ANALOG PINS

NAME	TYPE	DESCRIPTION
OST	-	A resistor to ground sets the RD pulse width.
VRC	-	Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA.
VRG	-	Reference voltage pin for the programmable filter. VRG is referenced to ground.
VBP	-	The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND.
RX	-	Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO.
IFO	-	Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin.
IFI	-	Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency.
BYP	-	The AGC integrating capacitor C_A is connected between BYP and VCA.
VCA, VCD	-	Analog and Digital +5V.
AGND, DGND	-	Pulse detector and filter ground. Must be tied together.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER		RATING
Storage Temperature		-65 to +150°C
Junction Operating Temperature	Tj	+130°C
Supply Voltage	VCC, VCD	-0.3 to 7V
Voltage Applied to Inputs		-0.7 to VCC, VCD + 0.7V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	VCD = VCC	4.5V < VCC < 5.5V
Ambient Temperature	Ta	0°C < Ta < 70°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current	ISS			92	118	mA
Power Dissipation	PD			460	650	mW

LOGIC SIGNALS

TTL Input Low Voltage	VIL		-0.3		0.8	V
TTL Input High Voltage	VIH		2.0		VCC +0.3	V
TTL Input Low Current	IIL	VIL = 0.4V	-0.4			mA
TTL Input High Current	IIH	VIH = 2.7V			0.1	mA
PECL Output High Voltage	VOHE		VCC -1.1		VCC -0.6	V
PECL Output Low Voltage	VOLE		VCC -1.9		VCC -1.4	V
PECL High Output Current	IOHE	RD $\overline{RD}$ VOHE = VCC - 0.6V			4	mA
		DO, $\overline{DO}$ VOHE = VCC - 0.6V			1	mA
PECL Low Output Current	IOLE	RD, $\overline{RD}$ VOHE = VCC - 1.4V	-4			mA
		DO, $\overline{DO}$ VOHE = VCC - 1.4V	-1			mA
PECL Output Swing	VES		0.75	0.85	0.95	Vpd
PECL Output Rise and Fall Time	TRF	CL ≤ 10 pF, RD, $\overline{RD}$ only			3.5	ns
Control Input Switching Times	TCS	Hold, LOW Z, FAST REC turn on/off times			0.1	µs

AGC AMPLIFIER

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. Ca 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-.

Input Range	VIR	Filter boost at fc = 0 dB	24		240	mVp-pd
		Filter boost at fc = 9 dB	20		100	mVp-pd
DP-DN voltage	VD	VIA± = 0.1 Vp-pd *	0.85		1.05	Vp-pd
DP-DN Voltage Variation	VDV	24 mV < VIA± < 240 mV *			8	%
AGC minimum gain	AVmin				1.7	V/V
AGC maximum gain	AVmax		28			V/V
Gain Sensitivity	AVPV			45		dB/V
VOA± Dynamic Range	DR	THD = 1% max	0.75			Vp-p
Differential Input Resistance	RINDA	LOW Z = low	3.7	5.3	7.4	kΩ

AGC AMPLIFIER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Single Ended Input Resistance	RINSA	LOW Z = low		2.65		kΩ
		LOW Z = high		78	150	Ω
Output Offset Voltage Variation	VOS	from min gain to max gain	-200		+200	mV
Input Referred Noise Voltage	VIN	gain = max, Rs = 0Ω filter not connected to VOA+, VOA-, BW = 15 MHz		13.5	20	nV/√Hz
Bandwidth	BW	No AGC action, 1.9<Av<22BW	55	77		MHz
Common mode Rejection Ratio	CMRR	gain = max, Vin = 0 VDC + 100 mVp-p @ 5 MHz	40	65		dB
Power Supply Rejection Ratio	PSRR	gain = max, 100 mVp-p on VCA, VCD @ 5 MHz	43	59		dB
Gain Decay Time	GDT	VIA± = 240 mV to 120 mV VOA± >0.9 Final Value		40		µs
Gain Attack Time	GAT	VIA± = 120 mV to 240 mV VOA± <1.1 Final Value		1.8		µs
* AGC loop closed						

AGC CONTROL

The input signals are AC coupled to DP and DN. Ca = 1000 pF, LEVEL load = 50 µA, SERVO load = 100 µA, 100 µA < IFI < 600 µA.

Discharge Current, Id	ID	FAST REC = low DP - DN = 0		0.0067 x IFI		mA
Fast Discharge Current, Idf	IDF	FAST REC = high		20 x ID		mA
Charge Pump Attack Current, Ich	ICH	DP - DN = 0.55V		30 x ID		mA
Charge Pump Fast Attack Current, Ichf	ICHF	DP-DN = 0.675V		6.4 x ICH		mA
BYP Pin Leakage Current	IK	$\overline{HOLD}$ = low, VBYP = VCC -1.5V	-0.1		0.1	µA
Reference Voltage	VRG	Isource = 0 to 1 mA	2.2		2.45	V
Reference Voltage	VRC		Vcc-2.55	Vcc-VRG	Vcc-2.1	V
Output Drive Current	IVRC	ΔVRC < 20 mV	-0.75		0.75	mA

EQUALIZER/FILTER The input signals are AC coupled to IN+ and IN-.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Filter Cutoff Frequency	*fc*	RX = 5 kΩ *fc* = 24 x IFI/(4 x IFO) MHz 4 ≥ IFI/IFO ≥ 5/6	5		24	MHz
IFO Reference Current Range	IFO	IFO = 0.75/RX; Tj = 27°C 7.5 kΩ > RX > 1.25 kΩ	0.10		0.6	mA
IFI Program Current Range	IFI	Tj = 27°C, 24 MHz > *fc* > 5 MHz	0.125		0.6	mA
FCA Filter FC Accuracy	FCA		-13		13	%
RX Range	RX		1.25		7.5	kΩ
Normal Low Pass Gain AO = (ON ±) / (IN±)	AO	Fin = 0.67*fc*	1.4		2.2	V/V
Differentiated Low Pass Gain AD = (OD ±) / (IN±)	AD	Fin = 0.67*fc*	0.8 AO		1.2 AO	V/V
Frequency Boost	FBA	FB nominal VBP = VRG	-1.5		+1.5	dB
Accuracy		VBP/VRG = 0.5	-1.0		+1.0	dB
Group Delay Variation	TGD1	*fc* = 24 MHz, *fc* > Fin > 0.3*fc*, VBP = 0 to VRG	-0.6		+0.6	ns
TGD2		*fc* = 5 to 24 MHz, *fc* > Fin > 0.3 *fc*, VBP = 0 to VRG	-2.5		+2.5	%
Output Offset Voltage Variation	VOSVF	Normal and differentiated outputs, 125 µA < IFI < 600 µA	-200		+200	mV
VOF Filter Output Dynamic Range	DRF	THD = 15% Fin = 0.67 *fc*	1.2			Vp-p
Filter Input Resistance	RINF		3.0			kΩ
Filter Input Capacitance	CINF				7	pF
Filter Output Resistance	ROF	IO = 1 mA		30	60	Ω
Filter Output Current	IOF		-1		1	mA
Output Noise Voltage; ON+, ON-	VNN	NBW = 100 MHz, RS = 50Ω VBP = 0, *fc* = 24 MHz		2.3	3.5	mVRms
		NBW = 100 MHz, RS = 50Ω VBP = VRG, *fc* = 24 MHz		5.1	8	mVRms
Output Noise Voltage; OD+, OD-	VND	NBW = 100 MHz, RS = 50Ω VBP = 0, *fc* = 24 MHz		4.9	7.5	mVRms
		NBW = 100 MHz, RS = 50Ω VBP = VRG, *fc* = 24 MHz		13	21	mVRms

ELECTRICAL SPECIFICATIONS (continued)

DATA COMPARATOR

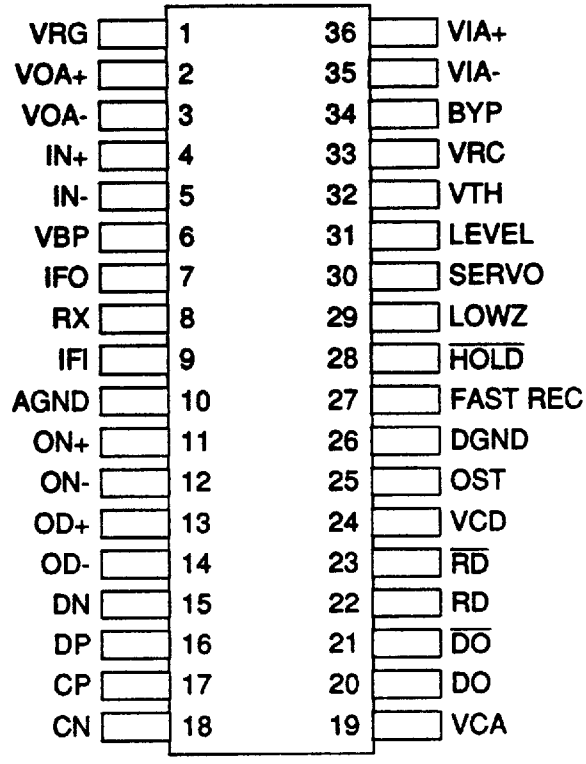
The input signals are AC coupled to DP and DN. I (LEVEL) = 50 µA, I (SERVO) = 100 µA, 0.01 µF capacitors tied from LEVEL and SERVO to VCA

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Differential Input Resistance	RIND		8	9.4	14	kΩ
Differential Input Capacitance	CIND				5	pF
Comparator Offset Voltage (Note 1)	OSD				4	mV
Level (Servo) Output Gain	LG	DP-DN = 0.25 to 0.5 VDC, LG = V_{LEVEL} - V_{RC} / 2 x (DP - DN)	0.712		0.788	V/V
Level (Servo) Output Bandwidth	LBW	±1 dB referenced to 1 MHz	20	53		MHz
Level Offset Voltage	VLOS	Output-VRC, IL = 50 µA	-30		+30	mV
Servo Offset Voltage	VSOS	Output - VRC, IL = 100 µA	-30		+30	mV
Threshold Voltage Gain	GHYS	0.3 < VTH-VRC < 0.9 @ 1 MHz	0.75	0.79	0.82	Vpd/V
Threshold Voltage Hysteresis (Note 1)	VSH			0.20 x GHYS x (VTH - VRC)		V/V
Minimum Threshold Voltage	VHM	VTH-VRC ≤ 0.11V		0.12		V/V
Propagation Delay	TPDD	From DP/DN to DO, $\overline{DO}$		5		ns
Input Bias Current	IVTH		-2		2	µA

CLOCKING The input signals are AC coupled to CP and CN.

Comparator Offset Voltage	VOSC	Not directly measurable			4	mV
Differential Input Resistance	RINC		8	9.5	14	kΩ
Differential Input Capacitance	CINC				5	pF
D F/F Set Up Time	TDS	DP-DN threshold to CP-CN zero cross	0			ns
Pulse Pairing	PP	Vs = 1 Vp-p, F = 10 MHz		0.15	0.5	ns
Propagation Delay to RD	TPDC	Vs = 20 mVp-p sq wave		12		ns
RD Output Pulse Width	PWRD	Tpd = 0.16 • R_{OST}(kΩ) • [15.5 = Cs(pF)] - 2 R_{OST} = 2 kΩ to 8 kΩ, Cs = stray capacitance in pF	0.78x Tpd		1.22x Tpd	ns

PACKAGE PIN DESIGNATIONS
(Top View)



36-Lead SOM

THERMAL CHARACTERISTICS : θja

36-Lead SOM	75° C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32P3001 36-Lead Small Outline (31.6 mil pitch)	32P3001-CM	32P3001-CM

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914