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MATRA M H S

September 1990

DATA SHEET

HM 65791

16 K x 4
HIGH SPEED CMOS SRAM
SEPARATE I/O AND TRANSPARENT WRITE

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FEATURES

- **FAST ACCESS TIME**
  MILITARY : 20/35/45 ns (max)
  COMMERCIAL : 15*/20/25/35/45 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 267 mW (typ)
  STANDBY : 75 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**
- **SEPARATE INPUTS/OUTPUTS**
- **TRANSPARENT WRITE**
- **OUTPUT ENABLE**

DESCRIPTION

The HM 65791 is a high speed CMOS static RAM organized as 16384 x 4 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 15 ns are available with maximum power consumption of only 385 mW.
The HM 65791 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 85 % when the circuit is deselected.

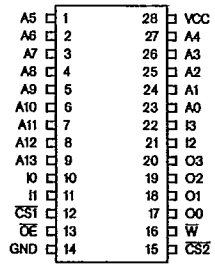
Easy memory expansion is provided by two active low chip select (CS1, CS2), an active low output enable (OE) and three state drivers.
All inputs and outputs of the HM 65791 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65791 is processed following the test methods of MIL STD 883C.

PACKAGES

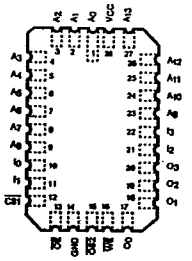
Plastic 300 mils, 28 pins, DIL.
Ceramic 300 mils, 28 pins, DIL.
Tape and Reel Service.

LCC 28 pins.

Pinout DIL 28 pins (top view)

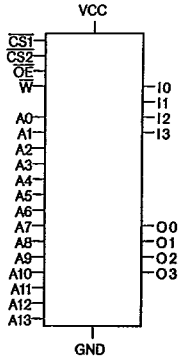


Pinout LCC 28 pins (top view)

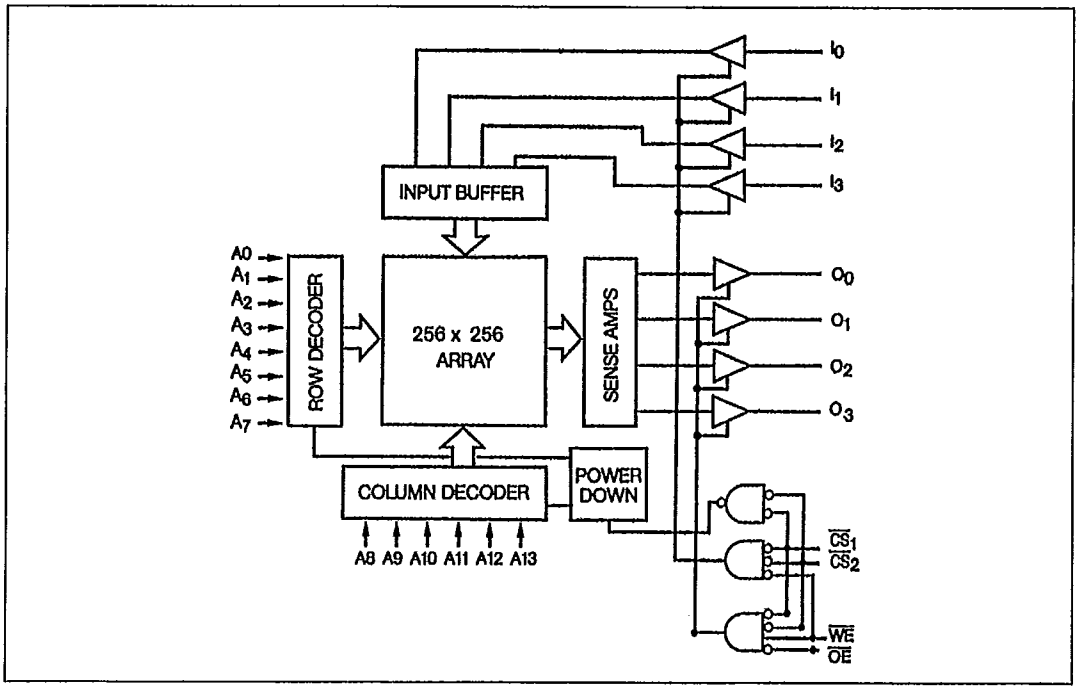


* Preliminary

LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A13 : Address inputs	$\overline{CS1}$-$\overline{CS2}$: Chip-Select
I0-I3 : Inputs	$\overline{OE}$: Output enable
O0-O3 : Outputs	$\overline{W}$: Write enable
VCC : Power	GND : Ground

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Valid	Write
L	L	L	Valid	Valid	Write

L = low, H = high, or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V
Storage temperature : – 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro static discharge voltage : > 2001 V (MIL STD 883C method 3015.2)

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OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

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CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C - f = 1 MHz - Vcc = 5.0 V, these parameters are not 100 % tested.

AC TEST LOADS WAVEFORMS

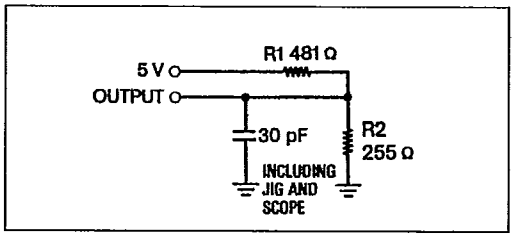


Fig. 1a.

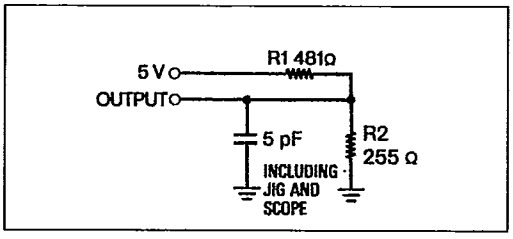
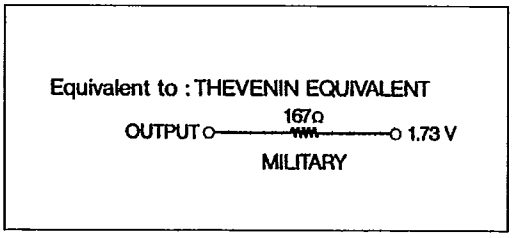


Fig. 1b.



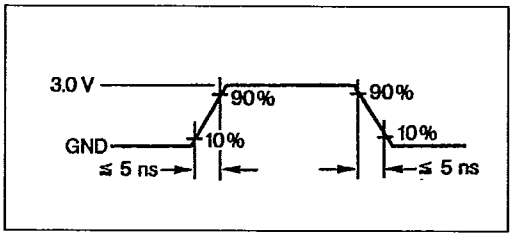


Fig. 2.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	– 350.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = - 4.0 mA.

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Consumption for Commercial specification (– 5) :

SYMBOL		PARAMETER	65791 E-5*	65791 F-5	65791 H-5	65791 K-5	65791 M-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	40	40	30	30	30	mA	max
ICCSB1	(7)	Standby supply current	20	20	20	20	20	mA	max
ICCOP	(8)	Dynamic Operating current	115	100	100	100	100	mA	max

Consumption for Industrial (– 9) and Military specification (2) :

SYMBOL		PARAMETER	65791 H-9/2	65791 K-9/2	65791 M-9/2	UNIT	VALUE
ICCSB	(6)	Standby supply current	40	30	30	mA	max
ICCSB1	(7)	Standby supply current	20	20	20	mA	max
ICCOP	(8)	Dynamic operating current	100	100	100	mA	max

Notes : 6. $\overline{CS} \geq$ VIH min duty cycle = 100 %. A pull-up resistor to VCC on the $\overline{CS}$ is required to keep the device unselected during VCC power-up. Otherwise ICC SB will exceed above values.
7. $\overline{CS}$ = Vcc – 0.3 V Iout = 0 mA.
8. Vcc max, Output current = 0mA, f = max, Vin = Vcc or Gnd.
* Preliminary.

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ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH *(see figure 1a and 1b)* : + 30 pF

WRITE CYCLE : Commercial specification

SYMBOL	PARAMETER	65791 E-5*	65791 F-5	65791 H-5	65791 K-5	65791 M-5	UNIT	VALUE
TAVAV	Write cycle time	15	20	20	25	40	ns	min
TAVWL	Address set-up time	0	0	0	0	0	ns	min
TAVWH	Address Valid to end of write	12	15	20	25	30	ns	min
TDVWH	Data set-up time	10	10	10	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	12	15	20	25	30	ns	min
TWLQZ	Write low to high Z	7	7	7	10	15	ns	max
TWLWH	Write pulse width	12	15	15	20	20	ns	min
TWHAX	Address hold from end of write	0	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	0	ns	min
TWLQV	$\overline{W}$ low to data valid	15	20	25	30	35	ns	max
TDVQV	Data valid to output valid	15	20	20	30	35	ns	max

WRITE CYCLE : Industrial and military specification

SYMBOL	PARAMETER	65791 H-9/2	65791 K-9/2	65791 M-9/2	UNIT	VALUE
TAVAV	Write cycle time	20	25	40	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	20	25	30	ns	min
TDVWH	Data set-up time	10	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	20	25	30	ns	min
TWLQZ (8)	Write low to high Z	7	10	15	ns	max
TWLWH	Write pulse width	15	20	20	ns	min
TWHAX	Address hold from end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWLQV	$\overline{W}$ low to data valid	25	30	35	ns	max
TDVQV	Data valid to output valid	20	30	35	ns	max

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
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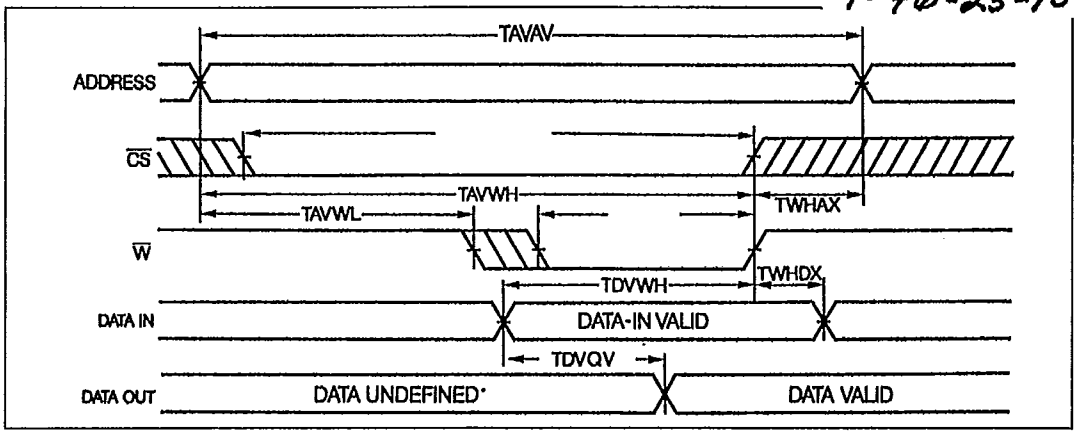
WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



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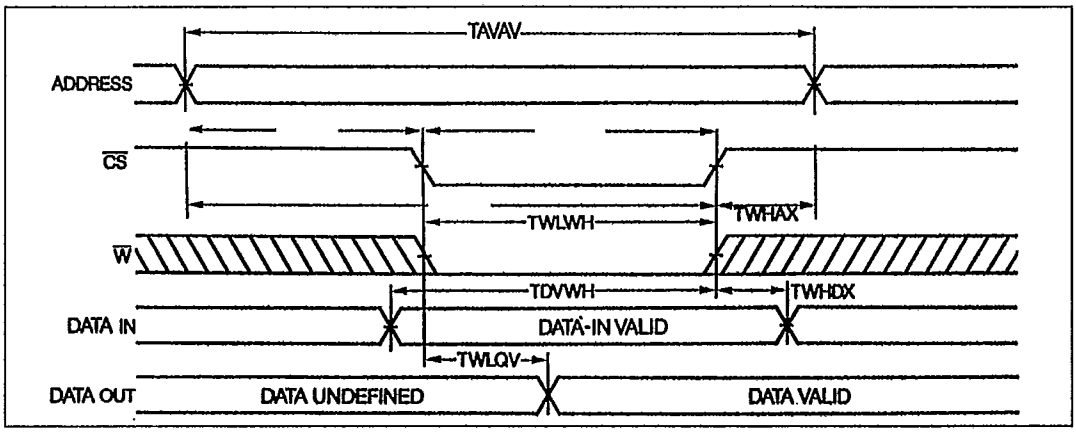
WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)



READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65791 E-5*	65791 F-5	65791 H-5	65791 K-5	65791 M-5	UNIT	VALUE
TAVAV	READ cycle time	15	20	25	35	45	ns	min
TAVQV	Address access time	15	20	25	35	45	ns	max
TAVQX	Address Valid to low Z	3	3	3	3	3	ns	min
TELQV	Chip-select access time	15	20	25	35	45	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	8	8	10	12	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	15	20	20	20	25	ns	max
TGLQV	Output enable access time	10	10	12	15	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	8	8	10	12	15	ns	max

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READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65791 H-9/2	65791 K-9/2	65791 M-9/2	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	ns	min
TAVQW	Address access time	25	35	45	ns	max
TAVQX	Address Valid to low Z	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	10	12	15	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	20	25	ns	max
TGLQV	Output enable access time	12	15	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	12	15	ns	min

* Preliminary

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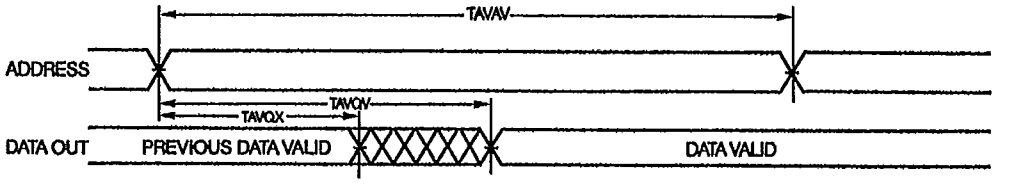
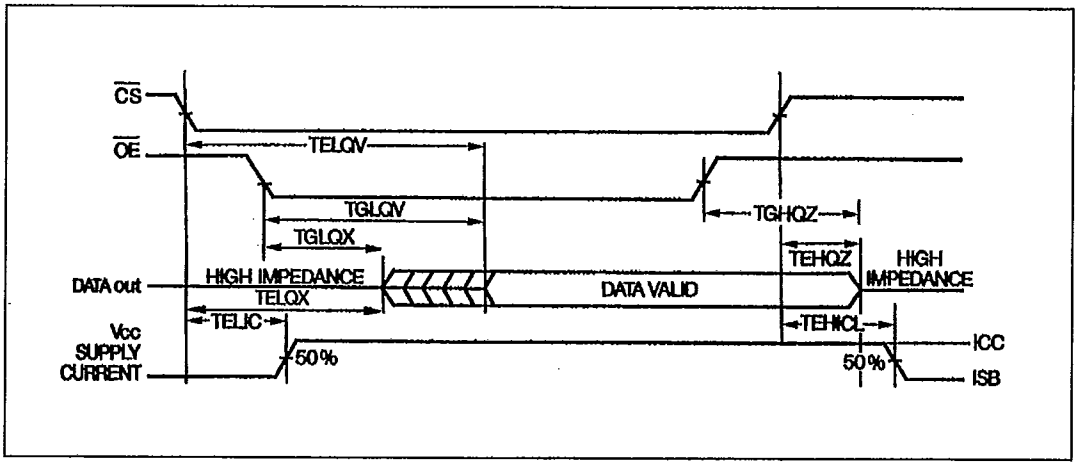
READ CYCLE nb 1



READ CYCLE nb 2



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ORDERING INFORMATION

Package	Device	Grade	Level
HM1	65791	H	–5
0 - Chip form 1 - Ceramic 24 pins 3 - Plastic 28 pins 4 - LCC 28 pins	16 k x 4 high speed static RAM with separate I/O and transparent write	E* = 15 ns F = 20 ns H = 25 ns K = 35 ns M = 45 ns	–5 : Commercial –9 : Industrial –2 : Military –8 : Military with B.I. (B.I. = Burn-in)

* Preliminary.

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PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 28 pins
SOIC DIL, 300 mils, 28 pins
Ceramic, 300 mils, 28 pins
LCC rectangular, 28 pins