GC101 / GC102

12/16 MHZ PC/AT COMPATIBLE CHIP SET

Features

- Highly integrated PC/AT compatible three chip set.
- Supports up to 4 Meg DRAM using 1M or 256k devices.
- Available in 16MHz and 12MHz versions.
- Designed in CMOS for low power consumption.
- All "MegaCells" are full implementations of standard devices.
- Available as "Cores" for customization in high volume applications.

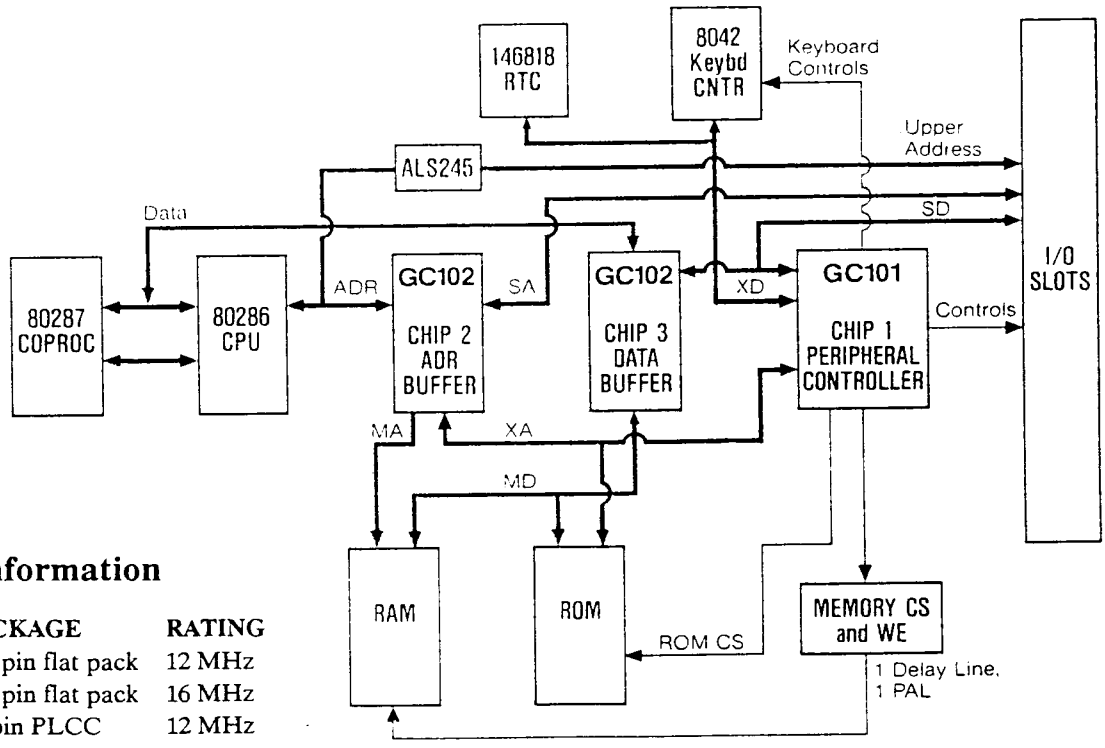
Description

The GC101/GC102 is a fully IBM PC/AT compatible chip set supporting the 80286 CPU at clock speeds up to 16MHz. This highly integrated three chip solution features high performance, low power consumption, low board space requirements, high reliability, and low cost. A fully PC/AT compatible system may be implemented with this chip set, the CPU, Co-Processor, 6 other devices and memory. This chip set supports 256k and 1 Mbit DRAMs in configurations up to 4 megabytes at one wait state. Zero wait state operation is possible with the addition of an external synchronization circuit.

The GC101 performs CPU and Peripheral support funtions including that of DMA Controllers, a Memory Mapper, Timers, Counters, Interrupt Controllers, a Bus Controller, and their supporting circuitry. This device is packaged in a 160 pin flat pack.

The GC102 may be configured as either an Address Buffer or Data Buffer by strapping one pin high or low. This chip replaces address buffers, data transceivers, memory drivers, parity generators and supporting circuitry. This device is packaged in an 84 pin PLCC.

System Board Block Diagram



Ordering Information

PART	PACKAGE	RATING
GC101-12	160 pin flat pack	12 MHz
GC101-16	160 pin flat pack	16 MHz
GC102-12	84 pin PLCC	12 MHz
GC102-16	84 pin PLCC	16 MHz

GC101 Peripheral Controller Functional Description

The GC101 Peripheral Controller chip is the heart of the three chip system and forms most of the control circuits and "glue" logic of the AT architecture in a single CMOS VLSI chip. In this device, an 82284 megafunction (MF) generates PROCCLK, /READY and /RESET signals for use by the system. MF82288 provides all the CPU I/O command signals for memory, peripherals, and add on boards. A 9-bit refresh counter is used in the circuit to provide the row address of the memory during refresh. MF74612 outputs memory mapping addresses. MF8284 uses a 14.318 MHz input clock to generate an OSC video signal and base clock for the MF8254 timer/counter. The timer is programmed by the CPU and provides signals for system timing, refresh, and speaker tone generation.

Two MF8237s support Direct Memory Access, transferring 8-bit and 16-bit data between memory and I/O devices. Two MF8259s are configured as master/slave and receive interrupt requests from Timer, Keyboard Controller, Real Time Clock, Numeric Processor and up to 11 other sources. The MF8259s issue a signal to the CPU to initiate an interrupt routine. For all peripherals of 8-bit data width, the GC101 provides conversion circuitry from a 16-bit bus to an 8-bit bus, thus maintaining compatibility with an 8088 PC.

The GC101 design encompasses one wait state for memory operation and four wait states for I/O operation. The design includes the option of improving performance by using faster RAM, faster CPU, or by reducing the memory wait state to zero with the addition of external synchronization logic. Designers can configure memory from 256K to 4 Mbytes (or more) by using RSEL0, SEL1 and RSEL2 (see pin listing). There are also select signals to establish chip and system speed. The chip can operate at up to 12/16 MHz in the full commercial temperature range.

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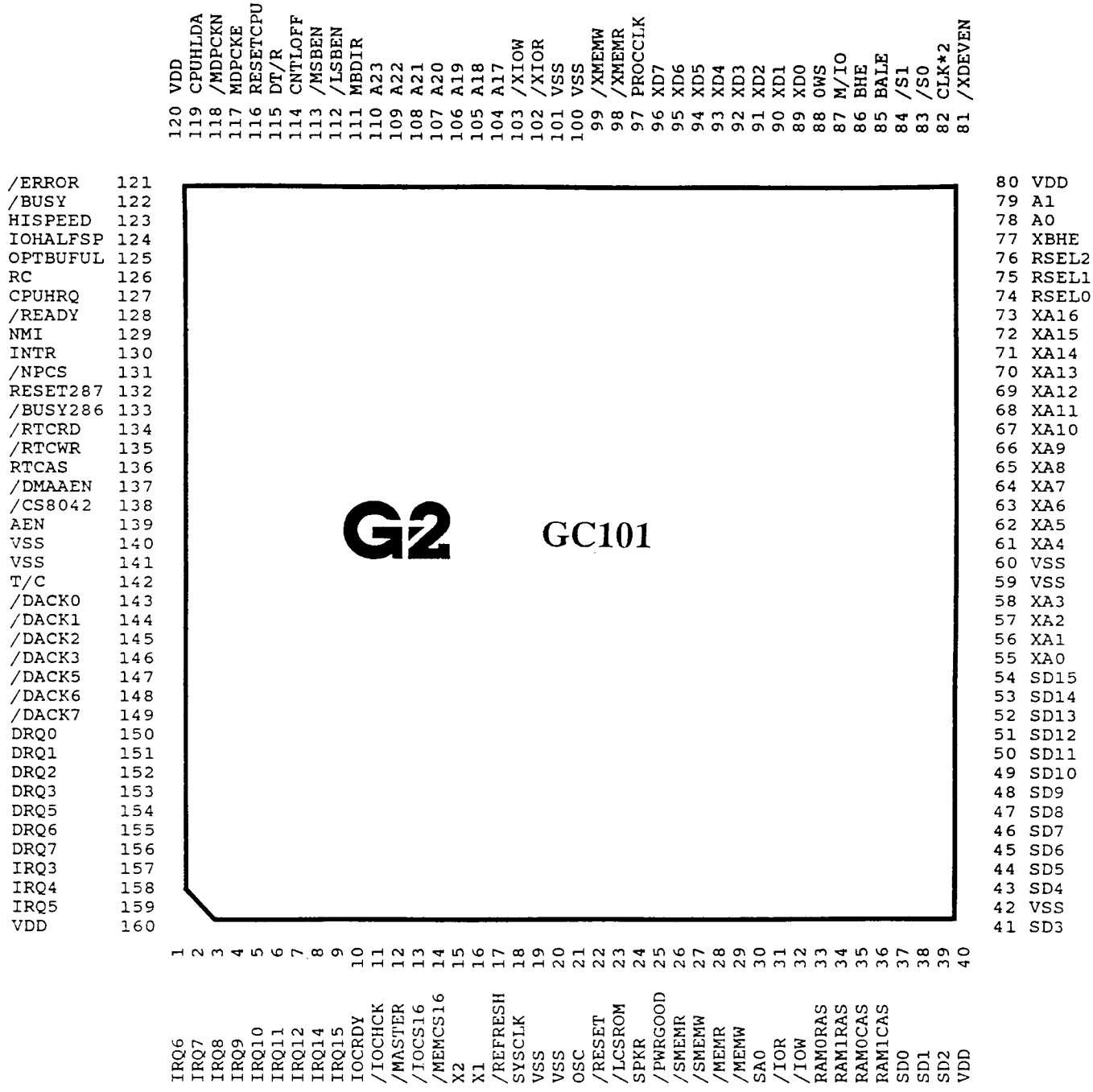
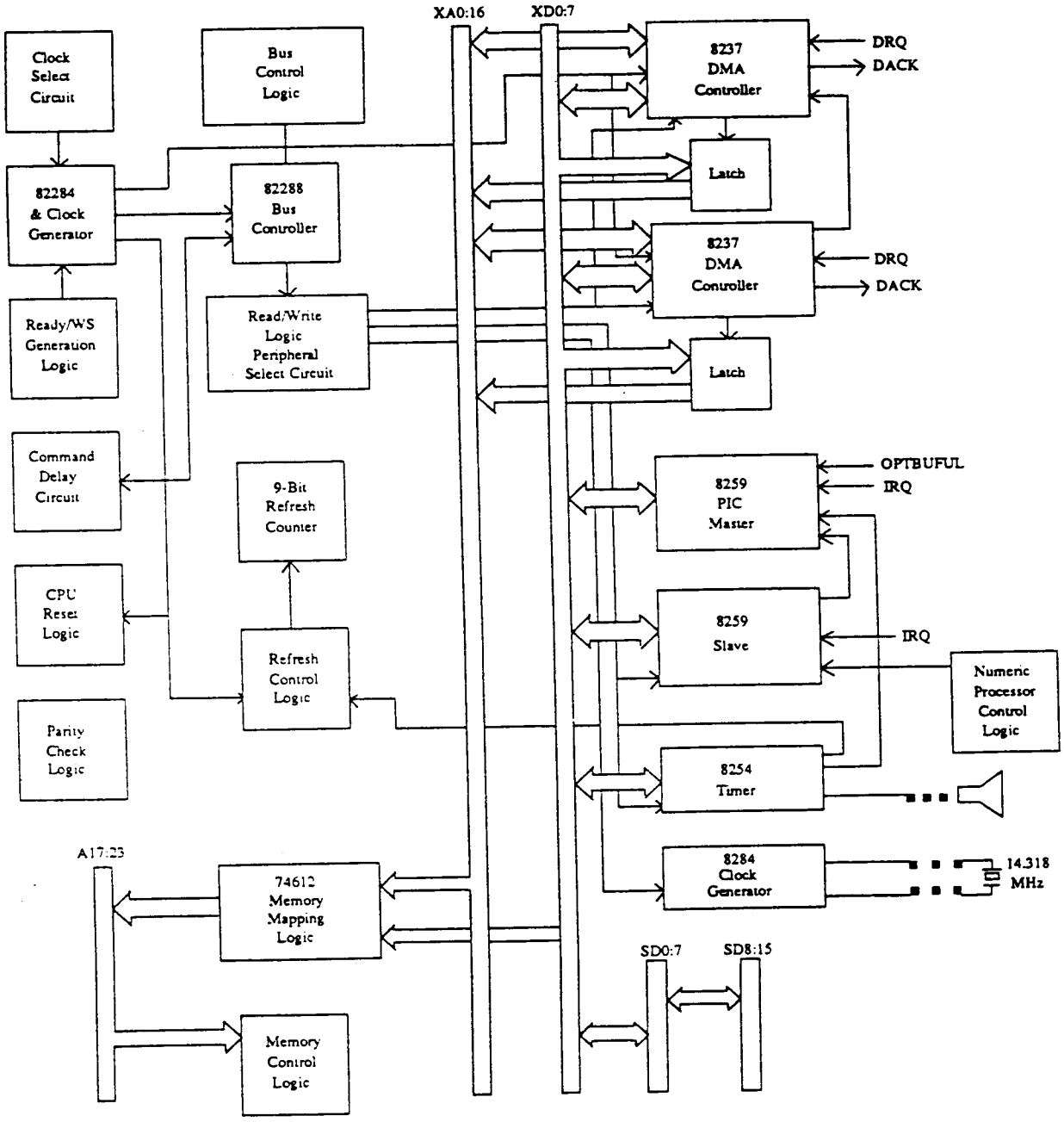
GC101 PIN ASSIGNMENT



GC101 Peripheral Controller Chip Block Diagram



GC101 Peripheral Controller - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
A0,1	I(TTL)	78,79/88,90	PU	A0,1 are the address inputs from the CPU. A0 generates SA0, while A1 and M/IO, S0, and S1 generate the CPU shutdown operation.
A17-23	I(TTL) O(B2)	104-110/116-122	PU	A17-23 are the input address lines from the CPU. These signals are used to decode the memory selection logic and can be output address lines of the memory mapper 74LS612.
AEN	O(B4)	139/157		DMA address enable signal. When High, AEN indicates that the DMA controller has control of the address, data, and read/write control buses.
BALE	O(B4)	85/97		Buffered Address Latch Enable signals the I/O slots that the present address is valid. SA0-19 is latched with the falling edge of BALE. BALE is forced High during DMA cycles.
BHE	I(TTL)	86/98	PU	Bus High Enable signal. BHE is active Low and is used to enable the High Byte of the data bus.
/BUSY	I(TTL)	122/138	PU	This input (active Low) should be connected to the BUSY output of the 80287.
/BUSY286	O(B2)	133/151		This is an active Low output that indicates the numeric processor 80287 is in operation mode. This pin is tied to busy input of the CPU.
CLK*2	I(TTL)	82/94	PU	This is the clock input and must be twice the desired processor clock frequency.
CNTLOFF	O(B2)	114/126		Control Off signal. When High, CNTLOFF enables the low byte data latch during 8-bit data transfer.
CPUHLDA	I(TTL)	119/132	PU	CPU Hold Acknowledge is the granting signal from the CPU to relinquish control of the system.
CPUHRQ	O(B2)	127/145		CPU Hold Request to the CPU for DMA and Refresh operation, active High.
/CS8042	O(B2)	138/156		Chip Select 8042 signal. When Low, /CS8042 selects the keyboard controller.
/DACK0-3 /DACK5-7	O(B2)	143-46/161-64 147-49/165-67		DMA Acknowledge signals. These signals are active Low and are used to acknowledge DMA requests (DRQ0-7)

Pin Symbols preceded by '/' are active low. Pin Type I = Input; O = Output; (TTL) = TTL level buffer; (CMOS) = CMOS level buffer. Pin Numbers to the left of '/' are for 160 pin flat pack. Numbers to the right are for the 180 pin PGA. PU = Pull Up; PD = Pull Down.

GC101 Peripheral Controller - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
/DMAAEN	O(B2)	137/155		DMA Address Enable signal. /DMAAEN is active Low when a DMA access is in operation.
DRQ0-3 DRQ5-7	I(TTL)	150-53/168-71 154-56/172-74	PD	DMA Requests signals. These active High signals are used to request DMA services or control of the system. Each signal should be held High until the corresponding DACK signal goes Active. DRQ0-3 will perform 8-bit DMA transfer. DRQ4-7 will perform16-bit DMA transfer.
DT/R	O(B2)	115/127		Data Transmit/Receive signal. When High, DT/R indicates data flow from CPU to SD0-15 bus; when Low, DT/R indicates data flow in the opposite direction.
/ERROR	I(TTL)	121/136	PU	This signal is active Low when 80287 has an unmasked error condition.
HISPEED	I(TTL)	123/140	PU	When HISPEED is active (high), the processor clock will run at half the CLK*2 clock. Otherwise the processor clock will run at one fourth CLK*2. Bus I/O speed is handled separately.
INTR	O(B2)	130/148		INTerrupt Request from the master Interrupt Controller INT output, is active High.
/IOCHCK	I(TTL)	11/14	PU	I/O CHannel Check. This signal is active low and indicates an error condition from an I/O device. The error condition will interrupt the CPU when enabled through NMI (Non-Maskable Interrupt) output.
IOCRDY	I(TTL)	10/13	PD	I/O Channel Ready signal. IOCHRDY is held Low by the I/O or memory devices to lengthen the cycles by an integral number of clock cycles. This signal should not be held Low for more than 2.5 microseconds or memory data can be lost due to inadequate refresh.
/IOCS16	I(TTL)	13/16	PU	I/O Chip Select 16 signals the CPU that the data transfer is a 16-bit, one-wait state I/O cycle. This signal should be driven by open collector or 3-state driver.
/IOR	I(TTL) O(B4)	31/35	PU	I/O Read signal from 82288 to read from peripheral devices, active Low.
/IOW	I(TTL) O(B4)	32/36	PU	I/O Write signal from 82288 to write to peripheral devices, active Low. TTL Input Buffer.

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GC101 Peripheral Controller - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
IOHALFSP	I(TTL)	124/142	PU	This signal controls the frequency of SYSCLK. When this signal is high and HISPEED is high, I/O will run at half the cpu clock. When HISPEED is low, I/O runs at the cpu clock speed. When IOHALFSP is low,I/O will run at the same speed as the cpu clock regardless of the state of HISPEED.
IRQ3-5 IRQ6-7 IRQ9-12 IRQ14-15	I(TTL) I(TTL) I(TTL) I(TTL)	157-159/176-178 1-2/2,4 4-7/7-10 8-9/11-12	PD	These are active High signals that interrupt the CPU.
/IRQ8	I(TTL)	3/6	PU	This signal is connected to the real time clock interrupt output.
/LSBEN	O(B2)	112/124		Least Significant Byte Enable signal. When Low, /LSBEN enables low-byte data.
/LCSROM	O(B4)	23/27		Latch Chip Select ROM signal, which selects the ROM address space 0E0000-0FFFFF and FE0000-FFFFFF.
/MASTER	I(TTL)	12/15	PU	/MASTER is an active Low signal and is used with the DRQ and DACK lines to gain control of the system. Upon receiving DACK, an I/O processor can pull /MASTER Low to gain control of the system address, data, and control buses.
M/IO	I(TTL)	87/99	PU	Memory I/O signal. When High, M/IO indicates a memory cycle; when Low, M/IO indicates an I/O cycle.
MBDIR	O(B2)	111/123		Memory Buffer Direction Signal. When MBDIR is High, data flows from MD0-15 to SD0-15; when MBDIR is Low, the data flows in the opposite direction.
/MDPCKN	I(TTL)	118/130	PU	Memory Data Parity Check signal. When Low, /MDPCKN indicates memory failure on parity test.
MDPCKE	O(B2)	117/129		Memory Data Parity Check Enable Signal. When High, MDPCKE selects parity checking logic.
/MEMCS16	I(TTL)	14/17	PU	Memory Chip Select 16 signals the CPU that the data transfer is a 16-bit, one-wait state I/O cycle. This signal should be driven by open collector or trisate driver.
/MEMR	I(TTL) O(B4)	28/32	PU	Memory Read signal. /MEMR is active Low during memory read and is 3-stated when CPUHLDA is High.

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GC101 Peripheral Controller - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
/MEMW	I(TTL) O(B4)	29/33	PU	Memory Write signal. /MEMW is active Low during memory write and is tristated when CPUHLDA is High.
/MSBEN	O(B2)	113/125		Most Significant Byte Enable signal. When Low, /MSBEN enables high-byte data.
NMI	O(B2)	129/147		Non-Maskable Interrupt signal. NMI is an active High signal that forces the CPU to execute the interrupt routine under any conditions.
/NPCS	O(B2)	131/149		Numeric Processor Chip Select signal. /NPCS is an active Low signal that ties to the NPS1 pin of 80287.
OSC	O(B4)	21/25		Oscillator is the 14.3818 MHZ color burst signal and is not synchronous with the SYSCLOCK.
OPTBUFUL	I(TTL)	125/143	PD	Output Buffer Full signal from keyboard controller P24. This signal is connected to IRQ1, which interrupts the CPU when the keyboard buffer is full.
/P0WERG00D	I(CMOS)	25/29	PD	This signal, when Low, resets the controller. Schmitt Trigger Input.
PROCCLK	O(B8)	97/109		Processor Clock is the output signal that ties to the clock input of the CPU and the numeric processor.
RAM0RAS	O(B2)	33/37		This signal selects RAM bank 0 RAS control.
RAM1RAS	O(B2)	34/38		This signal selects RAM bank 1 RAS control.
RAM0CAS	O(B2)	35/39		This signal is the same as RAM0RAS except during refresh.
RAM1CAS	O(B2)	36/40		This signal is the same as RAM1RAS except during refresh.
RC	I(TTL)	126/144	PU	Reset CPU signal. This is an active Low signal from keyboard controller P21 and causes CPU shutdown.
/READY	O(B2)	128/146		/READY is an active Low signal that indicates to the CPU that the current bus cycle is near completion.
/REFRESH	I(TTL) O(B4)	17/20	NO	Refresh indicates the current cycle is for memory refresh and can be driven Low by devices on the I/O channel. Open Drain Outputs.

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GC101 Peripheral Controller - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
/RESET	O(B4)	22/26	NO	This signal is active Low and is used to reset system logic at power-up or low-line voltage outage. Open Drain Outputs.
RESETCPU	O(B2)	116/128		This is an active High signal that resets 80286 CPU during powerup, keyboard reset, and during a halt status.
RESET287	O(B2)	132/150		Reset 80287 is an active High signal that resets 80287 co-processor.
RSEL2	O(TTL)	76/84	PU	RAM Select 2 signal. When High, RSEL2 selects 1MBIT DRAM; when Low, RSEL2 selects 256K -bit RAM.
RSEL1,0	I(TTL)	75,74/83,82		RSEL 2,1,0 as follows: 0 0 0 selects 0-256K 0 0 1 selects 0-512K 0 1 0 selects 0-640K 0 1 1 selects 0-640K, 1M-1.384M 1 0 0 selects 0-512K 1 0 1 selects 0-640K 1 1 0 selects 0-640K, 1M-2.384M 1 1 1 selects 0-640K, 1M-4.384M
RTCAS	O(B2)	136/154		Real Time Clock Address Strobe signal. When Low, RTCAS latches the RAM address for Read/Write operations.
/RTCRD	O(B2)	134/152		Real Time Clock Read signal. When Low, /RTCRD data is read from the RTC
/RTCWR	O(B2)	135/153		Real Time Clock WRite signal. When Low,/RTCWR data is written to the RTC.
SA0	I(TTL)/O(B6)	30/34	PU	I/O Slot Address bus 0. This signal enables the low byte SD0-7.
SD0-15	I(TTL) O(B6)	37-54/41-62	PU	I/O Slot Data bus bits 0-15. These support 8/16 bit data transfer from I/O slots to CPU.
/SMEMR	O(B4)	26/30		System MEMory Read, which is the buffered version of /MEMR, active Low. 3-State Output Buffer
/SMEMW	O(B4)	27/31		System MEMory Write, which is the buffered version of /MEMW, active Low. 3-State Output Buffer
/S0,/S1	I(TTL)	83,84/95,96		Status 0,1 signals are used to convey the current CPU status to the 80288 bus controller

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GC101 Peripheral Controller - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
SPKR	O(B4)	24/28		Output of the Timer 8254 Channel 2.
SYSCLK	O(B4)	18/22		System Clock is synchronous with the CPU clock. See Table 1.
T/C	O(B2)	142/160		Terminal Count signal. T/C will pulse when the DMA channel terminal count is reached.
XA0	I(TTL) O(B4)	55/63	PU	External Address 0 is the signal that enables the Low byte of the data bus.
XA1-9 XA10-16	I(TTL)/O(B4) I(TTL)/O(B4)	56-66/64-74 67-73/75-81	PU	External Address 1-16 are the external address lines that tie to EPROM, keyboard, the numeric processor, etc. XA10-16 are 3-State Buffers.
XBHE	I(TTL) O(B4)	77/86	PU	External Bus High Enable signal activates the High byte of the data bus.
XD0-7	I(TTL) O(B4)	89-96/101-108	PU	External data bus bits 0-7. These support only 8-bit data transfers from external devices such as clock chip, serial port, etc., to CPU.
/XDEVEN	I(TTL)	81/93	PU	External Device Enable signal. /XDEVEN is an active Low signal that gates external devices to the SD bus.
/XMEMW /XMEMR /XIOW /XIOR	I/O(B4) I/O(B4) I/O(B4) I/O(B4)	99/111 98/110 103/115 102/114	PU	When /DMAAEN is not active, external memory and external I/O commands follow M/IO commands. When /DMAAEN is active, external M/IO commands have control of the operations. TTL Input Buffers
X1 X2	I(CMOS) I(B64)	16/19 15/18	NO	Xl and X2 are inputs tied to a 14.31818 MHz crystal to create OSC output.
0WS	I(TTL)	88/100		Zero Wait State is an active Low signal that cues the CPU to complete the present memory or I/O data transfer without inserting additional wait states. This signal should be driven by open collector or 3-state driver.

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GC101 Peripheral Controller - AC Characteristics

Parameter	Time(ns)	
A0 Setup (to PROCCLK)	8	
A0 Hold	0	
A17-23 Setup (to PROCCLK)	10	
A17-23 Hold	0	
AEN Delay (from CPUHLDA)	18	(50pf)
BALE Delay (to PROCCLK)	9	(50pf)
BHE Setup (to PROCCLK)	6	
/BUSY286 Delay (from /XIOW)	15	(25pf)
CNTLOFF Delay (from PROCCLK)	11	(25pf)
CPUHRQ Delay (from SYSCLK)	15	
CPUHRQ Delay (from /XIOW)	19	(25pf)
/DACK0-3,5-7 Delay (from SYSCLK)	85	
/DMAAEN Delay (from SYSCLK)	81	(25pf)
DRQ0-3,5-7 Setup (to SYSCLK)	0	
DT/R Delay (from PROCCLK)	9	(25pf)
INTR Delay (from IRQ3-15,OPTBUFUL)	60	(25pf)
IOCRDY Setup (to SYSCLK)	12	
IOCRDY Hold	0	
/IOCS16 Setup (to PROCCLK)	9	
/IOCS16 Hold	0	
/IOR Delay (from PROCCLK)	17	
/IOR Delay (from SYSCLK)	86	
/IOW Delay (from PROCCLK)	17	
/IOW Delay (from SYSCLK)	86	
/LSBEN Delay (from PROCCLK)	9	(25pf)
MBDIR Delay (from PROCCLK)	15	(25pf)
MBDIR Delay (from /XMEMR)	14	
MDPCK Setup (to /XMEMR)	13	
/MDPCKN Delay (from PROCCLK)	16	(25pf)
/MEMCS16 Setup (to PROCCLK)	6	
/MEMCS16 Hold	0	
/MEMR Delay (from PROCCLK)	10	
/MEMW Delay (from PROCCLK)	10	
/M/IO Setup (to PROCCLK)	16	
/M/IO Hold	0	
/M/IO Setup (to A1,/A0,/S1)	1	
/M/IO Hold	3	
/MSBEN Delay (from PROCCLK)	9	(25pf)

Parameter	Time(ns)	
/MSBEN Delay (from XBHE)	14	
NMI Delay (from /XIOW)	17	(25pf)
/NPCS Delay (from PROCCLK)	16	(25pf)
OSC Frequency	14.31818MHz	
PROCCLK Delay (from CLK*2)	21	
PROCCLK Period	31	
RAM0CAS Delay (from PROCCLK)	14	(25pf)
RAM1CAS Delay (from PROCCLK)	14	(25pf)
RAM0RAS Delay (from PROCCLK)	14	(25pf)
RAM1RAS Delay (from PROCCLK)	14	(25pf)
RC Pulse Width	8	
/READY Delay (from PROCCLK)	6	(25pf)
RESET287 Delay (from /XIOW)	10	(25pf)
RESETCPU Delay (from SYSCLK)	9	(25pf)
/RESET Delay (from PROCCLK)	12	
RTCAS Delay (from /XIOR,/XIOW)	10	(25pf)
/RTCRD Delay (from /XIOR)	6	(25pf)
/RTCWR Delay (from /XIOW)	6	(25pf)
/S0, /S1 Setup (to PROCCLK)	18	
/S0, /S1 Hold	0	
SA0 Delay (from PROCCLK)	16	
(from CPUHLDA)	17	
SYSCLK Delay (from PROCCLK)	10	
XA0-9 Hold (to /XIOW)	26	
XD0-7 Delay (from /XIOR)	30	(50pf)
XD0-7 Setup (to /XIOW)	59	
XD0-7 Hold	25	
/XIOR Delay (from SYSCLK)	82	(50pf)
/XIOR Delay (inactive from PROCCLK)	12	
/XIOR Delay (active from PROCCLK)	17	
/XIOW Delay (from SYSCLK)	82	(50pf)
/XIOW Delay (inactive from PROCCLK)	12	
/XIOW Delay (active from PROCCLK)	17	
/XMEMR Delay (from SYSCLK)	82	(50pf)
/XMEMW Delay (from SYSCLK)	82	(50pf)
0WS Setup (to PROCCLK)	16	
0WS Hold	0	

These ratings are minimums for setup/hold time, maximums for delay. All output loadings are 85pf except where noted. These are worst case ratings.

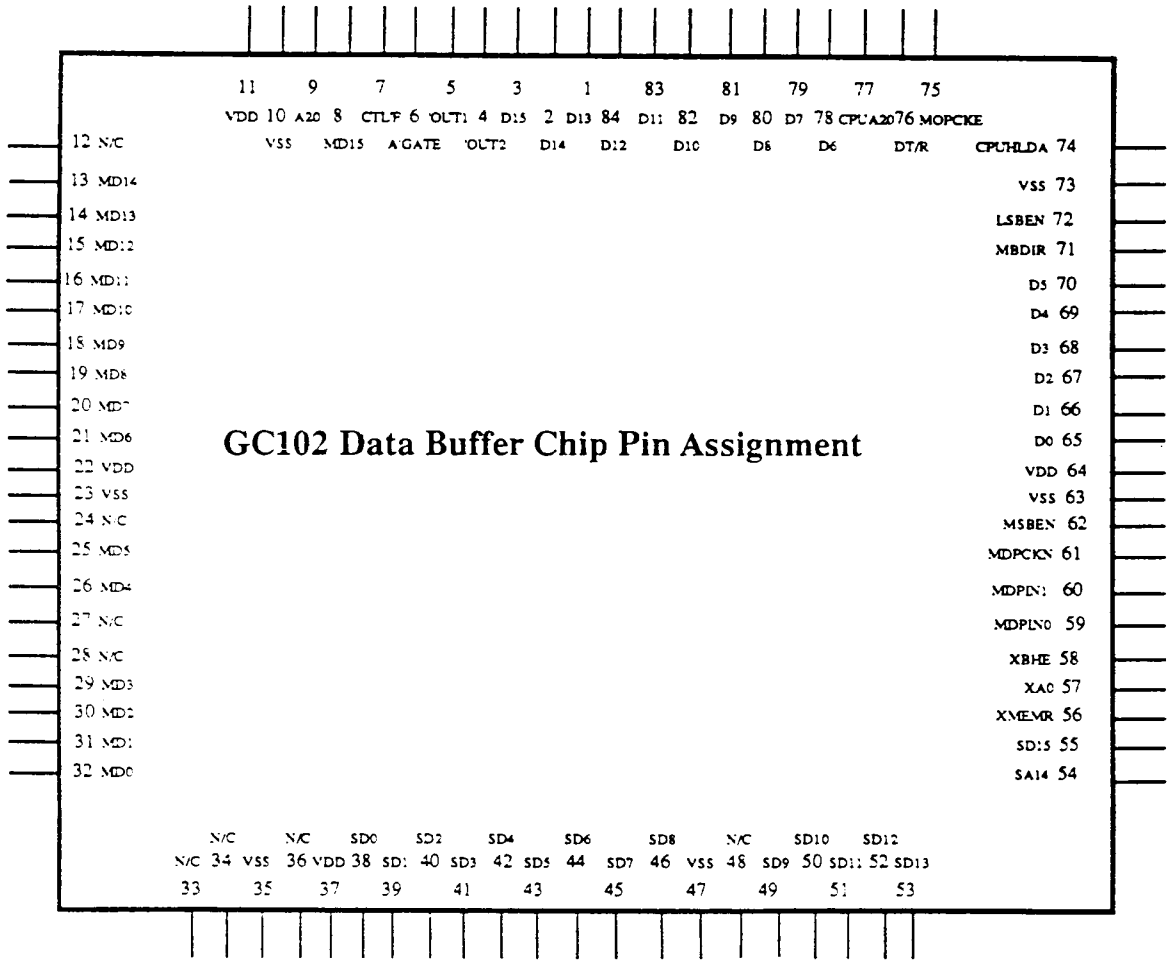
GC102 Data Buffer Chip

The GC102 Data Buffer chip buffers data for the CPU, the Expansion bus and the Memory data bus. Two signals control data flow direction. The DT/R signal controls data flow between the CPU data bus and the Expansion data bus. The MBDIR signal controls data flow between the Expansion bus and the Memory data bus.

Clocked by the CNTLOFF signal, latching is provided for data between the Expansion bus and the CPU bus.

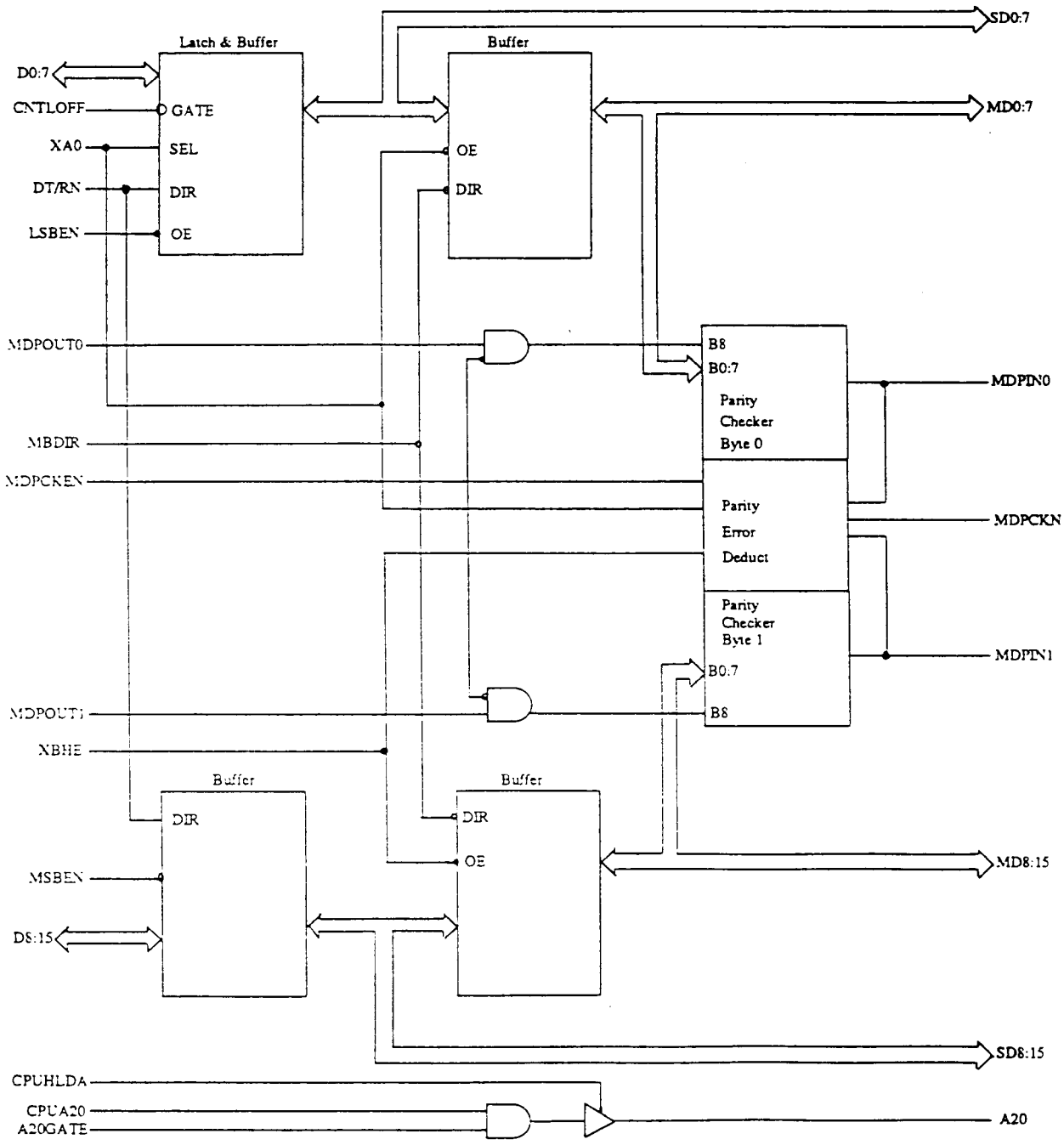
The GC102 Data Buffer chip also includes parity logic circuitry. During memory read cycles, the parity bits for byte 0 and byte 1 from the RAMs are connected to pins MDPOUT0 and MDPOUT1 as the ninth input to the 9-bit parity error detect circuits. The other eight inputs come from the Memory data bus.

When the output signal MDPCKN is enabled and an error is detected on either byte 0 or byte 1 of the Memory data bus, MDPCKN will be active (low). During memory write cycles, parity bits for byte 0 and byte 1 are generated through on-board parity generator circuitry and then output through the MDPIN0 and MDPIN1 pins and written to RAM. (Pin 73 = VSS)



GC102 Data Buffer Chip Pin Assignment

GC102 Data Buffer Chip Block Diagram



GC102 Data Buffer - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
A20	O(B12)	9		Address bit 20 of the CPU conditioned by A20GATE signal. 3-State Output Buffer.
A20G	I(TTL)	6		With a High on A20Gate and Low on CPUHLDA, A20 is the same state as that generated from the CPU. A Low on A20GATE and Low on CPUHLDA results in A20 being Low.
CNTLOFF	I(TTL)	7		An active High input to enable the low-byte data bus latch.
CPUA20	I(TTL)	77		Address bit 20 from CPU. This signal is conditioned by the A20GATE signal.
CPUHLDA	I(TTL)	74		CPU Hold Acknowledge signal. When High, the address bit 20 (A20GATE) is 3-stated. When CPUHLDA is Low, A20 is the same as the CPUA20 conditioned by A20GATE.
D0-D5 D6-D12 D13-D15	I/O(B6)	65-70 78-84 1-3	PU	Bidirectional Data Bus signals to and from the CPU.
DT/R	I(TTL)	76		Data Transmit/Receive signal. Indicates the direction of data flow between the D and SD buses. When DT/R is HIGH, data flows from D to SD. When DT/R is LOW data flows from SD to D.
/LSBEN	I(TTL)	72		Active Low to enable low-byte data transfer between D and SD buses.
MBDIR	I(TTL)	71		MD/SD bus directional control signal. When MBDIR is High, data flows from MD bus to SD bus; When MBDIR is Low, data flows from SD bus to MD bus.
MD0-MD3 MD4-MD5 MD6-MD14 MD15	I/O(B6) I/O(B6) I/O(B6) I/O(B6)	32-29 26-25 21-13 8	PU	On board memory data bus.
MDPCKE	I(TTL)	75		Memory Data Parity CheckK Enable signal. When High, MDPCKE enables the parity checking during memory read. TTL Input Buffer
/MDPCKN	O(B6)	61	PU	Memory Data Parity Check signal. Active Low to indicate a parity error during memory read.
MDPIN0 MDPIN1	O(B6)	59,60	PU	Memory data low and high parity bits. As generated, these signals are written into the RAMs during RAM write cycles.

Pin Symbols preceded by '/' are active low. Pin Type I = Input; O = Output; (TTL) = TTL level buffer; (CMOS) = CMOS level buffer. PU = Pull Up; PD = Pull Down.

GC102 Data Buffer - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
MDPOUT0 MDPOUT1	I(TTL)	4,5		Memory Data Low and High parity bit signals. These signals read data from the RAMs to generate parity check during read cycles.
/MSBEN	I(TTL)	62	PU	Active High to enable High-byte data transfer between D and SD buses. TTL Input Buffer.
VSS		10,23,35,47,63,73		GROUND
VDD		11, 22, 37, 64		POWER: +5 Volt Supply
[floating] [floating]		12, 24, 27-28 33-34, 36, 48		NOT CONNECTED NOT CONNECTED
SD0-SD8 SD9-SD15	I/O(B6)	38-46 49-55	PU	Expansion data bus, which makes possible data transfer between the D and MD buses.
XA0	I(TTL)	57		Local I/O bus address bit 0. This input enables the data transfer between the low byte of the SD and MD buses.
XBHE	I(TTL)	58		Local I/O Bus High Enable signal. This signal enables the data transfer between the high byte of the SD and MD buses.
/XMEMR	I(TTL)	56		Memory Read signal. This input enables the parity circuit during RAM read operations.

Pin Symbols preceded by '/' are active low. Pin Type I = Input; O = Output; (TTL) = TTL level buffer; (CMOS) = CMOS level buffer. PU = Pull Up; PD = Pull Down.

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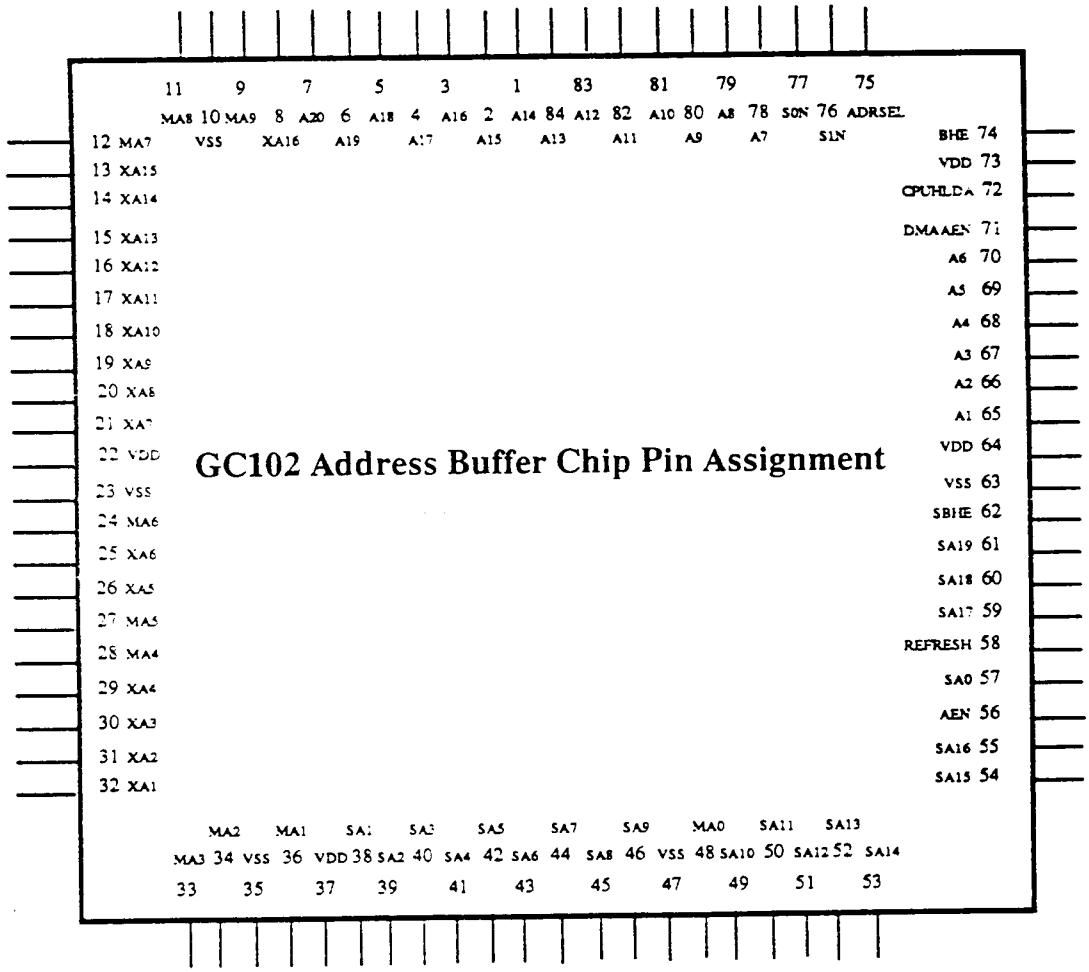
GC102 Data Buffer Chip -- AC Characteristics

Input	Output	Typical (ns)	WCCOM (ns)
any D	any SD	9.95	18.6
any D	any MD	10.31	19.3
LSBEN	any SD	10.98	20.5
LSBEN	any MD	11.86	22.2
LSBEN	any D	13.98	26.2
MSBEN	any SD	10.86	20.3
MSBEN	any MD	11.80	22.1
MSBEN	any D	9.28	17.4
DT/R	any SD	10.26	19.2
DT//R	any D	13.68	25.6
DT/R	any MD	11.59	21.7
SD	CBA (setup-time)	5.92	11.1
SD	CBA (hold-time)	0.00	
SD	any D	9.99	18.7
SD	any MD	8.53	16.0

Input	Output	Typical (ns)	WCCOM (ns)
XA0,XBHE	any MD	9.59	18.0
XA0,XBHE	any SD	11.51	21.5
XA0,XBHE	any D	13.64	25.5
XA0,XBHE	MDPCK	10.29	19.3
MBDIR	any MD	11. 92	22.3
MBDIR	any SD	10.69	20.0
MBDIR	any D	13.9	24.9
any MD	MDPIN0, MDPIN1	12.88	24.1
any MD	MDPCK	13.58	25.4
MDPCKEN	MDPCK	10.89	20.4
XMEMR	MDPIN0, MDPIN1	10.06	18.8
XMEMR	MDPCK	10.39	19.5
CPUHLDA	A20	5.03	9.4
CPUA20	A20	9.20	17.2
A20GATE	A20	6.43	12.0

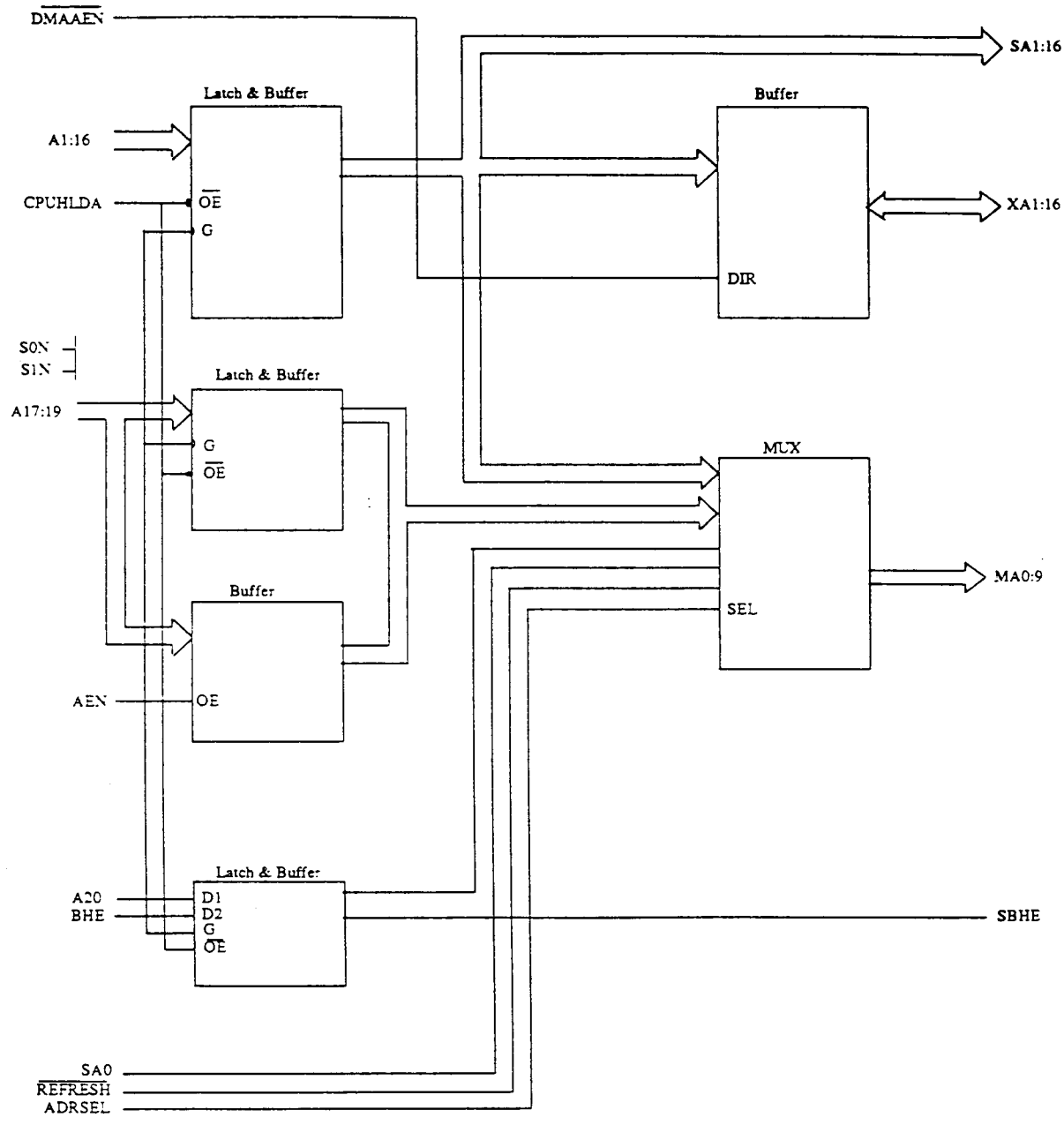
GC102 Address Buffer Chip

The GC102 Address Buffer chip provides address buffers for the Expansion bus, the Local I/O bus and the system board DRAMs. Early ALE is included to latch the address from the CPU. The /DMAAEN signal controls the address flow direction between the Expansion bus and Local I/O bus. The CPUHLDA signal controls the direction of address flow from the CPU to the Expansion bus. By multiplexing the address bits of the Expansion bus (via ADRSEL and /REFRESH), the Memory address bus (MA0:9), which drives the system board DRAMS, is generated. Ten bits of address allow for either 256K or 1 Mbit DRAMs. (Pin 73 = VDD)



GC102 Address Buffer Chip Pin Assignment

GC102 Address Buffer Chip Block Diagram



GC102 Address Buffer - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
A1-A6	I(TTL)	65-70	PU	Address input signals from CPU. These are latched when both /S0 and /S1 are High.
A7-A13	I(TTL)	78-84		
A14-A16	I(TTL)	1-3		
A17-A20	I(TTL)	4-7		
ADRSEL	I(TTL)	75		Address Select signal. ADRSEL controls the generation of the RAS and CAS addrresses on the MA bus for addressing the system RAMs.
AEN	I(B6)	56	PU	Address Enable signal. This pin conveys the A17-A19 signals directly into SA17-SA19, respectively.
BHE	I(TTL)	74		Bus High Enable signal. Transmitted from the CPU, BHE indicates a data transfer on the most significant byte of the bus.
CPUHLDA	I(TTL)	72		CPU Hold Acknowledge signal. When CPUHLDA is Low, the address latches drive the SA bus.
DMAAEN	I(TTL)	71		DMA Address ENable signal. DMAAEN controls the direction of data transfer between SA and XA buses. When DMAAEN is High, data flows from SA to XA.
MA0	O(B12)	48		Address signals for addressing system RAMs;
MA1	O(B12)	36		MA9 is for 1MB DRAMs.
MA3-MA2	O(B12)	33,34		3-State Output Buffers
MA5-MA4	O(B12)	27,28		
MA6	O(B12)	24		
MA8-MA7	O(B12)	11,12		
MA9	O(B12)	9		
/REFRESH	I(TTL)	58		Refresh active LOW signal. This signal selects SA0 as MA6 during refresh.
SA0	I(TTL)	57		Address bit 0 signal. SA0 is used during refresh. Bidirectional signals for the expansion bus.
SA1-SA9	I/O(B6)	38-46		
SA10-SA16	I/O(B6)	49-55		
SA17-SA19	I/O(B6)	59-61		
SBHE	O(B6)	62	PU	Bus High Enable signal for the expansion bus. This signal is the output of the BHE latch.
/S1	I(TTL)	76		CPU Status output signals. /S1 and /S0 generate the clock signals for
/S0	I(TTL)	77		the address latches in this chip.
VSS		10, 23, 35, 47, 63		GROUND

Pin Symbols preceded by '/' are active low. Pin Type I = Input: O = Output; (TTL) = TTL level buffer; (CMOS) = CMOS level buffer. PU = Pull Up: PD = Pull Down.

GC102 Address Buffer - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
VDD		22, 37, 64, 73		POWER: +5 Volts Supply
XA1-XA4	I/O(B6)	32-29	PU	Peripheral address signals for the local bus
XA5-XA6	I/O(B6)	26-25		
XA7-XA15	I/O(B6)	21-13		
XA16	I/O(B6)	8		

Pin Symbols preceded by '/' are active low. Pin Type I = Input; O = Output; (TTL) = TTL level buffer; (CMOS) = CMOS level buffer. PU = Pull Up; PD = Pull Down.

GC102 Address Buffer Chip -- AC Characteristics

Input	Output	Typical (ns)	WCCOM (ns)
$\overline{\text{any A}}$	$\overline{\text{any SA}}$	9.95	18.6
$\overline{\text{BHE}}$	$\overline{\text{SBHE}}$	8.76	16.4
$\overline{\text{S0 or S1}}$	$\overline{\text{any SA}}$	11.77	22.0
$\overline{\text{CPUHLDA}}$	$\overline{\text{any SA}}$	10.58	21.2
$\overline{\text{CPUHLDA}}$	$\overline{\text{SBHE}}$	8.46	15.8
$\overline{\text{AEN}}$	$\overline{\text{SA17,18,19}}$	10.78	20.2
$\overline{\text{any SA}}$	$\overline{\text{any XA}}$	8.49	15.9
$\overline{\text{any XA}}$	$\overline{\text{any SA}}$	8.39	15.7
$\overline{\text{any SA (SA0)}}$	$\overline{\text{any MA}}$ MA8	7.45 8.38	14.0 15.7

Input	Output	Typical (ns)	WCCOM (ns)
$\overline{\text{any XA}}$	$\overline{\text{any MA}}$	8.64	16.2
$\overline{\text{DMAAEN}}$	$\overline{\text{any XA}}$	11.92	22.3
$\overline{\text{DMAAEN}}$	$\overline{\text{any SA}}$	10.69	20.0
$\overline{\text{REFRESH}}$	$\overline{\text{MA}}$	8.05	15.1
$\overline{\text{ADRSEL}}$	$\overline{\text{MA}}$ MA8	8.29 9.40	15.5 17.6
$\overline{\text{any A}}$	$\overline{\text{MA}}$ MA8	10.22 11.50	19.1 21.5

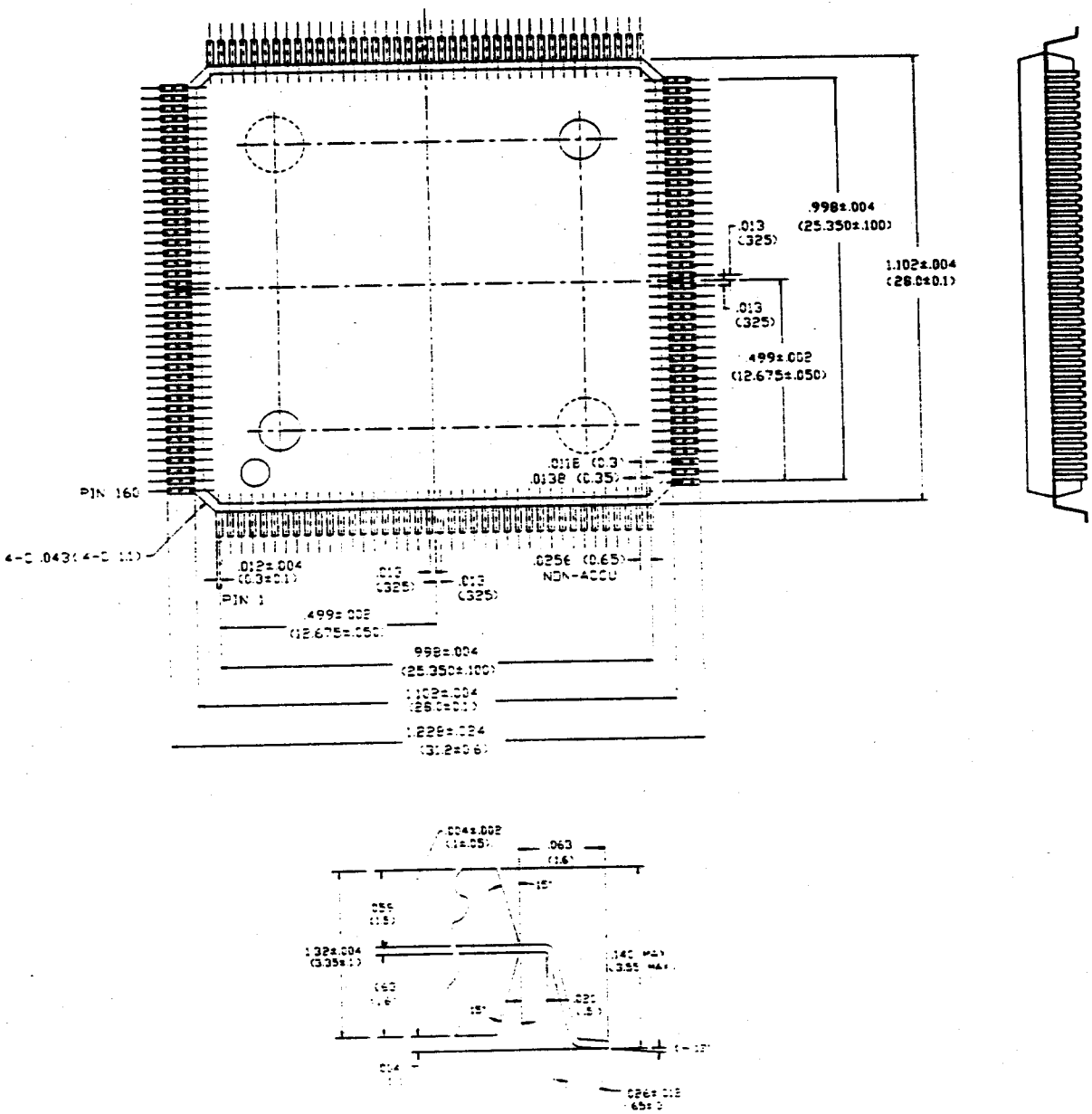
GC 101 / GC102 Chip Set - DC Characteristics

Specified at VDD = 5V +/-5% over the commercial temperature range (0-70C).

Symbol	Parameter	Condition	Min	Max	Units
VIL	Voltage Input LOW - TTL Inputs			0.8	V
VIH	Voltage Input HIGH -TTL Inputs		2.0		V
IIN	Input Current, TTL, CMOS Inputs	Vin = Vdd or Vss	-10	10	uA
	Inputs with Pull Down Resistors	Vin = Vdd	10	120	uA
	Inputs with Pull Up Resistors	Vin = Vss	-100	-8	uA
IDD	Quiescent Supply Current	Vin = Vdd or Vss		4	mA

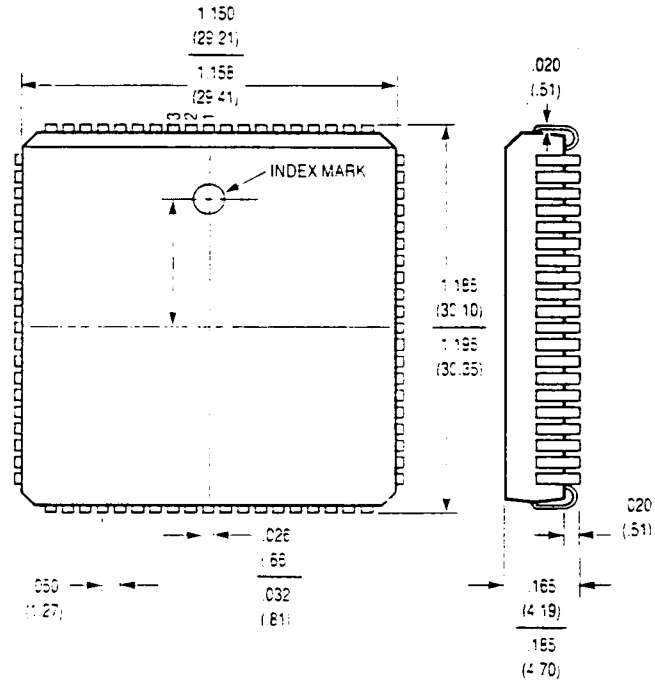
GC101

MECHANICAL SPECIFICATIONS

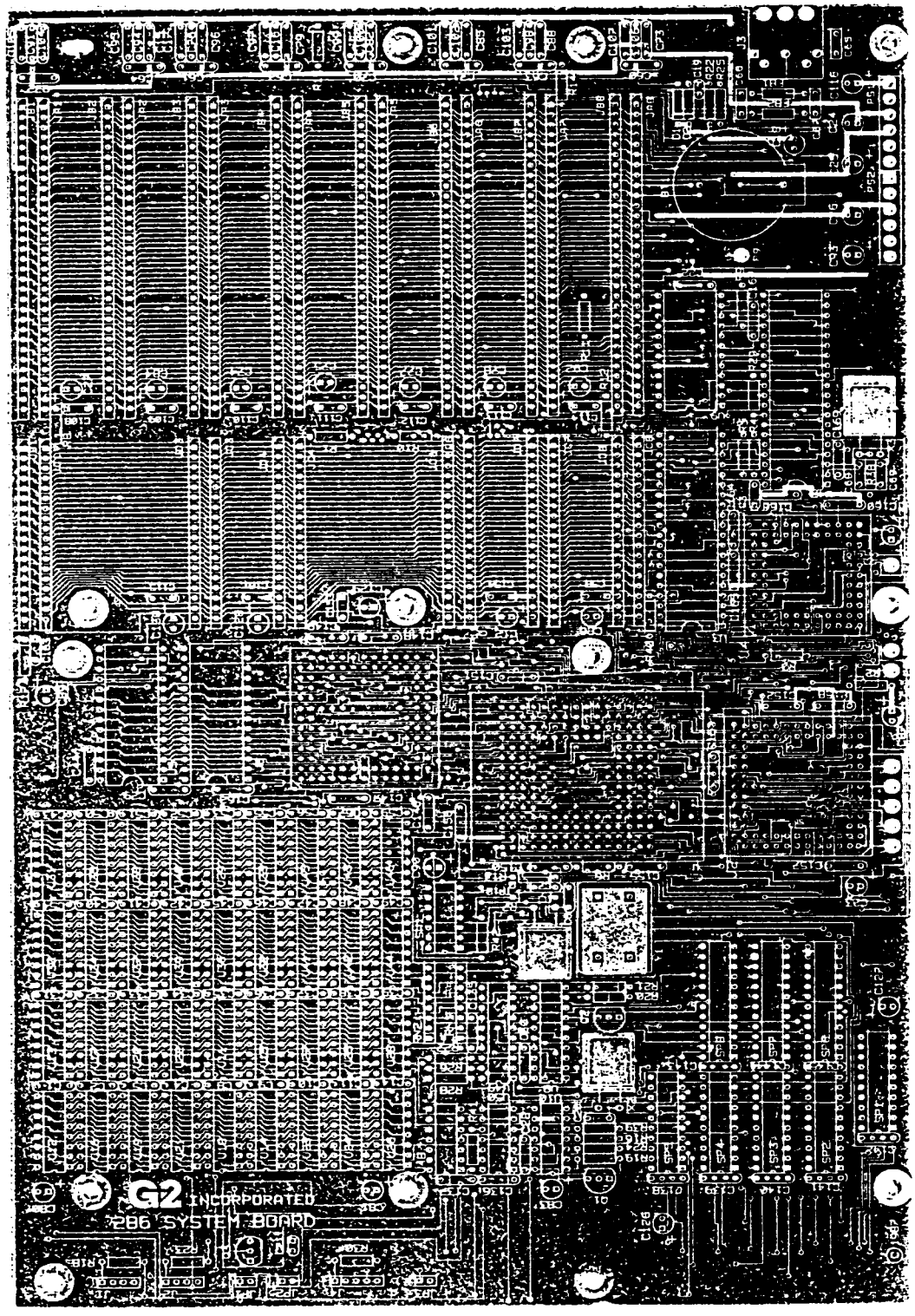


GC102

MECHANICAL SPECIFICATIONS



Prototype System Board Layout

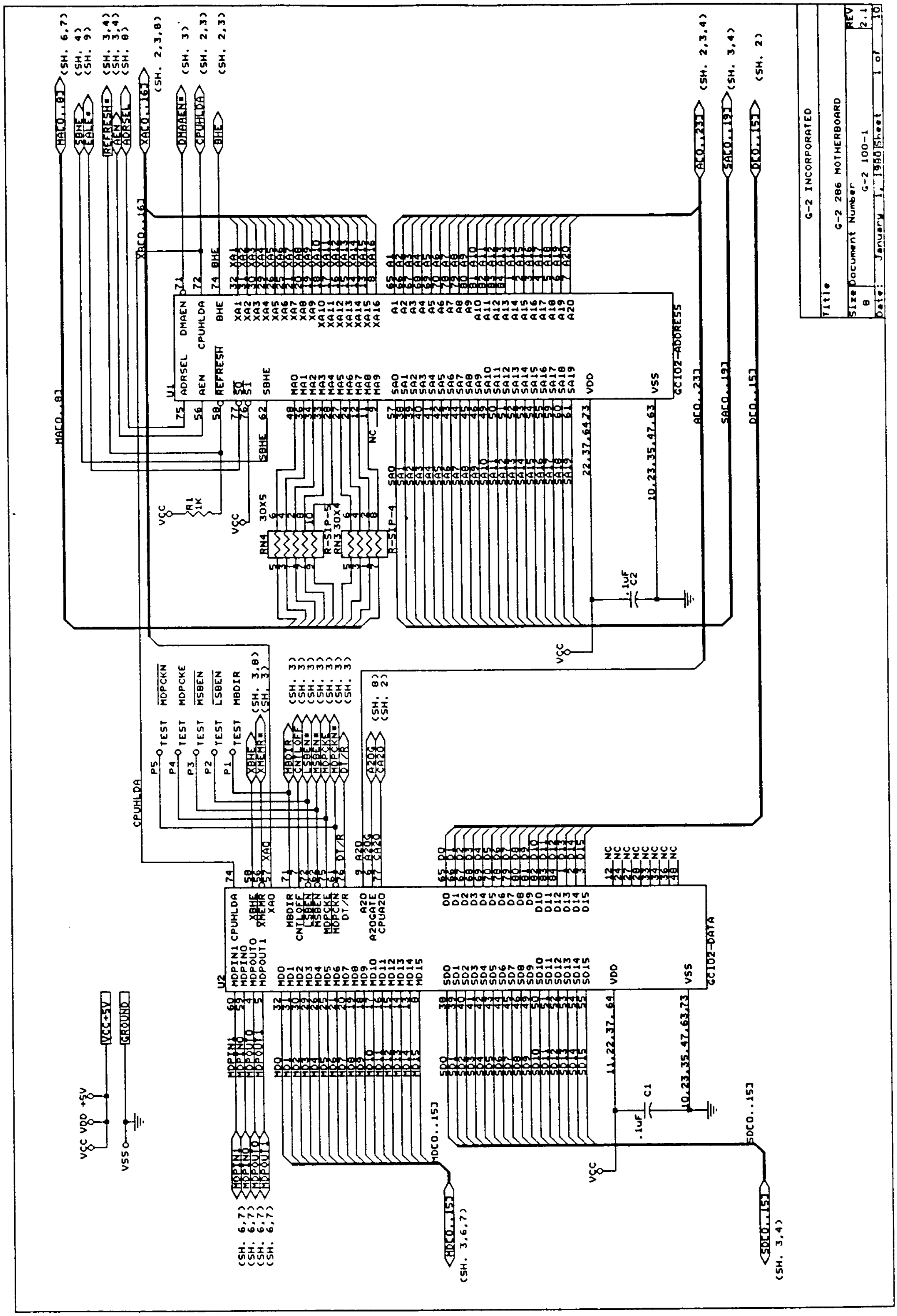


Device List for Prototype System Board

Device	Location on System Board
GC101	U7
GC102	U1, U2
4.7nf	C19
15pf	C68, C69
27pf	C20
47pf	C65, C67, C66
50pf NP	C6
100pf NP	C7
0.01 uf	C21
0.047uf	C3, C108, C109, C110, C111, C112, C113, C114, C115
0.1uf	C1, C2, C4, C5, C8, C9, C10, C11, C14, C15, C16, C17, C22, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63,C64, C70, C71, C72, C73, C76, C79, C82, C85, C88, C91, C94, C95, C96, C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C131, C132, C133, C134, C135, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C146, C147, C148, C149, C150, C151, C152, C153, C154, C155, C156, C157, C158, C159, C160, C161, C162, C163, C164, C165, C166, C167, C168, C169
10uf	C12, C13, C18, C23, C24, C25, C26, C27, C74, C75, C77, C78, C80, C81, C83, C84, C86, C87, C89, C90, C92, C93, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, C129, C130
1N914	D1, D2
2N3904	Q2, Q3
2N3906	Q1
DRAM-41256	U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U26, U27, U28, U29, U30, U31, U32, U33, U34, U35, U36, U37, U38, U39, U40, U41, U42, U43, U44, U45, U46
BATTERY	BT1
CONN\5	J4
CONN\2	JP1, JP2
CONN\4	J1, J2
CONN\6	PS1, PS2
CONN\6\KBD	J3
CONN\18	JC1, JC3, JC4, JC6, JC7, JC8, JD1, JD3, JD4, JD6, JD7, JD8
CONN\62	JA1, JA2, JA3, JA4, JA5, JA6, JA7, JA8, JB1, JB2, JB3, JB4, JB5, JB6, JB7, JB8

Device List for Prototype System Board

Device	Location on System Board
DELAY	U48
INDUCTOR	FB1, FB2
OSC\25MHZ	Y1
XTAL	X1, X2, X3
RES\15	R13, R40
RES\30	R11, R12, R23
RES\100	R42
RES\150	R30, R41
RES\300	R8, R9, R10, R17, R24
RES\1K	R1, R7, R14, R15, R22
RES\10K	R2, R3, R4, R5, R6, R16, R18, R21, R25, R26, R27, R28, R29, R39, R52, R53
RES\51K	R20
RES\2MEG	R38, R19
RNET\8P4R	RN1, RN2
SKT\14	U10, U50, U53
SKT/16	U52
SKT\20	U8, U49, U51, SP1, SP2, SP3, SP4, SP5
SKT\24	U9, SP6, SP7, SP8
SKT\28	U5, U6
SKT\40	U47, U3
SKT\68	U4
SW\DIP10	SW1
SW\SPST	JP3
CONN.PIN	JP4, JP5, JP6, JP7



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Size
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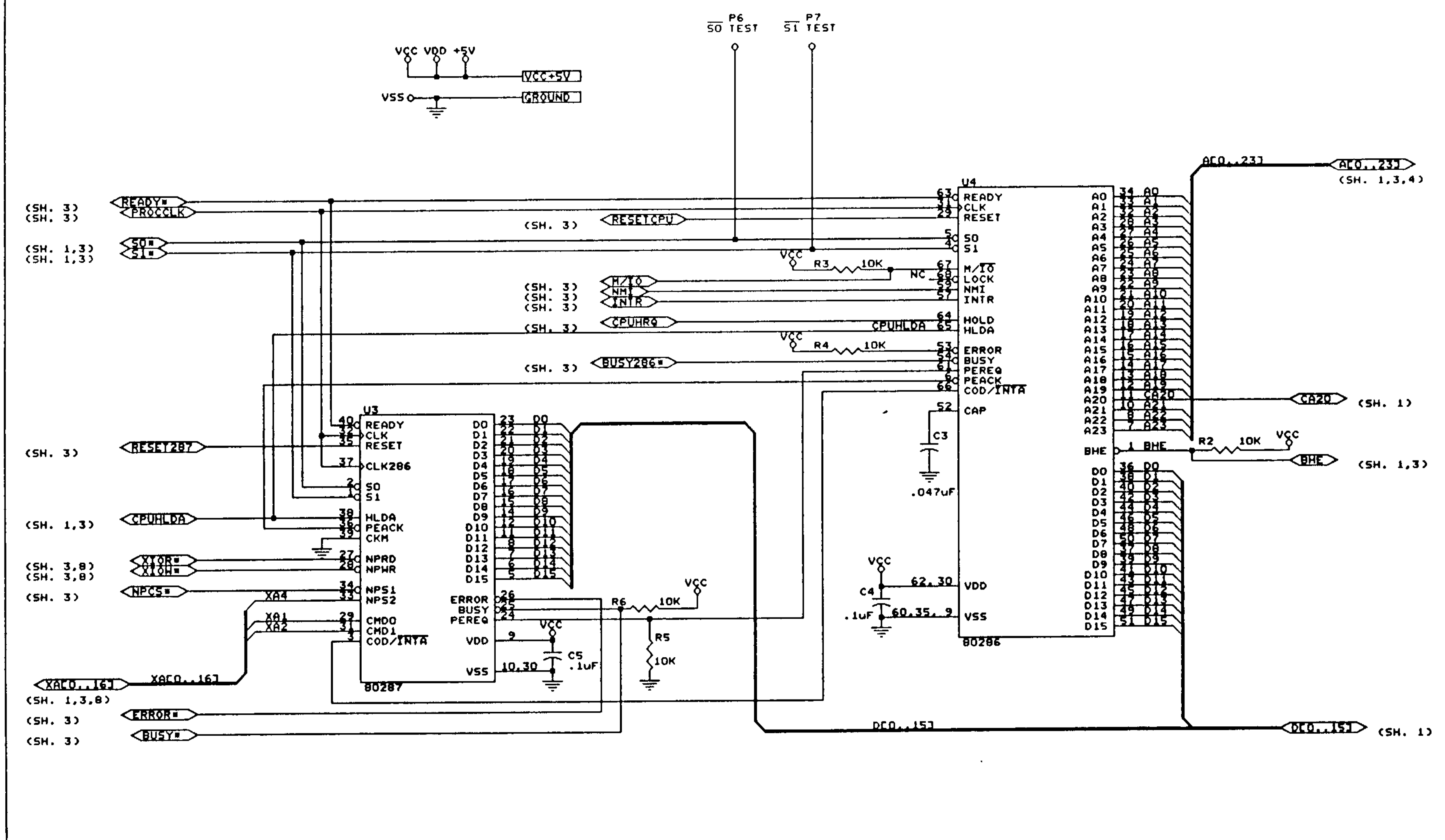
Document Number
G-2 100-1
REV
2.1
Date: January 1, 1990
Sheet 1 of 10
GC102-ADDRESS
GC102-DATA



S0 TEST P6
S1 TEST P7
VCC VDD +5V
VCC+5V
VSS
GROUND
READY*
PROCCLK
S0*
S1*
RESETCPU
M/IO
NMI
INTR
CPUHRQ
CPUHLDA
BUSY286*
RESET287
XIOR*
XIOW*
NPCS*
XA4
XA1
XA2
XA[0..16]
ERROR*
BUSY*
(SH. 3)
(SH. 1,3)
(SH. 3,8)
(SH. 1,3,8)
U4
80286
READY
CLK
RESET
S0
S1
M/IO
LOCK
NMI
INTR
HOLD
HLDA
ERROR
BUSY
PEREQ
PEACK
COD/INTA
CAP
VDD
VSS
NC
R3 10K
R4 10K
C3 .047uF
C4 .1uF
62,30
60,35,9
A[0..23]
(SH. 1,3,4)
CA20
(SH. 1)
BHE
R2 10K
(SH. 1,3)
D[0..15]
(SH. 1)
U3
80287
CLK286
CKM
NPRD
NPWR
NPS1
NPS2
CMD0
CMD1
R6 10K
R5 10K
C5 .1uF
10,30

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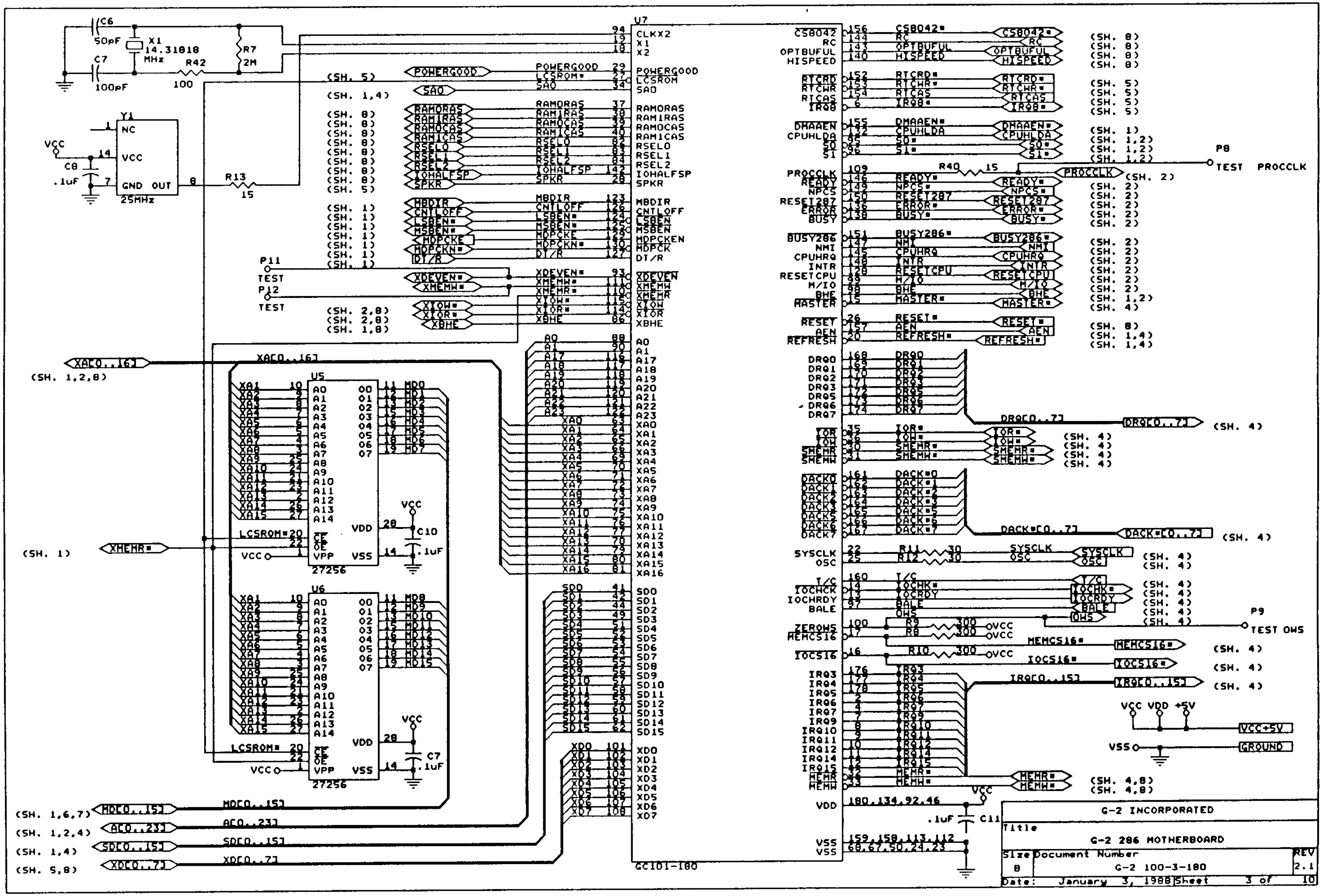
Size: B	Document Number: G-2 100-2		REV: 2.1
Date: January 3, 1988	Sheet 2 of 10		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Size Document Number
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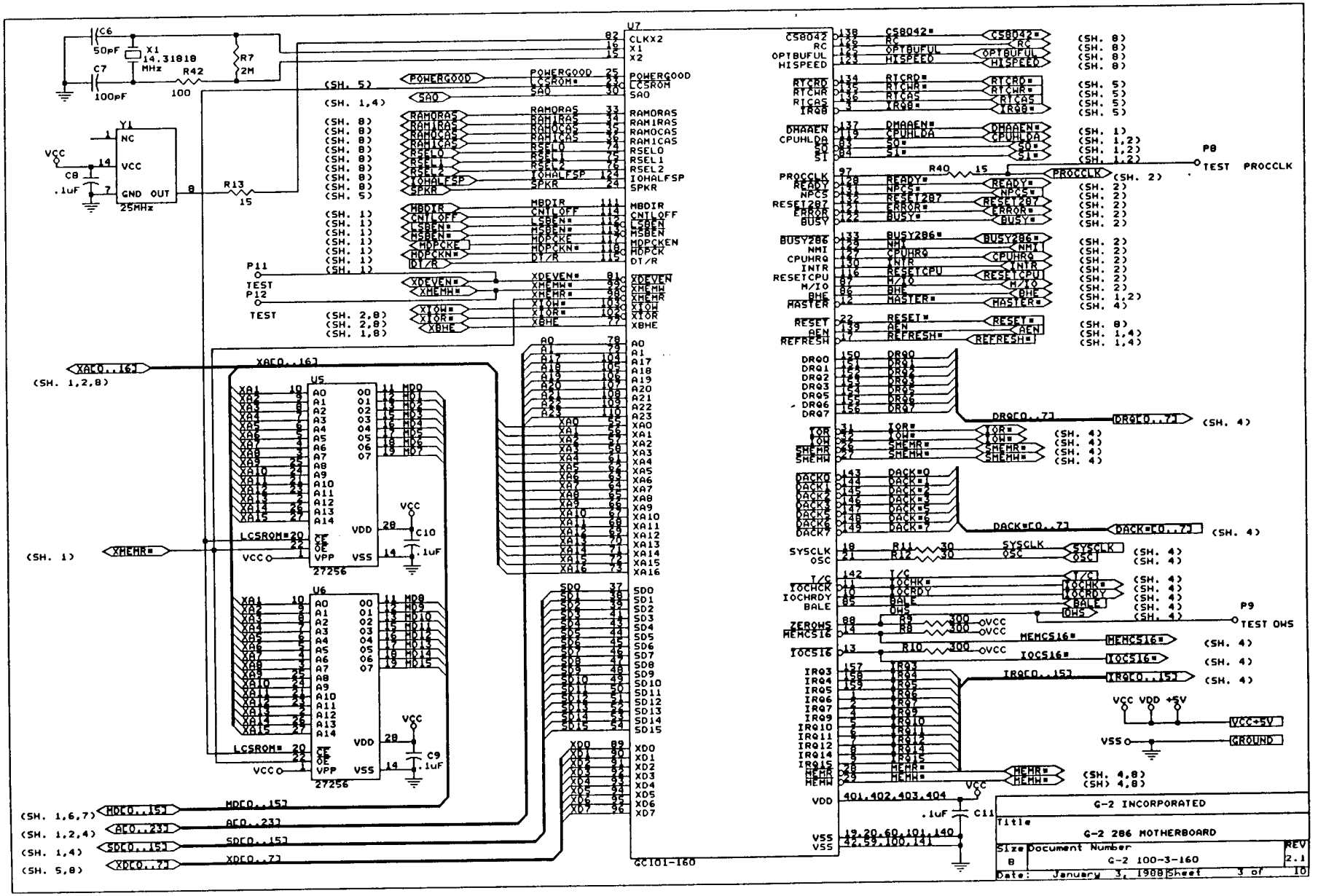
REV 2.1
Date: January 3, 1988 Sheet 3 of 10
U7
GC101-180
U5
27256
U6
27256
Y1
25MHz
X1 14.31818 MHz
P8 TEST PROCCLK
P9 TEST OWS
P11 TEST
P12 TEST


U7
GC101-160
U5
U6
27256
C6
50pF
X1
14.31818
MHz
C7
100pF
R42
100
R7
2M
Y1
25MHz
C8
.1uF
R13
15
R40
15
C10
C9
C11
.1uF
P8
TEST PROCCLK
P9
TEST OWS
P11
TEST
P12
TEST
G-2 INCORPORATED
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G-2 286 MOTHERBOARD
Size B
Document Number
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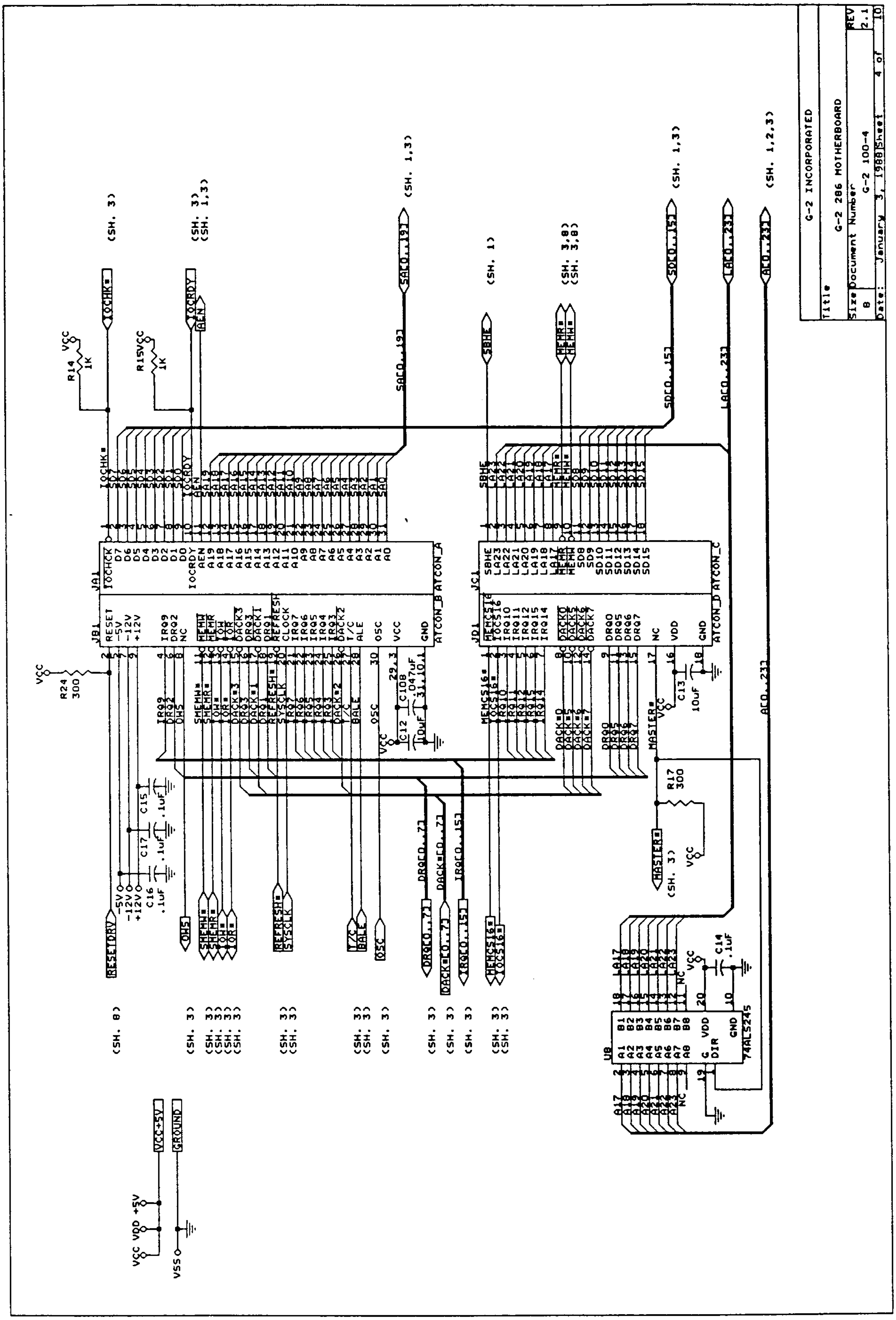
REV 2.1
Date: January 3, 1988
Sheet 3 of 10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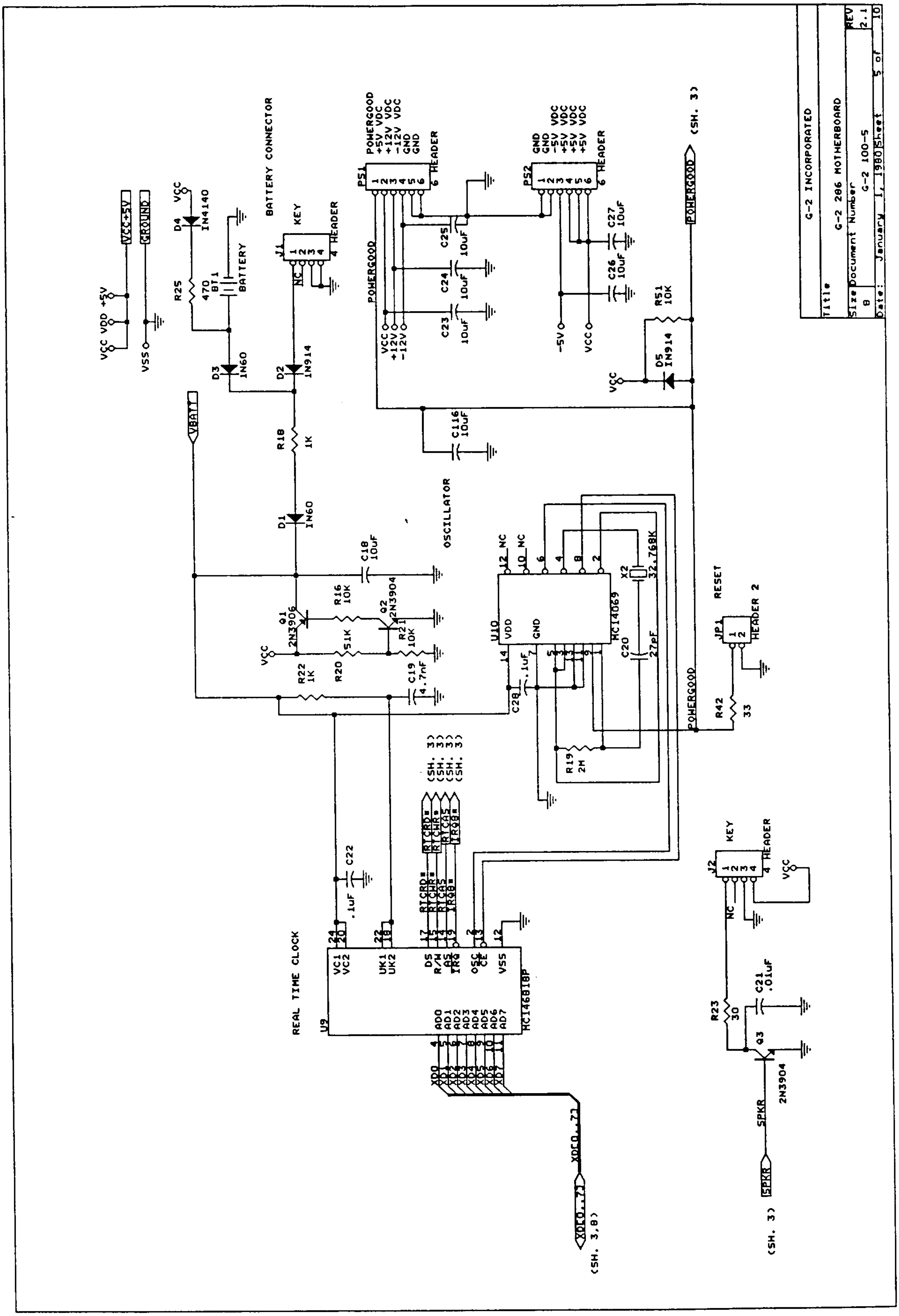
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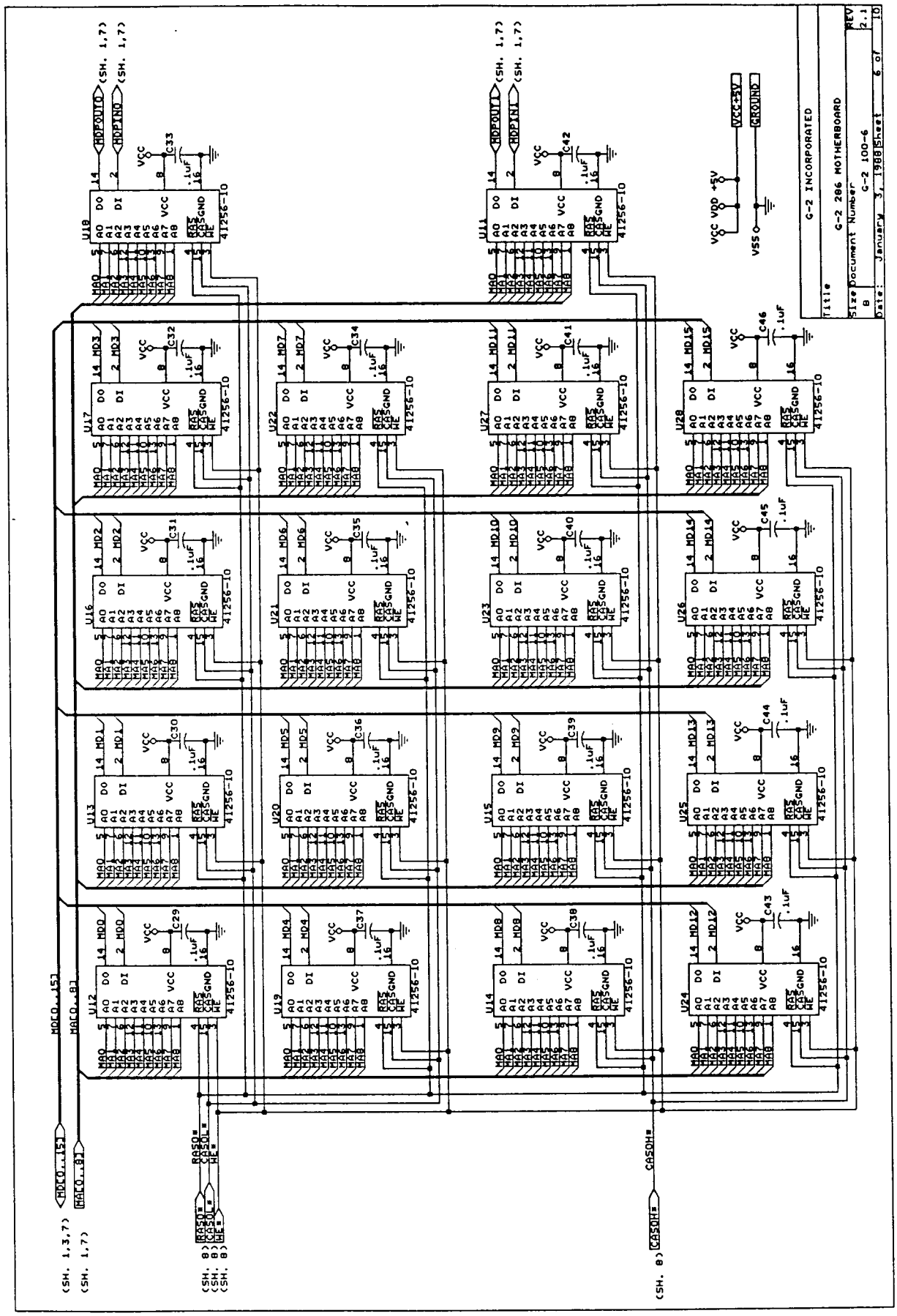
Size B
Document Number G-2 100-5
REV 2.1
Date: January 1, 1980
Sheet 5 of 10
BATTERY CONNECTOR
OSCILLATOR
REAL TIME CLOCK
RESET
KEY
4 HEADER
6 HEADER
HEADER 2
BATTERY
POWERGOOD
VBATT
VCC+5V
GROUND
MC146818P
MC14069
32.768K
2N3906
2N3904
IN4140
IN60
IN914
SPKR
XDC0..7
RTCRD*
RTCWR*
RTCAS
IRQ8*
(SH. 3)
(SH. 3,8)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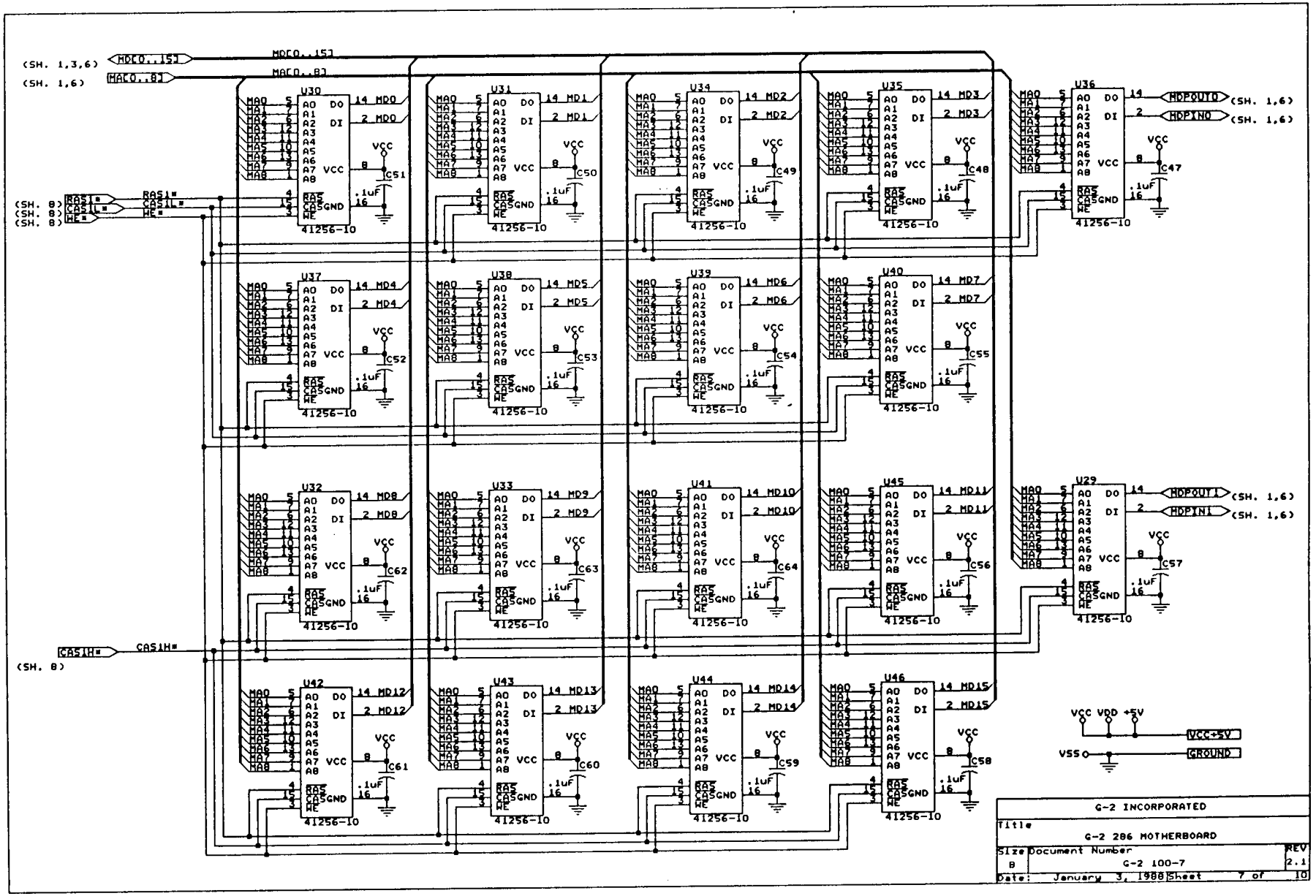
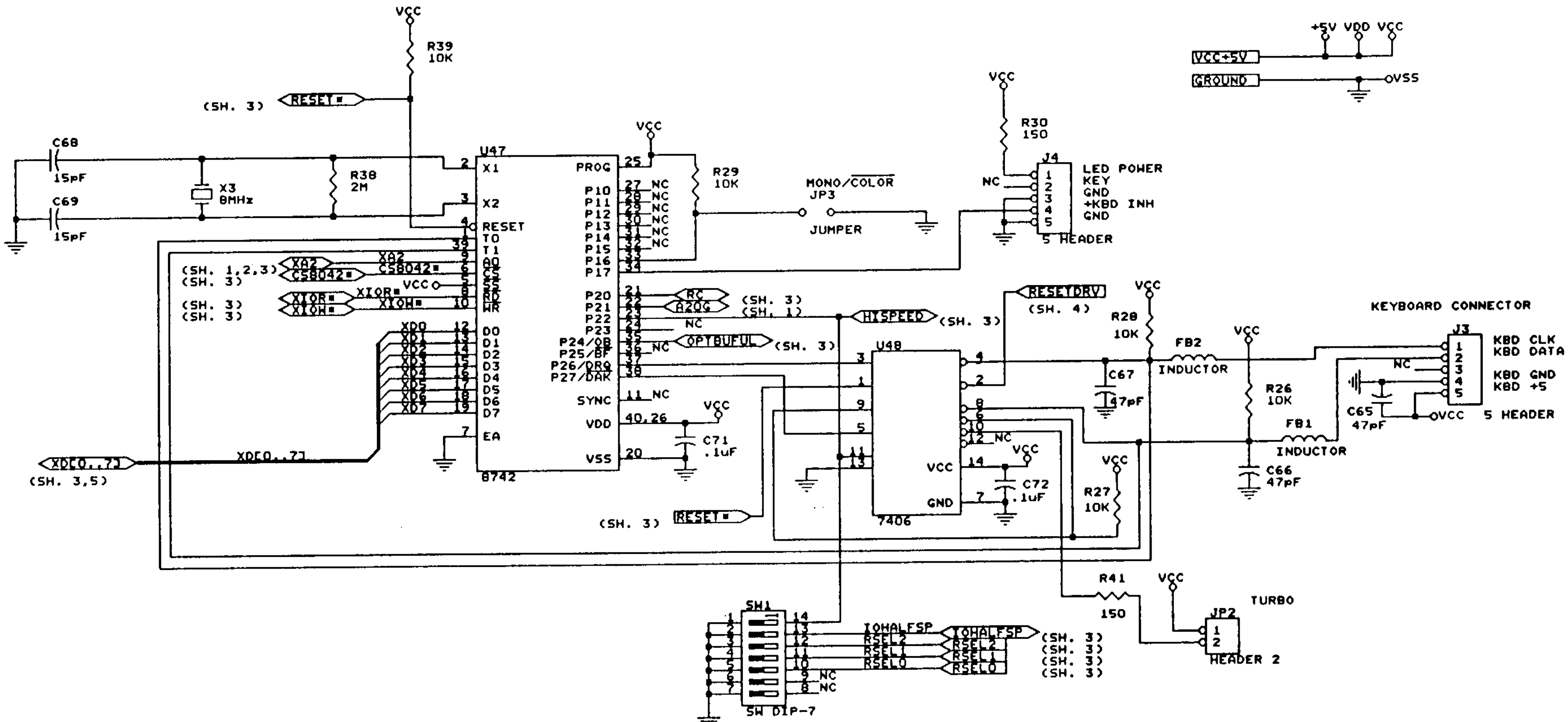
G-2 286 MOTHERBOARD
G-2 100-6
January 31, 1988
6 of 10
2.1
VCC VDD +5V
VSS
VCC+5V
GROUND
MDCO..15
MACO..8
RASO#
CASOL#
CASOH#
WE#
41256-10


(SH. 1,3,6) MDC0..15
(SH. 1,6) MAC0..8
(SH. 8) RAS1H*
(SH. 8) CAS1L*
(SH. 8) WE*
(SH. 8) CAS1H*
U30
U31
U34
U35
U36
U37
U38
U39
U40
U32
U33
U41
U45
U29
U42
U43
U44
U46
41256-10
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MD9
MD10
MD11
MD12
MD13
MD14
MD15
MDPOUT0
MDPIN0
MDPOUT1
MDPIN1
(SH. 1,6)
C51
C50
C49
C48
C47
C52
C53
C54
C55
C62
C63
C64
C56
C57
C61
C60
C59
C58
.1uF
VCC
VCC VDD +5V
VCC+5V
VSS
GROUND
G-2 INCORPORATED
Title
G-2 286 MOTHERBOARD
Size B
Document Number G-2 100-7
REV 2.1
Date: January 3, 1988 Sheet 7 of 10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R39
10K
(SH. 3)
RESET*
C68
15pF
C69
15pF
X3
8MHz
R38
2M
U47
X1
X2
RESET
T0
T1
A0
CS
SS
RD
WR
D0
D1
D2
D3
D4
D5
D6
D7
EA
8742
PROG
P10
P11
P12
P13
P14
P15
P16
P17
P20
P21
P22
P23
P24/OB
P25/BF
P26/DRQ
P27/DAK
SYNC
VDD
VSS
NC
40,26
C71
.1uF
(SH. 1,2,3)
(SH. 3)
XA2
CS8042*
XIOR*
XIOW*
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
XD[0..7]
(SH. 3,5)
R29
10K
MONO/COLOR
JP3
JUMPER
RC
A20G
HISPEED
(SH. 1)
(SH. 4)
OPTBUFUL
U48
7406
GND
C72
RESETDRV
R28
C67
47pF
FB2
INDUCTOR
R26
FB1
C66
C65
R27
R30
150
J4
LED POWER
KEY
+KBD INH
5 HEADER
+5V VDD VCC
VCC+5V
GROUND
VSS
KEYBOARD CONNECTOR
J3
KBD CLK
KBD DATA
KBD GND
KBD +5
R41
JP2
TURBO
HEADER 2
SW1
SW DIP-7
IOHALFSP
RSEL2
RSEL1
RSEL0

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Title: G-2 286 MOTHERBOARD		
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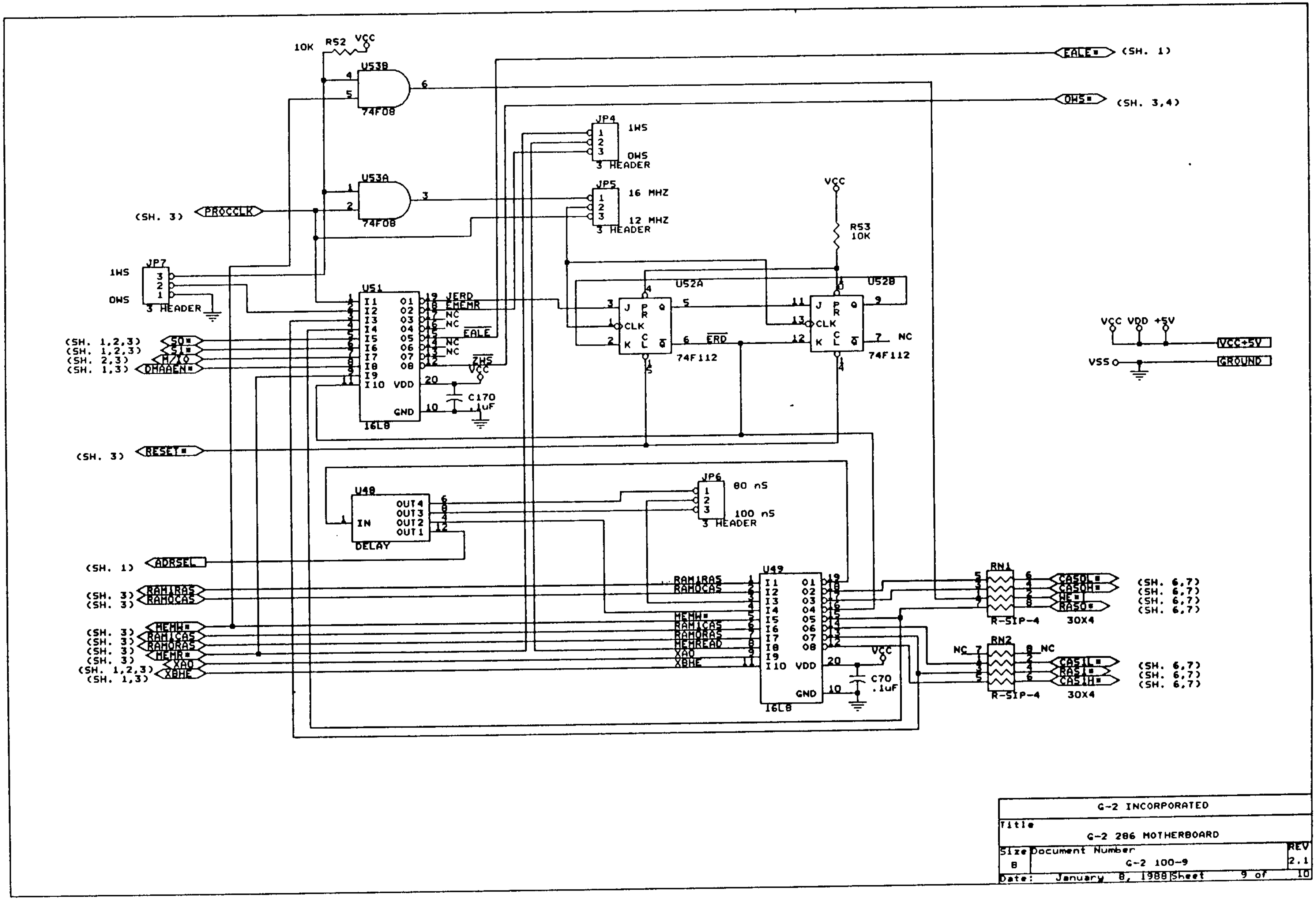
G-2 INCORPORATED
Title G-2 286 MOTHERBOARD
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Date: January 8, 1988 Sheet 9 of 10
EALE* (SH. 1)
OWS* (SH. 3,4)
PROCCLK (SH. 3)
RESET* (SH. 3)
ADRSEL (SH. 1)
S0* S1* M/IO DMAAEN*
RAM1RAS RAMOCAS MEMW* RAM1CAS RAMORAS MEMR* XA0 XBHE
CAS0L* CAS0H* WE* RAS0* CAS1L* RAS1* CAS1H* (SH. 6,7)
U51 16L8 U49 16L8 U48 DELAY U52A U52B 74F112 U53A U53B 74F08
JP4 1WS 0WS 3 HEADER
JP5 16 MHZ 12 MHZ 3 HEADER
JP6 80 nS 100 nS 3 HEADER
JP7 1WS 0WS 3 HEADER
RN1 RN2 R-SIP-4 30X4
R52 10K R53 10K C170 .1uF C70 .1uF
VCC VDD +5V VCC+5V VSS GROUND

PAL Equations

U49 - 16L8 RAS and CAS Generation

```
RAM1RAS RAM0CAS RAS100 RAS40 MEMWL RAM1CAS
RAM0RAS MEMRL XA0 GND XBHE /CAS1H /RAS1
/CAS1L /RAS0 ERD /CAS0H /CAS0L /RAS VCC

RAS=MEMRL*MEMWL*ERD

RAS0=RAM0RAS*/MEMRL*/RAS40
+    RAM0RAS*/MEMWL*/RAS40
+    RAM0RAS*/MEMRL*/RAS100
+    RAM0RAS*/MEMWL*/RAS100
+    RAM0RAS*/ERD*/RAS100

RAS1=RAM1RAS*/MEMRL*/RAS40
+    RAM1RAS*/MEMWL*/RAS40
+    RAM1RAS*/MEMRL*/RAS100
+    RAM1RAS*/MEMWL*/RAS100
+    RAM1RAS*/ERD*/RAS100

CAS0L=/XA0*RAS40*RAM0CAS*/MEMRL
+     /XA0*RAS40*RAM0CAS*/MEMWL

CAS1L=/XA0*RAS40*RAM1CAS*/MEMRL
+     /XA0*RAS40*RAM1CAS*/MEMWL

CAS0H=/XBHE*RAS40*RAM0CAS*/MEMRL
      /XBHE*RAS40*RAM0CAS*/MEMWL

CAS1H=/XBHE*RAS40*RAM1CAS*/MEMRL
+     /XBHE*RAS40*RAM1CAS*/MEMWL
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U51 - 16L8 Early Read and Zero Wait State Generator

```
PRCK ZWSEL RAS1 RAS0 S0 S1 MIOL DMAENL
MEMR GND ERD /ZWS /RAS01 /PRCK2 /EALE
NC /PRCK1 /EMEMR /JERD VCC

RAS01=/RAS0
+     /RAS1

JERD=S1+/S0+/MIOL+ZWSEL

EMEMR=/ERD
+    /MEMR

PRCK1=/PRCK
PRCK2=PRCK1

EALE=/S0*PRCK
+    /S0*EALE
+    /S1*PRCK
+    /S1*EALE
+    EALE*/PRCK

IF(/ZWSEL*DMAENL*/RAS01)ZWS=VCC
```