T-46-23-10

PRELIMINARY

CY7C101
CY7C102

CYPRESS SEMICONDUCTOR

262,144 x 4 Static R/W RAM with Separate I/O

Features

- **High speed**
  - **— t_{AA} = 25 ns**
- **Transparent write (7C101)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 825 mW**
- **Low standby power**
  - **— 165 mW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C101 and CY7C102 are high-performance CMOS static RAMs organized as 262,144 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by more than 70% when deselected.

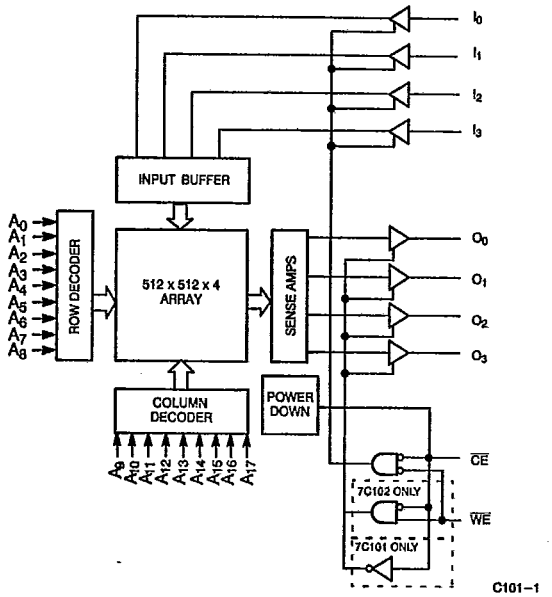
Writing to the device is accomplished by taking both chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

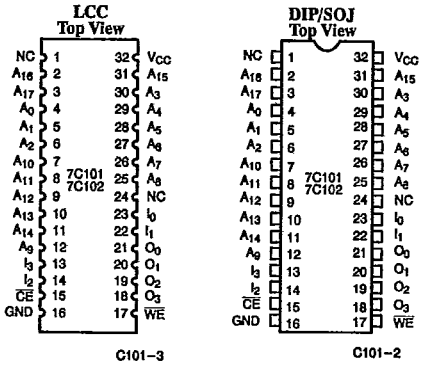
The data output pins on the CY7C101 and the CY7C102 are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH). The CY7C102's outputs are also placed in a high-impedance state during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW). In a write operation on the CY7C101, the output pins will track the inputs after a specified delay.

The CY7C101 and 7C102 are available in 32-pin leadless chip carriers and standard 400-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C101–25 7C102–25	7C101–35 7C102–35	7C101–45 7C102–45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	150	125	115
	Military	150	125	115
Maximum Standby Current (mA)	Commercial	30	25	25
	Military	35	30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to +7.0V

DC Input Voltage[1] ..... −0.5V to +7.0V

Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions		7C101−25 7C102−25 Min.	7C101−25 7C102−25 Max.	7C101−35 7C102−35 Min.	7C101−35 7C102−35 Max.	7C101−35 7C102−35 Min.	7C101−35 7C102−35 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		150		125		115	mA
			Mil		150		125		115	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		30		25		25	mA
			Mil		35		30		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		10		10		10	mA
			Mil		10		10		10	

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		12	pF

Notes:

1. $V_{IL\,(min.)}$ = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

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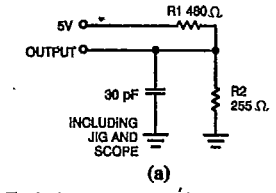
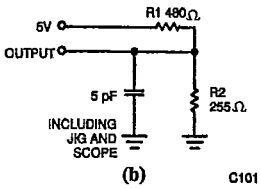
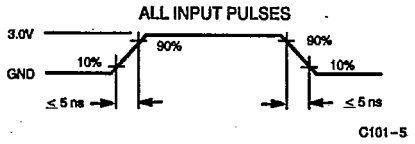
AC Test Loads and Waveforms





C101-4



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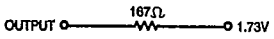
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 6]

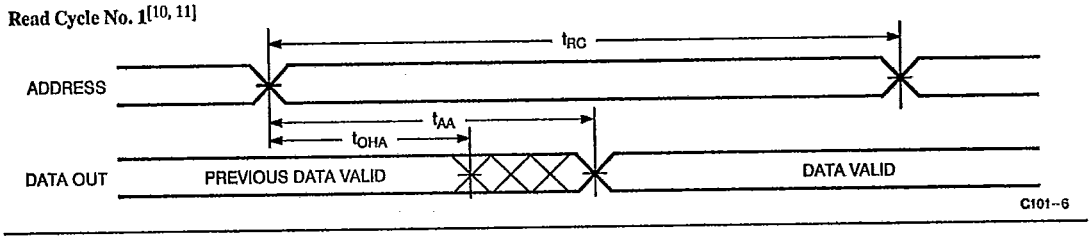
Parameters	Description	7C101–25 7C102–25		7C101–35 7C102–35		7C101–45 7C102–45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		10		15		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		35		45	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		15		20		25	ns
t_{DWE}	$\overline{WE}$ LOW to Data Valid (7C101)		20		25		30	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid (7C101)		25		35		45	ns
t_{ADV}	Data Valid to Output Valid (7C101)		20		25		30	ns

Notes:

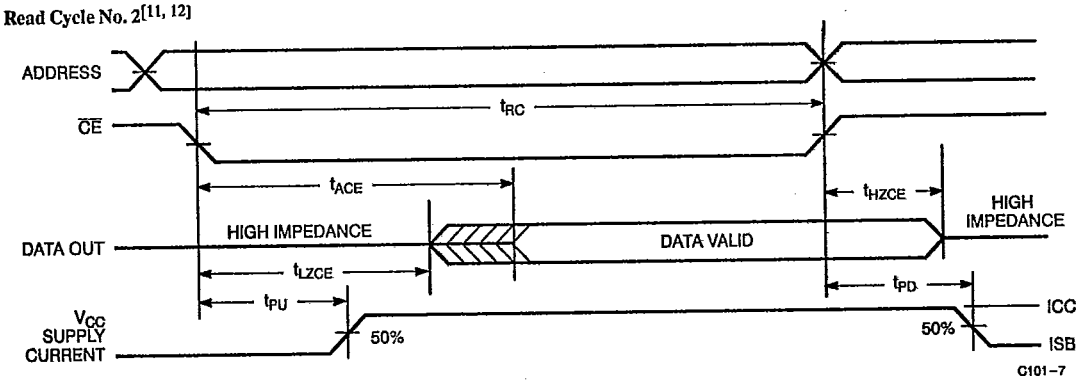
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Waveforms

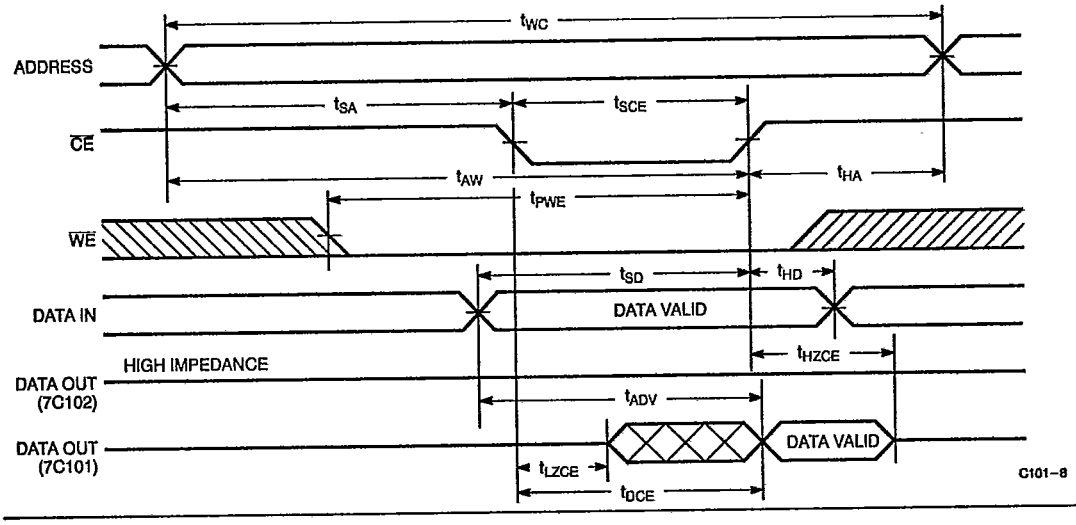
Read Cycle No. 1[10, 11]



Read Cycle No. 2[11, 12]



Write Cycle No. 1 ($\overline{CE}$ Controlled)[9, 13]



Notes:
10. Device is continuously selected. $\overline{CE} = V_{IL}$.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state (7C102 only).

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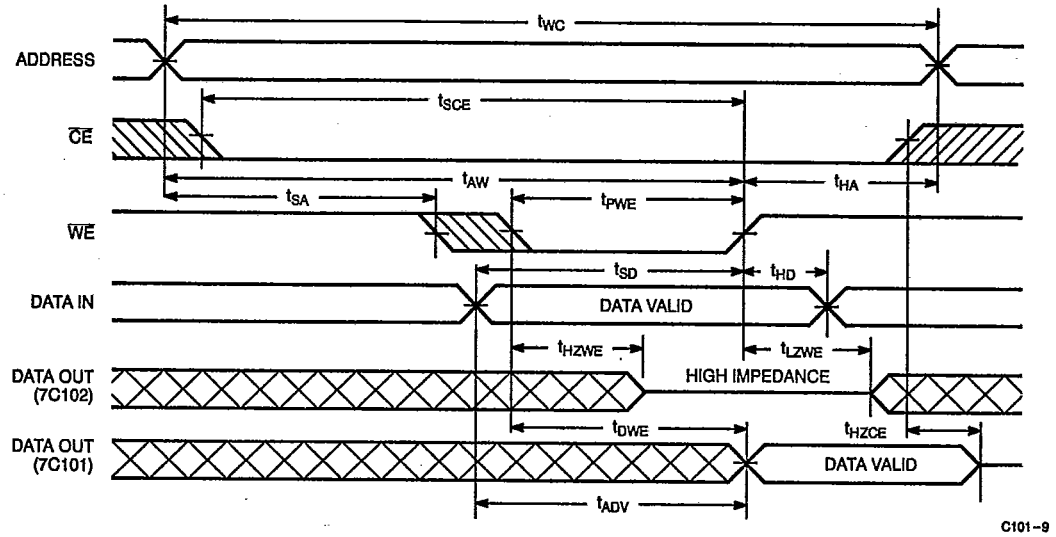
Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled)[9]



Truth Table

$\overline{CE}$	$\overline{WE}$	$O_0 - O_3$	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	7C102: Standard Write	Active (I_{CC})
L	L	Input Tracking	7C101: Transparent Write[14]	Active (I_{CC})

Notes:
14. Outputs track inputs after specified delay.

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PRELIMINARY

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SRAMs

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C101–25DC	D46	Commercial
	CY7C101–25LC	L75	
	CY7C101–25PC	P43	
	CY7C101–25VC	V33	
	CY7C101–25DMB	D46	Military
	CY7C101–25LMB	L75	
35	CY7C101–35DC	D46	Commercial
	CY7C101–35LC	L75	
	CY7C101–35PC	P43	
	CY7C101–35VC	V33	
	CY7C101–35DMB	D46	Military
	CY7C101–35LMB	L75	
45	CY7C101–45DC	D46	Commercial
	CY7C101–45LC	L75	
	CY7C101–45PC	P43	
	CY7C101–45VC	V33	
	CY7C101–45DMB	D46	Military
	CY7C101–45LMB	L75	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C102–25DC	D46	Commercial
	CY7C102–25LC	L75	
	CY7C102–25PC	P43	
	CY7C102–25VC	V33	
	CY7C102–25DMB	D46	Military
	CY7C102–25LMB	L75	
35	CY7C102–35DC	D46	Commercial
	CY7C102–35LC	L75	
	CY7C102–35PC	P43	
	CY7C102–35VC	V33	
	CY7C102–35DMB	D46	Military
	CY7C102–35LMB	L75	
45	CY7C102–45DC	D46	
	CY7C102–45LC	L75	
	CY7C102–45PC	P43	
	CY7C102–45VC	V33	
	CY7C102–45DMB	D46	Military
	CY7C102–45LMB	L75	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{DWE}[15]	7, 8, 9, 10, 11
t_{ADV}[15]	7, 8, 9, 10, 11

Note:
15. 7C101 only.

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