FUJITSU SEMICONDUCTOR
DATA SHEET

DS06-20208-3E

Semicustom

CMOS

Standard cell array

CS91 Series

■ DESCRIPTION

The CS91 series 0.11 µm CMOS standard cell is a line of highly integrated CMOS ASICs featuring high speed and low power consumption. This series incorporates up to 48 million gates which have a gate delay time of 16 ps, resulting in both integration and speed about three times higher than conventional products.

■ FEATURES

- Technology : 0.11 µm silicon-gate CMOS, 5- to 8-layer wiring (Copper is used as wire material.) , Low-K (2.7) Inter-layer material (Inter-layer material that has low permittivity)
- Support for high speed, high integration, low leak internal cell set. Capable of incorporating on the same chip.
- Supply voltage : +1.2 V ± 0.1 V (standard specification)
- Junction temperature range : –40 °C to +125 °C
- Gate delay time : t_{pd} = 16 ps (1.2 V, inverter, F/O = 1)
- Gate power consumption : Pd = 6.6 nW/MHz/BC (1.2 V, inverter, F/O = 1)
- Support for ultra high speed (622 Mbps to 780 Mbps, 2.5 Gbps to 3.125 Gbps, 10 Gbps) interface macros for transmission
- Special interfaces* : P-CML, LVDS, PCI, SSTL, HSTL, T-LVTTL, and others.
- Buffer cell dedicated to crystal oscillator
- IP macros* : CPU (ARM9, ARM7TDMI) , DSP, PCI, IEEE1394, USB, IrDA, PLL, ADC, DAC, and others.
- Compiled cells (RAM/ROM/multiplier, and others.)
- Uses industry standard tools and supports the optimum tools for the application
- Short-term development using a physical prototyping tool
- Hierarchical design environment for supporting large-scale circuits
- Support for SIGNAL INTEGRITY, EMI noise reduction
- Support for High resolution RC extraction base delay calculation environment
- Support for optimization environment of power supply wire

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- Support for static timing sign off
- Support for memory (RAM/ROM) BIST
- Support for boundary SCAN
- Support for LOGIC BIST
- A variety of package options* : FCBGA (2116 pin Max) , EBGA, FBGA, and others.

* : Including items under development.

■ MACRO LIBRARY (Including macros being prepared)

1. Logic cells (about 400 types)

- Adder
- AND-OR Inverter
- Clock Buffer
- Latch
- NAND
- AND
- NOR
- SCAN Flip Flop
- ENOR
- AND-OR
- Decoder
- Non-SCAN Flip Flop
- Inverter
- Buffer
- OR-AND Inverter
- OR
- Selector
- EOR
- Others

2. IP macros

CPU/DSP	ARM9, ARM7TDMI, Communications DSP, DSP for AV
Ultra high speed I/F macros	622 Mbps to 780 Mbps, 2.5 Gbps to 3.125 Gbps, 10 Gbps
Interface macros	PCI, IEEE1394, USB, IrDA, etc.
Multimedia processing macros	JPEG, MPEG, etc.
Mixed signal macros	ADC, DAC, OPAMP, etc.
Compiled macros	RAM, ROM, multiplier, adder, multiplier-accumulator, etc.
PLL	Analog PLL, digital PLL

3. Special I/O interface macros

- T-LVTTL
- LVDS
- SSTL
- PCI
- HSTL
- USB
- P-CML

■ COMPILED CELLS

Compiled cells are macro cells which are automatically generated with the bit/word configuration specified. The CS91 series has the following types of compiled cells. (Note that each macro is different in word/bit range depending on the column type.)

1. Clock synchronous single-port RAM (1 address : 1 RW)

Column type	Memory capacity	Word range	Bit range	Unit
4	32 to 128 K	16 to 1 K	2 to 128	bit
16	2176 to 288 K	1088 to 8 K	2 to 36	bit

2. Clock synchronous dual-port RAM (2 addresses : 2 RW)

Column type	Memory capacity	Word range	Bit range	Unit
4	32 to 288 K	16 to 2 K	2 to 144	bit
16	128 to 288 K	64 to 8 K	2 to 36	bit

3. Clock synchronous ROM

Column type	Memory capacity	Word range	Bit range	Unit
16	256 to 1 M	128 to 8 K	2 to 128	bit
64	1024 to 1 M	512 to 32 K	2 to 32	bit

4. High-capacity memory type of clock synchronous single port RAM (1 address : 1 RW)

Column type	Memory capacity	Word range	Bit range	Unit
32	16 K to 4 M	8 K to 32 K	2 to 128	bit

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

Parameter	Symbol	Application	Rating		Unit
			Min	Max	
Power supply voltage	V_{DD}	V_{DDI} (Internal)	– 0.5	+ 1.8	V
		V_{DDE} (External 2.5 V)	– 0.5	+ 3.6	V
		V_{DDE} (External 3.3 V)	– 0.5	+ 4.0	V
Input voltage*1	V_I	1.2 V	– 0.5	V_{DDI} + 0.5 (≤ 1.8 V)	V
		2.5 V	– 0.5	V_{DDE} + 0.5 (≤ 3.6 V)	V
		3.3 V	– 0.5	V_{DDE} + 0.5 (≤ 4.0 V)	V
Output voltage	V_O	1.2 V	– 0.5	V_{DDI} + 0.5 (≤ 1.8 V)	V
		2.5 V	– 0.5	V_{DDE} + 0.5 (≤ 3.6 V)	V
		3.3 V	– 0.5	V_{DDE} + 0.5 (≤ 4.0 V)	V
Storage temperature	T_{ST}	Plastic package	–55	+125	°C
Output current*2	I_O	L type simultaneous switching noise : minimum, delay : long	—	± 25	mA
		M type simultaneous switching noise : small, delay : middle	—	± 25	mA
		H type simultaneous switching noise : middle, delay : short	—	± 25	mA

*1 : Values are determined separately for LVDS, etc.

*2 : Maximum output current which can be supplied constantly.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

- **Single power supply (V_{DD} = 1.2 V ± 0.1 V)**

(V_{SS} = 0 V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage	V_{DD}	1.1	1.2	1.3	V
"H" level input voltage	V_{IH}	V_{DD} × 0.7	—	V_{DD} + 0.3	V
"L" level input voltage	V_{IL}	–0.3	—	V_{DD} × 0.3	V
Junction temperature	T_j	–40	—	+125	°C

- **Dual power supply (V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.2 V ± 0.1 V)**

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage	3.3 V supply voltage	V_{DDE}	3.0	3.3	3.6	V
	1.2 V supply voltage	V_{DDI}	1.1	1.2	1.3	V
"H" level input voltage	3.3 V CMOS level	V_{IH}	2.0	—	V_{DDE} + 0.3	V
	1.2 V CMOS level		V_{DDI} × 0.7	—	V_{DDI} + 0.3	V
"L" level input voltage	3.3 V CMOS level	V_{IL}	–0.3	—	+0.8	V
	1.2 V CMOS level		–0.3	—	V_{DDI} × 0.3	V
Junction temperature		T_j	–40	—	+125	°C

- **Dual power supply (V_{DDE} = 2.5 V ± 0.2 V, V_{DDI} = 1.2 V ± 0.1 V)**

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage	2.5 V supply voltage	V_{DDE}	2.3	2.5	2.7	V
	1.2 V supply voltage	V_{DDI}	1.1	1.2	1.3	V
"H" level input voltage	2.5 V CMOS level	V_{IH}	1.7	—	V_{DDE} + 0.3	V
	1.2 V CMOS level		V_{DDI} × 0.7	—	V_{DDI} + 0.3	V
"L" level input voltage	2.5 V CMOS level	V_{IL}	–0.3	—	+0.7	V
	1.2 V CMOS level		–0.3	—	V_{DDI} × 0.3	V
Junction temperature		T_j	–40	—	+125	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

- **Single power supply** : V_{DD} = **1.2 V**

(V_{DD} = 1.2 V ± 0.1 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
"H" level output voltage	V_{OH}	I_{OH} = –100 µA	V_{DD} – 0.2	—	V_{DD}	V
"L" level output voltage	V_{OL}	I_{OL} = 100 µA	0	—	0.2	V
Input leakage current*	I_L	—	—	—	±10	µA
Pull-up/pull-down resistance	R_P	Pull-up : V_{IL} = 0 Pull-down : V_{IH} = V_{DD}	—	12	—	kΩ

* : The input leakage current may exceed the above value when the input buffer with pull-up/pull-down resistor is used.

- **Dual power supply** : V_{DDE} = **3.3 V, V_{DDI}** = **1.2 V**

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.2 V ± 0.1 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
"H" level output voltage	V_{OH4}	I_{OH} = –100 µA	V_{DDE} – 0.2	—	V_{DDE}	V
	V_{OH2}	I_{OH} = –100 µA	V_{DDI} – 0.2	—	V_{DDI}	V
"L" level output voltage	V_{OL4}	I_{OL} = 100 µA	0	—	0.2	V
	V_{OL2}	I_{OL} = 100 µA	0	—	0.2	V
Input leakage current*	I_L	—	—	—	±10	µA
Pull-up/pull-down resistance	R_P	3.3 V Pull-up : V_I = 0 Pull-down : V_I = V_{DDE}	15	33	70	kΩ
		1.2 V Pull-up : V_I = 0 Pull-down : V_I = V_{DDI}	—	12	—	kΩ

* : The input leakage current may exceed the above value when the input buffer with pull-up/pull-down resistor is used.

- **Dual power supply** : V_{DDE} = +**2.5 V**, V_{DDI} = +**1.2 V**

(V_{DDE} = 2.5 V ± 0.2 V, V_{DDI} = 1.2 V ± 0.1 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
"H" level output voltage	V_{OH3}	I_{OH} = –100 µA	V_{DDE} – 0.2	—	V_{DDE}	V
	V_{OH2}	I_{OH} = –100 µA	V_{DDI} – 0.2	—	V_{DDI}	V
"L" level output voltage	V_{OL3}	I_{OL} = 100 µA	0	—	0.2	V
	V_{OL2}	I_{OL} = 100 µA	0	—	0.2	V
Input leakage current*	I_L	—	—	—	±10	µA
Pull-up/pull-down resistance	R_P	2.5 V Pull-up : V_I = 0 Pull-down : V_I = V_{DDE}	—	25	—	kΩ
		1.2 V Pull-up : V_I = 0 Pull-down : V_I = V_{DDI}	—	12	—	kΩ

* : The input leakage current may exceed the above value when the input buffer with pull-up/pull-down resistor is used.

■ AC CHARACTERISTICS

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Delay time	t_{pd}*1	typ*2 × tmin*3	typ*2 × ttyp*3	typ*2 × tmax*3	ns

*1 : Delay time = Propagation delay time, Enable time, Disable time

*2 : "typ" is calculated from the cell specification.

*3 : Measurement conditions

Measurement condition	tmin	ttyp	tmax
V_{DD} = 1.2 V ± 0.1 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C	0.65	1.00	1.66

Note : Reference values. The values according to the cell.

■ INPUT/OUTPUT PIN CAPACITANCE

($f = 1$ MHz, $V_{DD} = V_{DI} = 0$ V, $T_j = +25$ °C)

Parameter	Symbol	Value	Unit
Input pin	C_{IN}	16 Max	pF
Output pin	C_{OUT}	16 Max	pF
Input/output pin	$C_{I/O}$	16 Max	pF

Note : Capacitance values according to the package and the location of the pin.

■ DESIGN METHOD

Fujitsu's Reference Design Flow provides the following functions that shorten the development time of large scale and high quality LSIs.

- High reliability design estimation in the early stage of physical design realized by physical prototyping.
- Layout synthesis with optimized timing realized by physical synthesis tools.
- High accuracy design environment considering drop in power supply voltage, signal noise, delay penalty, and crosstalk.
- I/O design environment (power line design, assignment and selection of I/Os, package selection) considering noise.

■ PACKAGES

A variety of package types
Development of chips with narrow-pitch solder bump technology and high-pin count packages enables users to respond to the high-pin count, high-speed requirements of the network market. A variety of packages from existing series are also available for smooth transition from previously developed models.
Contact your FUJITSU representative for availability dates.

FCBGA package : maximum 2116 pins
EBGA package : maximum 672 pins
FBGA package : maximum 304 pins
QFP package : maximum 304 pins

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