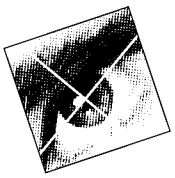


FUNCTIONAL DESCRIPTION

Functional Overview

Brooktree's VideoStream products are a family of single-chip, pin and register compatible solutions for processing analog NTSC/PAL video into digital 4:2:2 YCrCb video. They provide a comprehensive choice of capabilities to enable the feature set and cost to be tailored to different system hardware configurations. All solutions are housed in a 100-pin QFP package. A detailed block diagram is shown in Figure 1.

Bt819A Video Capture Processor for TV/VCR Analog Input

The Bt819A Video Capture Processor is a fully integrated single-chip decoding and scaling solution for analog NTSC/PAL input signals from TV tuners, VCRs, cameras, and other sources of composite or Y/C video. It is the first front-end input solution for low-cost PC video/graphics systems to deliver complete integration and high-performance video synchronization, Y/C separation, filtered scaling and optional FIFOed output pixel data. The Bt819A has all the mixed signal and DSP circuitry required to convert an analog composite waveform into a scaled digital video stream supporting a variety of video formats, resolutions and frame rates.

Bt817A Composite/S-Video Decoder

The Bt817A provides full composite and S-video capability along with filtered horizontal scaling. However, vertical scaling can be implemented by line-dropping only, and there is no output FIFO option.

Bt815A Composite Video Decoder

The Bt815A has the minimum feature set with composite-only video decoding (no S-video capability). As with the Bt817A, vertical scaling is implemented through line dropping, and there is no output FIFO option.

See Table 1 for a comparison of Bt819A, Bt817A and Bt815A features.

Table 1. VideoStream Feature Options

Feature Options	Bt819A	Bt817A	Bt815A
Composite Video Decoding	✓	✓	✓
S-Video Decoding	✓	✓	
Filtered Vertical Scaling	✓		
Optional Output FIFO	✓		

The Synchronous Pixel Interface (non-FIFOed output) is common to all three pin-compatible devices, which enables a single system hardware design to be used for all three. Similarly, a common I^2C register set allows a single piece of driver code to be written for software control of all three options.

Bt819A Architecture and Partitioning

The Bt819A has been developed to provide the most cost-effective, high-quality video input solution for low-cost multimedia subsystems that integrate both graphics display and video capabilities. The feature set of the Bt819A supports a video/graphics system partitioning which optimizes the total cost of a system configured both with and without video capture capabilities. This enables system vendors to easily offer products with various levels of video support using a single base-system design.

As graphics chip vendors move from graphics-only to video/graphics coprocessors and eventually to single-chip video/graphics processor implementations, the ability to efficiently use silicon and package pins to support both graphics acceleration, video playback acceleration and video capture becomes critical. This problem becomes more acute as the race towards higher performance graphics requires more and more package pins to be consumed for wide 64-bit memory interfaces and glueless local bus interfaces.

The Bt819A minimizes the cost of the video capture function integration in a number of ways. Recognizing that YCrCb to RGB color space conversion is becoming a required feature of multimedia controllers for acceleration of digital video playback, the Bt819A avoids redundant functionality and allows the downstream controller to perform this task. Secondly, the Bt819A integrates the FIFO which would otherwise be dedicated to feeding a live video stream to the direct memory access engine (DMA) in a video controller. Finally, the Bt819A can minimize the number of interface pins required by a downstream multimedia controller in order to keep package costs to a minimum.

Controller systems that are designed to take advantage of these features enable video capture capability to be added to the base system in a modular fashion using only a single Integrated Circuit (IC).

The Bt817A and Bt815A are targeted at system configurations using stand-alone video controllers or CODECs which typically integrate the scaling and video FIFO functions.

UltraLock™

The Bt819A, Bt817A and Bt815A employ a proprietary technique known as UltraLock to lock to the incoming analog video signal. It will always generate the required number of pixels per line from an analog source in which the line length can vary by as much as a few microseconds. UltraLock's digital locking circuitry enables the VideoStream decoders to quickly and accurately lock on to video signals, regardless of their source. Since the technique is completely digital, UltraLock can recognize unstable signals caused by VCR headswitches or any other deviation and adapt the locking mechanism to accommodate the source. UltraLock uses nonlinear techniques which are difficult, if not impossible, to implement in genlock systems. And unlike linear techniques, it adapts the locking mechanism automatically.

Scaling and Cropping

The Bt819A can reduce the video image size in both horizontal and vertical directions independently using arbitrarily selected scaling ratios. The X and Y dimensions can be scaled down to one-fourteenth of the full resolution. Horizontal scaling is implemented with a six-tap interpolation filter while two-tap interpolation is used for vertical scaling with a line store. The Bt817A and Bt815A support vertical scaling by line-dropping.

The video image can be arbitrarily cropped by programming the ACTIVE flag to reduce the number of active scan lines and active horizontal pixels per line.

The Bt819A, Bt817A and Bt815A also support a temporal decimation feature that reduces video bandwidth by allowing frames or fields to be dropped from a video sequence at regular but arbitrarily selected intervals.

Input Interface

Analog video signals are input to the Bt819A/7A/5A via a three-input multiplexer that can select between three composite source inputs or between two composite and a single S-video input source. When an S-video source is input to the Bt819A, the luma component is fed through the input analog multiplexer, and the chroma component is fed directly into the C input pin (the Bt815A does not support S-video input). An automatic gain control circuit enables the Bt819A/7A/5A to compensate for reduced amplitude in the analog signal input.

The clock signal interface consists of two pairs of pins for crystal connection and two clock output pins. One pair of crystal pins is for connection to a 28.64 MHz (8*NTSC Fsc) crystal which is selected for NTSC operation. The other is for PAL operation with a 35.47 MHz (8*PAL Fsc) crystal. Either of the two crystal frequencies can be selected to generate CLKX1 and CLKX2 output signals. CLKX2 operates at the full crystal frequency (8*Fsc) whereas CLKX1 operates at half the crystal frequency (4*Fsc). Either fundamental or third harmonic crystals may be used. Alternatively, CMOS oscillators may be used.

Output Interface

The Bt819A's output interface can be set up to support two different configurations: the Synchronous Pixel Interface (SPI) and the Asynchronous Pixel Interface (API). The Bt817A and Bt815A support the Synchronous Pixel Interface only.

Both the SPI and the API can support a YCrCb 4:2:2 data stream over a 16-bit-wide path. The SPI also supports an 8-bit path. When the pixel output port is configured to operate 8 bits wide, 8 bits of chrominance data are output on the first clock cycle followed by 8 bits of luminance data on the next clock cycle for each pixel. Two clocks are required to output one pixel in this mode, thus a 2x clock is used to output the data.

In SPI mode, the Bt819A/7A/5A output interface is similar to the Bt812 interface. The Bt819A/7A/5A outputs all horizontal and vertical blanking pixels in addition to the active pixels synchronous with CLKX1 (16-bit mode) or CLKX2 (8-bit mode). It is also possible to insert control codes into the pixel stream using chrominance and luminance values that are outside the allowable chroma and luma ranges. These control codes can be used to flag video events such as ACTIVE, HRESET, and VRESET. Decoding these video events downstream enables the vid-

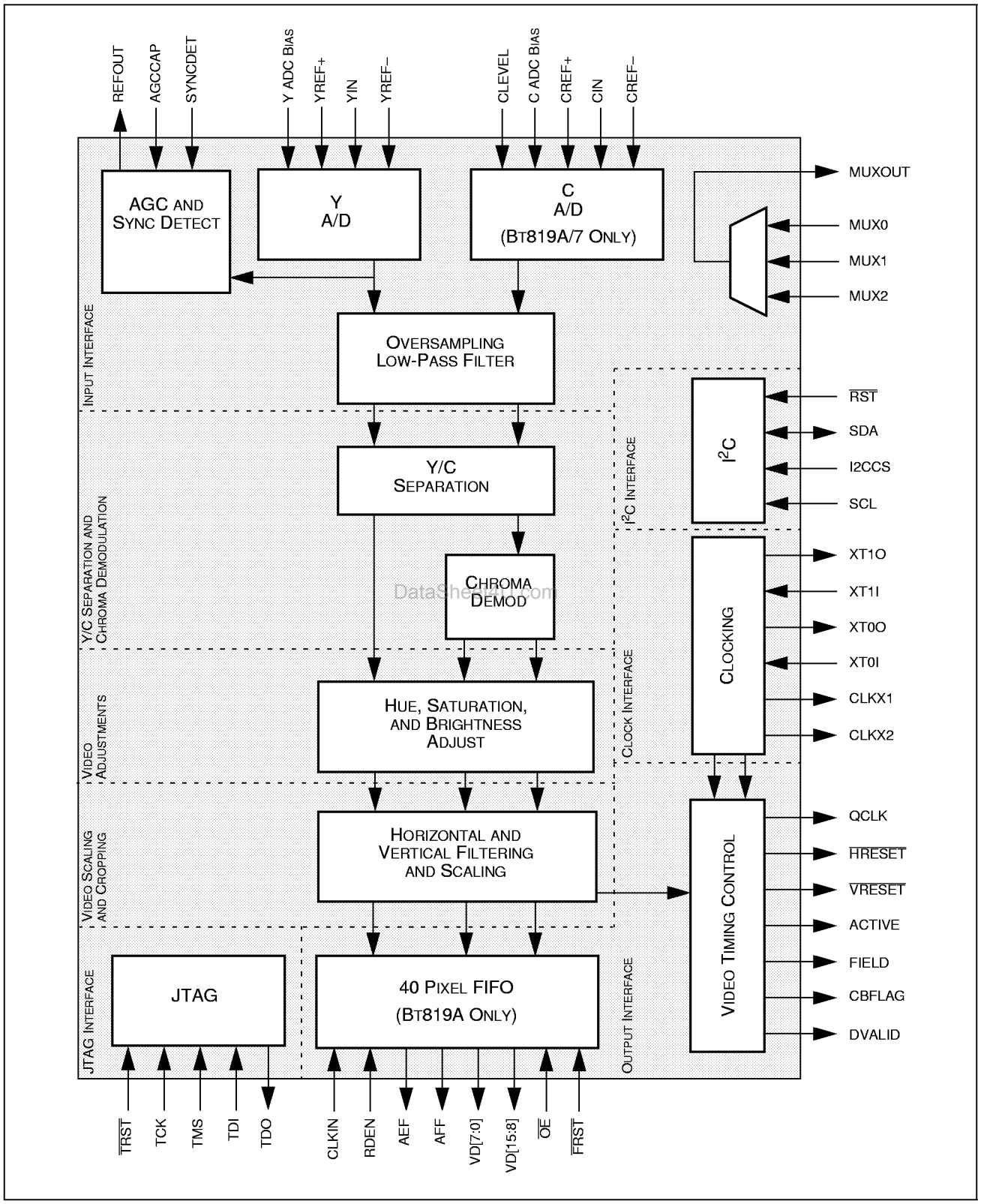
eo controller to do away with pins required for the corresponding video control signals.

In the API mode, the Bt819A outputs only the active pixels and control codes at a rate asynchronous with the sample clock. A 40-pixel-deep FIFO buffers the pixel output port and enables the system to burst pixels out of the Bt819A at rates up to 35 Mpixels/sec. An input clock must be provided on CLKIN for operation in this mode. The Bt819A outputs the DVALID, AEF and AFF flags to provide the system information on the status of the FIFO.

I²C Interface

The Bt819A/7A/5A registers are accessed via a two-wire Inter-Integrated Circuit (I^2C) interface. The Bt819A/7A/5A operates as a slave device. Serial clock and data lines, SCL and SDA, are used to transfer data from the bus master at a rate of 100 Kbits/s. Chip select and reset signals are also available to select one of two possible Bt819A/7A/5A devices in the same system and to set the registers to their default values.

Figure 1. Bt819A/7A/5A Detailed Block Diagram



Pin Descriptions

Pins with alternate definitions on the Bt817A or Bt815A are indicated by shading (e.g., see pin number 67).

Table 2. Pin Descriptions Grouped By Pin Function *(1 of 6)*

Pin #	I/O	Pin Name	Description
The Input Stage Pins			
55	I	MUX0	Analog composite video inputs to the on-chip input multiplexer. Used to select between three composite sources or two composite and one S-video source. Unused pins should be connected to GND.
57	I	MUX1	
45	I	MUX2	
53	O	MUXOUT	The analog video output of the 3 to 1 multiplexer. Connected to the YIN pin.
52	I	YIN	The analog composite or luma input to theY-ADC.
67	I	CIN	The analog chroma input to the C-ADC.
		NC	May be left unconnected.
59	I	SYNCDET	The sync stripper input used to generate timing information for AGC circuit. Must be connected through a 0.1 µF capacitor to the same source as the Y-ADC. A 1 MΩ bleeder resistor should be connected to ground.
41	A	AGCCAP	The AGC time constant control capacitor node. Must be connected to a 0.1 µF capacitor to ground.
43	O	REFOUT	Output of the AGC which drives the YREF+ and CREF+ pins.
49	I	YREF+	The top of the reference ladder of the Y-ADC. This should be connected to REFOUT.
62	I	YREF–	The bottom of the reference ladder of the Y-ADC. This should be connected to analog ground (AGND).
64	I	CREF+	The top of the reference ladder of the C-ADC. This should be connected to REFOUT.
		AGND/CREF+	May be connected to either AGND or REFOUT.
73	I	CREF–	The bottom of the reference ladder of the C-ADC. This should be connected to analog ground (AGND).
	G	AGND	Ground for analog circuitry on Bt815A.
74	I	CLEVEL	An input to provide the DC level reference for the C-ADC. This voltage should be one half of CREF+.
		AGND/CLEVEL	May be connected to either AGND or 1/2 the voltage on CREF+ (the same connection as on the Bt819A and Bt817A.)

Table 2. Pin Descriptions Grouped By Pin Function *(2 of 6)*

Pin #	I/O	Pin Name	Description
51	A	YABIAS	The Y ADC Bias pins. Should be left unconnected. For backward compatibility with the Bt819/7/5, these pins may optionally be connected with 0.1 µF capacitors to ground.
46	A	YCBIAS	
50	A	YDBIAS	
70	A	CABIAS	The C ADC Bias pins. Should be left unconnected. For backward compatibility with the Bt819/7/5, these pins may optionally be connected with 0.1 µF capacitors to ground.
69	A	CCBIAS	
63	A	CDBIAS	
70		NC	No Connect on Bt815A.
69		NC	
63		NC	
The I^2C Interface Pins			
19	I	SCL	The I^2C Serial Clock Line.
18	I/O	SDA	The I^2C Serial Data Line.
14	I	I2CCS	The I^2C Chip Select Input (TTL compatible). This pin is used to select one of two Bt819A devices in the same system. This pin is internally pulled to ground with an effective 18 KΩ resistance.
15	I	$\overline{RST}$	Reset control input (TTL compatible). A logical zero for a minimum of four consecutive clock cycles resets the device to its default state. A logical zero for less than eight XTAL cycles will leave the device in an undetermined state.

Table 2. Pin Descriptions Grouped By Pin Function *(3 of 6)*

Pin #	I/O	Pin Name	Description
			The Video Timing Unit Pins
82	O	$\overline{\text{HRESET}}$	Horizontal Reset Output (TTL Compatible). This signal indicates the beginning of a new line of video. **In SPI mode**: this signal is 64 CLKx1 clock cycles wide. In SPI mode, the falling edge of this output indicates the beginning of a new scan line of video. **In API mode**: this signal is one clock cycle wide and is output relative to CLKIN. In API mode, it immediately follows the last active pixel of a line. Note: The polarity of this pin is programmable through the VPOLE register.
79	O	$\overline{\text{VRESET}}$	Vertical Reset Output (TTL Compatible). This signal indicates the beginning of a new field of video. **In SPI mode**: this signal is output coincident with the rising edge of CLKx1, and is normally six lines wide. The falling edge of $\overline{\text{VRESET}}$ indicates the beginning of a new field of video. **In API mode**: this signal is a one clock cycle wide, active low pulse output relative to CLKIN. It immediately follows the HRESET pixel, and it indicates that the next active pixel is the first active pixel of the next field. Note: The polarity of this pin is programmable through the VPOLE register.
83	O	ACTIVE	Active Video output (TTL compatible). This pin is a logical high during the active/viewable periods of the video stream. The active region of the video stream is programmable. Note: The polarity of this pin is programmable through the VPOLE register.
85	I	RDEN	Asynchronous FIFO Read Enable signal (TTL compatible). A logical high on this pin enables a read from the output FIFO. When using the Bt819A in SPI mode, RDEN must be pulled low.
	G	GND	Ground for digital circuitry on Bt817A and Bt815A.
94	O	QCLK	Qualified Clock Output. See “Output Interface” on page 37 for a complete description of the QCLK pin functions.
98	I	$\overline{\text{OE}}$	Output Enable control (TTL compatible). All video timing unit output pins and all clock interface output pins contain valid data following the rising edge of CLKIN, after $\overline{\text{OE}}$ has been asserted low. The above outputs are three-stated when $\overline{\text{OE}}$ is held high. This function is asynchronous. The three-stated pins include: VD[15:0], $\overline{\text{HRESET}}$, $\overline{\text{VRESET}}$, ACTIVE, DVALID, CBFLAG, FIELD, AEF, AFF, QCLK, CLKx1, and CLKx2.
78	O	FIELD	Odd/even field output (TTL compatible). High state on FIELD pin indicates that an even field is being digitized. Note: The polarity of this pin is programmable through the VPOLE register.
89	O	CBFLAG	Cb data identifier (TTL compatible). High state on this pin indicates that VD[7:0] bus contains Cb chroma information. Note: The polarity of this pin is programmable through the VPOLE register.

Table 2. Pin Descriptions Grouped By Pin Function *(4 of 6)*

Pin #	I/O	Pin Name	Description
2–9	O	VD[15:8]	Digitized Video Data Outputs (TTL Compatible). VD0 is the least significant bit of the bus in 16-bit mode. VD8 is the least significant bit of the bus in 8-bit mode. **In SPI mode**: the information is output with respect to CLKx1 in 16-bit mode, and CLKx2 in 8-bit mode. In SPI mode 2, this port is configured to output control codes as well as data. **In API mode**: this port may be used only in 16-bit mode with VD0 as the least significant bit. The data is output with respect to CLKIN. In API mode, control codes for $\overline{\text{HRESET}}$ and $\overline{\text{VRESET}}$ are always inserted into the data stream.
22–29	O	VD[7:0]	
84	O	DVALID	Data Valid Output (TTL Compatible). **In SPI mode**: this pin indicates if a valid pixel is being output onto the data bus. The Bt819A digitizes video at eight times the subcarrier rate, and outputs scaled video. Therefore, there are more clocks than valid data. DVALID indicates when valid pixel data is being output. **In API mode**: DVALID performs a different function. It toggles high when the FIFO has 20 locations filled, and remains high until the FIFO is empty. It can be used to control FIFO reads for bursting information out of the FIFO. DVALID may be programmed to toggle when almost full (32 pixels). In API mode, DVALID indicates valid data in the FIFO, which includes both pixel information and control codes. Note: The polarity of this pin is programmable through the VPOLE register.
The FIFO Pins (Bt819A Only)			
87	O	AEF	Almost Empty Flag. Indicates when there are less than 9 pixels in the FIFO. Note: The AEF flag is pipelined to the output of the chip. Also, the FIFO is being written into during this time. Therefore, the actual number of pixels in the FIFO when AEF toggles will vary. The number of pixels remaining could be as low as 2. The system should stop reading from the FIFO as soon as AEF indicates almost empty. See Figure 28 for a recommended circuit.
		NC	No Connect on Bt817A and Bt815A.
86	O	AFF	Almost Full Flag. Indicates when there are more than 32 FIFO locations full. It can also be programmed to signal a half full condition (with 20 locations full). Note: The polarity of this pin is programmable through the VPOLE register.
		NC	No Connect on Bt817A and Bt815A.
91	I	CLKIN	Asynchronous FIFO output clock (TTL compatible). This asynchronous clock is used to output data onto the VD15-VD0 bus and other VTU control signals. CLKX2 or CLKX1 outputs of the Bt819A can be tied to this pin. *When using the Bt819A in SPI mode, CLKIN must be pulled low.*
	G	GND	Ground for digital circuitry on Bt817A and Bt815A.
88	I	$\overline{\text{FRST}}$	FIFO Reset (TTL compatible). A logical 0 on this pin asynchronously resets the read and write address pointers to zero. *When using the Bt819A in SPI mode, $\overline{\text{FRST}}$ must be pulled high.*
	P	VDD	Power supply for digital circuitry on Bt817A and Bt815A.

Table 2. Pin Descriptions Grouped By Pin Function *(5 of 6)*

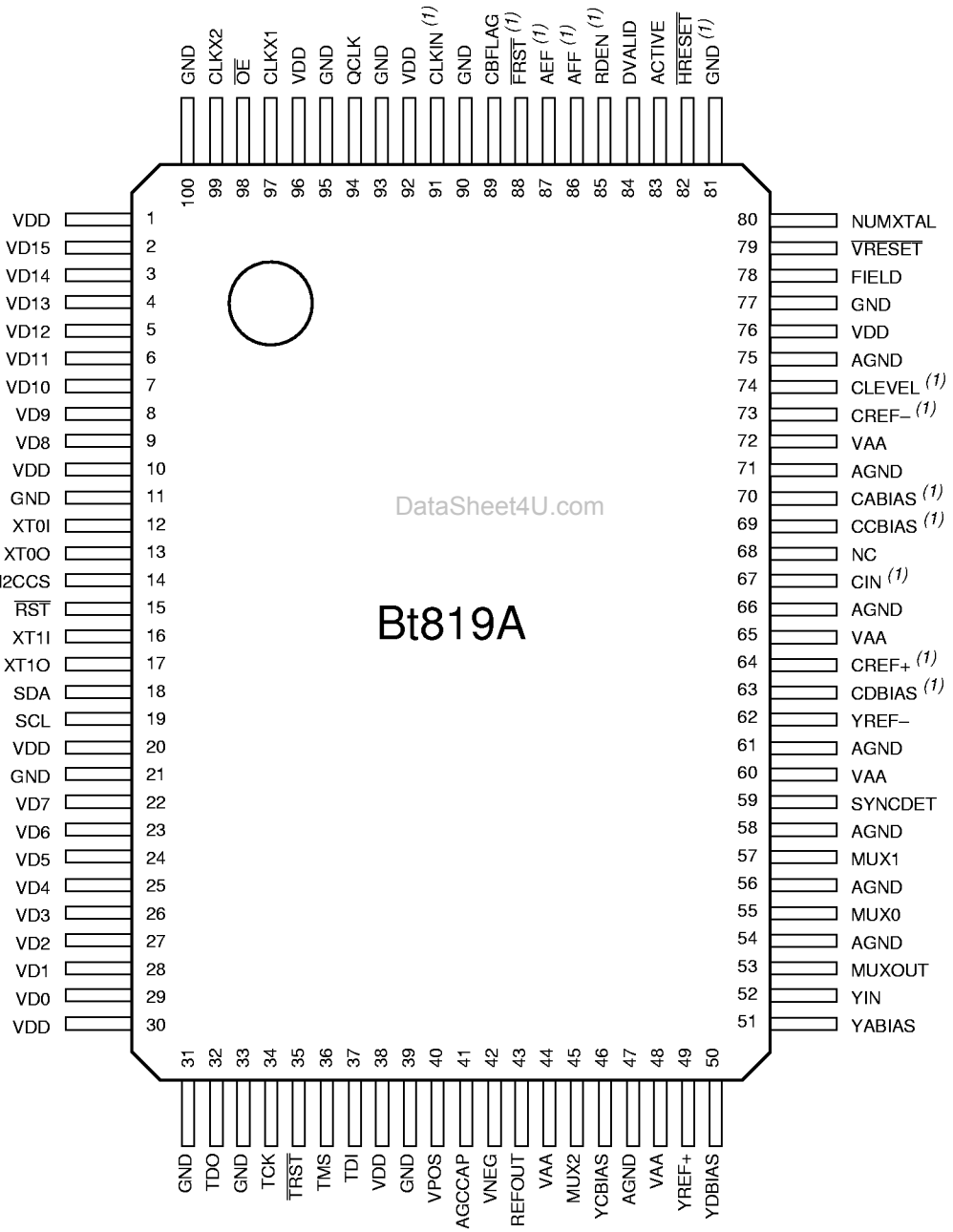
Pin #	I/O	Pin Name	Description
The Clock Interface Pins			
12	A	XT0I	Clock Zero pins. A 28.64 MHz (8*Fsc) fundamental (or third harmonic) crystal can be tied directly to these pins, or a single-ended oscillator can be connected to XT0I. CMOS level inputs must be used. This clock source is selected for NTSC input sources. When the chip is configured to decode PAL but not NTSC (and therefore only one clock source is needed), the 35.47 MHz source is connected to this port (XT0).
13	A	XT0O	
16	A	XT1I	Clock One pins. A 35.47 MHz (8*Fsc) fundamental (or third harmonic) crystal can be tied directly to these pins, or a single-ended oscillator can be connected to XT1I. CMOS level inputs must be used. This clock source is selected for PAL input sources. If either NTSC or PAL is being decoded, and therefore only XT0I and XT0O are connected to a crystal, XT1I should be tied either high or low, and XT1O *must* be left floating.
17	A	XT1O	
97	O	CLKX1	1x clock output (TTL compatible). The frequency of this clock is 4*Fsc (14.31818 MHz for NTSC or 17.734475 MHz for PAL).
99	O	CLKX2	2x clock output (TTL compatible). The frequency of this clock is 8*Fsc (28.63636 MHz for NTSC, or 35.46895 MHz for PAL).
80	I	NUMXTAL	Crystal Format Pin. This pin is set to indicate whether one or two crystals are present so that the Bt819A can select XT1 or XT0 as the default in auto format mode. A logical zero on this pin indicates one crystal is present. A logical one indicates two crystals are present. This pin is internally pulled down to ground with an effective 18 KΩ resistance.
The JTAG Pins			
34	I	TCK	Test clock (TTL compatible). Used to synchronize all JTAG test structures. When JTAG operations are not being performed, this pin must be driven to a logical low.
36	I	TMS	Test Mode Select (TTL compatible). JTAG input pin whose transitions drive the JTAG state machine through it sequences. When JTAG operations are not being performed, this pin must be left floating or tied high.
37	I	TDI	Test Data Input (TTL compatible). JTAG pin used for loading instruction to the TAP controller or for loading test vector data for boundary-scan operation. When JTAG operations are not being performed, this pin must be left floating or tied high.
32	O	TDO	Test Data Output (TTL compatible). JTAG pin used for verifying test results of all JTAG sampling operations. This output pin is active for certain JTAG operations and will be three-stated at all other times.
35	I	$\overline{\text{TRST}}$	Test Reset (TTL compatible). JTAG pin used to initialize the JTAG controller. This pin is tied low for normal device operation. When pulled high, the JTAG controller is ready for device testing.

Table 2. Pin Descriptions Grouped By Pin Function *(6 of 6)*

Pin #	I/O	Pin Name	Description
Power And Ground Pins			
1, 10, 20, 30, 38, 76, 92, 96	P	VDD +5 V	Power supply for digital circuitry. All VDD pins must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VDD pins and the ground plane as close to the device as possible.
40, 44, 48, 60, 65, 72	P	VAA +5 V VPOS +5 V	Power supply for analog circuitry. All VAA pins and VPOS must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VAA pins and the ground plane as close to the device as possible.
11, 21, 31, 33, 39, 77, 81, 90, 93, 95, 100	G	GND	Ground for digital circuitry. All GND pins must be connected together as close to the device as possible.
81		NC	May be left unconnected.
42, 47, 54, 56, 58, 61, 66, 71, 75	G	AGND VNEG	Ground for analog circuitry. All AGND pins and VNEG must be connected together as close to the device as possible.
I/O Column Legend: I = Digital Input O = Digital Output I/O = Digital Bidirectional A = Analog G = Ground P = Power			

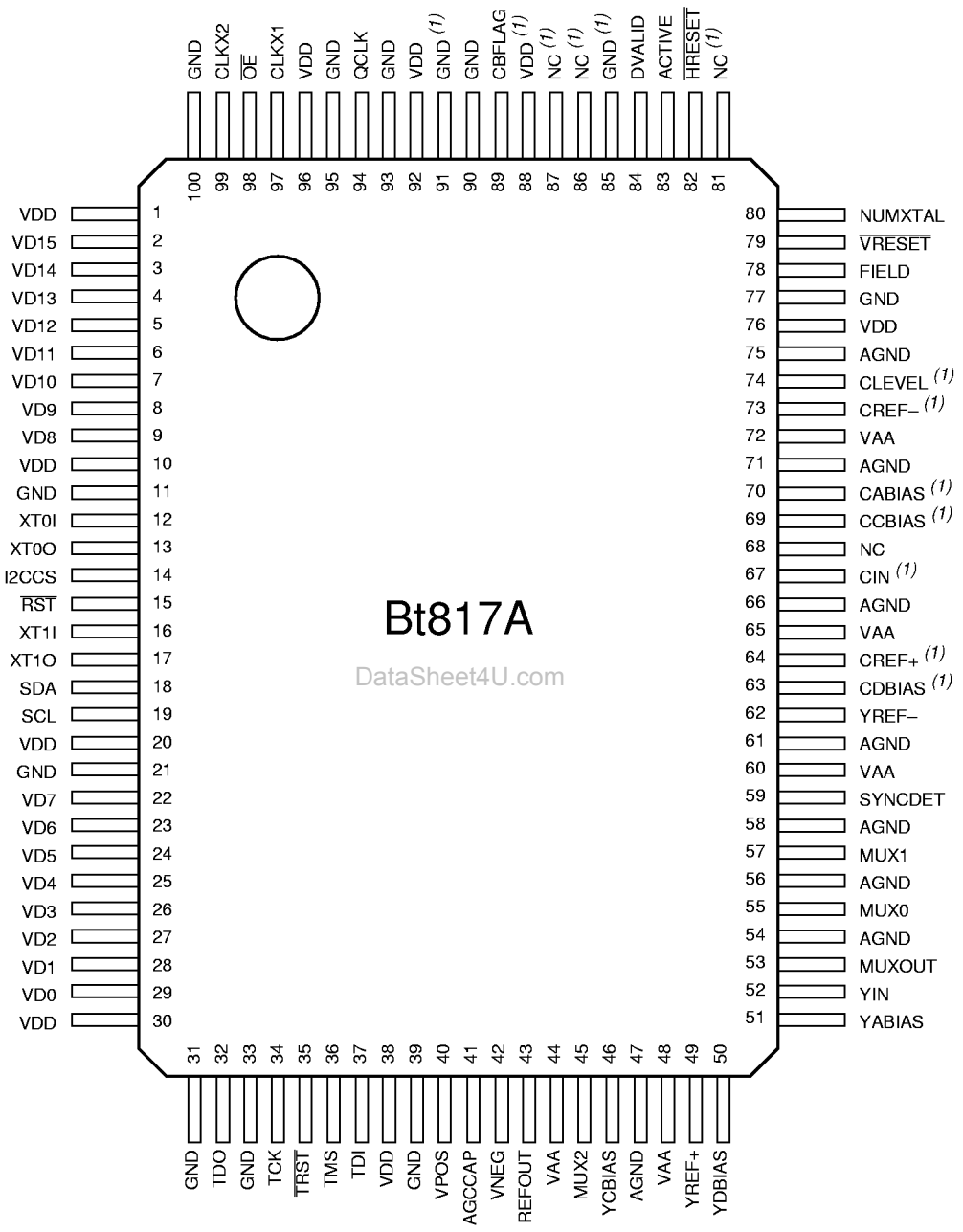
Pin Assignments

Figure 2. Bt819A Pinout



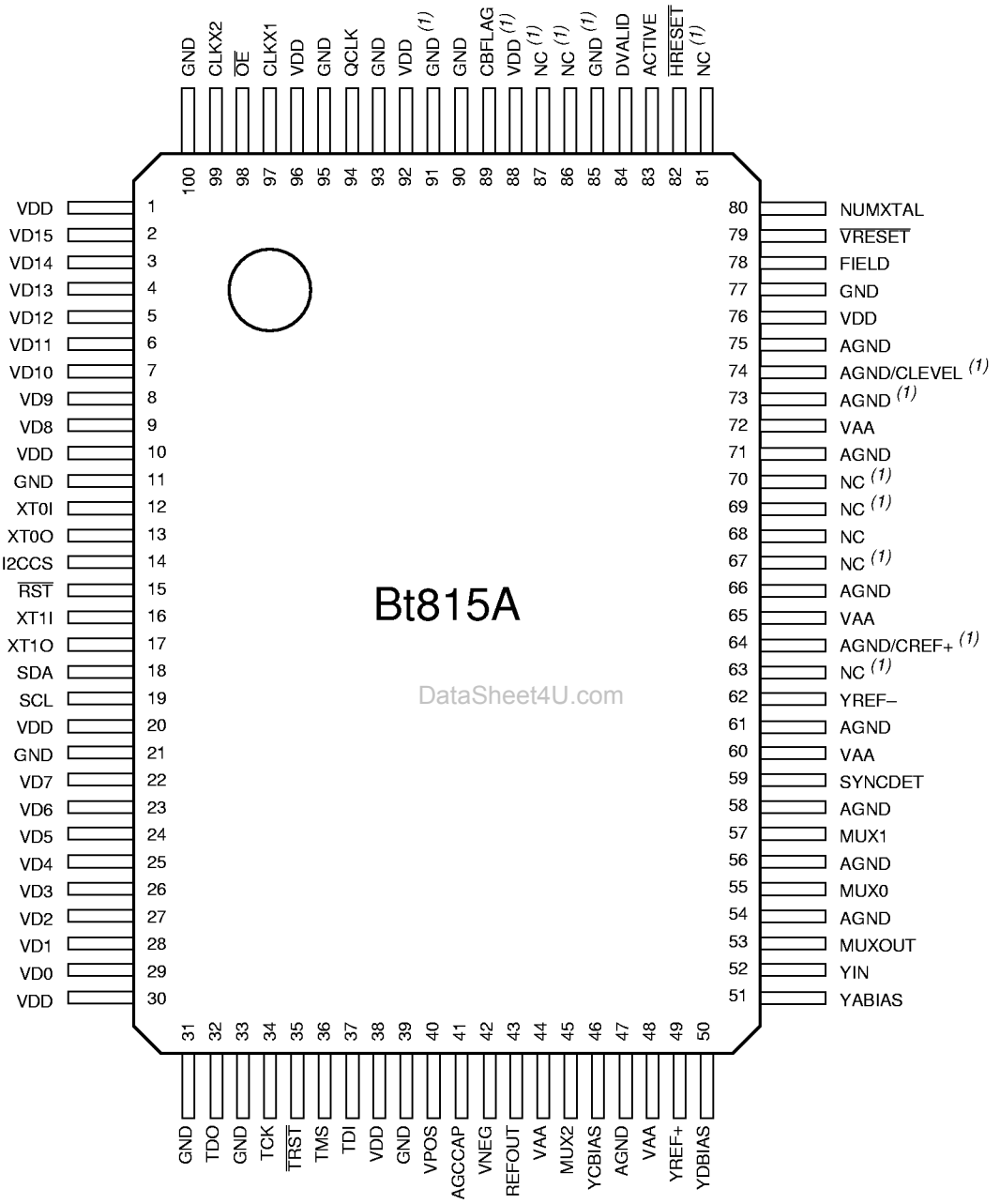
Notes: (1). Alternate pin definitions for Bt817A and Bt815A

Figure 3. Bt817A Pinout



Notes: (1). Alternate pin definitions for Bt819A and Bt815A

Figure 4. Bt815A Pinout



Notes: (1). Alternate pin definitions for Bt819A and Bt817A

UltraLock

The Challenge

The line length (the interval between the midpoints of succeeding horizontal sync pulses) of analog video sources is not constant. For a stable source such as studio quality source or test signal generators, this variation is very small: ±2 ns. However, for an unstable source such as a VCR, laser disk player, or TV tuner, line length variation is as much as a few microseconds.

Digital display systems require a fixed number of pixels per line despite these variations. The Bt819A employs a technique known as UltraLock to implement locking to the horizontal sync and the subcarrier of the incoming analog video signal by generating the required number of pixels per line.

Operation Principles of UltraLock

UltraLock is based on sampling using a fixed-frequency stable clock. Since the video line length will vary, the number of samples generated using a fixed-frequency sample clock will also vary from line to line. If the number of generated samples per line is always greater than the number of samples per line required by the particular video format, the number of acquired samples can be reduced to fit the required number of pixels per line.

The Bt819A requires an 8*Fsc (28.64 MHz for NTSC and 35.47 MHz for PAL) crystal or oscillator input signal source. The 8*Fsc clock signal, or CLKx2, is divided down to CLKx1 internally (14.32 MHz for NTSC and 17.73 MHz for PAL). Both CLKx2 and CLKx1 are made available to the system. UltraLock operates at CLKx1 although the input waveform is sampled at CLKx2 then low pass filtered and decimated to CLKx1 sample rate.

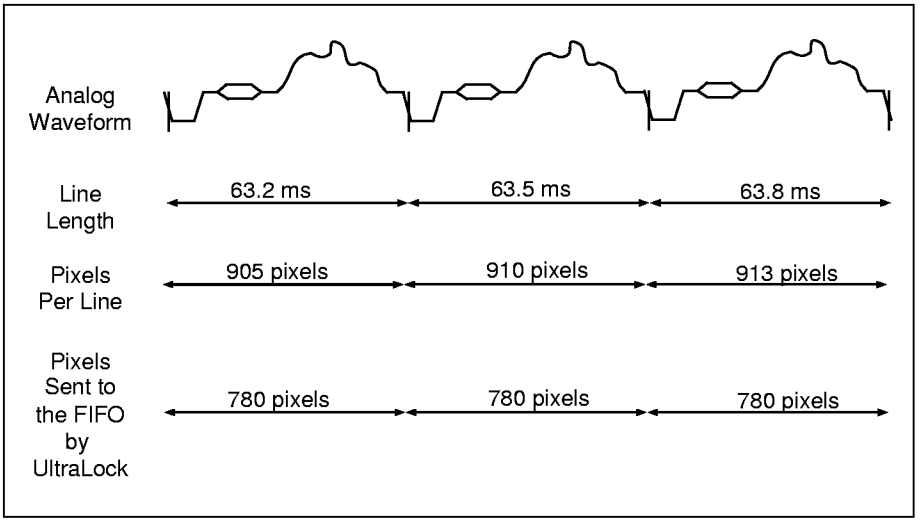
At a 4*Fsc (CLKx1) sample rate there are 910 pixels for NTSC and 1,135 pixels for PAL within a nominal line time interval (63.5 µs for NTSC and 64 µs for PAL). For square pixel NTSC and PAL formats there should only be 780 and 944 pixels per video line, respectively. This is because the square pixel clock rates are slower than a 4*Fsc clock rate, i.e., 12.27 MHz for NTSC and 14.75 MHz for PAL.

UltraLock accommodates line length variations from nominal in the incoming video by always acquiring more samples, at an effective 4*Fsc rate, than are required by the particular video format and outputting the correct number of pixels per line. UltraLock then interpolates the required number of pixels in a way that maintains the stability of the original image despite variation in the line length of the incoming analog waveform.

The example illustrated in Figure 5 shows three successive lines of video being decoded for square pixel NTSC output. The first line is shorter than the nominal NTSC line time interval of 63.5 µs. On this first line, a line time of 63.2 µs sampled at 4*Fsc (14.32 MHz) generates only 905 pixels. The second line matches the nominal line time of 63.5 µs and provides the expected 910 pixels. Finally, the

third line is too long at 63.8 µs within which 913 pixels are generated. In all three cases, UltraLock sends only 780 pixels through the output FIFO.

Figure 5. UltraLock Behavior for NTSC Square Pixel Output



UltraLock can be used to extract any programmable number of pixels from the original video stream as long as the sum of the nominal pixel line length (910 for NTSC and 1,135 for PAL) and the worst case line length variation from nominal in the active region is greater than or equal to the required number of output pixels per line, i.e.,

$$P_{Nom} + P_{Var} \geq P_{Desired}$$

where: P_{Nom} = Nominal number of pixels per line at 4*Fsc sample rate (910 for NTSC, 1,135 for PAL)

P_{Var} = Variation of pixel count from nominal at 4*Fsc (can be a positive or negative number)

$P_{Desired}$ = Desired number of output pixels per line

For a description of how the Bt819A uses the FIFO and the output interface, please see the Output Interface section in the Electrical Interfaces chapter.

It should be noted that, for stable inputs, UltraLock guarantees the time between the falling edges of HRESET only to within one pixel. UltraLock does, however, guarantee the number of active pixels in a line as long as the above relationship holds.

Y/C Separation and Chroma Demodulation

Y/C separation and chroma decoding are handled as shown in Figure 6. Bandpass and notch filters are implemented to separate the composite video stream. The filter responses are shown in Figure 7. The optional chroma comb filter is implemented in the vertical scaling block. See the Video Scaling, Cropping, and Temporal Decimation section in this chapter.

Figure 6. Y/C Separation and Chroma Demodulation for Composite Video

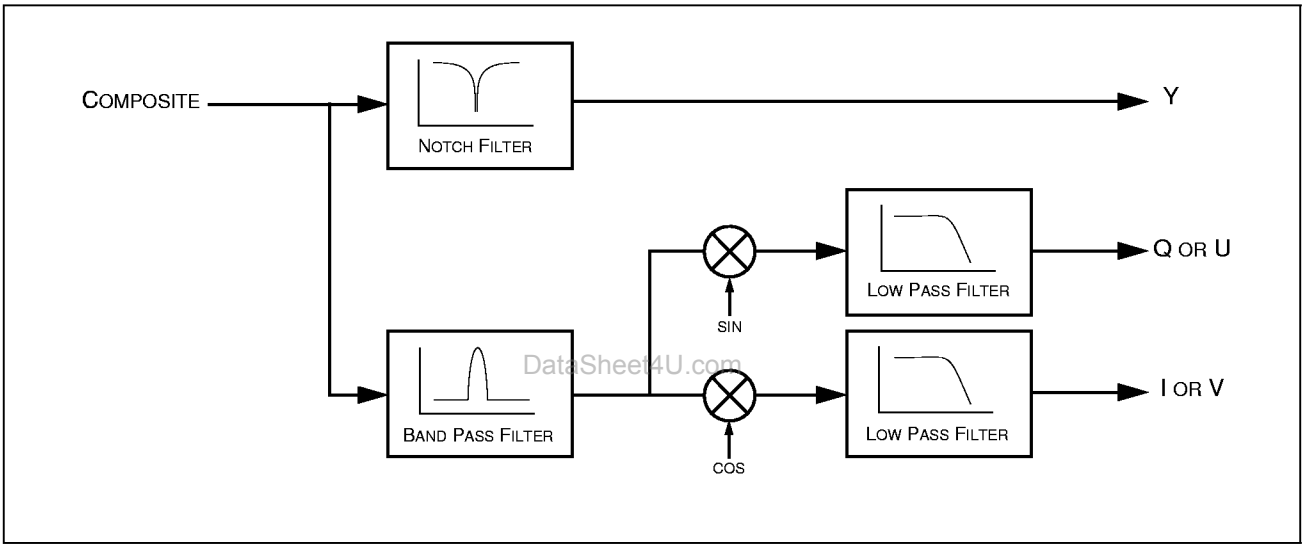


Figure 7. Y/C Separation Filter Responses

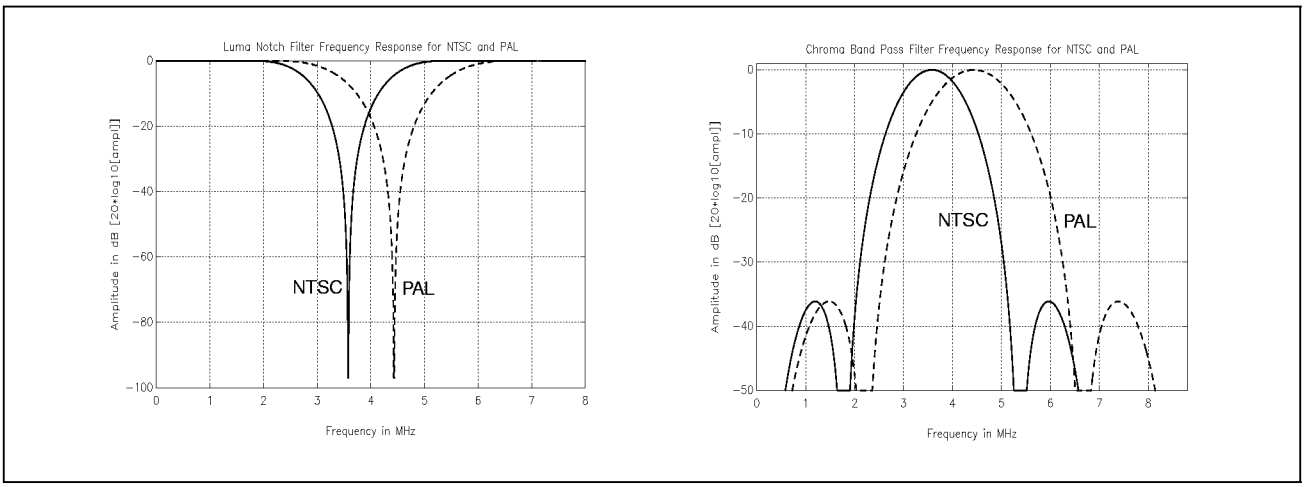


Figure 8. Combined Luma Notch and Optional Luma 3 MHz Low Pass Filter Response

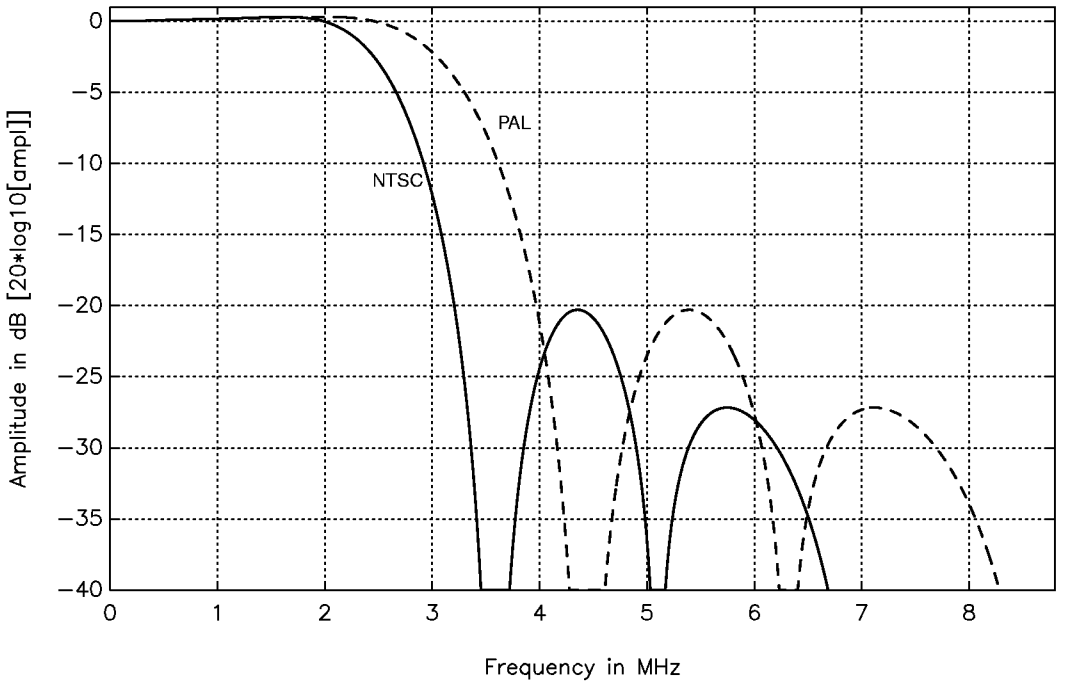


Figure 8 is the combined frequency response of the optional luma 3 MHz low pass filter (Figure 9 in the Video Scaling section), and the luma notch filter in Figure 7. The luma decimation filter is typically enabled during scaling to CIF resolution or below. When scaling is not implemented, the luma decimation filter will normally be bypassed (optional), providing a luma spectrum as shown in Figure 7. Figure 8 shows the combined filter response of the Luma Notch, the Optional Luma 3 MHz Low Pass and the Oversampling filters. Figure 11 shows the combined filter response of the Luma Notch and Oversampling filters. Figure 12 schematically describes the filtering and scaling operations.

In addition to the Y/C separation and chroma demodulation illustrated in Figure 6, the Bt819A also supports chrominance comb filtering as an optional filtering stage after chroma demodulation. The chroma demodulation generates baseband I and Q (NTSC) or U and V (PAL) color difference signals.

For S-Video operation, the digitized luma data bypasses the Y/C separation block completely, and the digitized chrominance is passed directly to the chroma demodulator.

For monochrome operation, the Y/C separation block is also bypassed, and the saturation registers (SAT_U and SAT_V) are set to zero.

Video Scaling, Cropping, and Temporal Decimation

Overview

The Bt819A provides three mechanisms to reduce the amount of video pixel data in its output stream; down-scaling, cropping, and temporal decimation. All three can be controlled independently.

Figure 9. Optional Luma 3 MHz Low Pass Filter Response

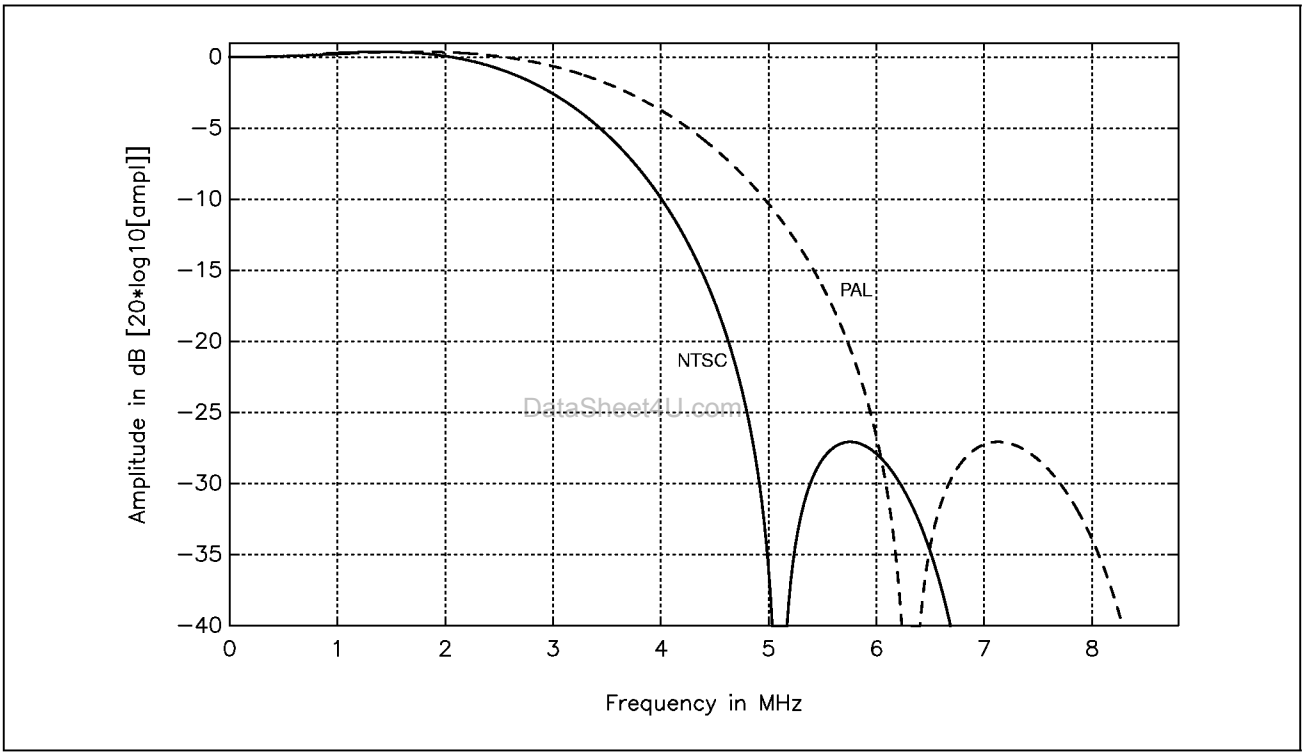
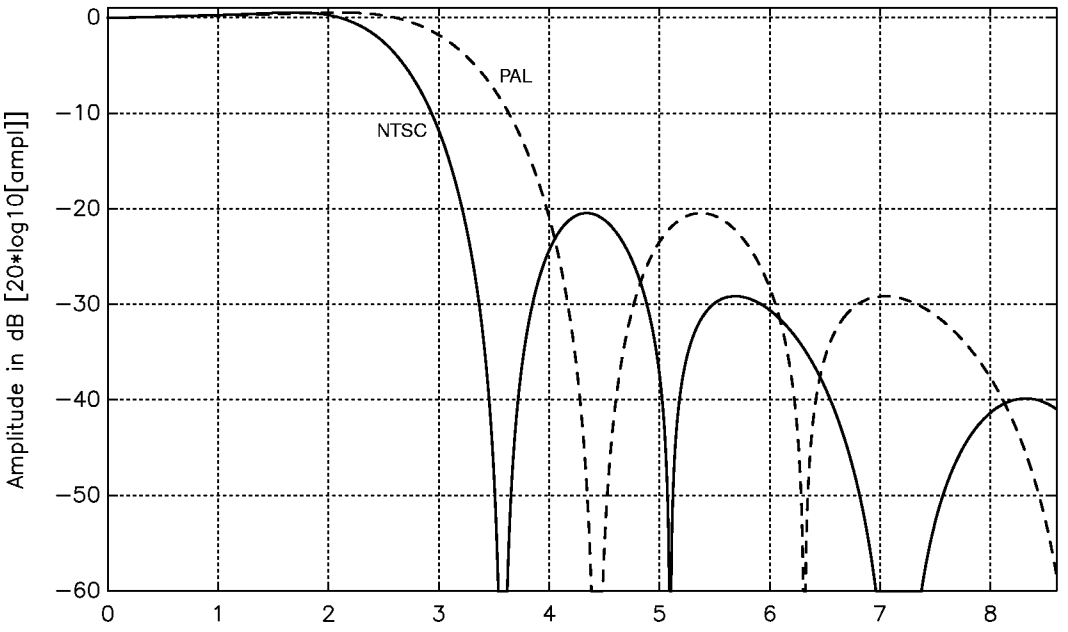
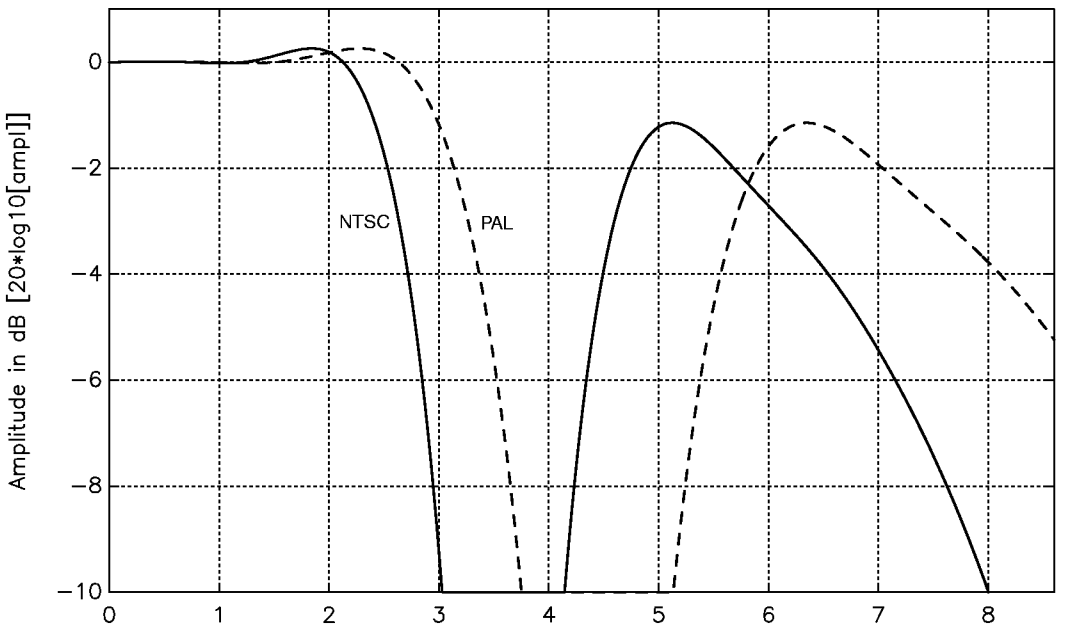


Figure 10. Combined Luma Notch, Optional Luma 3 MHz Low Pass, and Oversampling Filter Response



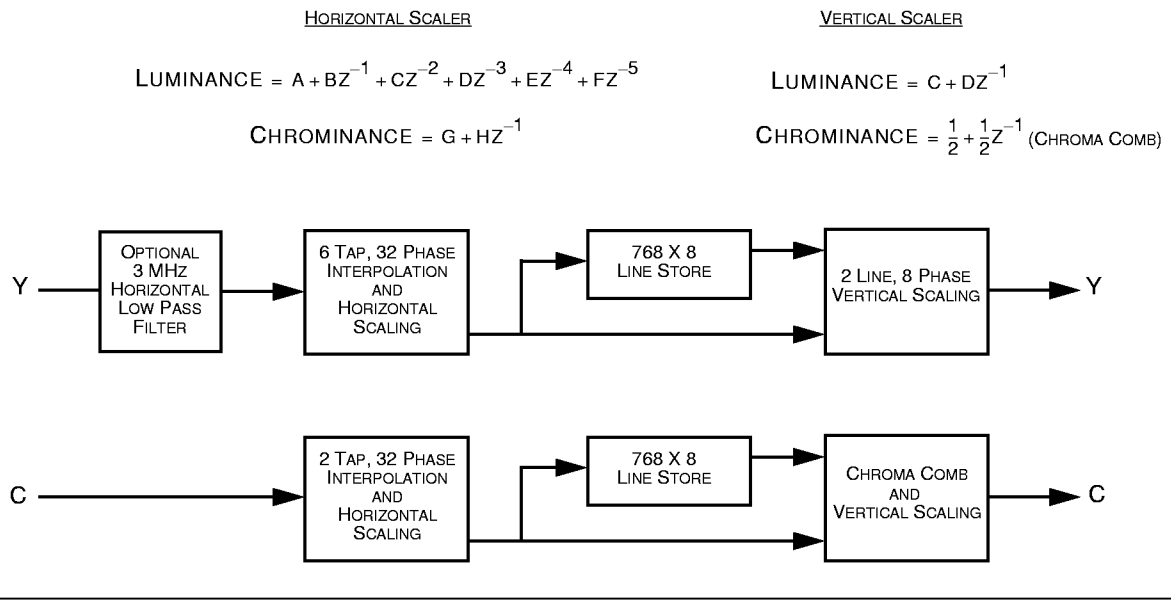
COMBINED RESPONSE OF FILTERS IN FIGURES 7, 9, AND 17

Figure 11. Combined Luma Notch and Oversampling Filter Response



COMBINED RESPONSE OF FILTERS IN FIGURES 7 AND 17

Figure 12. Filtering and Scaling



Note: Z^{-1} refers to a pixel delay in the horizontal direction, and a line delay in the vertical direction. The coefficients are determined by UltraLock and the scaling algorithm

Horizontal and Vertical Scaling

The Bt819A provides independent and arbitrary horizontal and vertical down scaling. The maximum scaling ratio is 14:1 in both X and Y dimensions. The different methods utilized for scaling luminance and chrominance are described in the following sections.

Luminance Scaling

The first stage in horizontal luminance scaling is an optional pre-filter which provides the capability to reduce anti-aliasing artifacts. It is generally desirable to limit the bandwidth of the luminance spectrum prior to performing horizontal scaling because the scaling of high-frequency components may cause image artifacts in the resized image. The 3 MHz low pass filter shown in Figure 9 reduces the horizontal high-frequency spectrum in the luminance signal.

The Bt819A implements horizontal scaling through poly-phase interpolation. The Bt819A uses 32 different phases to accurately interpolate the value of a pixel. This provides an effective pixel jitter of 6 ns.

In simple pixel- and line-dropping algorithms, non-integer scaling ratios introduce a step function in the video signal that effectively introduces high-frequency spectral components. Poly-phase interpolation accurately interpolates to the correct pixel and line position providing more accurate information. This results in aesthetically pleasing video as well as higher compression ratios in bandwidth limited applications. For vertical scaling, the Bt819A uses a 768x8-bit line store to implement a 2-tap, 8-phase interpolation filter. The Bt817A and Bt815A employ line dropping for vertical scaling.

Chrominance Scaling

A 2-tap, 32-phase interpolation filter is used for horizontal scaling of chrominance. Vertical scaling of chrominance is implemented through simple decimation or line dropping, followed by chrominance comb filtering using a 768x8-bit line store.

Scaling Registers

The Horizontal Scaling Ratio Register (HSCALE) is programmed with the horizontal scaling ratio. When outputting unscaled video (in NTSC), the Bt819A will output 910 pixels per line. This corresponds to the pixel rate at f_{CLKx1} (4*Fsc). This register is the control for scaling the video to the desired size. For example, square pixel NTSC requires 780 samples per line, while CCIR601 requires 858 samples per line. HSCALE_HI and HSCALE_LO are two 8-bit registers that, when concatenated, form the 16-bit HSCALE register.

The method below uses pixel ratios to determine the scaling ratio. As such, no floating point math is involved. This is an advantage in certain applications, such as when the scaling is being dynamically controlled by the user with a mouse. The following formula should be used to determine the scaling ratio to be entered into the 16-bit register:

$$\text{NTSC:} \quad HSCALE = [\,(910/P_{desired}) - 1] * 4096$$
$$\text{PAL:} \quad HSCALE = [\,(1135/P_{desired}) - 1] * 4096$$

where: $P_{desired}$ = Desired number of pixels per line of video, including active, sync and blanking.

For example, to scale PAL input to square pixel QCIF, the total number of horizontal pixels is 236:

$$HSCALE = [\,(1135/236) - 1\,] * 4096$$
$$= 15602$$
$$= 0x3CF2$$

An alternative method for determining the HSCALE value uses the ratio of the scaled active region to the unscaled active region as shown below:

$$\text{NTSC:} \quad HSCALE = [\,(754 / HACTIVE) - 1] * 4096$$
$$\text{PAL:} \quad HSCALE = [\,(922 / HACTIVE) - 1] * 4096$$

where: $HACTIVE$ = Desired number of pixels per line of video, not including sync or blanking.

In this equation, the HACTIVE value cannot be cropped; it represents the total active region of the video line. This equation produces roughly the same result as using the full line length ratio shown in the first example. However, due to truncation, the HSCALE values determined using the active pixel ratio will be slightly different than those obtained using the total line length pixel ratio. The values in Table 3 were calculated using the full line length ratio.

The Vertical Scaling Ratio Register (VSCALE) is programmed with the vertical scaling ratio. It defines the number of vertical lines output by the Bt819A. The following formula should be used to determine the value to be entered into this 13-bit register. The loaded value is a two's-complement, negative value.

$$VSCALE = (0x10000 - \{ [(scaling\_ratio) - 1] * 512 \}) \& 0x1FFF$$

For example, to scale PAL input to square pixel QCIF, the total number of vertical lines is 156:

$$VSCALE = (0x10000 - \{ [(4/1) - 1] * 512 \}) \& 0x1FFF$$
$$= 0x1A00$$

Note that only the 13 least significant bits of the VSCALE value are used. The five LSB's of VSCALE_HI and the 8-bit VSCALE_LO register form the 13-bit VSCALE register. The three MSB's of VSCALE_HI are used to control other functions. The user must take care not to alter the values of the three most significant bits when writing a vertical scaling value. The following C-code fragment illustrates changing the vertical scaling value:

```
#define BYTE unsigned char
#define WORD unsigned int
#define VSCALE_HI 0x13
#define VSCALE_LO 0x14

BYTE ReadFromBt819A( BYTE regAddress );
void WriteToBt819A( BYTE regAddress, BYTE regValue );

void SetBt819AVScaling( WORD VSCALE )
{
  BYTE oldVscaleMSByte, newVscaleMSByte;

  /* get existing VscaleMSByte value from */
  /* Bt819A VSCALE_HI register */
  oldVscaleMSByte = ReadFromBt819A( VSCALE_HI );

  /* create a new VscaleMSByte, preserving top 3 bits */
  newVscaleMSByte = (oldVscaleMSByte & 0xE0) | (VSCALE >> 8);

  /* send the new VscaleMSByte to the VSCALE_HI reg */
  WriteToBt819A( VSCALE_HI, newVscaleMSByte );

  /* send the new VscaleLSByte to the VSCALE_LO reg */
  WriteToBt819A( VSCALE_LO, (BYTE) VSCALE );
}
```

where: & = bitwise AND
| = bitwise OR
>> = bit shift, MSB to LSB

If your target machine has sufficient memory to statically store the scaling values locally, the READ operation can be eliminated.

Note on vertical scaling: When scaling below CIF resolution, it may be useful to use a single field as opposed to using both fields. Using a single field will ensure there are no inter-field motion artifacts on the scaled output. When performing single field scaling, the vertical scaling ratio will be twice as large as when scaling with both fields. For example, CIF scaling from one field does not require any vertical scaling, but when scaling from both fields, the scaling ratio is 50%. Also, the non-interlaced bit should be reset when scaling from a single field (INT=0 in the VSCALE_HI register). Table 3 lists scaling ratios for various video formats, and the register values required.

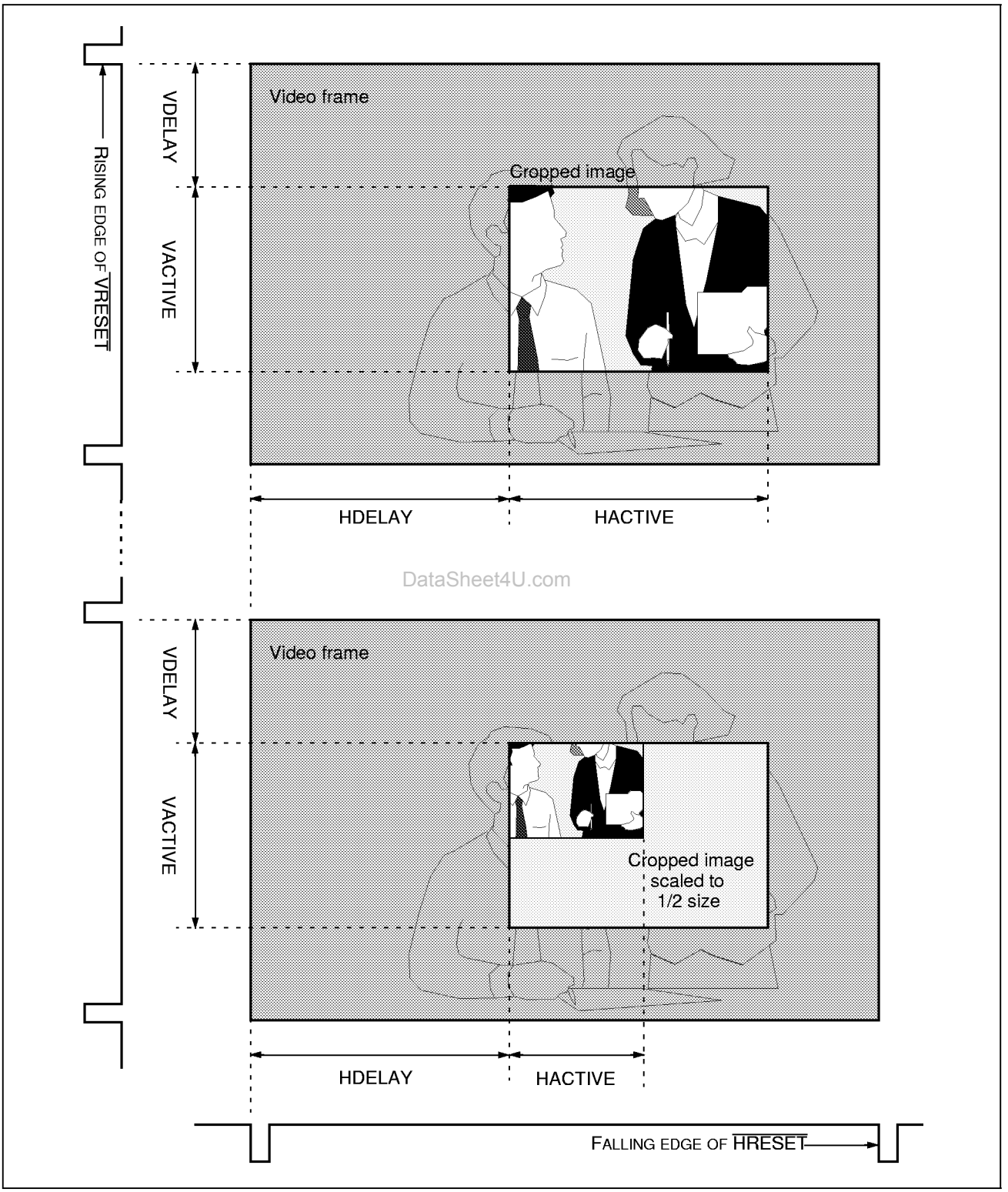
Table 3. Scaling Ratios for Popular Formats Using Frequency Values

Scaling Ratio	Format	Total Resolution (including sync and blanking interval)	Output Resolution (Active Pixels)	HSCALE Register Values	VSCALE Register Values	
					Use Both Fields	Single Field
Full Resolution 1:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR601 PAL SQ Pixel	780x525 858x525 864x625 944x625	640x480 720x480 720x576 768x576	0x02AA 0x00F8 0x0504 0x033C	0x0000 0x0000 0x0000 0x0000	N/A N/A N/A N/A
CIF 2:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR601 PAL SQ Pixel	390x262 429x262 432x312 472x312	320x240 360x240 360x288 384x288	0x1555 0x11F0 0x1A09 0x1679	0x1E00 0x1E00 0x1E00 0x1E00	0x0000 0x0000 0x0000 0x0000
QCIF 4:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR601 PAL SQ Pixel	195x131 214x131 216x156 236x156	160x120 180x120 180x144 192x144	0x3AAA 0x3409 0x4412 0x3CF2	0x1A00 0x1A00 0x1A00 0x1A00	0x1E00 0x1E00 0x1E00 0x1E00
ICON 8:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR601 PAL SQ Pixel	97x65 107x65 108x78 118x78	80x60 90x60 90x72 96x72	0x861A 0x7813 0x9825 0x89E5	0x1200 0x1200 0x1200 0x1200	0x1A00 0x1A00 0x1A00 0x1A00

Image Cropping

Cropping enables the user to output any subsection of the video image. The ACTIVE flag can be programmed to start and stop at any position on the video frame as shown in Figure 13. The start of the active area in the vertical direction is referenced to $\overline{\text{VRESET}}$ (beginning of a new field). In the horizontal direction it is referenced to $\overline{\text{HRESET}}$ (beginning of a new line). The dimensions of the active video region are defined by HDELAY, HACTIVE, VDELAY, and VACTIVE. All four registers are 10-bit values. The two MSBs of each register are contained in the CROP register, while the lower eight bits are in the respective HDELAY_LO, HACTIVE_LO, VDELAY_LO and VACTIVE_LO registers. The vertical and horizontal delay values determine the position of the cropped image within a frame while the horizontal and vertical active values set the pixel dimensions of the cropped image as illustrated in Figure 13.

Figure 13. Effect of the Cropping and Active Registers



Cropping Registers

The Horizontal Delay Register (HDELAY) is programmed with the delay between the falling edge of $\overline{\text{HRESET}}$ and the rising edge of ACTIVE. The count is programmed with respect to the scaled frequency clock. Note that HDELAY should always be an even number.

The Horizontal Active Register (HACTIVE) is programmed with the actual number of active pixels per line of video. This is equivalent to the number of scaled pixels that the Bt819A should generate on a line. For example, if this register contained 90, and HSCALE was programmed to downscale by 4:1, then 90 active pixels would be output. The 90 pixels would be a 4:1 scaled image of the 360 pixels (at CLKx1) starting at count HDELAY. HACTIVE is restricted in the following manner:

HACTIVE + HDELAY ≤ Total Number of Scaled Pixels.

For example, in the NTSC square pixel format, there is a total of 780 pixels, including blanking, sync and active regions. Therefore:

HACTIVE + HDELAY ≤ 780.

When scaled by 2:1 for CIF, the total number of active pixels is 390. Therefore:

HACTIVE +HDELAY ≤ 390.

The HDELAY register is programmed with the number of scaled pixels between HRESET and the first active pixel. Because the front porch is defined as the distance between the last active pixel and the next horizontal sync, the video line can be considered in three components: HDELAY, HACTIVE and the front porch. See Figure 14. When cropping is not implemented, the number of clocks at the 4x sample rate (the CLKx1 rate) in each of these regions is shown below:

	CLKx1 Front Porch	CLKx1 HDELAY	CLKx1 HACTIVE	CLKx1 Total
NTSC	21	135	754	910
PAL	27	186	922	1135

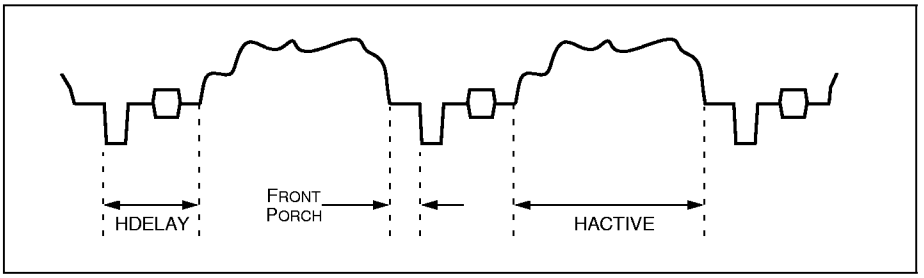
The value for HDELAY is calculated using the following formula:

HDELAY = [(CLKx1_HDELAY / CLKx1_HACTIVE) * HACTIVE] & 0x3FE

CLKx1_HDELAY and CLKx1_HACTIVE are constant values, so the equation becomes:

NTSC: HDELAY = [(135 / 754) * HACTIVE] & 0x3FE
PAL: HDELAY = [(186 / 922) * HACTIVE] & 0x3FE

Figure 14. Regions of the Video Signal



The Vertical Delay Register (VDELAY) is programmed with the delay between the rising edge of $\overline{\text{VRESET}}$ and the start of active video lines. It determines how many lines to skip before initiating the ACTIVE signal. It is programmed with the number of lines to skip at the beginning of a frame.

The Vertical Active Register (VACTIVE) is programmed with the number of lines used in the vertical scaling process. The actual number of vertical lines output from the Bt819A is equal to this register times the vertical scaling ratio. If VSCALE is set to 0x1A00 (4:1) then the actual number of lines output is VACTIVE/4. If VSCALE is set to 0x0000 (1:1) then VACTIVE contains the actual number of vertical lines output.

Note: It is important to note the difference between the implementation of the horizontal registers (HSCALE, HDELAY, and HACTIVE) and the vertical registers (VSCALE, VDELAY, and VACTIVE). Horizontally, HDELAY and HACTIVE are programmed with respect to the scaled pixels defined by HSCALE. Vertically, VDELAY and VACTIVE are programmed with respect to the number of lines before scaling (before VSCALE is applied).

Temporal Decimation

Temporal decimation provides a solution for video synchronization during periods when full frame rate can not be supported due to bandwidth and system restrictions.

For example, when capturing live video for storage, system limitations such as hard disk transfer rates or system bus bandwidth may limit the frame capture rate. If these restrictions limit the frame rate to 15 frames per second, the Bt819A's time scaling operation will enable the system to capture every other frame instead of allowing the hard disk timing restrictions to dictate which frame to capture. This maintains an even distribution of captured frames and alleviates the "jerky" effects caused by systems that simply burst in data when the bandwidth becomes available.

The Bt819A provides temporal decimation on either a field or frame basis. The temporal decimation register (TDEC) is loaded with a value from 1 to 60 (NTSC) or 1 to 50 (PAL). This value is the number of fields or frames skipped by the chip during a sequence of 60 for NTSC or 50 for PAL. Skipped fields and frames are considered inactive, which is indicated by the ACTIVE pin remaining low and QCLK becoming inactive.

Examples:

TDEC = 0x02	Decimation is performed by frames. Two frames are skipped per 60 frames of video, assuming NTSC decoding. Frames 1–29 are output normally, then ACTIVE remains low for one frame. Frames 30–59 are then output followed by another frame of inactive video.
TDEC = 0x9E	Decimation is performed by fields. Thirty fields are output per 60 fields of video, assuming NTSC decoding. This value outputs every other field (every odd field) of video starting with field one in frame one.
TDEC = 0x01	Decimation is performed by frames. One frame is skipped per 50 frames of video, assuming PAL decoding.
TDEC = 0x00	Decimation is not performed. Full frame rate video is output by the Bt819A.

When changing the programming in the temporal decimation register, 0x00 should be loaded first, and then the decimation value. This will ensure that the decimation counter is reset to zero. If zero is not first loaded, the decimation may start on any field or frame in the sequence of 60 (or 50 for PAL). On power-up, this preload is not necessary because the counter is internally reset.

When decimating fields, The Bt819A/7A/5A does not guarantee starting on an even or odd field.

Video Adjustments

The Bt819A provides programmable hue, contrast, saturation, and brightness.

The Hue Adjust Register (HUE)

The Hue Adjust Register is used to offset the hue of the decoded signal. In NTSC, the hue of the video signal is defined as the phase of the subcarrier with reference to the burst. The value programmed in this register is added or subtracted from the phase of the subcarrier, which effectively changes the hue of the video. The hue can be shifted by plus or minus 90 degrees. Because of the nature of PAL encoding, hue adjustments can not be made when decoding PAL.

The Contrast Adjust Register (CONTRAST)

The Contrast Adjust Register (also called the luma gain) provides the ability to change the contrast from approximately 0% to 200% of the original value. The decoded luma value is multiplied by the 9-bit coefficient loaded into this register.

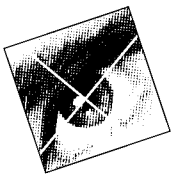
The Saturation Adjust Registers (SAT_U, SAT_V)

The Saturation Adjust Registers are additional color adjustment registers. It is a multiplicative gain of the U and V signals. The value programmed in these registers are the coefficients for the multiplication. The saturation range is from approximately 0% to 200% of the original value.

The Brightness Register (BRIGHT)

The Brightness Register is simply an offset for the decoded luma value. The programmed value is added or subtracted from the original luma value which changes the brightness of the video output. The luma output is in the range of 0 to 255. Brightness adjustment can be made over a range of –64 to +63.

Insert a blank page here. This is page 30



ELECTRICAL INTERFACES

Input Interface

Analog Signal Selection

The Bt819A contains an on-chip 3:1 mux. This mux can be used to switch between three composite sources or two composite sources and one S-video source. In the first configuration, connect the inputs of the mux (MUX0, MUX1 and MUX2) to the three composite sources. In the second configuration, connect two inputs to the composite sources and the other input to the luma component of the S-video connector. In both configurations the output of the mux (MUXOUT) should be connected to the input to the luma A/D (YIN) and the input to the sync detection circuitry (SYNCDET). When implementing S-video, the input to the chroma A/D (CIN) should be connected to the chroma signal of the S-video connector.

Use of the multiplexer is not a requirement for operation. If digitization of only one video source is required, the source may be connected directly to YIN and SYNCDET.

Multiplexer Considerations

The multiplexer is not a break-before-make design. Therefore, during the multiplexer switching time it is possible for the input video signals to be momentarily connected together through the equivalent of 200 ohms.

The multiplexers cannot be switched on a real-time pixel-by-pixel basis.

Autodetection of NTSC or PAL Video

If the Bt819A is configured to decode both NTSC and PAL, the Bt819A can be programmed to automatically detect which format is being input to the chip. Autodetection will select the proper clock source for the format detected, (if NTSC is detected then XTAL0 is selected, if PAL is detected XTAL1 is selected.) Alternatively, the decoding configuration can be programmed by writing to the Input Format Register (0x01).

The Bt819A determines the video source input to the chip by counting the number of lines in a frame. The result of this is indicated in bit NUML in the STATUS register. Based on this bit, the format of the video is determined, and XT0 or XT1 is selected for the clock source. Automatic format detection will select the clock source, but it will not program the required registers. The scaling and cropping registers (VSCALE, HSCALE, VDELAY, HDELAY, VACTIVE, and HACTIVE) as well as the burst delay and AGC delay registers (BDELAY and ADELAY) must be programmed accordingly.

Flash A/D Converters

The Bt819A and Bt817A use two on-chip flash A/D converters to digitize the video signals. YREF+, CREF+ and YREF–, CREF– are the respective top and bottom of the internal resistor ladder.

The input video is always AC-coupled to the decoder. CREF– and YREF– are connected to analog ground. The voltage levels for YREF+ and CREF+ are controlled by the gain control circuitry. If the input video momentarily exceeds the corresponding REF+ voltage it is indicated by LOF and COF in the STATUS register. The Bt815A has only the luma A/D for decoding composite video. The chroma A/D pins are not available on the Bt815A.

A/D Clamping

An internally generated clamp control signal is used to clamp the inputs of the A/D converter for DC restoration of the video signals. Clamping for both the YIN and CIN analog inputs occurs within the horizontal sync tip. The YIN input is always restored to ground while the CIN input is always restored to CLEVEL. CLEVEL must be set with an external resistor network so that it is biased to the midpoint between CREF– and CREF+. External clamping is not required because internal clamping is automatically performed.

Automatic Gain Controls

The REFOUT, CREF+ and YREF+ pins should be connected together as shown in Figure 15. In this configuration, the Bt819A controls the voltage for the top of the reference ladder for each A/D. The automatic gain control adjusts the YREF+ and CREF+ voltage levels until the back porch of the Y video input generates a digital code 0x38 from the A/D. If the video being digitized has a non-standard sync height to video height ratio, the digital code used for AGC may be changed by programming the ADC Interface Register (0x1A).

Crystal Inputs and Clock Generation

The Bt819A has two pairs of pins, XT0I/XT0O and XT1I/XT1O, that are used to input a clock source. If both NTSC and PAL video are being digitized, both clock inputs must be implemented. The XT0 port is used to decode NTSC video and must be configured with a 28.63636 MHz source. The XT1 port is used to decode PAL video and must be configured with a 35.46895 MHz source.

If the Bt819A is configured to decode either NTSC or PAL but not both, then only one clock source must be provided to the chip and it must be connected to the XT0I/XT0O port.

Crystals are specified as follows:

- 28.636363 MHz or 35.468950 MHz
- Third overtone
- Parallel resonant
- 30 pF load capacitance
- 50 ppm
- Series resistance 40 Ω or less

The following crystals are recommended for use with the Bt819A:

1 Standard : This vendor will support very short lead times.
(818) 443-2121
2BAK28M636363GLE30A
2BAK35M468950GLE30A

2 MMD
(714) 444-1402
A30AA3-28.63636MHZ
A30AA3-35.46895MHZ

3 GED
(619) 591-4170
PKHC49-28.63636-.030-005-40R, 3rd overtone crystal
PKHC49-35.46895-.030-005-40R, 3rd overtone crystal

4 M-Tron
(800) 762-8800
MP-1 28.63636, 3rd overtone crystal
MP-1 35.46895, 3rd overtone crystal

5 Monitor
(619) 433-4510
MM49X3C3A-28.63636, 3rd overtone crystal
MM49X3C3A-35.46895, 3rd overtone crystal

6 CTS
(815) 786-8411
R3B55A30-28.63636, 3rd overtone crystal
R3B55A30-35.46895, 3rd overtone crystal

7 Fox
(813) 693-0099
HC49U-28.63636, 3rd overtone crystal
HC49U-35.46895, 3rd overtone crystal

The two clock sources may be configured with either single-ended oscillators, fundamental cut crystals or third overtone mode crystals, parallel resonant. If single-ended oscillators are used they must be connected to XT0I and XT1I. The clock source options and circuit requirements are shown in Figure 16.

The clock source tolerance should be 50 parts-per-million (ppm) or less. Devices that output CMOS voltage levels are required. The load capacitance in the crystal configurations may vary depending on the magnitude of board parasitic capacitance. The Bt819A is dynamic, and, to ensure proper operation, the clocks must be always running, with a minimum frequency of 28.64 MHz.

The CLKx1 and CLKx2 outputs from the Bt819A are generated from XT0 and XT1 clock sources. CLKx2 operates at the crystal frequency (8xFsc) while CLKx1 operates at half the crystal frequency (4xFsc).

Figure 15. Typical External Circuitry

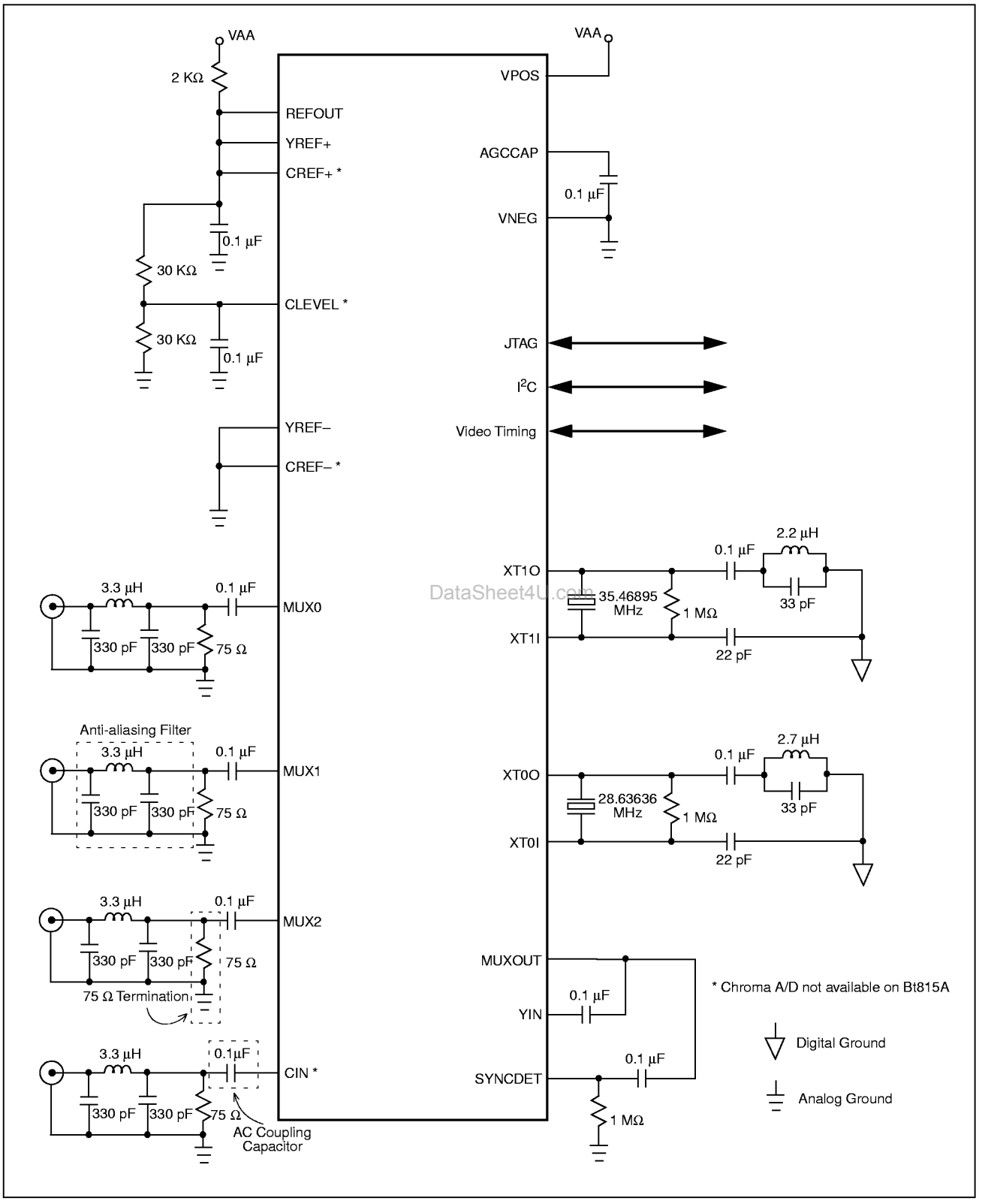
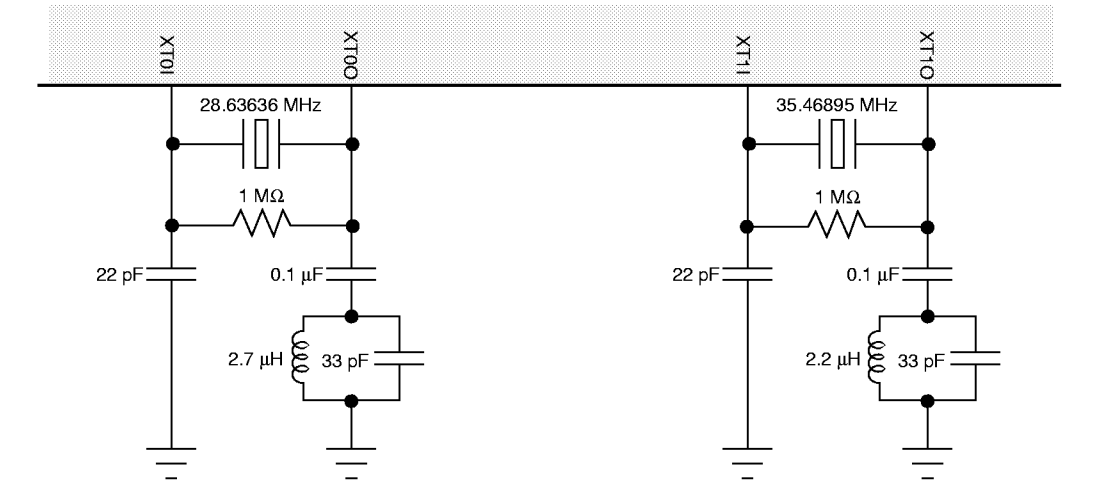


Figure 16. Clock Options

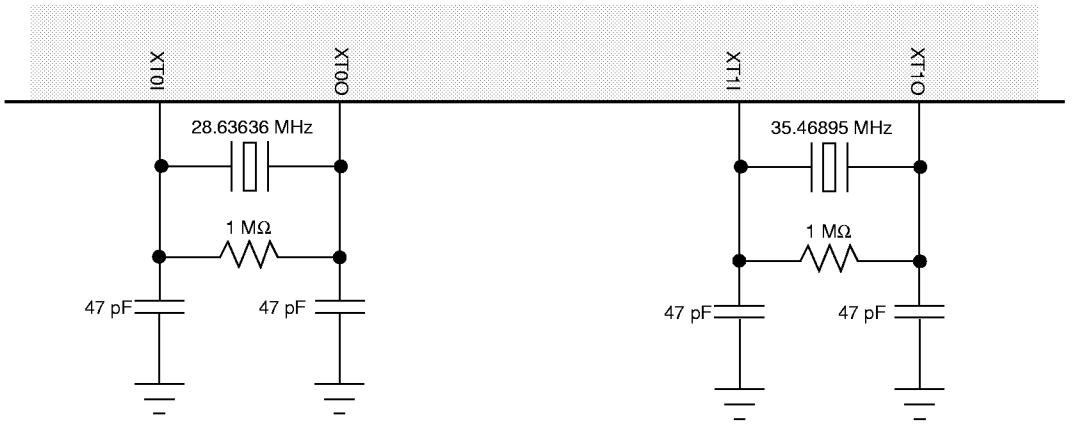


NTSC Third Overtone Mode Crystal Oscillator

PAL Third Overtone Mode Crystal Oscillator

NTSC Single-ended Oscillator

PAL Single-ended Oscillator



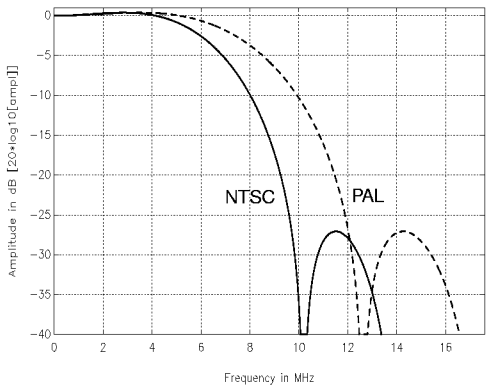
NTSC Fundamental Crystal Oscillator

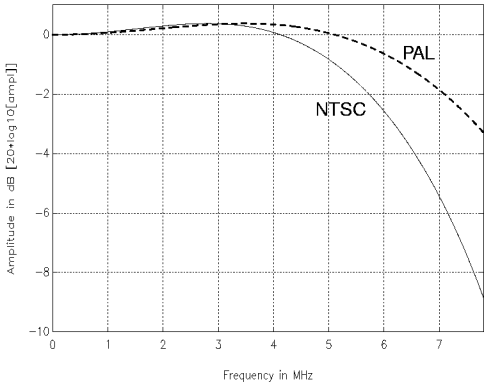
PAL Fundamental Crystal Oscillator

2X Oversampling and Input Filtering

Digitized video needs to be bandlimited in order to avoid aliasing artifacts. Because the Bt819A samples at CLKx2 (8xFsc - twice the normal rate) the analog filtering required at the input to the A/Ds is minimal. The analog video needs to be band limited to 14 MHz. The suggested filters to do this are shown in Figure 15. After digitization, the samples are digitally low pass filtered and then decimated to CLKx1. The response of this low pass filter is shown in Figure 17. The digital low pass filter provides additional bandwidth reduction to limit the video to 6 MHz.

Figure 17. Luma & Chroma 2X Oversampling Filter





Output Interface

Output Interfaces

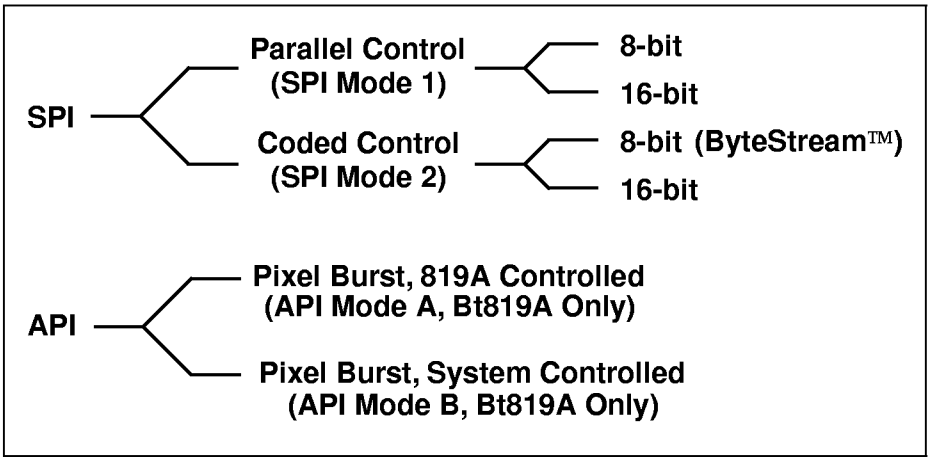
The Bt819A supports two output interfaces: the Synchronous Pixel Interface (SPI) and the Asynchronous Pixel Interface (API). The SPI can support 8-bit or 16-bit YCrCb 4:2:2 data streams, API supports a 16-bit data stream.

In the SPI mode, Bt819A outputs all pixel and control data synchronous with CLKx1 (16-bit mode), or CLKx2 (8-bit mode). Events such as $\overline{\text{HRESET}}$ and $\overline{\text{VRESET}}$ may also be encoded as control codes in the data stream to enable a reduced pin interface (ByteStream™).

In the API mode, only the active pixel data is output synchronous with the CLKIN provided by the system. The pixels are output via a 40-pixel-deep, 16-bit-wide FIFO. $\overline{\text{HRESET}}$ and $\overline{\text{VRESET}}$ are always output on independent pins and, when programmed, are coded onto the data stream.

Mode selections are controlled by the state of the OFORM register. Figure 18 shows a diagram summarizing the different operating modes. Each mode will be covered in detail individually. On power-up, the Bt819A automatically initializes to SPI mode 1, 16 bits wide.

Figure 18. Output Mode Summary (API Mode Only for Bt819A)



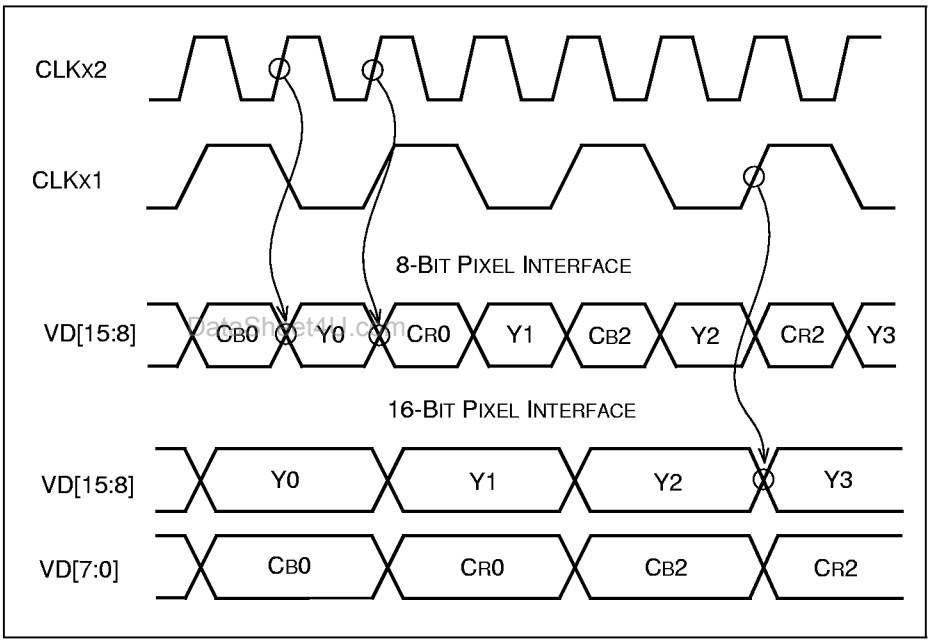
YCrCb Pixel Stream Format, SPI Mode 8- and 16-bit Formats

When the output is configured for an 8-bit pixel interface, the data is output on pins VD[15:8] with the 8 bits of chrominance data preceding 8 bits of luminance data for each pixel. New pixel data is output on the pixel port after each rising edge of CLKx2. When the output is configured for the 16-bit pixel interface, the luminance data is output on VD[15:8], and the chrominance data is output on VD[7:0]. In 16-bit mode, the data is output with respect to CLKx1. See Table 4 for a summary of output interface configurations. The YCrCb 4:2:2 pixel stream follows the CCIR recommendation as illustrated in Figure 19.

Table 4. Pixel/Pin Map

16-bit Pixel Interface																
Pin Name	VD15	VD14	VD13	VD12	VD11	VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0
Data Bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	CrCb7	CrCb6	CrCb5	CrCb4	CrCb3	CrCb2	CrCb1	CrCb0
8-bit Pixel Interface																
Pin Name	VD15	VD14	VD13	VD12	VD11	VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0
Y Data Bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0								
C Data Bit	CrCb7	CrCb6	CrCb5	CrCb4	CrCb3	CrCb2	CrCb1	CrCb0								

Figure 19. YCrCb 4:2:2 Pixel Stream Format (SPI Mode, 8 and16 Bits)



Synchronous Pixel Interface (SPI, Mode 1)

Upon reset, the Bt819A initializes to the SPI output mode 1. In this mode, Bt819A outputs all horizontal and vertical blanking interval pixels in addition to the active pixels synchronous with CLKx1 (16-bit mode), or CLKx2 (8-bit mode). In the SPI-1 mode, the Bt819A output interface is similar to the Bt812 output interface. Figure 20 illustrates Bt819A SPI-1. Figure 21 illustrates the basic timing relationships in the SPI modes. The relationships remain the same for the 16-bit or 8-bit modes. The 16-bit modes use CLKx1 as the reference, and the 8-bit modes use CLKx2. Figure 23 shows the video timing for SPI modes 1 and 2.

Figure 20. Bt819A, Bt817A, Bt815A Synchronous Pixel Interface, Mode 1 (SPI-1)

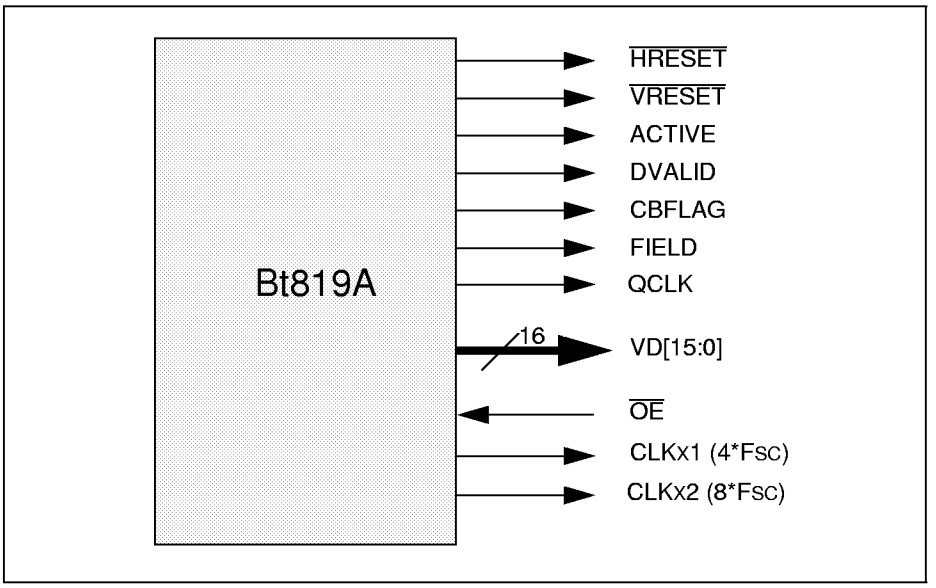
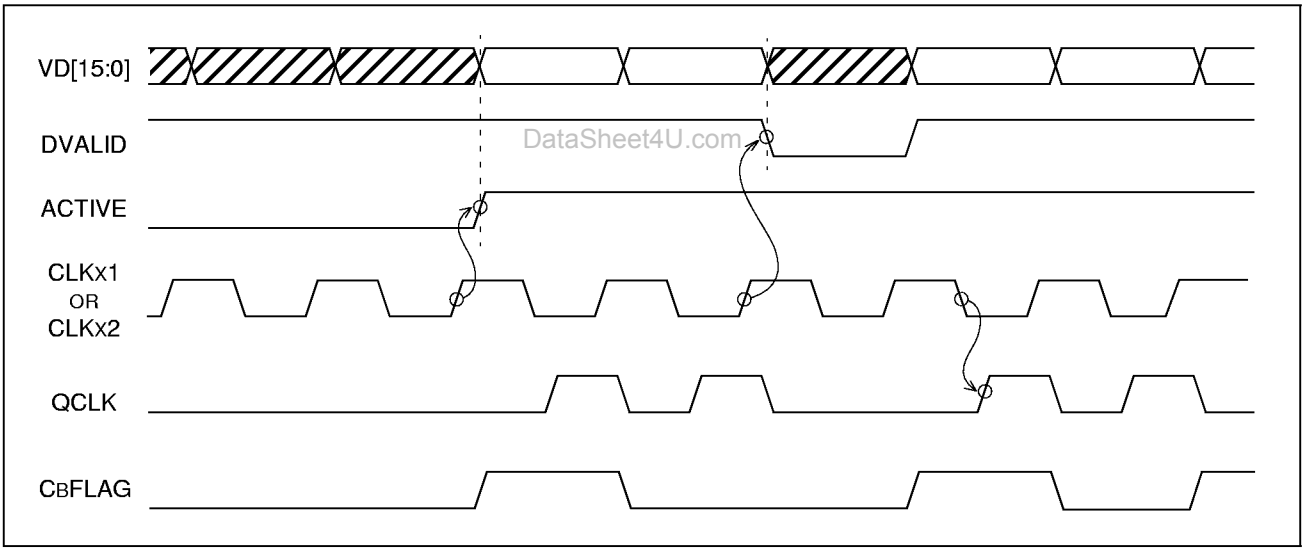


Figure 21. Basic Timing Relationships for SPI Mode 1.



Synchronous Pixel Interface (SPI, Mode 2, ByteStream)

In SPI mode 2, the Bt819A encodes all video timing control signals onto the pixel data bus. ByteStream™ is the 8-bit version of this configuration. Because all timing data is included on the data bus, a complete interface to a video controller can be implemented in only 9 pins: one for CLKx2 and eight for data.

When using coded control, the RANGE bit and the CODE bit must be programmed high. When the RANGE bit is high, the chrominance pixels (both Cr and Cb) are saturated to the range 2 to 253, and the luminance range is limited to the range 16 to 253. In SPI mode 2, the chroma values of 255 and 254, and the luminance values of 0 to 15 are inserted as control codes to indicate video events (Table 5). Chroma value of 255 is used to indicate that the associated luma pixel is a control code; pixel value of 255 also indicates that the CbFlag is high (i.e. the current pixel is a Cb pixel). Similarly, a pixel value of 254 indicates that the luma value is a control code, and the CbFlag is low (Cr pixel).

The first pixel of a line is guaranteed to be a Cb flag;however, due to code precedence relationships, the $\overline{\text{HRESET}}$ code may be delayed by one pixel, so $\overline{\text{HRESET}}$ can occur on a Cr or a Cb pixel. Also, at the beginning of a new field the relationship between $\overline{\text{VRESET}}$ and $\overline{\text{HRESET}}$ may be lost, typically with video from a VCR. As a result, $\overline{\text{VRESET}}$ can occur during either a Cb or a Cr pixel. Figure 22 demonstrates coded control for SPI mode 2 (ByteStream).

Pixel data output ranges are shown in Table 6. Independent of RANGE, decimal 128 indicates zero color information for Cr and Cb. Black is decimal 16 when RANGE=0, and code 0 when RANGE=1.

Table 7 provides a summary of the control sifnal functions for the SPI modes.

Table 5. Description of the Control Codes in the Pixel Stream

Luma Value	Chroma Value	Video Event Description
0x00	0xFF 0xFE	This is an invalid pixel; last valid pixel was a Cb pixel This is an invalid pixel; last valid pixel was a Cr pixel
0x01	0xFF 0xFE	Cb pixel; last pixel was the last active pixel of the line Cr pixel; last pixel was the last active pixel of the line
0x02	0xFF 0xFE	Cb pixel; next pixel is the first active pixel of the line Cr pixel; next pixel is the first active pixel of the line
0x03	0xFF 0xFE	Cb pixel; HRESET of a vertical active line Cr pixel; HRESET of a vertical active line
0x04	0xFF 0xFE	Cb pixel; HRESET of a vertical blank line Cr pixel; HRESET of a vertical blank line
0x05	0xFF 0xFE	Cb pixel; VRESET followed by an even field Cr pixel; VRESET followed by an even field
0x06	0xFF 0xFE	Cb pixel; VRESET followed by an odd field Cr pixel; VRESET followed by an odd field

Table 6. Data Output Ranges

	RANGE = 0	RANGE = 1
Y	16 —> 253	0 —> 255
Cr	2 —> 253	2 —> 253
Cb	2 —> 253	2 —> 253

CCIR 601 Compliance

When the RANGE bit is set to zero, the output levels are fully compliant with the CCIR 601 recommendation. CCIR 601 specifies that nominal video will have Y values ranging from 16 to 235, and Cr and Cb values ranging from 16 to 240. However, excursions outside this range are allowed to handle non-standard video. The only mandatory requirement is that 0 and 255 be reserved for timing information.

Figure 22. Data Output in SPI Mode 2 (ByteStream)

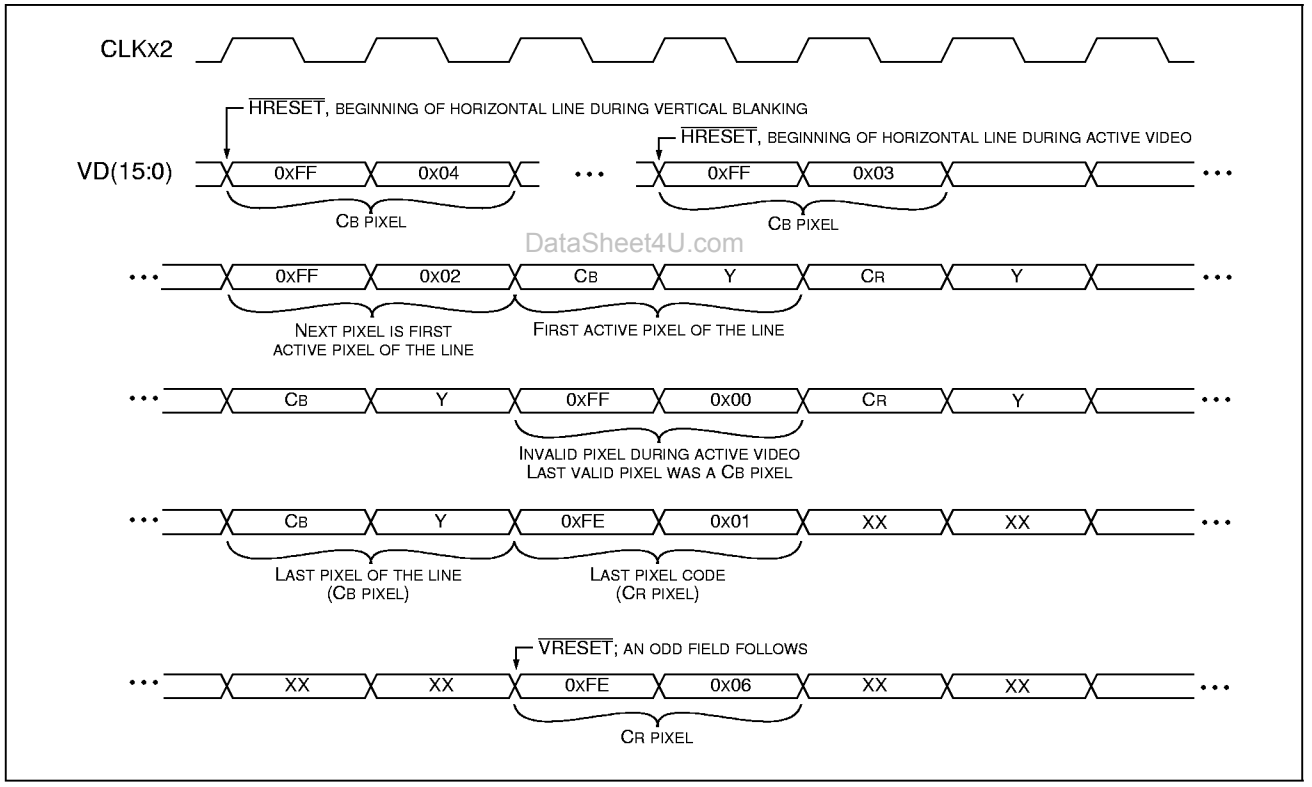
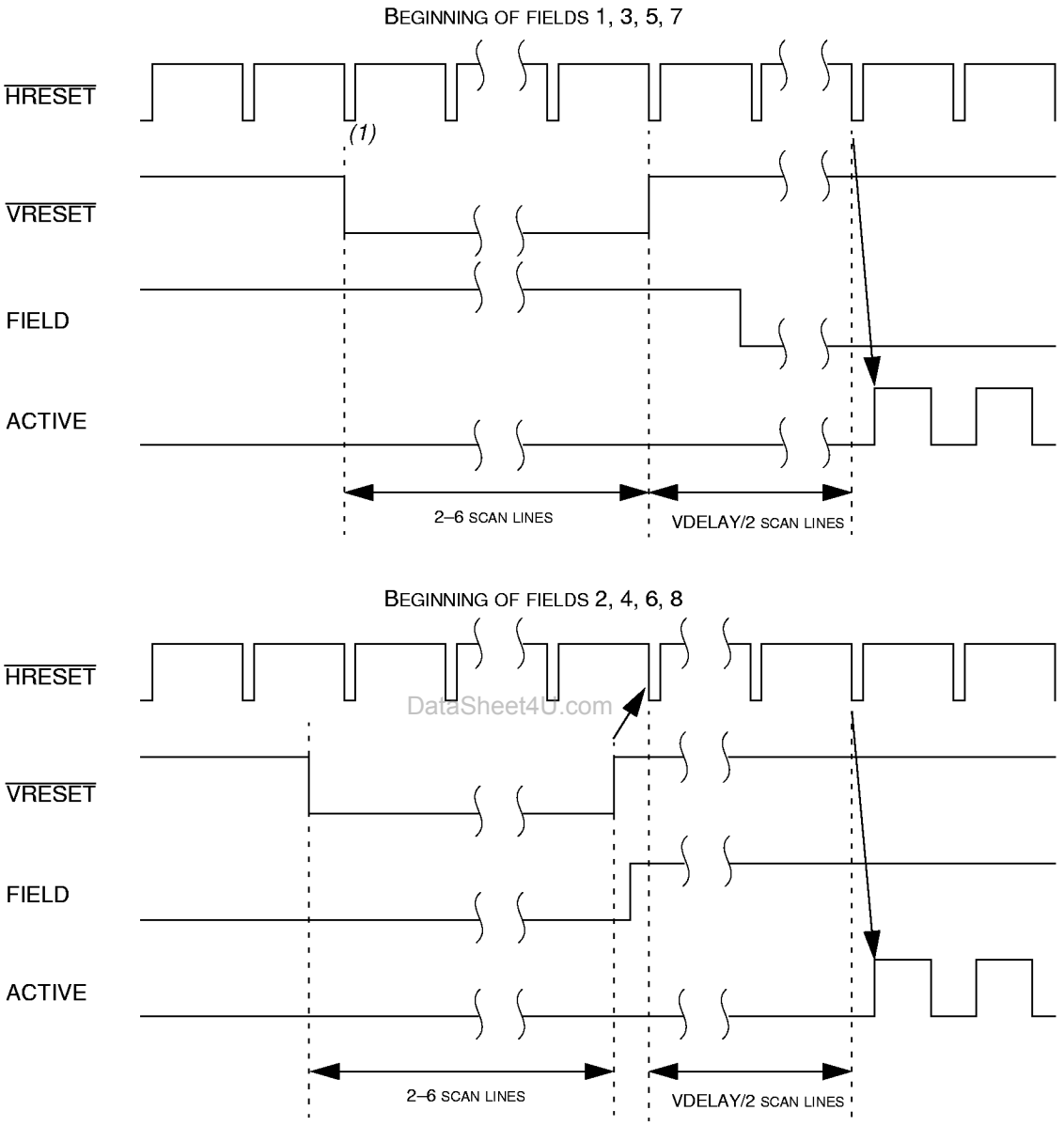


Table 7. Synchronous Pixel Interface (SPI) Control Signals

Signal	Description
$\overline{\text{HRESET}}$	A 64-clock-long active low pulse. It is output following the rising edge of CLKx1. The falling edge of $\overline{\text{HRESET}}$ indicates the beginning of a new video line. See Figure 23 and Figure 24.
$\overline{\text{VRESET}}$	An active low signal that is at least two lines long (for non-VCR sources, $\overline{\text{VRESET}}$ is normally six lines long). It is output following the rising edge of CLKx1. The falling edge of $\overline{\text{VRESET}}$ indicates the beginning of a new field of video output. The falling edge of $\overline{\text{VRESET}}$ lags the falling edge of $\overline{\text{HRESET}}$ by two clock cycles at the start of an odd field. At the start of even fields, the falling edge of $\overline{\text{VRESET}}$ is in the middle of a scan line, horizontal count (HPIXEL/2)+1, on scan line 263 for NTSC and scan line 313 for PAL (Figure 23).
ACTIVE	An active high signal that indicates the beginning of the active video and is output following the rising edge of CLKx1. The ACTIVE flag is used to indicate where nonblanking pixels are present. The start and the end of the ACTIVE signal can be adjusted by programming the VDELAY, VACTIVE, HDELAY, and HACTIVE registers via the I^2C interface. See Figure 23 and Figure 24.
DVALID	An active high pixel qualifier that indicates whether or not the associated pixel is valid. DVALID is independent of the ACTIVE signal. The ACTIVE signal is programmed to output a certain set of pixels. DVALID indicates which pixels are valid within this window. DVALID will toggle high outside of the ACTIVE window, indicating a valid pixel outside the programmed ACTIVE region.
CBFLAG	An active high pulse that indicates when Cb data is being output on the chroma stream. During invalid pixels, CBFLAG holds the value of the last valid pixel.
FIELD	When high, indicates that an even field (field 2) is being output; when low it indicates that an odd field (field 1) is being output. The transition of FIELD is synchronous with the end of active video (i.e. the trailing edge of ACTIVE). The same information can also be derived by latching the $\overline{\text{HRESET}}$ signal with $\overline{\text{VRESET}}$ (Figure 23).
VD[15:0]	The digital output pins for the video data stream.
CLKx1	The 4*Fsc clock output for the format (NTSC or PAL) currently selected. The data is output based on this clock in SPI, 16-bit mode.
CLKx2	The 8*Fsc clock output for the format (NTSC or PAL) currently selected. The data is output based on this clock in SPI, 8-bit mode.
QCLK	A qualified clock output. This pin provides a rising edge only during valid, active pixel data. This output is generated from CLKx1 (or CLKx2 in 8-bit mode), ACTIVE and DVALID. The phase of QCLK is inverted from the CLKx1 (or CLKx2) to ensure adequate setup and hold time with respect to the data outputs. QCLK is not output during control codes when using SPI mode 2.

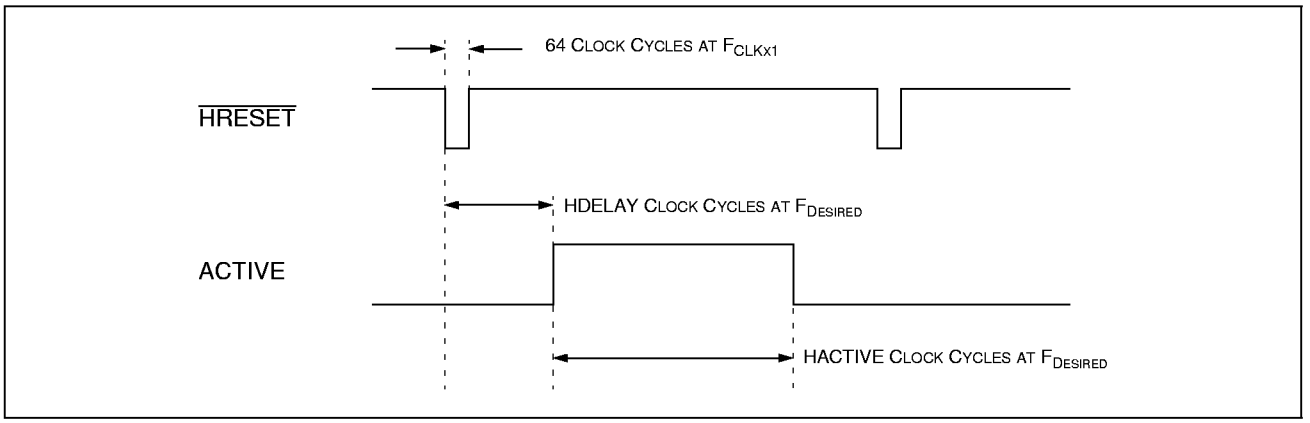
Figure 23. Video Timing in SPI Modes 1 and 2



Notes: (1). HRESET precedes VRESET by two clock cycles at the beginning of fields 1, 3, 5 and 7 to facilitate external field generation.

2. ACTIVE, HRESET, VRESET and FIELD are shown here with their default polarity. The polarity is programmable via the VPOLE register.
3. FIELD transitions with the end of horizontal active video defined by HDELAY and HACTIVE.

Figure 24. Horizontal Timing Signals in the SPI Modes

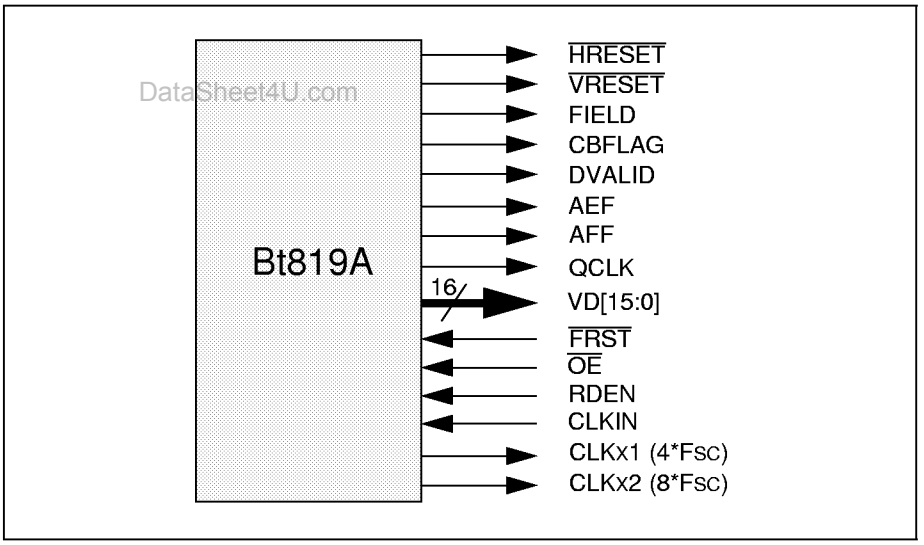


Asynchronous Pixel Interface (API) (Bt819A Only)

In the API modes, the pixel stream generated by the Bt819A is buffered prior to the pixel port outputs by a 40-pixel-deep FIFO. The FIFO input sees a pixel stream coming in 4*Fsc pixels/s. The number of acquired samples or pixels is reduced at the FIFO input by using a pixel qualifier of valid flag that indicates which pixels are to be dropped (i.e., not written into the FIFO). Thus, the Bt819A only writes active, valid video pixels and control codes into the FIFO. When the output is operating asynchronously, CLKIN is used to clock pixels out of the FIFO. CLKIN must be fast enough that the FIFO does not overflow. Thus, CLKIN must operate faster than the effective write rate to the FIFO. Figure 25 illustrates the basic interface. This rate is determined by the number of active pixels per line. For example, in square pixel NTSC, there are 640 active pixels per line input to the FIFO over a period of about 52 µs. As long as the CLKIN rate is greater than 12.27 MHz, the FIFO will never overflow.

API can be used with the external video timing signals, or with coded control signals on the video data bus (as in SPI mode 2). However, in API mode, only the last active pixel and $\overline{\text{VRESET}}$ codes are output (luma values 0x01, 0x05 and 0x06.) In API mode, the control codes are output during either the blanking interval or during invalid data.

Figure 25. Asynchronous Pixel Interface (API)



Mode A: FIFO Controlled by Bt819A (Bt819A Only)

In API mode A, the Bt819A controls the FIFO. DVALID is fed back to RDEN internally. This mode is programmed via the FIFO_BURST bit in the OFORM register. Unlike in SPI mode, DVALID makes no statement about the validity of the current pixel in API. DVALID acts as an indication of how much data is stored in the FIFO. DVALID will go high at the same time that the Almost Full Flag (AFF) goes high, and will go low when the FIFO is empty. RDEN is an input control which allows data to be read from the FIFO. By internally connecting DVALID to RDEN, the user can be assured that the FIFO never overflows.

In mode A CLKIN must be connected to CLKx1. Data will be present at the VD outputs whenever valid data are in the FIFO. There are two indicators of the status of the data present at the FIFO output. One is the DVALID pin. Although this signal is connected internally to the RDEN pin, the signal is still present at the DVALID pin itself. DVALID will go high one CLKIN cycle before valid data is present. The second indicator of valid data is the QCLK signal. This pin provides a qualified clock output, based upon CLKIN, and gated by the presence of readable data in the FIFO. QCLK may be used as a load clock for capturing data from the FIFO. These timing relationships are shown in Figure 26 and Figure 27. While DVALID indicates there is data in the FIFO, ACTIVE or QCLK must be used to differentiate between pixel information and control codes. DVALID indicates the presence of both while ACTIVE and QCLK indicate the presence of only active valid pixels. After the last pixel is read from the FIFO, the data bus and control signals are undefined.

Mode B: FIFO Controlled by System (Bt819A Only)

API mode B is similar to mode A. The only difference is that the DVALID signal is not connected internally to RDEN. The user must monitor the Almost Full Flag (AFF), and the Almost Empty Flag (AEF), and control RDEN manually. In API mode B, QCLK is continuous, and not gated (effectively a delayed output of CLKIN). The timing relationships for API mode B are shown in Figure 28. In addition, Figure 28 shows an external circuit that can be used to control RDEN using the AEF and AFF flags.

Note: In API mode B, the FIFO should not be emptied while active video data is being written into the FIFO. If the FIFO is emptied during the active video line, the last two or three pixels read out of the FIFO will be corrupted. To avoid this, simply use the AEF and AFF flags to control RDEN as shown in Figure 28.

Figure 26. Basic Timing Relationships for API Mode A

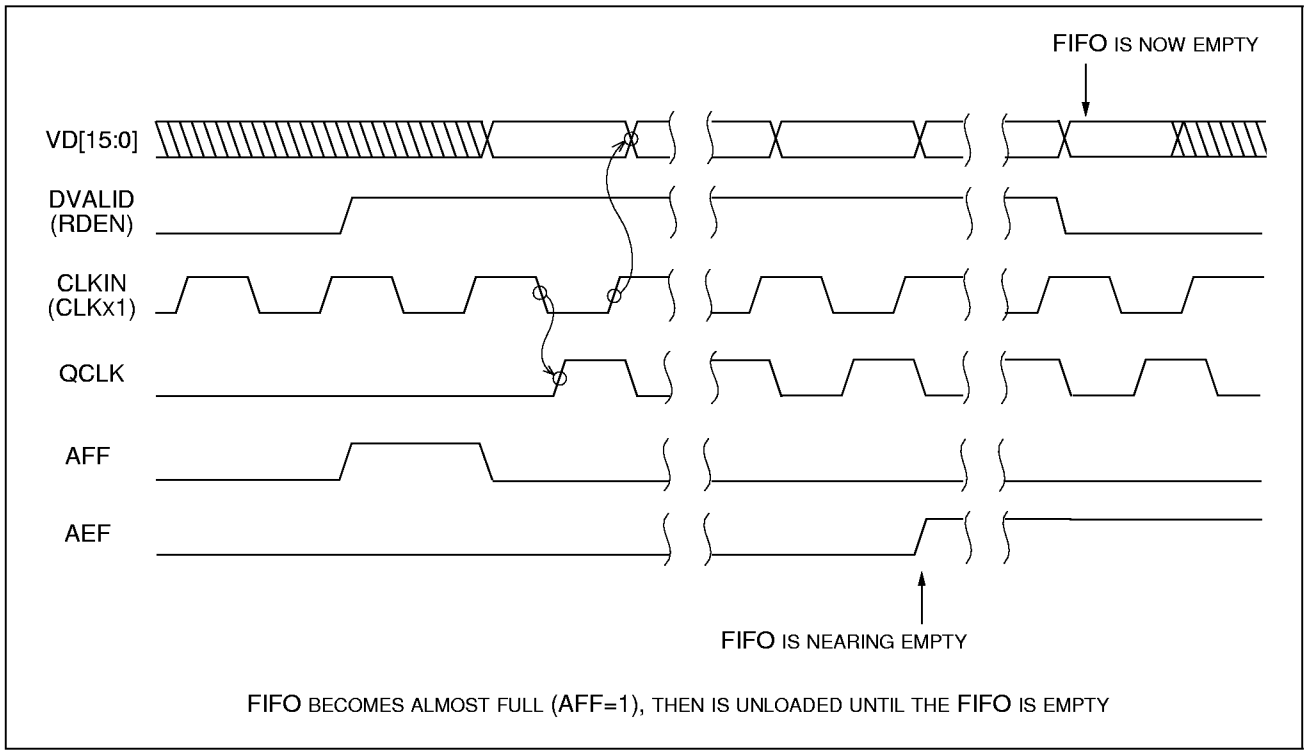


Figure 27. API-A Datastream During a Field Transition

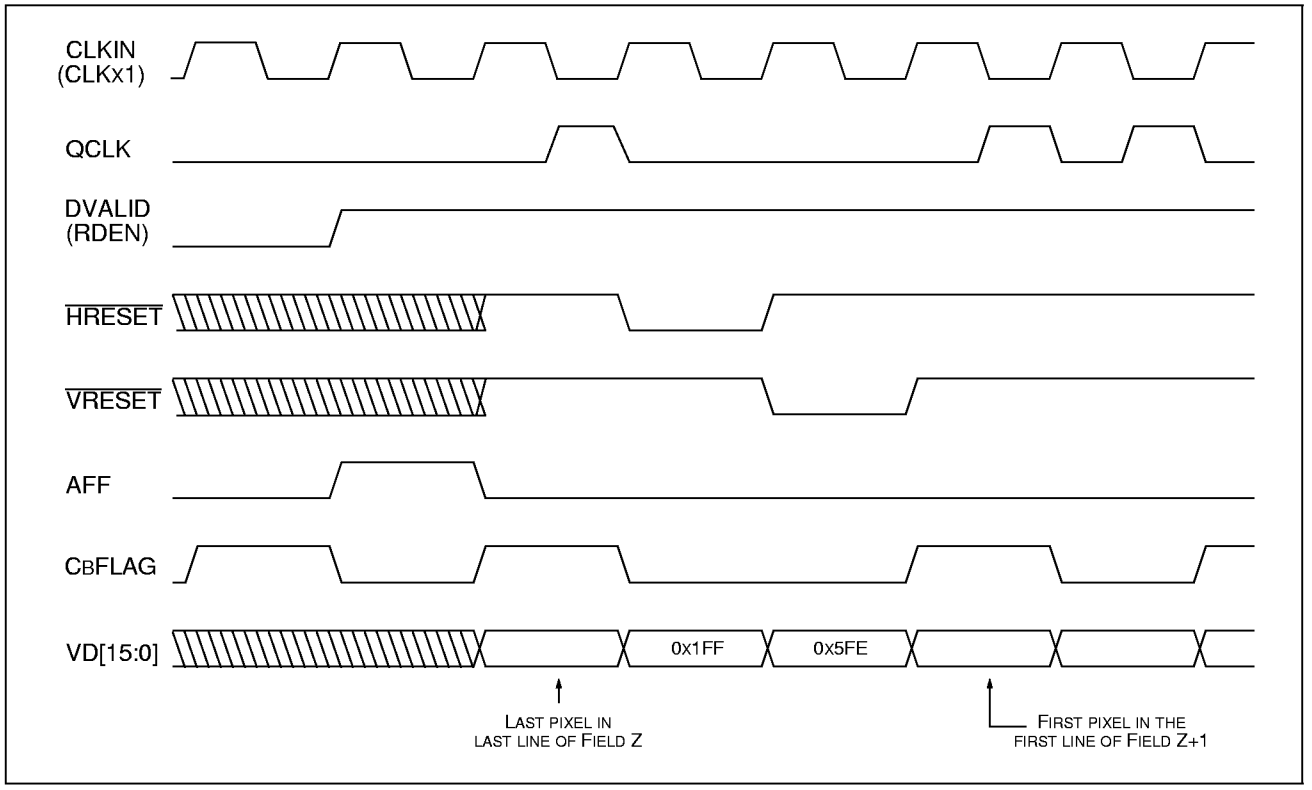
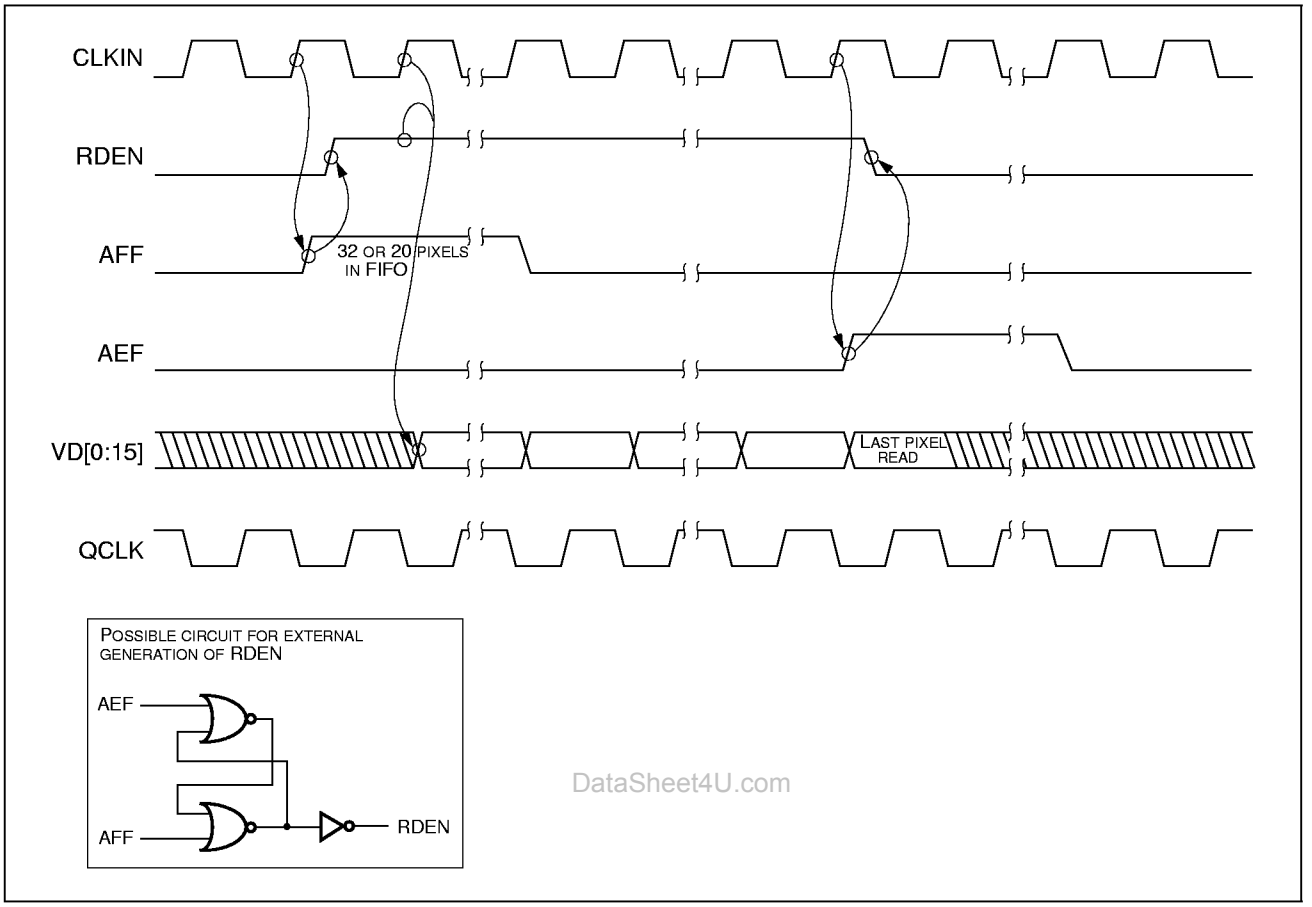


Figure 28. Basic Timing Relationships for API Mode B



Asynchronous Pixel Interface Control Signals

Figure 26, Figure 27 and Table 8 demonstrate the operation of the video timing signals in API mode. As shown in these diagrams, the control codes for HRESET and VRESET are also included in the pixel data stream. This enables a smaller pin count interface to the Bt819A should that be a system requirement. The full video timing interface is also available, and defined in Table 9.

Table 8. Operation of Timing Signals, API (both modes A and B)

	RDEN	ACTIVE	HRESET	VRESET	VD[15:0]	Comment
Line Transition	1	1	1	1	A(1)	
	1	1	1	1	A	
	1	1	1	1	A	
	1	1	1	1	A	Last pixel of old line.
	1	0	0	1	H(2)	End of video line (Code 01FF or 01FE).
	1	1	1	1	A	First pixel of new line.
	0	1	1	1	A	
	0	0	X	X	X	Stop reading from FIFO.
	0	0	X	X	X	
	0	0	X	X	X	
	. .	. .	. .	. .	. .	
Field Transition	0	0	X	X	X	
	1	0	X	X	X	
	1	1	1	1	A	
	1	1	1	1	A	Last pixel in last line of field Z.
	1	0	0	1	H(2)	End of video line (Code 01FF or 01FE).
	1	0	1	0	V(2)	Field transition (Code 05FF for example).
	1	1	1	1	A	First pixel in first line of field Z+1.
	1	1	1	1	A	
	. .	. .	. .	. .	. .	
Field Transition (FIFO Read Until Empty)	0	0	X	X	X	
	1	0	X	X	X	
	1	1	1	1	A	
	1	1	1	1	A	
	1	0	0	1	H(2)	
	0	0	1	0	V(2)	Field transition (Code 06FF for example).
	0	0	X	X	X	
	0	0	X	X	X	
	0	0	X	X	X	

Notes: (1). "A" indicates active pixel data.
(2). If the CODE bit is programmed low (disabling code outputs) the data on the VD bus is invalid. All other outputs remain the same.

Table 9. Asynchronous Pixel Interface Control Signals, Bt819A Only *(1 of 2)*

Pin Name	Comments
$\overline{\text{HRESET}}$	A one-clock-cycle-wide active low pulse. It is output after the last active pixel of a line, and it indicates that the next pixel is the first pixel of the next active line. When the FIFO happens to empty at the end of a line, $\overline{\text{HRESET}}$ remains low until another valid pixel, or $\overline{\text{VRESET}}$.
$\overline{\text{VRESET}}$	A one-clock-cycle-wide active low pulse. It is output after $\overline{\text{HRESET}}$ for the last line in the field. The next pixel is the first active pixel of the next field.
FIELD	When high, indicates an even field (field 2); when low it indicates an odd field (field 1). Field information does not get buffered through the FIFO.
CBFLAG	A one-clock-cycle-wide active high pulse that indicates that Cb chroma data is being output.
DVALID	Goes high when the FIFO has 20 locations filled. This pin will remain high until the FIFO is empty. When the FIFO output rate is the same as the CLKIN rate, DVALID can be connected to RDEN to provide a continuous pixel data stream. DVALID may also be used to gate DMA cycles from the FIFO. DVALID may be programmed to toggle high when the FIFO holds 32 pixels.
AFF	An active high pulse. It transitions high when there are more than 31 pixels of valid data in the FIFO and stays high as long as 32 or more pixels are in the FIFO to be read. This flag may be programmed to toggle high when the FIFO holds 20 pixels. This is useful in API mode B.
AEF	Almost Empty Flag. Indicates that the FIFO is about to empty. Note: The AEF flag is pipelined to the output of the chip. Also, the FIFO is being written into during this time. Therefore, the actual number of pixels in the FIFO when AEF toggles will vary. The number of pixels remaining could be as low as 2 or as high as 8. The system should stop reading from the FIFO as soon as AEF indicates almost empty. See Figure 28 for a recommended circuit.

Table 9. Asynchronous Pixel Interface Control Signals, Bt819A Only *(2 of 2)*

Pin Name	Comments
VD[15:0]	The digital output pins for the video data stream.
RDEN	A read enable for the FIFO. When RDEN is high and there is data in the FIFO, a positive edge on CLKIN outputs a pixel on VD[15:0].
CLKIN	The clock that determines the transfer rate of data from the Bt819A in the API mode. When RDEN is high, this clock puts pixel data on VD[15:0].
CLKx1	The 4*Fsc clock output for the format (NTSC or PAL) currently selected.
CLKx2	The 8*Fsc clock output for the format (NTSC or PAL) currently selected.
QCLK	In mode A, QCLK will generate a clock edge only during active, valid pixels, not during control codes. May be used as a load clock signal with the pixel data. In mode B, QCLK is continuous and not gated (effectively a delayed output of CLKIN).
ACTIVE	Indicates valid pixel data out of the FIFO. This pin toggles high at the same time as DVALID except that DVALID is also high during control codes.
$\overline{\text{FRST}}$	FIFO Reset. Driving this pin low for at least 4 CLKIN cycles will reset the FIFO.

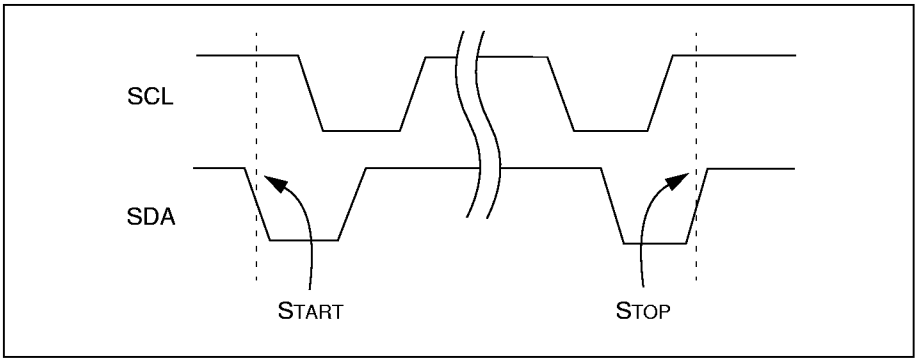
I²C Interface

The Inter-Integrated Circuit (I²C) bus is a two-wire serial interface. Serial clock and data lines, SCL and SDA, are used to transfer data between the bus master and the slave device. The Bt819A can transfer data at a maximum rate of 100 kbits/s. The Bt819A operates as a slave device.

Starting and Stopping

The relationship between SCL and SDA is decoded to provide both a start and stop condition on the bus. To initiate a transfer on the I²C bus, the master must transmit a start pulse to the slave device. This is accomplished by taking the SDA line low while the SCL line is held high. The master should only generate a start pulse at the beginning of the cycle, or after the transfer of a data byte to or from the slave. To terminate a transfer, the master must take the SDA line high while the SCL line is held high. The master may issue a stop pulse at any time during an I²C cycle. Since the I²C bus will interpret any transition on the SDA line during the high phase of the SCL line as a start or stop pulse, care must be taken to ensure that data is stable during the high phase of the clock. This is illustrated in Figure 29.

Figure 29. The Relationship between SCL and SDA



Addressing the Bt819A

An I²C slave address consists of two parts: a 7-bit base address and a single bit R/$\overline{W}$ command. The R/$\overline{W}$ bit is appended to the base address to form the transmitted I²C address, as shown in Figure 30 and Table 10.

Figure 30. I²C Slave Address Configuration

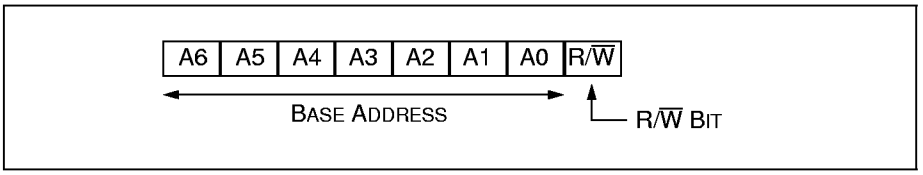


Table 10. Bt819A Address Matrix

I2CCS Pin	Bt819A Base	R/$\overline{W}$ Bit	Action
0	1000100	0	Write
	1000100	1	Read
1	1000101	0	Write
	1000101	1	Read

Reading and Writing

After transmitting a start pulse to initiate a cycle, the master must address the Bt819A. To do this, the master must transmit one of the four valid Bt819A addresses, Most Significant Bit (MSB) first. After transmitting the address, the master must release the SDA line during the low phase of the serial clock, SCL, and wait for an acknowledge. If the transmitted address matches the selected Bt819A address, the Bt819A will respond by driving the SDA line low, generating an acknowledge to the master. The master will sample the SDA line at the rising edge of the SCL line, and proceed with the cycle. If no device responds, including the Bt819A, the master transmits a stop pulse and ends the cycle.

If the slave address R/$\overline{W}$ bit was low, indicating a write, the master will transmit an 8-bit byte to the Bt819A, MSB first. The Bt819A will acknowledge the transfer and load the data into its internal address register. The master may now issue a stop command, a start command, or transfer another 8-bit byte, MSB first, to be loaded into the register pointed to by the internal address register. The Bt819A will then acknowledge the transfer and increment the address register in preparation for the next transfer. As before, the master may now issue a stop command, a start command, or transfer another 8 bits to be loaded into the next location.

If the slave address R/$\overline{W}$ bit was high, indicating a read, the Bt819A will transfer the contents of the register pointed to by its internal address register, MSB first. The master should acknowledge the receipt of the data and pull the SDA line low. As with the write cycle, the address register will be autoincremented in preparation for the next read.

To stop a read transfer, the host must *not* acknowledge the last read cycle. The Bt819A will then release the data bus in preparation for a stop command. If an acknowledge is received, the Bt819A will proceed to transfer the next register.

When the master generates a read from the Bt819A, the Bt819A will start its transfer from whatever location is currently loaded in the address register. Since the address register may not contain the address of the desired register, the master should execute a write cycle, setting the address register to the desired location. After receiving an acknowledge for the transfer of the data into the address register, the master should initiate a read of the Bt819A by starting a new I²C cycle with an appropriate read address. The Bt819A will now transfer the contents of the desired register.

For example, to read register 0x0A, Brightness Control, the master should start a write cycle with an I²C address of 0x88 or 0x8A. After receiving an acknowledge from the Bt819A, the master should transmit the desired address, 0x0A. After re-

ceiving an acknowledge, the master should then start a read cycle with an I²C slave address of 0x89 or 0x8B. The Bt819A will then acknowledge and transfer the contents of register 0x0A. It should be noted that there is no need to issue a stop command after the write cycle. The Bt819A will detect the repeated start command, and start a new I²C cycle. This process is illustrated in Table 11 and Figure 31.

For detailed information on the I²C bus, refer to *"The I²C-Bus and How to Use It,"* published by Philips.

Table 11. Example I²C Data Transactions

Master	Data Flow	Bt819A	Comment
Write to Bt819A			
I²C Start	——>		Master sends Bt819A chip address, i.e. 0x88 or 0x8A.
		ACK	Bt819A generates ACK on successful receipt of chip address.
Sub-address	——>		Master sends sub-address to Bt819A.
		ACK	Bt819A generates ACK on successful receipt of sub-address.
Data(0)	——>		Master sends first data byte to Bt819A.
		ACK(0)	Bt819A generates ACK on successful receipt of 1st data byte.
.	——>	.	
.	——>	.	
.	——>	.	
Data(n)	——>		Master sends nth data byte to Bt819A.
		ACK(n)	Bt819A generates ACK on successful receipt of nth data byte.
I²C Stop			Master generates STOP to end transfer.
Read from Bt819A			
I²C Start	——>		Master sends Bt819A chip address, i.e. 0x89 or 0x8B.
		ACK	Bt819A generates ACK on successful receipt of chip address.
	<——	Data(0)	Bt819A sends first data byte to Master.
ACK(0)			Master generates ACK on successful receipt of 1st data byte.
.	<——	.	
.	<——	.	
.	<——	.	
	<——	Data(n-1)	Bt819A sends (n-1)th data byte to Master.
ACK(n-1)			Master generates ACK on successful receipt of (n-1)th data byte.
	<——	Data(n)	Bt819A sends nth data byte to Master.
NO ACK			Master does not acknowledge nth data byte.
I²C Stop			Master generates STOP to end transfer.

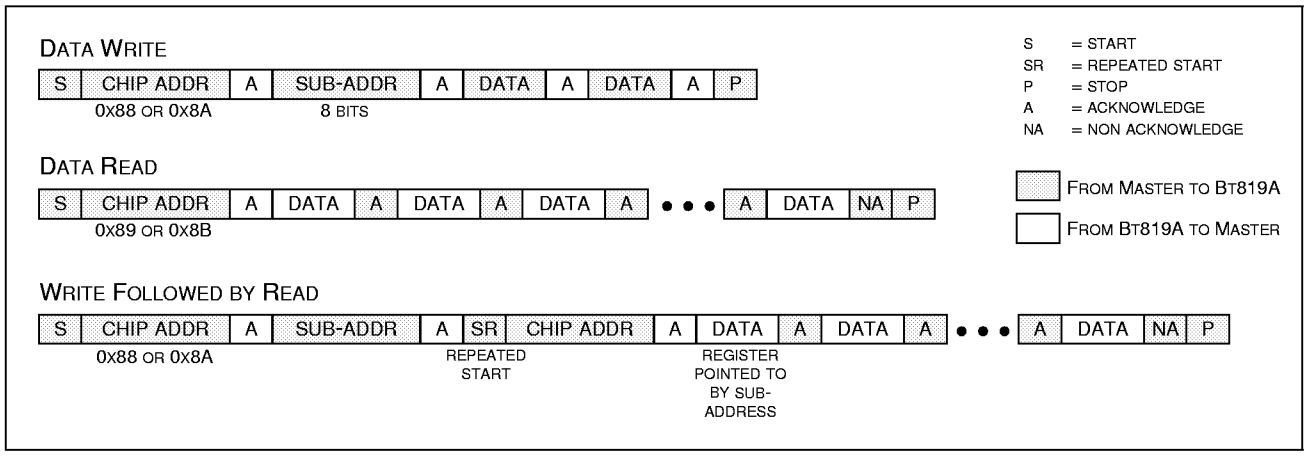
where: I²C Start = I²C start condition and Bt819A chip address (including the R/$\overline{W}$ bit)

Sub-address = the 8-bit sub-address of the Bt819A register, MSB first.

Data(n) = the data to be transferred to/from the addressed register

I²C Stop = I²C stop condition

Figure 31. I²C Protocol Diagram



Software Reset

The contents of the control registers may be reset to their default values by issuing a software reset. A software reset can be accomplished by writing any value to subaddress 0x1F. A read of this location will return an undefined value.

JTAG Interface

Need for Functional Verification

As the complexity of imaging chips increases, the need to easily access individual chips for functional verification is becoming vital. The Bt819A has incorporated special circuitry that allows it to be accessed in full compliance with standards set by the Joint Test Action Group (JTAG). Conforming to IEEE P1149.1 "Standard Test Access Port and Boundary Scan Architecture," the Bt819A has dedicated pins that are used for testability purposes only.

JTAG Approach to Testability

JTAG's approach to testability utilizes boundary scan cells placed at each digital pin and digital interface (a digital interface is the boundary between an analog block and a digital block within the Bt819A). All cells are interconnected into a boundary scan register, as shown in Table 12, that applies or captures test data to be used for functional verification of the integrated circuit. JTAG is particularly useful for board testers using functional testing methods.

JTAG consists of five dedicated pins comprising the Test Access Port (TAP). These pins are Test Mode Select (TMS), Test Clock (TCK), Test Data Input (TDI), Test Data Out (TDO) and Test Reset ($\overline{\text{TRST}}$). The $\overline{\text{TRST}}$ pin will reset the JTAG controller when pulled low at any time.Verification of the integrated circuit and its connection to other modules on the printed circuit board can be achieved through these five TAP pins. With boundary scan cells at each digital interface and pin, the Bt819A has the capability to apply and capture the respective logic levels. Since all of the digital pins are interconnected as a long shift register, the TAP logic has access and control of all the necessary pins to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry. The output result is scanned out on the TDO pin and externally checked. While isolating the Bt819A from other components on the board, the user has easy access to all Bt819A digital pins and digital interfaces through the TAP and can perform complete functionality tests without using expensive bed-of-nails testers.

Optional Device ID Register

The Bt819A has the optional device identification register defined by the JTAG specification. This register contains information concerning the revision, actual part number, and manufacturers identification code specific to Brooktree. This register can be accessed through the TAP controller via an optional JTAG instruction. Refer to Table 13.

Verification with the Tap Controller

A variety of verification procedures can be performed through the TAP controller. With a set of four instructions, the Bt819A can verify board connectivity at all digital interfaces and pins. The instructions are accessible by using a state machine standard to all JTAG controllers and are: Sample/Preload, Extest, ID Code, and Bypass (see Figure 32). Refer to the IEEE P1149.1 specification for details concerning the Instruction Register and JTAG state machine.

Brooktree has created a BSDL with the AT&T BSD Editor. Table 12 shows the boundary scan definition from this file. Should JTAG testing be implemented, a disk with an ASCII version of the complete BSDL file may be obtained by calling 1-800-2Bt Apps.

Table 12. Bt819A Boundary Scan Register Definition *(1 of 2)*

```
attribute BOUNDARY_REGISTER of 819A: entity is
        "   0 (BC_1, *, internal, X)," &
        "   1 (BC_1, *, control, 1)," &
        "   2 (BC_1, *, internal, X)," &
        "   3 (BC_1, *, internal, X)," &
        "   4 (BC_1, *, internal, X)," &
        "   5 (BC_1, *, internal, X)," &
        "   6 (BC_1, *, internal, X)," &
        "   7 (BC_1, *, internal, X)," &
        "   8 (BC_1, *, internal, X)," &
        "   9 (BC_1, *, internal, X)," &
        "  10 (BC_1, *, internal, 0)," &
        "  11 (BC_1, *, internal, 0)," &
        "  12 (BC_1, *, internal, 0)," &
        "  13 (BC_1, *, internal, 0)," &
        "  14 (BC_1, *, internal, 0)," &
        "  15 (BC_1, *, internal, 0)," &
        "  16 (BC_1, *, internal, 0)," &
        "  17 (BC_1, *, internal, 0)," &
        "  18 (BC_1, *, internal, 0)," &
        "  19 (BC_1, *, internal, 0)," &
        "  20 (BC_1, *, internal, 0)," &
        "  21 (BC_1, *, internal, 0)," &
        "  22 (BC_1, *, internal, 0)," &
        "  23 (BC_1, *, internal, 0)," &
        "  24 (BC_1, *, internal, 0)," &
        "  25 (BC_1, *, control, 0)," &
        "  26 (BC_1, FIELD, output3, X, 25, 0, Z)," &
        "  27 (BC_1, NVRESET, output3, X, 25, 0, Z)," &
        "  28 (BC_1, XTFMT, input, X)," &
        "  29 (BC_1, NOSEN, input, X)," &
        "  30 (BC_1, NHRESET, output3, X, 25, 0, Z)," &
        "  31 (BC_1, ACTIVE, output3, X, 25, 0, Z)," &
        "  32 (BC_1, DVALID, output3, X, 25, 0, Z)," &
        "  33 (BC_1, RDEN, input, X)," &
```

Table 12. Bt819A Boundary Scan Register Definition *(2 of 2)*

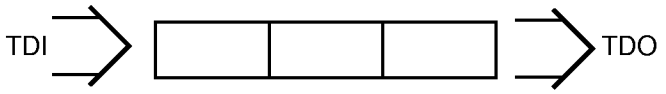
```
        "  34 (BC_1, AFF, output3, X, 25, 0, Z)," &
        "  35 (BC_1, AEF, output3, X, 25, 0, Z)," &
        "  36 (BC_1, NFRST, input, X)," &
        "  37 (BC_1, CBFLAG, output3, X, 25, 0, Z)," &
        "  38 (BC_3, NVSEN, input, X)," &
        "  39 (BC_1, CLKIN, input, X)," &
        "  40 (BC_1, QCLK, output3, X, 25, 0, Z)," &
        "  41 (BC_1, CLKX1, output3, X, 25, 0, Z)," &
        "  42 (BC_1, NOE, input, 1)," &
        "  43 (BC_1, CLKX2, output3, X, 25, 0, Z)," &
        "  44 (BC_1, VDB(8), output3, X, 25, 0, Z)," &
        "  45 (BC_1, VDB(9), output3, X, 25, 0, Z)," &
        "  46 (BC_1, VDB(10), output3, X, 25, 0, Z)," &
        "  47 (BC_1, VDB(11), output3, X, 25, 0, Z)," &
        "  48 (BC_1, VDB(12), output3, X, 25, 0, Z)," &
        "  49 (BC_1, VDB(13), output3, X, 25, 0, Z)," &
        "  50 (BC_1, VDB(14), output3, X, 25, 0, Z)," &
        "  51 (BC_1, VDB(15), output3, X, 25, 0, Z)," &
        "  52 (BC_1, *, internal, X)," &
        "  53 (BC_1, XT0I, input, X)," &
        "  54 (BC_1, I2CCS, input, X)," &
        "  55 (BC_1, NRST, input, X)," &
        "  56 (BC_1, *, internal, X)," &
        "  57 (BC_1, XT1I, input, X)," &
        "  58 (BC_1, SDA, output3, 1, 58, 1, Weak1)," &
        "  59 (BC_1, SDA, input, X)," &
        "  60 (BC_1, SCL, input, X)," &
        "  61 (BC_1, VDA(0), output3, 0, 1, 1, Z)," &
        "  62 (BC_1, VDA(0), input, X)," &
        "  63 (BC_1, VDA(1), output3, 0, 1, 1, Z)," &
        "  64 (BC_1, VDA(1), input, X)," &
        "  65 (BC_1, VDA(2), output3, 0, 1, 1, Z)," &
        "  66 (BC_1, VDA(2), input, X)," &
        "  67 (BC_1, VDA(3), output3, 0, 1, 1, Z)," &
        "  68 (BC_1, VDA(3), input, X)," &
        "  69 (BC_1, VDA(4), output3, 0, 1, 1, Z)," &
        "  70 (BC_1, VDA(4), input, X)," &
        "  71 (BC_1, VDA(5), output3, 0, 1, 1, Z)," &
        "  72 (BC_1, VDA(5), input, X)," &
        "  73 (BC_1, VDA(6), output3, 0, 1, 1, Z)," &
        "  74 (BC_1, VDA(6), input, X)," &
        "  75 (BC_1, VDA(7), output3, 0, 1, 1, Z)," &
        "  76 (BC_1, VDA(7), input, X)," &
        "  77 (BC_1, TWREN, input, X)," &
        "  78 (BC_0, *, internal, 0)," &
        "  79 (BC_0, *, internal, 0)";
end 819A;
```

Table 13. Device Identification Register

VERSION	PART NUMBER	MANUFACTURER ID	
X X X X	0 0 0 0 0 0 1 1 0 0 1 1 0 0 1 1	0 0 0 1 1 0 1 0 1 1 0 1	
0	0819, 0x0333	0x0D6	

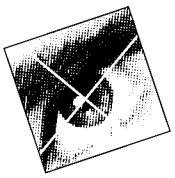
Note: The Part Number remains the same for all three parts: Bt819A, Bt817A and Bt815A

Figure 32. Instruction Register (IR)



EXTEST	0
Sample/Preload	0
ID Code	0
Bypass	1

Insert a blank page here. This is page 60



PC BOARD LAYOUT CONSIDERATIONS

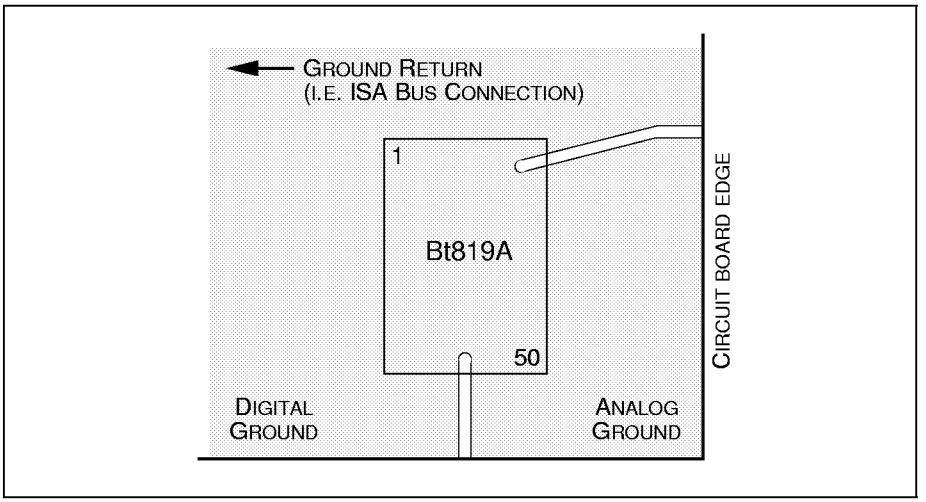
The layout should be optimized for lowest noise on the Bt819A power and ground lines by shielding the digital inputs/outputs and providing good decoupling. The lead length between groups of power and ground pins should be minimized to reduce inductive ringing. Figure 36 shows an example schematic.

Ground Planes

The ground plane area should encompass all Bt819A ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt819A, the analog input traces, any input amplifiers, and all the digital signal traces leading to the Bt819A.

The Bt819A has digital grounds (GND) and analog grounds (AGND and VNEG). The layout for the ground plane should be such that the two planes are at the same electrical potential, but they should be isolated from each other in the areas surrounding the chip. Also, the return path for current should be through the digital plane. See Figure 33.

Figure 33. Example Ground Plane Layout



Power Planes

The power plane area should encompass all Bt819A power pins, voltage reference circuitry, power supply bypass circuitry for the Bt819A, the analog input traces, any input amplifiers, and all the digital signal traces leading to the Bt819A.

The Bt819A has digital power (VDD) and analog power (VAA and VPOS). The layout for the power plane should be such that the two planes are at the same electrical potential, but they should be isolated from each other in the areas surrounding the chip. Also, the return path for current should be through the digital plane. This is the same layout as shown for the ground plane (Figure 33). When using a regulator, circuitry must be included to ensure proper power sequencing. The circuitry shown in Figure 34 should help in this regard.

Supply Decoupling

The bypass capacitors should be installed with the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. These capacitors should also be placed as close as possible to the device.

Each group of VAA and VDD pins should have a 0.1 µF ceramic bypass capacitor to ground, located as close as possible to the device.

Additionally, 10 µF capacitors should be connected between the analog power and ground planes, as well as between the digital power and ground planes. These capacitors are at the same electrical potential, but provide additional decoupling by being physically close to the Bt819A power and ground planes. See Figure 35 for additional information about power supply decoupling.

Digital Signal Interconnect

The digital signals of the Bt819A should be isolated as much as possible from the analog signals and other analog circuitry. Also, the digital signals should not overlay the analog power plane.

Any termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

Long lengths of closely-spaced parallel video signals should be avoided to minimize crosstalk. Ideally, there should be a ground line between the video signal traces driving the YIN and CIN inputs.

Also, high-speed TTL signals should not be routed close to the analog signals to minimize noise coupling.

Latch-up Avoidance

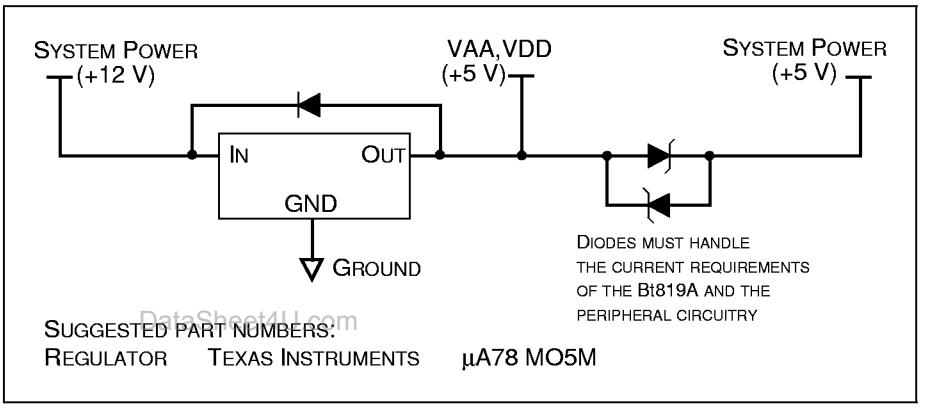
Latch-up is a failure mechanism inherent to any CMOS device. It is triggered by static or impulse voltages on any signal input pin exceeding the voltage on the power pins by more than 0.5 V, or falling below the GND pins by more than 0.5 V. Latch-up can also occur if the voltage on any power pin exceeds the voltage on any other power pin by more than 0.5 V.

In some cases, devices with mixed signal interfaces, such as the Bt819A, can appear more sensitive to latch-up. In reality, this is not the case. However, mixed signal devices tend to interact with peripheral devices such as video monitors or cameras that are referenced to different ground potentials, or apply voltages to the device prior to the time that its power system is stable. This interaction sometimes creates conditions amenable to the onset of latch-up.

To maintain a robust design with the Bt819A, the following precautions should be taken:

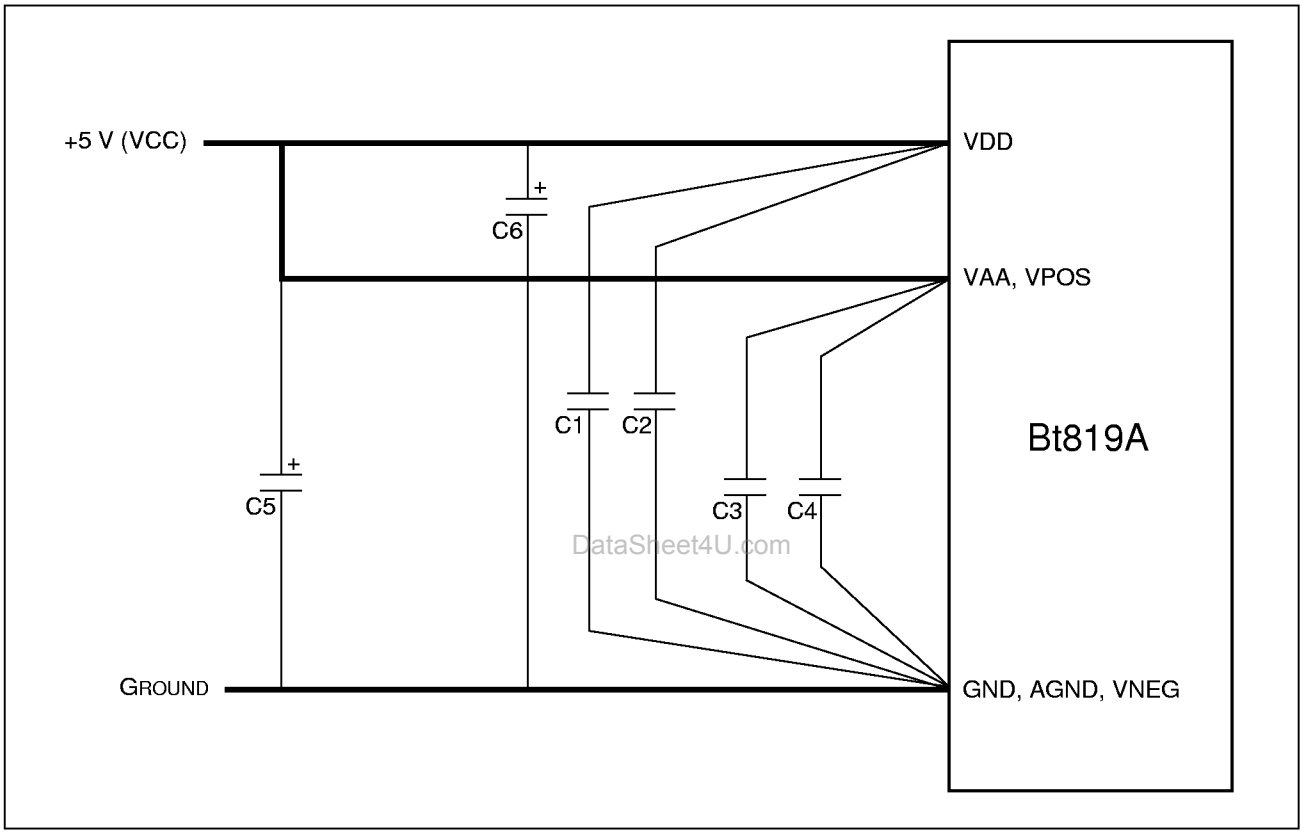
- Apply power to the device before or at the same time as the interface circuitry.
- Do not apply voltages below GND–0.5 V, or higher than VAA+0.5 V to any pin on the device. Do not use negative supply op-amps or any other negative voltage interface circuitry. All logic inputs should be held low until power to the device has settled to the specified tolerance.
- Connect all VDD, VAA and VPOS pins together through a low impedance plane.
- Connect all GND, AGND and VNEG pins together through a low impedance plane.

Figure 34. Optional Regulator Circuitry



Schematics

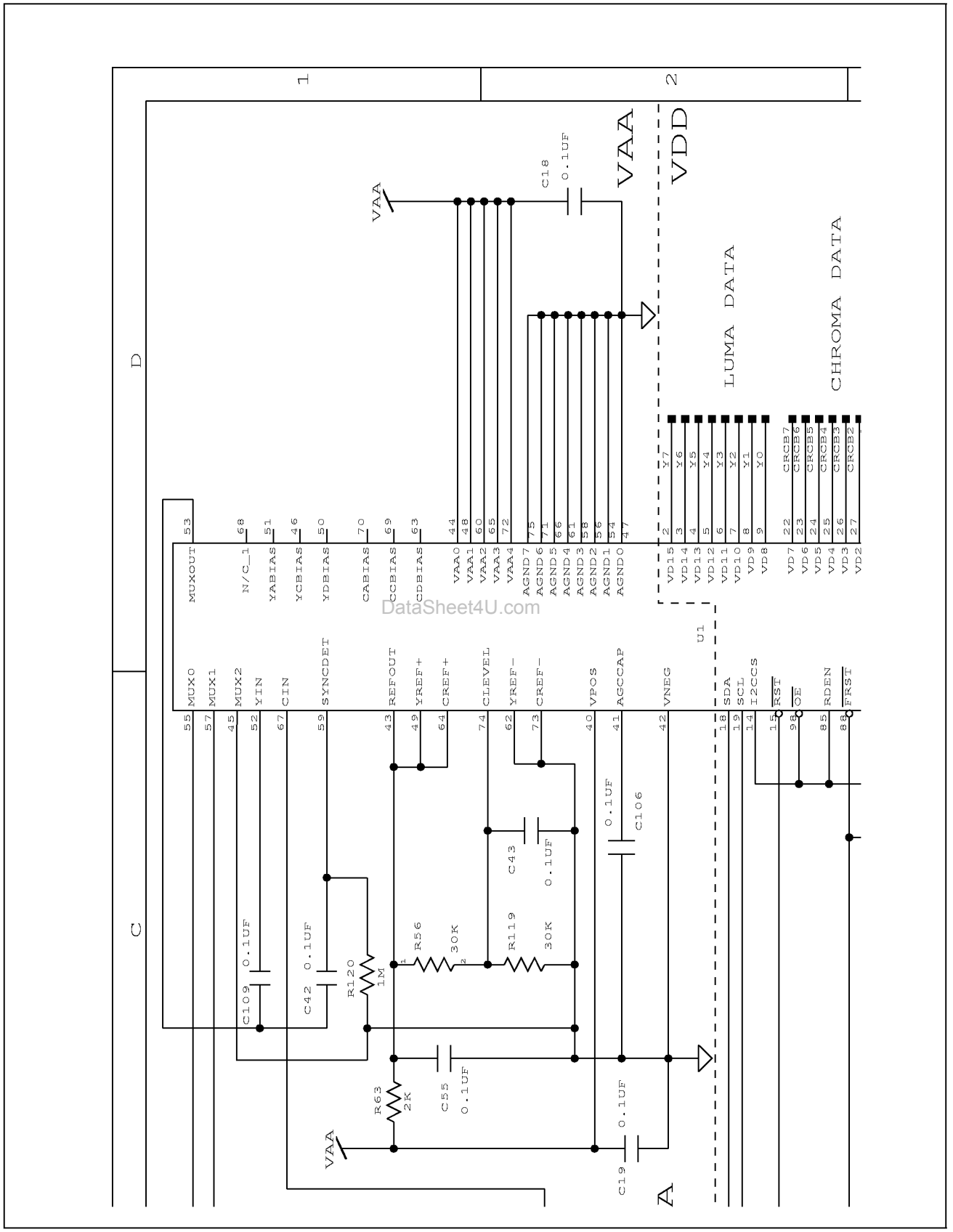
Figure 35. Typical Power and Ground Connection Diagram and Parts List



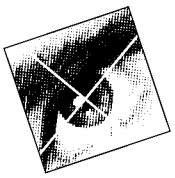
Location	Description	Vendor Part Number
C1, C2, C3, C4(1)	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V(3)
C5, C6(2)	10 µF tantalum capacitor	Mallory CSR13G106KM(3)

Notes: (1). A 0.1 µF capacitor should be connected between each group of power pins and ground as close to the device as possible, (ceramic chip capacitors are preferred).
(2). The 10 µF capacitors should be connected between the analog supply and the analog ground, as well as the digital supply and the digital ground. These should be connected as close to the Bt819A as possible.
(3). These vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt819A.

Figure 36. Example Schematic



Insert a blank page here. This is page 66



CONTROL REGISTER DEFINITIONS

The following tables describe the function of the various control registers. The section begins with a summary of the register functions and follows with details of each register.

Register Name	Mnemonic	Register Address	640 x 480 Square Pixel NTSC (Default)	768 x 576 Square Pixel PAL	720 x 480 CCIR NTSC	720 x 576 CCIR PAL	360 x 240 2:1 CCIR NTSC (Single Field, CIF)	360 x 288 2:1 CCIR PAL (Single Field, CIF)
Device Status	STATUS	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Input Format	IFORM	0x01	0x58	0x78	0x58	0x78	0x58	0x78
Temporal Decimation	TDEC	0x02	0x00	0x00	0x00	0x00	0x00	0x00
MSB Cropping	CROP	0x03	0x12	0x23	0x12	0x22	0x11	0x21
Vertical Delay, Lower Byte	VDELAY_LO	0x04	0x16	0x16	0x16	0x16	0x16	0x16
Vertical Active, Lower Byte	VACTIVE_LO	0x05	0xE0	0x40	0xE0	0x40	0xE0	0x40
Horizontal Delay, Lower Byte	HDELAY_LO	0x06	0x78	0x9A	0x80	0x90	0x38	0x48
Horizontal Active, Lower Byte	HACTIVE_LO	0x07	0x80	0x00	0xD0	0xD0	0x40	0x0C
Horizontal Scaling, Upper Byte	HSCALE_HI	0x08	0x02	0x03	0x00	0x05	0x11	0x1A
Horizontal Scaling, Lower Byte	HSCALE_LO	0x09	0xAA	0x3C	0xF8	0x04	0xF0	0x09
Brightness Control	BRIGHT	0x0A	0x00	0x00	0x00	0x00	0x00	0x00
Miscellaneous Control	CONTROL	0x0B	0x20	0x20	0x20	0x20	0x20	0x20
Luma Gain, Lower Byte (Contrast)	CONTRAST_LO	0x0C	0xD8	0xD8	0xD8	0xD8	0xD8	0xD8
Chroma (U) Gain, Lower Byte (Saturation)	SAT_U_LO	0x0D	0xFE	0xFE	0xFE	0xFE	0xFE	0xFE
Chroma (V) Gain, Upper Byte (Saturation)	SAT_V_LO	0x0E	0xB4	0xB4	0xB4	0xB4	0xB4	0xB4
Hue Control	HUE	0x0F	0x00	0x00	0x00	0x00	0x00	0x00
Reserved		0x10	0x00	0x00	0x00	0x00	0x00	0x00
Reserved		0x11	0x00	0x00	0x00	0x00	0x00	0x00

Register Name	Mnemonic	Register Address	640 x 480 Square Pixel NTSC (Default)	768 x 576 Square Pixel PAL	720 x 480 CCIR NTSC	720 x 576 CCIR PAL	360 x 240 2:1 CCIR NTSC (Single Field, CIF)	360 x 288 2:1 CCIR PAL (Single Field, CIF)
Output Format	OFORM	0x12	0x06	0x06	0x06	0x06	0x06	0x06
Vertical Scaling, Upper Byte	VSCALE_HI	0x13	0x60	0x60	0x60	0x60	0x60	0x60
Vertical Scaling, Lower Byte	VSCALE_LO	0x14	0x00	0x00	0x00	0x00	0x00	0x00
Test Control	TEST	0x15	0x00	0x00	0x00	0x00	0x00	0x00
Video Timing Polarity Register	VPOLE	0x16	0x00	0x00	0x00	0x00	0x00	0x00
ID Code	IDCODE	0x17	0x70	0x70	0x70	0x70	0x70	0x70
AGC Delay	ADELAY	0x18	0x68	0x7F	0x68	0x7F	0x68	0x7F
Burst Gate Delay	BDELAY	0x19	0x5D	0x72	0x5D	0x72	0x5D	0x72
ADC Interface	ADC	0x1A	0x82	0x82	0x82	0x82	0x82	0x82
Reserved	—	0x1B-0x1E	—	—	—	—	—	—
Software Reset	SRESET	0x1F	—	—	—	—	—	—

0x00 — Device Status Register (STATUS)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x00. COF is the least significant bit. An asterisk indicates the default option. The COF and LOF status bits hold their values until reset to their default values by writing to them. The other six bits do not hold their values, but continually output the status.

7	6	5	4	3	2	1	0
PRES	HLOC	FIELD	NUML	CSEL	Reserved	LOF	COF
0	0	0	0	0	0	0	0

PRES Video Present Status. Video is determined as present when an input signal is determined to have a signal above one half the sync height for 31 consecutive clock cycles. In the presence of video, this bit is set to a logical one. It can be reset to zero by writing a logical zero to this bit. Due to the nature of the AGC circuitry, it is possible that noise could induce this bit to be set. Therefore, it can not be used for precise determination of the presence of a video source.

0* = Video not present
1 = Video present

HLOC Device in H-lock. If HSYNC is found within ±1 clock cycle of the expected position of HSYNC for 32 consecutive lines, this bit is set to a logical 1. Once set, if HSYNC is not found within ±1 clock cycle of the expected position of HSYNC for 32 consecutive lines, this bit is set to a logical 0. MPU writes to this bit are ignored. This bit indicates the stability of the incoming video. While it is an indicator of horizontal locking, some video sources will characteristically vary from line to line by more than one clock cycle so that this bit will never be set. Consumer VCR's are examples of sources that will tend to never set this bit.

0* = Device not in H-lock
1 = Device in H-lock

FIELD Field Status. This bit reflects whether an odd or even field is being decoded. The FIELD bit is determined by the relationship between $\overline{\text{HRESET}}$ and $\overline{\text{VRESET}}$.

0* = Odd field
1 = Even field

NUML Number of Lines. This bit identifies the number of lines found in the video stream. This bit is used to determine the type of video input to the Bt819A. Thirty-two consecutive fields with the same number of lines is required before this status bit will change.

0* = 525 line format (NTSC)
1 = 625 line format (PAL)

CSEL Crystal Select. This bit identifies which crystal port is selected. When automatic format detection is enabled, this bit will be the same as NUML.

0* = XTAL0 input selected
1 = XTAL1 input selected

Reserved This bit should only be written with a logical zero.

LOF Luma ADC Overflow. On power-up, this bit is set to 0. If an ADC overflow occurs, the bit is set to a logical 1. It is reset after being written to or a chip reset occurs. If an overflow occurs in the luma ADC, the clamp level used for AGC may be adjusted by programming the CLAMP bits in the ADC register (0x1A). This is beneficial if the amplitude of the video signal is not accurate with respect to the sync height. The state of this bit is not valid and should be ignored when the ADC is in power-down mode (Y_SLEEP = 1). When the luma A/D is in sleep mode, LOF is set to 1.

COF Chroma ADC Overflow. On power-up, this bit is set to 0. If an ADC overflow occurs, the bit is set to a logical 1. It is reset after being written to or a chip reset occurs. The state of this bit is not valid and should be ignored when the ADC is in power-down mode (C_SLEEP = 1). When the chroma A/D is in sleep mode, COF is set to 1. Reads from this bit are insignificant on the Bt815A.

0x01 — Input Format Register (IFORM)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x58. FORMAT(0) is the least significant bit. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
HACTIVE	MUXSEL		XTSEL		Reserved	FORMAT	
0	1	0	1	1	0	0	0

HACTIVE When using the Bt819A with a packed memory architecture, for example, with field memories, this bit should be programmed with a logical 1. When implementing a VRAM based architecture, program with a logical 0.

0* = Reset HACTIVE with HRESET
1 = Extend HACTIVE beyond HRESET

MUXSEL Used for software control of video input selection. The Bt819A can select between two composite video sources, or one composite and one S-video source.

00 = Reserved
01 = Select MUX2 input to MUXOUT
10* = Select MUX0 input to MUXOUT
11 = Select MUX1 input to MUXOUT

XTSEL If automatic format detection is required, logical 11 must be loaded. Logical 01 and 10 are used if software format selection is desired.

00 = Reserved
01 = Select XT0 input (only XT0 present)
10 = Select XT1 input (both XTs present)
11* = Auto XT select enabled (both XTs present)

Reserved This bit should only be written with a logical zero.

FORMAT Automatic format detection may be enabled or disabled. The NUML bit is used to determine the input format when automatic format detection is enabled.

00* = Auto format detect enabled
01 = NTSC (M) input format
10 = Reserved
11 = PAL (B, D, G, H, I) input format

0x02 — Temporal Decimation Register (TDEC)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x00. DEC_RAT(0) is the least significant bit. An asterisk indicates the default option. This register enables temporal decimation by discarding a finite number of fields or frames from the incoming video.

7	6	5	4	3	2	1	0
DEC_FIELD	DEC_RAT						
0	0	0	0	0	0	0	0

DEC_FIELD Defines whether decimation is by fields or frames.

0* = Decimate frames
1 = Decimate fields

DEC_RAT DEC_RAT is the number of fields or frames dropped out of 60 (NTSC) or 50 (PAL) fields or frames. 0x00 value disables decimation (all video frames and fields are output).

Caution: When changing the programming in the TDEC register, 0x00 must be loaded first and then the decimation value. This will ensure decimation does not start on the wrong field or frame. The register should not be loaded with greater than 60 (0x3C) for NTSC, or 50 (0x34) for PAL.

0x00–0xFF = Number of fields / frames output.

0x03 — MSB Cropping Register (CROP)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x12. HACTIVE_MSB(0) is the least significant bit. See the VACTIVE, VDELAY, HACTIVE and HDELAY registers for descriptions on the operation of this register.

7	6	5	4	3	2	1	0
VDELAY_MSB		VACTIVE_MSB		HDELAY_MSB		HACTIVE_MSB	
0	0	0	1	0	0	1	0

VDELAY_MSB 00xx xxxx–11xx xxxx = The most significant two bits of vertical delay register

VACTIVE_MSB xx00 xxxx–xx11 xxxx = The most significant two bits of vertical active register

HDELAY_MSB xxxx 00xx–xxxx 11xx = The most significant two bits of horizontal delay register

HACTIVE_MSB xxxx xx00–xxxx xx11 = The most significant two bits of horizontal active register

0x04 — Vertical Delay Register, Lower Byte (VDELAY_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x16. VDELAY_LO(0) is the least significant bit. This 8-bit register is the lower byte of the 10-bit VDELAY register. The two MSB's of VDELAY are contained in the CROP register. VDELAY defines the number of half lines between the trailing edge of VRESET and the start of active video.

7	6	5	4	3	2	1	0
VDELAY_LO							
0	0	0	1	0	1	1	0

VDELAY_LO 0x01–0xFF = The least significant byte of the vertical delay register.

0x05 — Vertical Active Register, Lower Byte (VACTIVE_LO)

This control register may be written to or read by the MPU at any time, and upon reset it is initialized to 0xE0. VACTIVE_LO(0) is the least significant bit. This 8-bit register is the lower byte of the 10-bit VACTIVE register. The two MSB's of VACTIVE are contained in the CROP register. VACTIVE defines the number of lines used in the vertical scaling process. The actual number of lines output by the Bt819A is SCALING_RATIO * VACTIVE.

7	6	5	4	3	2	1	0
VACTIVE_LO							
1	1	1	0	0	0	0	0

VACTIVE_LO 0x00–0xFF = The least significant byte of the vertical active register.

0x06 — Horizontal Delay Register, Lower Byte (HDELAY_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x78. HDELAY_LO(0) is the least significant bit. This 8-bit register is the lower byte of the 10-bit HDELAY register. The two MSB's of HDELAY are contained in the CROP register. HDELAY defines the number of scaled pixels between the falling edge of HRESET and the start of active video.

7	6	5	4	3	2	1	0
HDELAY_LO							
0	1	1	1	1	0	0	0

HDELAY_LO 0x01–0xFF = The least significant byte of the horizontal delay register. HACTIVE pixels will be output by the chip starting at the fall of HRESET.

Caution: HDELAY must be programmed with an even number.

0x07 — Horizontal Active Register, Lower Byte (HACTIVE_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x80. HACTIVE_LO(0) is the least significant bit. HACTIVE defines the number of horizontal active pixels per line output by the Bt819A.

7	6	5	4	3	2	1	0
HACTIVE_LO							
1	0	0	0	0	0	0	0

HACTIVE_LO 0x00–0xFF = The least significant byte of the horizontal active register. This 8-bit register is the lower byte of the 10-bit HACTIVE register. The two MSB's of HACTIVE are contained in the CROP register.

0x08 — Horizontal Scaling Register, Upper Byte (HSCALE_HI)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x02. This 8-bit register is the upper byte of the 16-bit HSCALE register.

7	6	5	4	3	2	1	0
HSCALE_HI							
0	0	0	0	0	0	1	0

HSCALE_HI 0x00–0xFF = The most significant byte of the horizontal scaling ratio

0x09 — Horizontal Scaling Register, Lower Byte (HSCALE_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0xAC. This 8-bit register is the lower byte of the 16-bit HSCALE register.

7	6	5	4	3	2	1	0
HSCALE_LO							
1	0	1	0	1	1	0	0

HSCALE_LO 0x00–0xFF = The least significant byte of the horizontal scaling ratio

0x0A — Brightness Control Register (BRIGHT)

The brightness control involves the addition of a two's complement number to the luma channel. Brightness can be adjusted in 255 steps, from –128 to +127. The resolution of brightness change is one LSB (0.39% with respect to the full luma range).

7	6	5	4	3	2	1	0
BRIGHT							
0	0	0	0	0	0	0	0

BRIGHT

Hex Value	Binary Value	Brightness Changed By	
		Number of LSBs	Percent of Full Scale
0x80	1000 0000	–128	–50%
0x81	1000 0001	–127	–49.6%
. .	. .	. .	
0xFF	1111 1111	–01	–0.39%
0x00*	0000 0000*	00	0%
0x01	0000 0001	+01	+0.39%
. .	. .	. .	
0x7E	0111 1110	+126	+49.2%
0x7F	0111 1111	+127	+49.6%

0x0B — Miscellaneous Control Register (CONTROL)

This control register may be written to or read by the MPU at any time, and upon reset it is initialized to 0x20. SAT_V_MSB is the least significant bit.

7	6	5	4	3	2	1	0
LNOTCH	COMP**	LDEC	CBSENSE	INTERP	CON_MSB	SAT_U_MSB	SAT_V_MSB
0	0	1	0	0	0	0	0

LNOTCH This bit is used to include the luma notch filter. For monochrome video, the notch should not be used. This will output full bandwidth luminance.

0* = Enable the luma notch filter
1 = Disable the luma notch filter

COMP When COMP is set to logical one, the luma notch is disabled. When COMP is set to logical zero, the C ADC is disabled. When using the Bt815A, this bit *must* be programmed with a zero.

** Bt819A and Bt817A only.

0* = Composite Video
1 = Y/C Component Video

LDEC The luma decimation filter is used to reduce the high-frequency component of the luma signal. Useful when scaling to CIF resolutions or lower.

0 = Enable luma decimation
1* = Disable luma decimation

CBSENSE This bit controls whether the first pixel of a line is a Cb pixel or a Cr pixel. For example, if CBSENSE is low and HDELAY is an even number, the first active pixel output is a Cb pixel. If HDELAY is odd, CBSENSE may be programmed high to produce a Cb pixel as the first active pixel output.

0* = Normal CbFLAG (high for the 1st pixel of line)
1 = Invert the CbFLAG polarity

INTERP This is primarily a test mode. The interpolator should always be enabled.

0* = Enable interpolation
1 = Disable interpolation

CON_MSB The most significant bit of the luma gain (contrast) value

SAT_U_MSB The most significant bit of the chroma (u) gain value

SAT_V_MSB The most significant bit of the chroma (v) gain value

0x0C — Luma Gain Register, Lower Byte (CONTRAST_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0xD8. CONTRAST_LO(0) is the least significant bit. The CON_L_MSB bit and the CONTRAST_LO register concatenate to form the 9-bit CONTRAST register. The value in this register is multiplied by the luminance value to provide contrast adjustment.

7	6	5	4	3	2	1	0
CONTRAST_LO							
1	1	0	1	1	0	0	0

CONTRAST_LO The least significant byte of the luma gain (contrast) value.

Decimal Value	Hex Value	% of Original Signal
511	0x1FF	236.57%
510	0x1FE	236.13%
. .	. .	. .
217	0x0D9	100.46%
216	0x0D8*	100.00%
. .	. .	. .
128	0x080	59.26%
. .	. .	. .
1	0x001	0.46%
0	0x000	0.00%

0x0D — Chroma (U) Gain Register, Lower Byte (SAT_U_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0xFE. SAT_U_LO(0) is the least significant bit. SAT_U_MSB in the CONTROL register, and SAT_U_LO concatenate to give a 9-bit register (SAT_U). This register is used to add a gain adjustment to the U component of the video signal. By adjusting the U and V color components of the video stream by the same amount, the saturation is adjusted. For normal saturation adjustment, the gain in both the color difference paths must be the same (i.e. the ratio between the value in the U gain register and the value in the V gain register should be kept constant at the default power-up ratio). When changing the saturation, if the SAT_U_MSB bit is altered, care must be taken to ensure that the other bits in the CONTROL register are not affected.

7	6	5	4	3	2	1	0
SAT_U_LO							
1	1	1	1	1	1	1	0

SAT_U_LO

Decimal Value	Hex Value	% of Original Signal
511	0x1FF	201.18%
510	0x1FE	200.79%
. .	. .	. .
255	0x0FF	100.39%
254	0x0FE*	100.00%
. .	. .	. .
128	0x080	50.39%
. .	. .	. .
1	0x001	0.39%
0	0x000	0.00%

0x0E — Chroma (V) Gain Register, Lower Byte (SAT_V_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0xB4. SAT_V_LO(0) is the least significant bit. SAT_V_MSB in the CONTROL register and SAT_V_LO concatenate to give a 9-bit register (SAT_V). This register is used to add a gain adjustment to the V component of the video signal. By adjusting the U and V color components of the video stream by the same amount, the saturation is adjusted. For normal saturation adjustment, the gain in both the color difference paths must be the same (i.e. the ratio between the value in the U gain register and the value in the V gain register should be kept constant at the default power-up ratio). When changing the saturation, if the SAT_V_MSB bit is altered, care must be taken to ensure that the other bits in the CONTROL register are not affected.

7	6	5	4	3	2	1	0
SAT_V_LO							
1	0	1	1	0	1	0	0

SAT_V_LO

Decimal Value	Hex Value	% of Original Signal
511	0x1FF	283.89%
510	0x1FE	283.33%
. .	.	. .
181	0x0B5	100.56%
180	0x0B4*	100.00%
. .	.	. .
128	0x080	71.11%
. .	.	. .
1	0x001	0.56%
0	0x000	0.00%

0x0F — Hue Control Register (HUE)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x00. HUE(0) is the least significant bit. An asterisk indicates the default option. Hue adjustment involves the addition of a two's complement number to the demodulating subcarrier phase. Hue can be adjusted in 256 steps in the range –90° to +89.3°, in increments of 0.7°.

7	6	5	4	3	2	1	0
HUE							
0	0	0	0	0	0	0	0

HUE

Hex Value	Binary Value	Subcarrier Reference Changed By	Resulting Hue Changed By
0x80	1000 0000	–90°	+90°
0x81	1000 0001	–89.3°	+89.3°
. .	. .	. .	. .
0xFF	1111 1111	–0.7°	+0.7°
0x00*	0000 0000*	00°	00°
0x01	0000 0001	+0.7°	–0.7°
. .	. .	. .	. .
0x7E	0111 1110	+88.6°	–88.6°
0x7F	0111 1111	+89.3°	–89.3°

0x10 — Reserved

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x00, and must only be written to with 0x00.

0x11 — Reserved

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x00, and must only be written to with 0x00.

0x12 — Output Format Register (OFORM)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x06. FULL is the least significant bit. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
RANGE	RND		FIFO_BURST**	CODE	LEN	SPI**	FULL
0	0	0	0	0	1	1	0

RANGE Luma Output Range: This bit determines the range for the luminance output on the Bt819A. The range must be limited when using the control codes as video timing.

0* = Normal operation (Luma range 16–253, chroma range 2–253).
Y=16 is black (pedestal).
Cr, Cb=128 is zero color information.

1 = Full-range Output (Luma range 0–255, chroma range 2–253)
Y=0 is black (pedestal).
Cr, Cb=128 is zero color information.

RND Output Rounding: These bits control the number of bits output from the Bt819A, MSB justified. When rounding is implemented, the unused LSBs are set to zero.

00* = Normal Operation
01 = 6-bit Luma & 4-bit Chroma Output (Rounded)
10 = 7-bit Luma & 5-bit Chroma Output (Rounded)
11 = Reserved

FIFO_BURST FIFO Read Control: When enabled, this pin internally connects RDEN to DVALID. In API mode, when these pins are connected, the data is automatically burst out of the FIFO. If these pins are not connected, the system must control reads from the FIFO, and ensure the data does not overflow. Reads and writes to this bit are ignored on the Bt817A and Bt815A.

** Applies only to Bt819A.

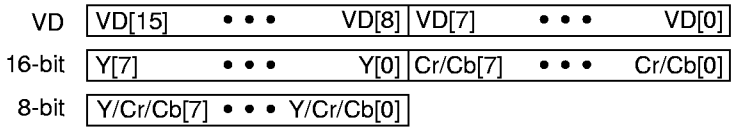
0* = Internally Feedback DVALID to RDEN
1 = Control RDEN externally

CODE Code Control Disable: This bit determines if control codes are output with the video data. SPI mode 2 requires this bit to be programmed with a logical 1. When control codes are inserted into the data stream, the external control signals are still available.

0* = Disable control code insertion
1 = Enable control code insertion

LEN Eight or Sixteen Bit Format: This bit determines the output data format. In 8-bit mode, the data is output on VD[15:8].

0 = 8-bit YCrCb 4:2:2 output stream
1* = 16-Bit YCrCb 4:2:2 output stream



SPI Pixel Interface Control: When programmed with a logical zero, the data is output using the FIFO in API mode. When programmed with a logical one, the FIFO is bypassed and the data is output in SPI mode. On the Bt817A and Bt815A, this bit must be loaded with a logical one.

** Applies only to Bt819A.

0 = Asynchronous pixel interface
1* = Synchronous pixel interface

FULL This bit controls the point at which the FIFO full flag toggles. When programmed with a logical zero, the FIFO signals that it is half full by setting AFF high at 20 pixels (out of a possible 40). When programmed with a logical one, AFF toggles high at 32 pixels indicating that the FIFO is approaching full. Writes and reads to this pin are ignored on the Bt817A and Bt815A.

0* = AFF and DVALID go high when there are at least 20 pixels in the output FIFO.
1 = AFF and DVALID go high when there are at least 32 pixels in the output FIFO.

0x13 — Vertical Scaling Register, Upper Byte (VSCALE_HI)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x60.

7	6	5	4	3	2	1	0
LINE**	COMB	INT	VSCALE_HI				
0	1	1	0	0	0	0	0

LINE Line Store Enable: This bit enables operation of the line store for use in vertical scaling. When enabled, the luminance component of the video signal is scaled using two-tap, poly-phase scaling. When disabled, simple line dropping is implemented. Reads and writes to this bit are ignored on the Bt817A and Bt815A.
** Applies to Bt819A only.

0* = Luma VS using Line Store
1 = Luma VS using DDA

COMB Chroma Comb Enable: This bit determines if the chroma comb is included in the data path. If enabled, a full line store is used to average adjacent lines of color information, reducing cross-color artifacts. The chroma comb is available on all three parts (Bt819A, Bt817A and Bt815A).

0 = Chroma comb disabled
1* = Chroma comb enabled

INT Interlace: This bit is programmed to indicate if the incoming video is interlaced or non-interlaced. For example, if using the full frame as input for vertical scaling, this bit should be programmed high. If using a single field for vertical scaling, this bit should be programmed low. Single field scaling is normally used when scaling below CIF resolution and outputting to a non-interlaced monitor. Using a single field will reduce motion artifacts.

0 = Non-interlace VS
1* = Interlace VS

VSCALE_HI Vertical Scaling Ratio: These five bits represent the most significant portion of the 13-bit vertical scaling ratio register. The system must take care not to alter the contents of the LINE, COMB and INT bits while adjusting the scaling ratio.

0x14 — Vertical Scaling Register, Lower Byte (VSCALE_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x00.

7	6	5	4	3	2	1	0
VSCALE_LO							
0	0	0	0	0	0	0	0

VSCALE_LO Vertical Scaling Ratio: These eight bits represent the least significant byte of the 13-bit vertical scaling ratio register. They are concatenated with five bits in VSCALE_HI. The following equation should be used to determine the value for this register:

$$VSCALE = (0x10000 - \{ [(scaling\_ratio) - 1] * 512 \}) \& 0x1FFF$$

For example, to scale PAL input to square pixel QCIF, the total number of vertical lines is 156:

$$VSCALE = (0x10000 - \{ [(4/1) - 1] * 512 \}) \& 0x1FFF$$
$$= 0x1A00$$

0x15 — Test Control Register (TEST)

This control register is reserved for putting the part into test mode. Write operation to this register may cause undetermined behavior and should not be attempted. A read cycle from this register returns 0x01, and only a write of 0x01 is permitted.

0x16 — Video Timing Polarity Register (VPOLE)

This control register may be written to or read by the MPU at any time. Upon reset, it is initialized to 0x00.

7	6	5	4	3	2	1	0
OUT_EN	DVALID	AFF**	CBFLAG	FIELD	ACTIVE	HRESET	VRESET
0	0	0	0	0	0	0	0

OUTEN Three-states the following pins: VD[15:0], $\overline{\text{HRESET}}$, $\overline{\text{VRESET}}$, ACTIVE, DVALID, CBFLAG, FIELD, AEF, AFF, QCLK, CLKx1, and CLKx2.

0* = Enable Outputs
1 = Three-stated outputs

DVALID

0* = DVALID Pin: Active high
1 = DVALID Pin: Active low

AFF ** This bit applies only to the Bt819A. Reads and writes to this bit are ignored on the Bt817A and Bt815A.

0* = AFF Pin: Active high
1 = AFF Pin: Active low

CBFLAG

0* = CBFLAG Pin: Active high
1 = CBFLAG Pin: Active low

FIELD

0* = FIELD Pin: High indicates odd field
1 = FIELD Pin: High indicates even field

ACTIVE

0* = ACTIVE Pin: Active high
1 = ACTIVE Pin: Active low

HRESET

0* = $\overline{\text{HRESET}}$ Pin: Active low
1 = $\overline{\text{HRESET}}$ Pin: Active high

VRESET

0* = $\overline{\text{VRESET}}$ Pin: Active low
1 = $\overline{\text{VRESET}}$ Pin: Active high

Note: In API mode, the FIELD, VALID and AFF pins do not have programmable polarities. They are programmable only in SPI mode.

0x17 — ID Code Register (IDCODE)

This control register may be read by the MPU at any time. IDCODE(0) is the least significant bit.

7	6	5	4	3	2	1	0
PART_ID				PART_REV			
0	1	1	1	0	0	0	0

PART_ID

0111 Bt819A Part ID Code
0110 Bt817A Part ID Code
0010 Bt815A Part ID Code

PART_REV 0x0 – 0xF = Current Revision ID Code

0x18 — AGC Delay Register (ADELAY)

This control register may be written to or read by the MPU at any time. Upon reset, it is initialized to 0x68.

7	6	5	4	3	2	1	0
ADELAY							
0	1	1	0	1	0	0	0

ADELAY AGC gate delay for back-porch sampling. The following equation should be used to determine the value for this register:

$$ADELAY = (6.8\ \mu S * f_{CLKx1}) + 7$$

For example, for an NTSC input signal:

$$ADELAY = (6.8\ \mu S * 14.32\ MHz) + 7$$
$$= 104\ (0x68)$$

0x19 — Burst Delay Register (BDELAY)

This control register may be written to or read by the MPU at any time. Upon reset, it is initialized to 0x5D. BDELAY(0) is the least significant bit.

7	6	5	4	3	2	1	0
BDELAY							
0	1	0	1	1	1	0	1

BDELAY The burst gate delay for sub-carrier sampling. The following equation should be used to determine the value for this register:

$$BDELAY = (6.5\ \mu S * f_{CLKx1})$$

For example, for an NTSC input signal:

$$BDELAY = (6.5\ \mu S * 14.32\ MHz)$$
$$= 93\ (0x5D)$$

0x1A — ADC Interface Register (ADC)

This control register may be written to or read by the MPU at any time. Upon reset, it is initialized to 0x82. ADC(0) is the least significant bit.

7	6	5	4	3	2	1	0
CLAMP		SYNC_T	AGC_EN	CLK_SLEEP	Y_SLEEP	C_SLEEP**	Reserved
1	0	0	0	0	0	1	0

CLAMP
00 = Clamp on the Back Porch to 0x30
01 = Clamp on the Back Porch to 0x34
10* = Clamp on the Back Porch to 0x38
11 = Clamp on the Back Porch to 0x3C

SYNC_T
0* = Analog SYNCDET threshold high (~125 mV)
1 = Analog SYNCDET threshold low (~75 mV)

AGC_EN
0* = AGC Enabled
1 = AGC Disabled

CLK_SLEEP Output clocks are still running, I^2C registers are still accessible. Recovery time is approximately one second.
0* = Normal Clock Operation
1 = Shut down the System Clock (Power Down)

Y_SLEEP
0* = Normal Y ADC operation
1 = Sleep Y ADC operation

C_SLEEP ** Applies only to Bt819A and Bt817A. Reads and writes to this bit are ignored on Bt815A.
0 = Normal C ADC operation
1* = Sleep C ADC operation

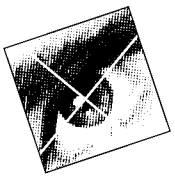
Reserved This bit should only be written with a logical zero.

0x1B to 0x1E — Reserved Registers

These control registers are reserved for future use. Write operations to these registers may cause undetermined behavior and should not be attempted. A read cycle from these registers returns an undefined value.

0x1F — Software Reset Register (SRESET)

This command register can be written at any time. Read cycles to this register return an undefined value. A data write cycle to this register resets the device to the default state (indicated in the command register definitions by an asterisk). Writing any data value into this address resets the device.



PARAMETRIC INFORMATION

DC Electrical Parameters

Table 14. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply — Analog	V_{AA}	4.75	5.00	5.25	V
Power Supply — Digital	V_{DD}	4.75	5.00	5.25	V
Maximum $\Delta \lvert V_{DD} - V_{AA} \rvert$				0.5	V
Mux0, Mux1 and Mux2Input Range (AC coupling required)		0.5	1.00	2.00	V
VIn Amplitude Range (AC coupling required)		0.5	1.00	2.00	V
Ambient Operating Temperature	T_A	0		+70	˚C

Table 15. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
V_{AA} (measured to AGND)				7.00	V
V_{DD} (measured to DGND)				7.00	V
Voltage on any signal pin (See the note below)		DGND – 0.5		V_{DD} + 0.5	V
Analog Input Voltage		AGND – 0.5		V_{AA} + 0.5	V
Storage Temperature	T_S	–65		+150	˚C
Junction Temperature	T_J			+125	˚C
Vapor Phase Soldering (15 Seconds)	T_{VSOL}			+220	˚C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V or drops below ground by more than 0.5 V can induce destructive latchup.

Table 16. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0		V_{DD} + 0.5	V
Input Low Voltage (TTL)	V_{IL}			0.8	V
Input High Voltage (XT0I, XT1I)	V_{IH}	3.5		V_{DD} + 0.5	V
Input Low Voltage (XT0I, XT1I)	V_{IL}	GND – 0.5		1.5	V
Input High Current (V_{In}=V_{DD})	I_{IH}			10	µA
Input Low Current (V_{IN}=GND)	I_{IL}			–10	µA
Input Capacitance (f=1 MHz, V_{IN}=2.4 V)	C_{IN}		5		pF
Digital Outputs					
Output High Voltage (I_{OH} = –400 µA)	V_{OH}	2.4		V_{DD}	V
Output Low Voltage (I_{OL}= 3.2 mA)	V_{OL}			0.4	V
3-State Current	I_{OZ}			10	µA
Output Capacitance	C_O		5		pF
Analog Pin Input Capacitance	C_A		5		pF

AC Electrical Parameters

Table 17. Clock Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
NTSC:					
CLKx1 Rate	F_{S1}		14.318181		MHz
CLKx2 Rate (50 PPM source required)	F_{S2}		28.636363		MHz
PAL:					
CLKx1 Rate	F_{S1}		17.734475		MHz
CLKx2 Rate (50 PPM source required)	F_{S2}		35.468950		MHz
XT0 and XT1 Inputs					
Cycle Time	1	28.2			ns
High Time	2	12			ns
Low Time	3	12			ns
CLKx1 Duty Cycle		45		55	%
CLKx2 Duty Cycle		40		60	%
CLKx2 to CLKx1 Delay	4	1		8	ns
CLKx1 to Data Delay	5	5		20	ns
CLKx2 to Data Delay	6	8		20	ns
8-Bit mode:					
Data to QCLK (Rising Edge) Delay	7a	5			ns
QCLK (Rising Edge) to Data Delay	8a	15			ns
16-Bit Mode:					
Data to QCLK (Rising Edge) Delay	7b	15			ns
QCLK (Rising Edge) to Data Delay	8b	25			ns

Figure 37. Clock Timing Diagram

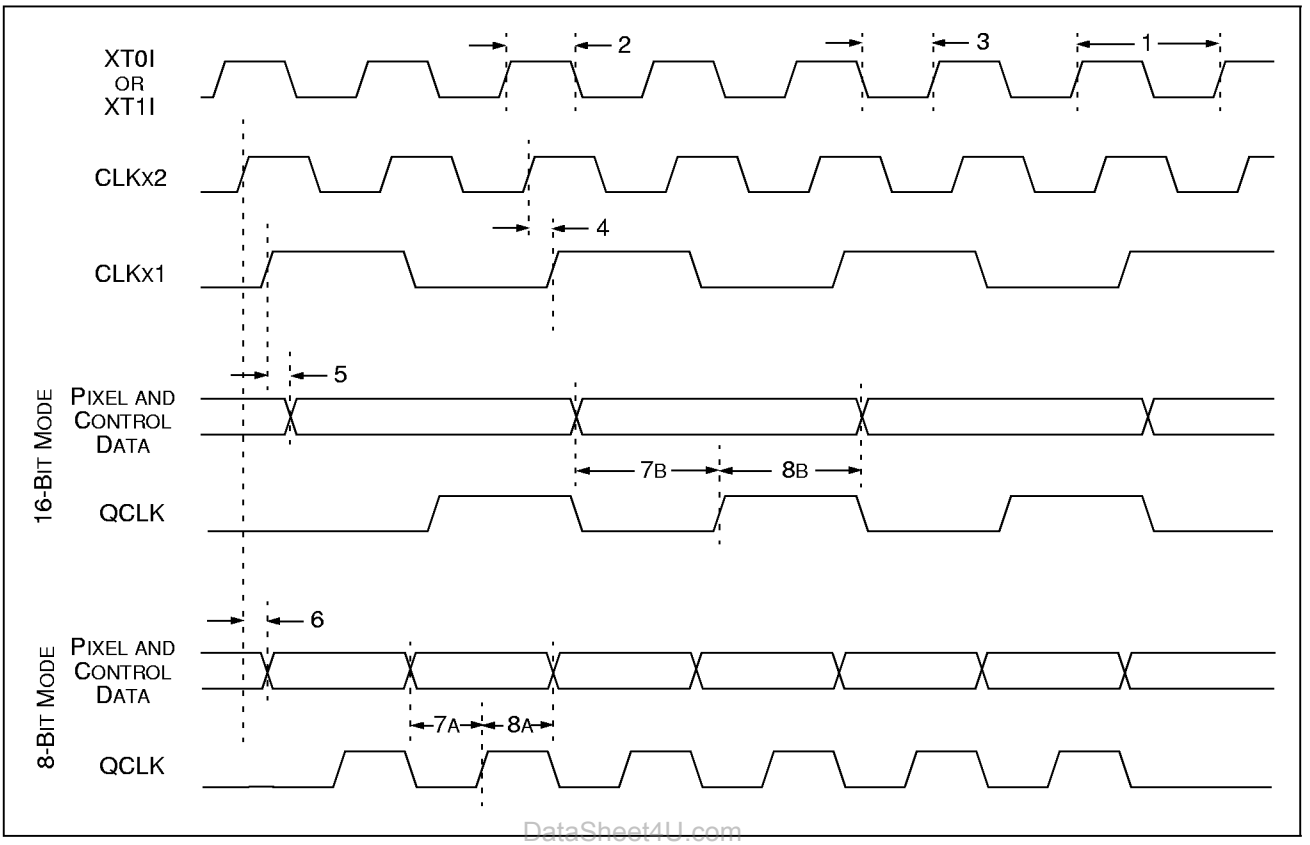


Table 18. Power Supply Current Parameters

Parameter	Symbol	Min	Typ	Max	Units
Supply Current (Bt819A and Bt817A)	I				
$V_{AA}=V_{DD}$=5.0V, F_{CLKx2}=28.64 MHz, T=25˚C			230		mA
$V_{AA}=V_{DD}$=5.25V, F_{CLKx2}=35.47 MHz, T=70˚C				310	mA
$V_{AA}=V_{DD}$=5.25V, F_{CLKx2}=35.47 MHz, T=0˚C				340	mA
Supply Current, Power Down			100		mA
Supply Current (Bt815A)	I				
$V_{AA}=V_{DD}$=5.0V, F_{CLKx2}=28.64 MHz, T=25˚C			230		mA
$V_{AA}=V_{DD}$=5.25V, F_{CLKx2}=35.47 MHz, T=70˚C				265	mA
$V_{AA}=V_{DD}$=5.25V, F_{CLKx2}=35.47 MHz, T=0˚C				285	mA
Supply Current, Power Down			100		mA

Table 19. Output Enable Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
$\overline{OE}$ Asserted to Data Bus Driven	9	0			nS
$\overline{OE}$ Asserted to Data Valid	10			100	nS
$\overline{OE}$ Negated to Data Bus Not Driven	11			100	nS
$\overline{RST}$ Low Time		8			XTAL cycles

Figure 38. Output Enable TIming Diagram

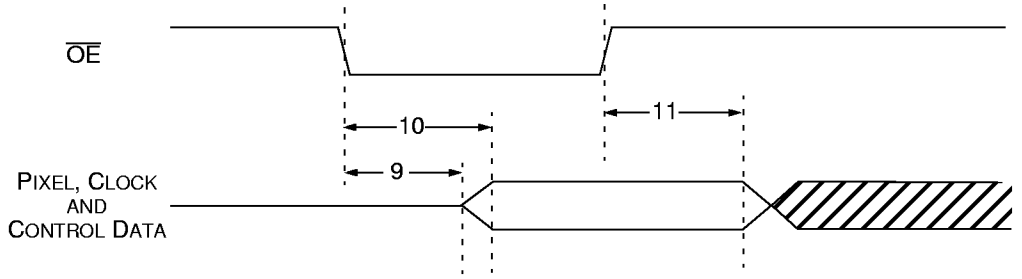


Table 20. JTAG Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
TMS, TDI Setup Time	12		10		ns
TMS, TDI Hold Time	13		10		ns
TCK Asserted to TDO Valid	14		60		ns
TCK Asserted to TDO Driven	15		5		ns
TCK Negated to TDO Three-stated	16		80		ns
TCK Low Time	17	25			ns
TCK High TIme	18	25			ns

Figure 39. JTAG TIming Diagram

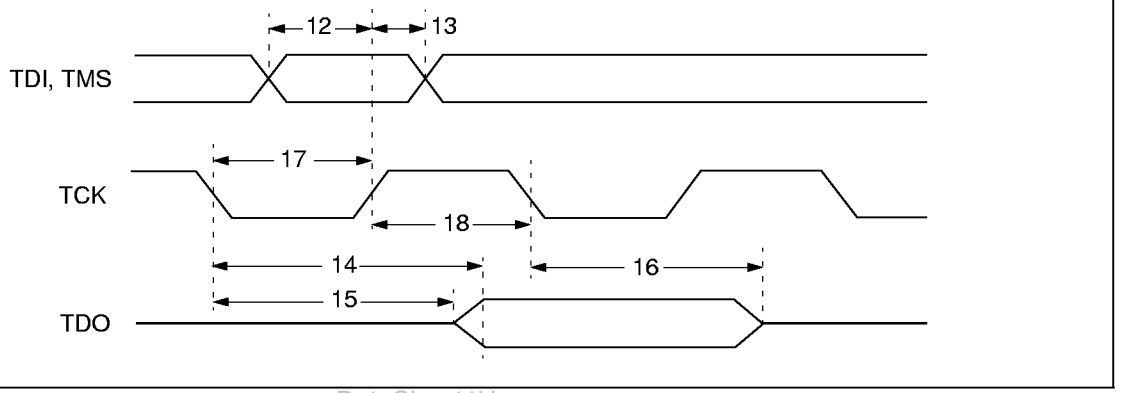


Table 21. FIFO Timing Parameters (Bt819A Only)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{\text{FRST}}$ Low Time		4			CLKx1 cycles
CLKIN Rate				36	MHz
CLKIN Duty Cycle	19	40		60	%
RDEN Setup Time	20	10			ns
RDEN Hold Time	21	5			ns
CLKIN to Data Delay (except DVALID)	22	5		20	ns
FIFO Data Retention Time		64			ms
Data to QCLK (Rising Edge) Delay	23	10			ns
QCLK (Rising Edge) to Data Delay	24	6			ns
CLKIN to DVALID Data Delay		5		22	ns

Figure 40. FIFO Output Timing Diagram

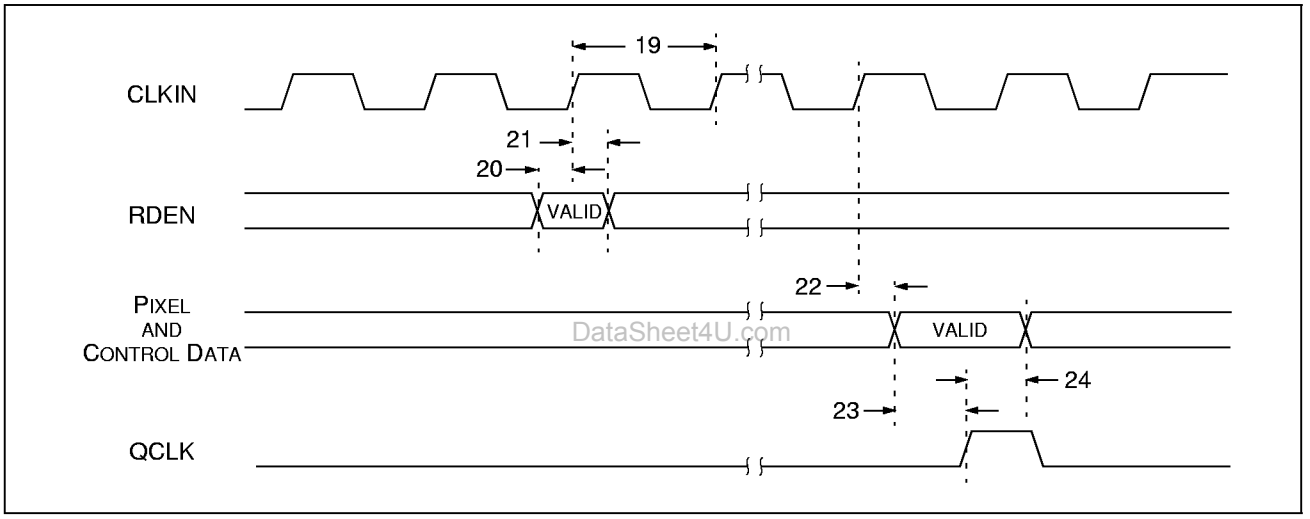


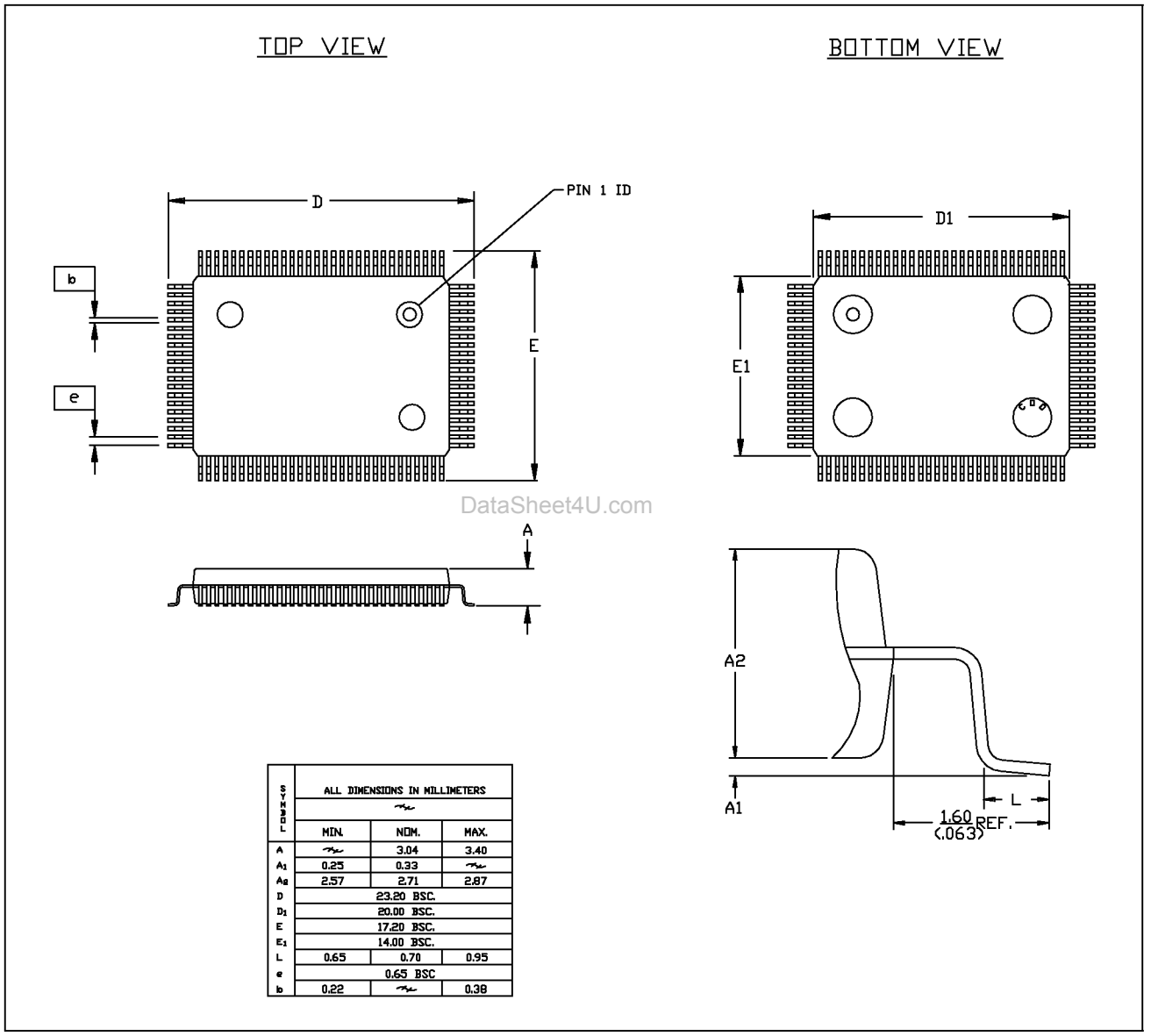
Table 22. Decoder Performance Parameters

Parameter	Symbol	Min	Typ	Max	Units
Horizontal Lock Range				±7	% of Line Length
Fsc, Lock-in Range		±800			Hz
Gain Range		–6		6	dB

Note: Test conditions (unless otherwise specified): "Recommended Operating Conditions." TTL input values are 0–3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for digital inputs and outputs. Pixel and control data loads ≤ 30 pF and ≥10 pF. CLKx1 and CLKx2 loads ≤ 50 pF. Control data includes CBFLAG, DVALID, ACTIVE, $\overline{\text{HRESET}}$, $\overline{\text{VRESET}}$ and FIELD

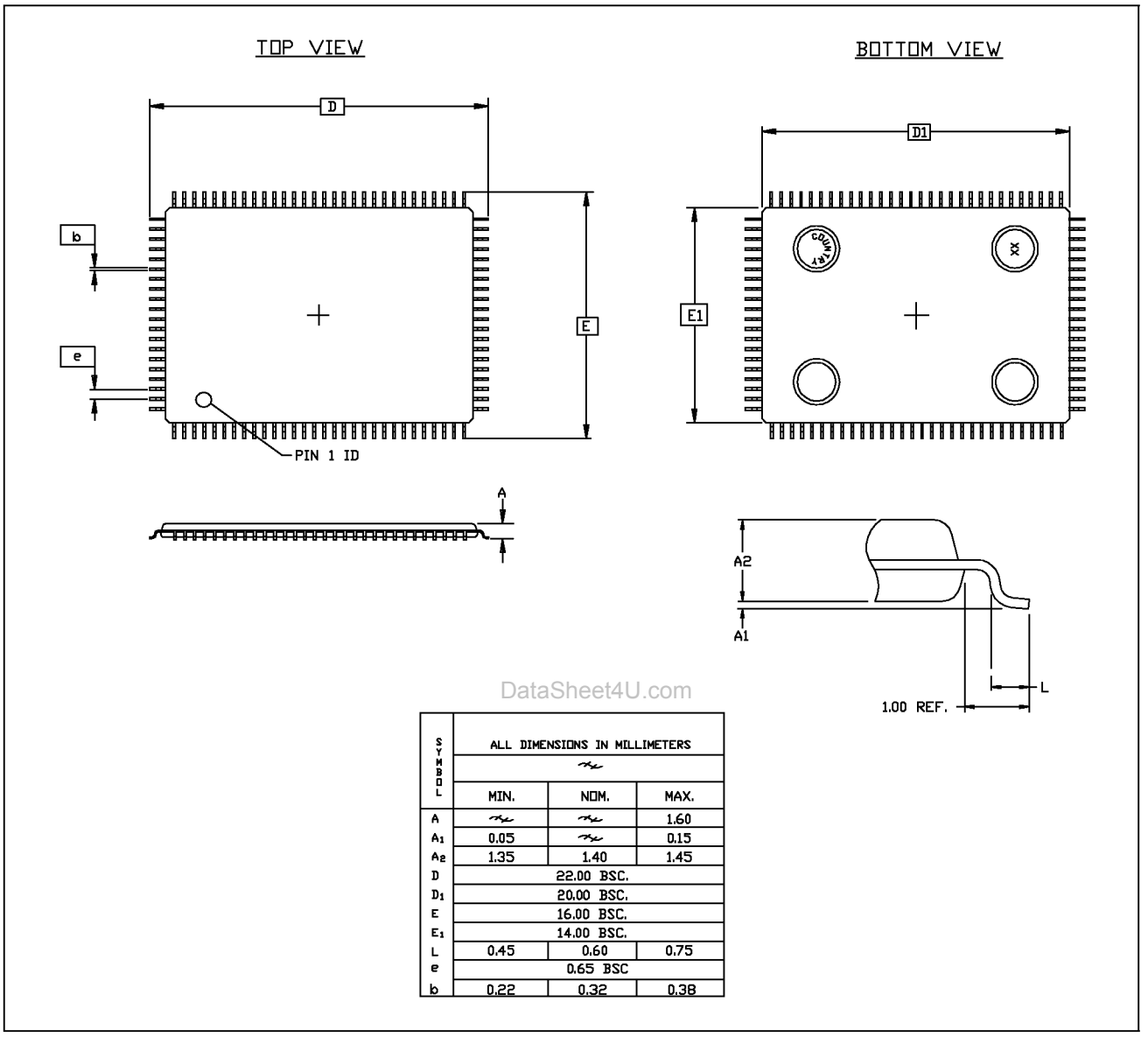
Package Mechanical Drawings

Figure 41. 100PQFP Package Mechanical Drawing



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A		3.04	3.40
A_1	0.25	0.33	
A_2	2.57	2.71	2.87
D		23.20 BSC.	
D_1		20.00 BSC.	
E		17.20 BSC.	
E_1		14.00 BSC.	
L	0.65	0.70	0.95
e		0.65 BSC	
b	0.22		0.38

Figure 42. 100TQFP Package Mechanical Drawing



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.60
A_1	0.05		0.15
A_2	1.35	1.40	1.45
D		22.00 BSC.	
D_1		20.00 BSC.	
E		16.00 BSC.	
E_1		14.00 BSC.	
L	0.45	0.60	0.75
e		0.65 BSC	
b	0.22	0.32	0.38

Datasheet Revision History

Table 23. Bt819A Datasheet Revision History *(1 of 2)*

Revision	Date	Change	Description
Rev. A	4/21/95	Corrections from L819001 Rev. B	1) Description of ByteStream changed to indicate CLKx2 is normally used and not QCLK. 2) The recommended inductor value in the anti-aliasing filter in "Typical External Circuitry" changed to 3.3 µH from 3.6 µH. Note the recommended tolerance for all inductors in the datasheet is ±10% 3) Figure 26 changed to indicate that pixel output data changes one clock after DVALID transitions low. 4) Table 9 changed to indicate that HRESET is output after the last pixel in a line and VRESET is output after the HRESET of the last line in the field. 5) Typographical mistake in the recommended entry for the HSCALE_LO value at the beginning of the Control Register Definition section. The value for square pixel NTSC was changed from 0xAC to 0xAA. 6) The power numbers have been added to Table 18 for all three devices. 7) Suggested configuration for use of the FIFO in API mode B has been added to the API section of the datasheet.

Table 23. Bt819A Datasheet Revision History *(2 of 2)*

Revision	Date	Change	Description
Rev. B	12/29/95		1) Bt815 pin definitions changed to provide complete compatibility between Bt819, Bt817 and Bt815 (Pin numbers 64, 67, 74 and 81). 2) Bt817 pin definition for pin 81 changed to provide compatibility between Bt819, Bt817 and Bt815. 3) Standard Crystal included in recommended crystal manufacturers as they offer very short lead times. 4) Bias capacitors changed to optional. Not recommended for new designs. 5) FIFO pin definitions in Table 7 and Table 9 are incorrect. The even field is field 2, and the odd field is field 1. 6) API mode-A change: CLKIN must be connected to CLKx1. 7) API mode-B change: The FIFO should not be emptied while active video is being written into the FIFO. Do not read the FIFO until empty, during the active video line. 8) In both API modes A and B: The control codes are not valid when the FIFO is not being read. 9) Example schematic in Figure 36 changed to reflect Bt819A. 10) Typographical error in the STATUS register corrected. COF is the least significant bit. 11) Additional crystal vendors added. Short lead times available from Standard Crystal. 12) The timing from QCLK to Data Valid in 8-bit mode was changed. See Figure 37. 13) The VPOLE register definition was changed to indicate that DVALID, FIELD and AFF do not have programmable polarities in API mode.
Rev. C	09/18/96		In Functional Description section under Scaling Registers, HSCALE: was = 12331 changed to = 15602