Am29501

Multi-Port Pipelined Processor (Byte-Slice™)

DISTINCTIVE CHARACTERISTICS

- Expandable Byte-Slice™ Register-ALU
  - Sign extend input and output
  - Carry and $\overline{P}/\overline{G}$ expansion with force/inhibit/normal carry modes
- Eight instruction ALU
  - Four arithmetic operations
  - Four logic operations
- Ten internal data paths
  - Highly parallel architectures
  - Multiple simultaneous data manipulations
- Pipelining register file has six 8-bit registers
  - Multilevel pipelining
  - Multiple register-to-register moves
- Completely microprogrammable
  - No instruction encoding
  - All operation combinations available
- Three I/O ports for maximum system interconnect flexibility

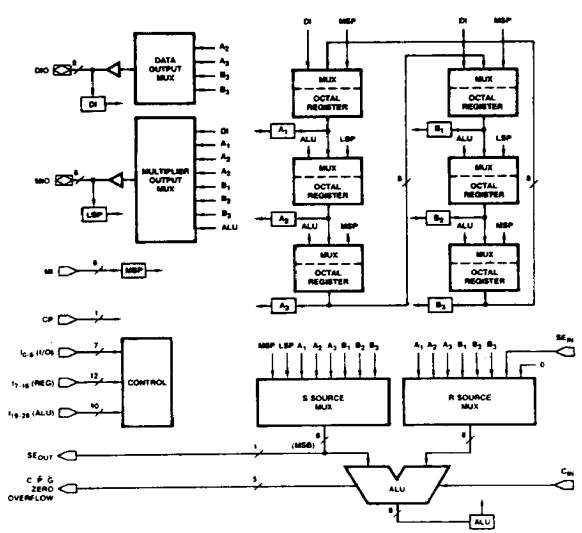
GENERAL DESCRIPTION

The Am29501 is an expandable Byte-Slice™ register-ALU designed to bring maximum speed to array processor and digital signal processor systems. It provides a flexible processor building block for implementing highly pipelined, highly parallel architectures where speed is achieved by a combination of optimized integrated circuit technology (IMOX™ process and internal ECL circuitry) and customized system architecture. I/O port flexibility and multiple concurrent data moves make it possible to construct processors capable of very high throughput. Parallel processors are especially efficient for array/vector operations or signal processing algorithms requiring complex number arithmetic (e.g. FFT, convolution, correlation, etc.).

The Am29501's Pipeline Register File provides data storage and pipelining flexibility. Any combination of register instructions, ALU instructions, and I/O instructions can be microprogrammed to occur in the same cycle. This allows overlap of external multiplication, ALU operations, and memory I/O.

Three I/O ports support a wide variety of parallel, pipelined architectures by providing separate I/O ports for the multiplier and the memory data bus. Either of two bidirectional I/O ports, DIO and MIO, can interface to the data bus or multiplier Y-input port, and a separate MI port connects to the multiplier output port.

BLOCK DIAGRAM



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IMOX is a trademark of Advanced Micro Devices, Inc.

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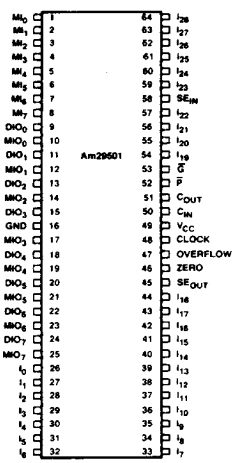
RELATED PRODUCTS

Part No.	Description
Am2902A	Carry look-ahead generator
Am29516/17	16 x 16-bit high speed multipliers
Am25S558	8 x 8-bit multiplier

CONNECTION DIAGRAM

Top View

D-64-3



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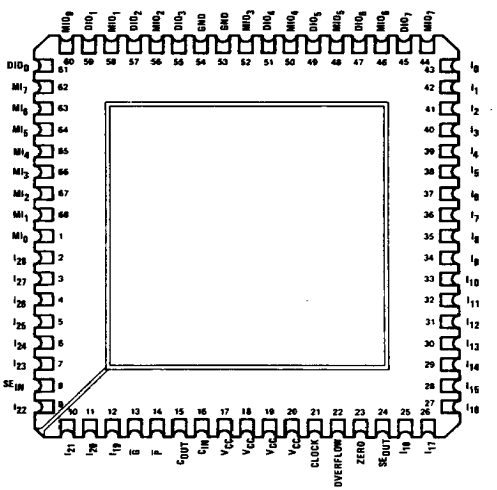
Leadless Chip Carrier



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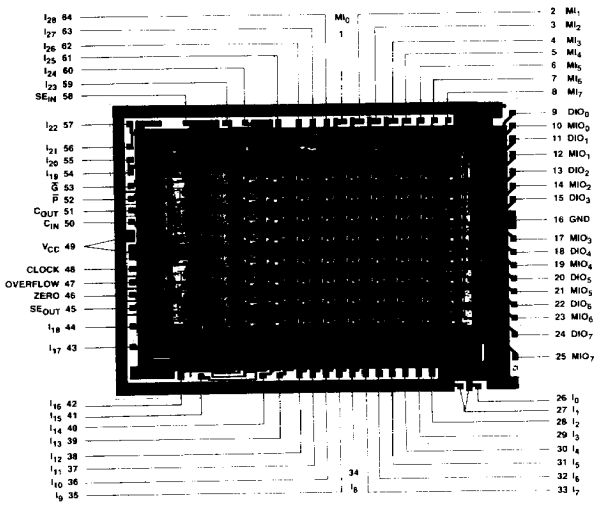
METALLIZATION AND PAD LAYOUT



Die Size: .289" x .222"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29501 **P** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in (Note 1)
- **C** — Temperature (see Operating Range)
  - C – Commercial (0 to +70°C)
  - M – Military (–55 to +125°C)
- **P** — Package
  - D – 64-pin CERDIP (D-64-3)
  - L – 68-TERMINAL Leadless Chip Carrier
- **Am29501** — Device type
  - Multi-port Pipelined Processor

Note 1: 160 Hour Burn-in
Heatsink Parts, $T_A = 125°C$
Non-Heatsink Parts, $T_A = 85°C$

Valid Combinations	
Am29501	DC, DCB, DMB, LC, LMB

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

*Pin No.	Name	I/O	Description
50	C_{IN}	I	Carry-in input to the internal 8-bit ALU.
51	C_{OUT}	O	Carry-out output from the internal 8-bit ALU.
48	CP	I	Clock input for the internal pipeline register file. Data selected by I_7-I_{18}, meeting the set-up and hold time requirements of the respective register, is clocked into the register on the clock LOW-to-HIGH transition.
9, 11, 13, 15, 18, 20, 22, 24	DIO_0-DIO_7	I/O	Bidirectional data I/O port (see Note).
53, 52	$\overline{G}$, $\overline{P}$	O	The carry generate and propagate outputs of the internal ALU. These signals are used with the Am2902A for carry-lookahead.
26-44, 54-57, 59-64	I_0-I_{28}	I	Instruction inputs designed to be driven under microprogram control. All instruction inputs control multiplexers or drivers or the ALU directly. There is no instruction encoding. See Control Input Function Tables for operating modes.
1-8	MI_0-MI_7	I	Data Input port (Multiplier Input - see Note).
10, 12, 14, 17, 19, 21, 23, 25	MIO_0-MIO_7	I/O	Bidirectional data I/O port (Multiplier I/O - see Note).
47	OVR	O	Overflow This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.
45	SE_{OUT}	O	The most significant bit of the S-operand. This is used in multiple precision arithmetic operations for sign extension of two's complement numbers.
58	SE_{IN}	I	A single-bit input which generates an 8-bit sign extension R-operand for multiple precision two's complement arithmetic operations.
46	ZERO	O	This is an open collector output which goes HIGH if the data on the ALU outputs are all LOW.

Note: This is a general purpose data port. The names are derived from the typical usage in a typical Am29500 system but are not restricted to this interconnection scheme.

*DIP Configuration

CONTROL INPUT FUNCTION TABLES

1. Data I/O Port (DIO) Output Select

I_3	I_2	I_0	Source
L	L	L	A_2
L	H	L	A_3
H	L	L	B_2
H	H	L	B_3
X	X	H	Output Disabled

2. Multiplier I/O Port (MIO) Output Select

I_6	I_5	I_4	I_1	Source
L	L	L	L	A_1
L	L	H	L	A_2
L	H	L	L	A_3
L	H	H	L	B_1
H	L	L	L	B_2
H	L	H	L	B_3
H	H	L	L	ALU
H	H	H	L	DI
X	X	X	H	Output Disabled

3. Register A_1 Data Source Select

I_8	I_7	Source
L	L	MSP (MI)
L	H	DI (DIO)
H	L	B_3
H	H	A_1 (Hold)

4. Register A_2 Data Source Select

I_{10}	I_9	Source
L	L	LSP (MIO)
L	H	ALU
H	L	A_1
H	H	A_2 (Hold)

03564A

CONTROL INPUT FUNCTION TABLES (Cont.)

5. Register A_3 Data Source Select

I_{12}	I_{11}	Source
L	L	MSP (MI)
L	H	ALU
H	L	A_2
H	H	A_3 (Hold)

6. Register B_1 Data Source Select

I_{14}	I_{13}	Source
L	L	MSP (MI)
L	H	DI (DIO)
H	L	A_3
H	H	B_1 (Hold)

7. Register B_2 Data Source Select

I_{16}	I_{15}	Source
L	L	LSP (MIO)
L	H	ALU
H	L	B_1
H	H	B_2 (Hold)

8. Register B_3 Data Source Select

I_{18}	I_{17}	Source
L	L	MSP (MI)
L	H	ALU
H	L	B_2
H	H	B_3 (Hold)

9. ALU Operating Instructions

I_{22}	I_{21}	I_{20}	I_{19}	OP	C_{OUT}	$\overline{P}$	$\overline{G}$	
L L H H	L H L H	L	L	R + S + C_{IN} R − S − C_{IN} R + C_{IN} −R + S − C_{IN}	Carry	$\overline{P}$	$\overline{G}$	Normal Operating Mode**
L L H H	L H L H	L	H	R + S + C_{IN} R − S − C_{IN} R + C_{IN} −R + S − C_{IN}	L	H	H	Inhibit Carry Mode
L L H H	L H L H	H	L	R + S + C_{IN} R − S − C_{IN} R + C_{IN} −R + S − C_{IN}	H	$\overline{P}$	L	Force Carry Mode
L L H H	L H L H	H	H	R XOR S R AND S $\overline{R}$ R OR S	(L)*	(H)*	(H)*	Logic Operations

*C_{OUT}, $\overline{P}$ and $\overline{G}$ are not applicable to logic operation, Am29501 functions as shown.
**Carry is used for 16-bit expansion. $\overline{P}$ and $\overline{G}$ are used with an Am2902A for expansion to more than 16 bits.

10. ALU R Operand Selection

I_{25}	I_{24}	I_{23}	Source
L L L	L L H	L H L	A_1 A_2 A_3
L H H	H L L	H L H	B_1 B_2 B_3
H	H	L	Sign Extend Input Bussed to All Bits
H	H	H	Arithmetic Zero (All Inputs LOW)

11. ALU S Operand Selection

I_{28}	I_{27}	I_{26}	Source
L L L	L L H	L H L	A_1 A_2 A_3
L H H	H L L	H L H	B_1 B_2 B_3
H H	H H	L H	MSP (MI) LSP (MIO)

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Refer to Page 13-1 for Essential Information on Military Devices

DETAILED DESCRIPTION

Figure 1 contains a block diagram of the Am29501. It shows four major sections – an eight-bit cascadable ALU, a register file consisting of six eight-bit registers, three I/O ports, and a microcode control section.

DETAILED Am29501 BLOCK DIAGRAM

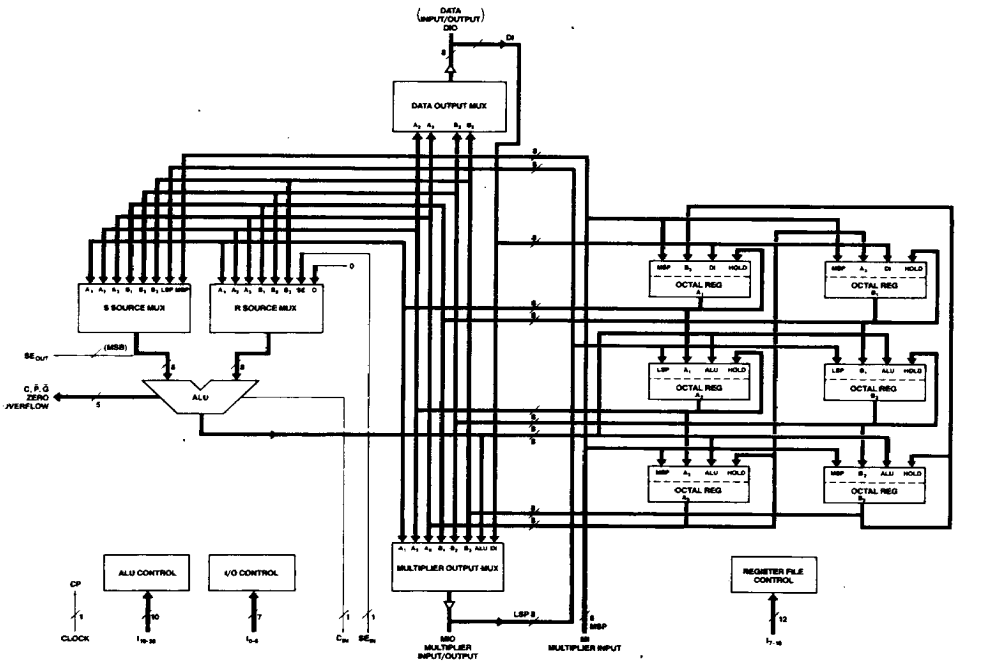

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Figure 1.

ALU

The ALU performs arithmetic on an eight-bit Byte-Slice™ with full internal carry lookahead and carry input and output for cascading. The carry can ripple between byte-slices by connecting the C_{OUT} of one slice to C_{IN} of the next byte-slice. Carry generate ($\overline{G}$) and propagate ($\overline{P}$) outputs are also provided for faster operation when the ALU is used in conjunction with a carry lookahead generator such as the Am2902A.

There are three arithmetic modes – cascade, carry inhibit and forced carry. The cascade mode produces an output carry based on the results of the operation and is the normal mode. The carry inhibit mode produces no carry output and is used to decouple cascaded ALUs. A 16-bit ALU consisting of two Am29501s can operate as two 8-bit ALUs simultaneously by programming the carry inhibit mode. This mode could also be used with a second 16-bit ALU for double precision where the more significant slice is programmed in the carry inhibit mode for single precision and in the cascade mode for double precision. The less significant slices would be programmed in normal mode for either case. The forced carry mode is the converse and always produces a carry. All three modes treat the input carry in the same way. The Am29501 uses the input carry as a true borrow during subtraction as opposed to most two's complement ALUs which use $\overline{\text{borrow}}$. The usual requirement is that input borrow be programmed HIGH (inactive) when doing a subtraction. Since the Am29501 has a true borrow, the input carry is programmed to be LOW for both addition and subtraction. This is consistent with the carry inhibit mode discussed previously.

In addition to arithmetic operations the ALU also does bitwise logic operations – OR, AND, exclusive OR, and invert. Carries are not applicable for these operations and are inactive. Codes to program the ALU function are contained in Control Input Function Table 9.

Each operand of the ALU has eight possible sources. Operand R can be any register in the register file or one of the I/O ports MI or MIO as shown in Table 10. Operand S can be any register, zero or a sign extension input (SE_{IN}) from another ALU (Table 11). The ALU result can be steered to registers A2, A3, B2, and B3 of the register file or the MIO I/O port.

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REGISTER FILE

The register file provides for fully independent use of the registers. Each register has a four-input mux which can be programmed so that the register holds its previous contents or is loaded from the ALU and I/O port or the "preceding" register. If all registers are programmed for the preceding register, a ring is formed and data circulates through all the registers. This facilitates constructing a pipelined data flow. Various combinations of I/O ports and the ALU make up the remaining inputs to each register. The sources for each register are shown in the Control Input Function Tables 3–8.

I/O PORTS

The Am29501 has two bidirectional ports (DIO and MIO) and one input port (MI). As an input the DIO port can be loaded into registers A1 and B1 and directed to the MIO output port. Output from the DIO comes from registers A2, A3, B2 or B3 using the codes from Control Input Function Table 1. This separation of input and output registers connected to the DIO port is in keeping with the pipelined organization of the part when the DIO port is used for data flow in and out of the processor.

Input through the MIO port can be directed to registers A2 and B2 in the register file and to the ALU. Output can come from any of the six registers, the DIO input port or from the ALU. This structure allows the user to direct operands to an auxiliary processor (such as a multiplier or barrel shifter) from any point in the pipeline. The MIO port could be connected to a processor with bidirectional data bus. The auxiliary processor would receive data and return its results to registers A2 and B2 through the MIO port.

The MI port provides another entry point for inserting data in the processing pipeline. An auxiliary processor with flow-through architecture could receive data from the MIO port and return data through the MI port which can be directed to registers A1, A3, B1 and B3 and to the ALU.

A potential use of the ports is connecting the bidirectional bus of an Am29116 microprocessor to the MIO port. An Am29516 would have its inputs connected to the same MIO port and its output to the MI port. This architecture could calculate magnitudes by computing the sum of the squares with the Am29516 and Am29501 and the square root with the Am29116.

CONTROL

The Am29501 is controlled by 29 microcode bits which select operations with no encoding. This provides the maximum flexibility for the independent control of parallel operations. Sources may be directed to multiple destinations simultaneously wherever data paths are provided.

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Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Temperature Under Bias-T_C ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5 to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30 to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature
DIPs ..... T_A = 0°C to +70°C
Chip Carriers ..... T_C = 0°C to 85°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

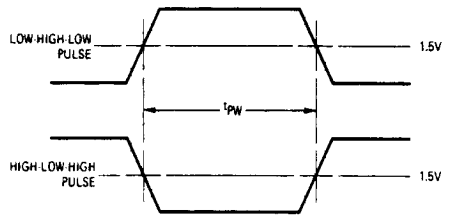
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OH} = −2.6mA (COM'L)	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	COM'L	I_{OL} = 24mA DIO, MIO			0.5	Volts
				I_{OL} = 8mA Others			0.5	
			MIL	I_{OL} = 16mA DIO, MIO				
				I_{OL} = 8mA Others			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					20	µA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					0.1	mA
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = MAX		V_O = 0.5V			−55	µA
I_{OZL}				V_O = 2.4V			100	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−100	mA
I_{CC}	Power Supply Current	COM'L and MIL		T_A = 25°C		300		mA
		COM'L Only, V_{CC} = MAX		T_A = 0 to +70°C (Note 4)			400	
				T_A = +70°C (Note 4)			375	
		MIL Only, V_{CC} = MAX		T_C = −55 to +125°C				
				T_C = +125°C				

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Chip Carriers: T_C = 85°C.

PULSE WIDTH



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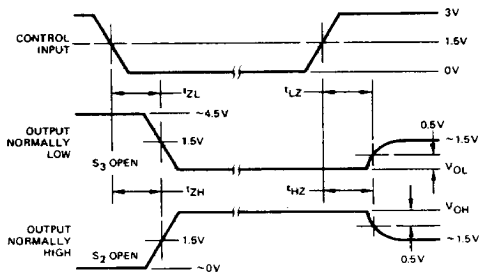
ENABLE AND DISABLE TIMES



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Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1, S_2 and S_3 of Load Circuit are closed except where shown.

NOTE: 1. Pulse generator for all pulses: Rate ≤ 1.0MHz; Z_O = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

SWITCHING CHARACTERISTICS AT ROOM TEMPERATURE

Typical Set-up/Hold Times and Propagation Delays
V_{CC} = 5.0V, T_A = + 25°C, C_L = 50pF

	To Output											
	Set-up, t_s/Hold, t_h		Propagation Delay Times, t_{PD}									
From Input	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	C_{OUT}	$\overline{P}$	$\overline{G}$	Z	Overflow	SE_{OUT}	Units
CLK			17	27	17	23	23	23	27	34	18	ns
DIO			12									ns
MIO						22	22	22	25	22	17	ns
MI				24		22	22	22	25	22	17	ns
C_{IN}				16		10			17	13		ns
SE_{IN}				23		19	19	19	16	22	19		ns
I_{2-3}(DIO)					17								ns
I_{4-6}(MIO)			15										ns
I_{7-18}(REG)													ns
I_{19-22}(ALU OP)						19	19	19	22	19		ns
I_{23-28}(ALU SEL)				31		20	20	20	25	22	14	ns

Am29501 Three-State Timing

			Typ	Max	Commercial	Military	
Parameters	Description	Test Conditions	V_{CC} = 5V, T_A = 25°C	V_{CC} = 5V, T_A = 25°C	Max	Max	Units
t_{LZ}	$I_0 \rightarrow DIO_{0-7}$ $I_1 \rightarrow MIO_{0-7}$	C_L = 5pF, R_L = 667Ω	10		15		ns
t_{HZ}	$I_0 \rightarrow DIO_{0-7}$ $I_1 \rightarrow MIO_{0-7}$	C_L = 5pF, R_L = 667Ω	10		15		ns
t_{ZL}	$I_0 \rightarrow DIO_{0-7}$ $I_1 \rightarrow MIO_{0-7}$	C_L = 50pF, R_L = 667Ω	12		20		ns
t_{ZH}	$I_0 \rightarrow DIO_{0-7}$ $I_1 \rightarrow MIO_{0-4}$	C_L = 50pF, R_L = 667Ω	12		20		ns

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Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS, COMMERCIAL

Minimum Set-up/Hold Times and Maximum Propagation Delays

	To Output											
	Set-up, t_s/Hold, t_h		Propagation Delay Times, t_{PD}									
From Input	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	C_{OUT}	$\overline{P}$	$\overline{G}$	Z	Overflow	SE_{OUT}	Units
CLK			23	35	24	31	31	31	39	34	26	ns
DIO	10/5		17									ns
MIO	10/5	20/0				29	29	29	34	29	24	ns
MI	10/5	20/0		32		30	29	29	34	29	24	ns
C_{IN}		10/5		25		15			26	19		ns
SE_{IN}		20/0		29		27	27	22	32	27		ns
I_{2-3}(DIO)					21							ns
I_{4-6}(MIO)			22									ns
I_{7-18}(REG)	10/5											ns
I_{19-22}(ALU OP)		20/0	32			27	27	27	32	29		ns
I_{23-28}(ALU SEL)		20/0				29	29	29	35	32	22	ns

SWITCHING CHARACTERISTICS, MILITARY

Minimum Set-up/Hold Times and Maximum Propagation Delays

	To Output											
	Set-up, t_s/Hold, t_h		Propagation Delay Times, t_{PD}									
From Input	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	C_{OUT}	$\overline{P}$	$\overline{G}$	Z	Overflow	SE_{OUT}	Units
CLK												ns
DIO												ns
MIO												ns
MI												ns
C_{IN}												ns
SE_{IN}												ns
I_{2-3}(DIO)												ns
I_{4-6}(MIO)												ns
I_{7-18}(REG)												ns
I_{19-22}(ALU OP)												ns
I_{23-28}(ALU SEL)												ns

Note: Please refer to *Guidelines for Testing Am2900 Family Devices* in section 13 of this data book.

Am29501 Minimum Clock Pulse Widths

Parameter	Description		TYPICAL	COMMERCIAL	MILITARY	Units
t_{PW}	Clock Pulse Width	High		15		ns
		Low		15		ns

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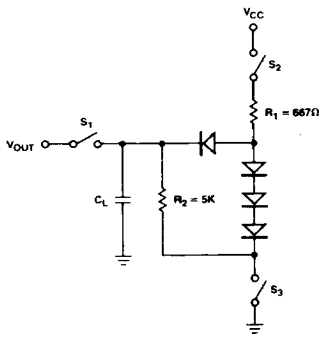
SWITCHING TEST CIRCUIT

A. THREE-STATE OUTPUTS



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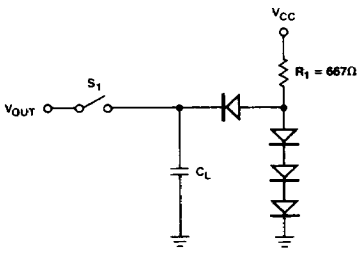
B. NORMAL OUTPUTS



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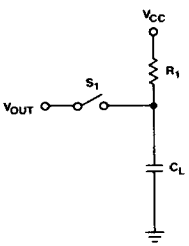
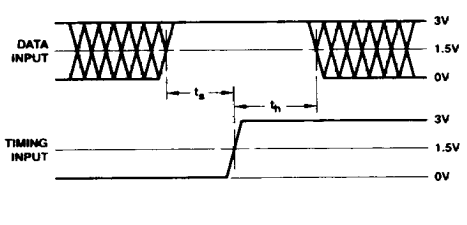
C. OPEN-COLLECTOR OUTPUTS



TC001420

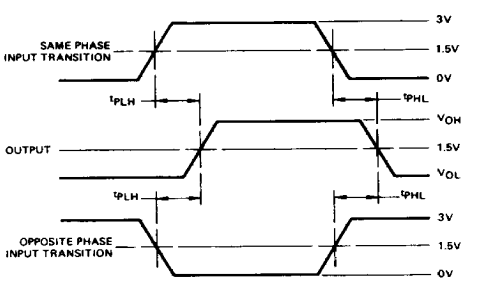
Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

SET-UP, HOLD, AND RELEASE TIMES



WFR02970

PROPAGATION DELAY



WFR02980

Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

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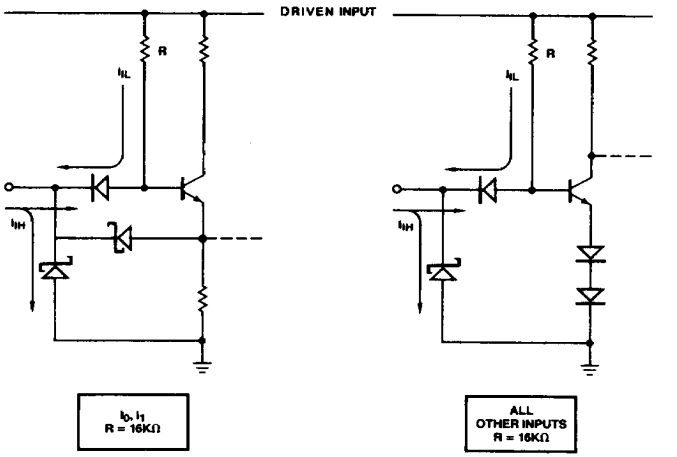
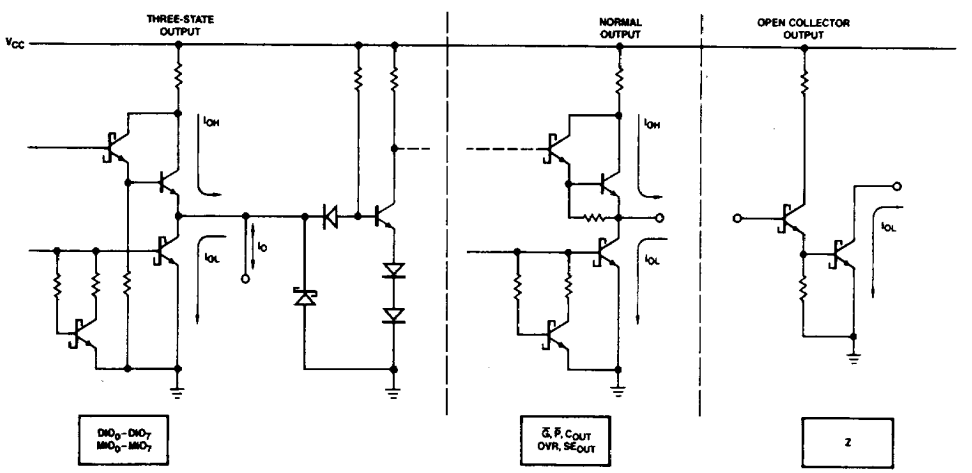
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



ICR00530

$C_I \cong 5.0pF$, all inputs



ICR00520

$C_O \cong 5.0pF$, all outputs
Note: Actual current flow direction shown.

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Refer to Page 13-1 for Essential Information on Military Devices