NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD3735, 3735A

5000-BIT CCD LINEAR IMAGE SENSOR WITH PERIPHERAL CIRCUIT

The μPD3735 (3735A) is a 5000-bit high sensitivity CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The μPD3735 (3735A) has an output amplifier which has high gain and wide output range.

Built-in sample and hold circuit converts and outputs independent CCD register in every bit to continuous video signal. So it is easy to interface to A/D converter or Bi-level converter.

FEATURES

• Valid photocell	5000-bit
• Photocell's pitch	7 μm
• High response sensitivity	Providing a response 8 times (μPD3735)/6.3 times (μPD3735A) better than the existing equivalent NEC product (μPD3571) to the light from a daylight fluorescent lamp
• Peak response wavelength	550 nm (green)
• Resolution	16 dot/mm across the shorter side of an A3-size (297 × 420 mm) sheet
• Power supply	+12 V
• Drive clock level	CMOS 5 V clock
• High speed scan	720 μs/line (μPD3735), 560 μs/line (μPD3735A)
• Built-in circuit	Sample and hold circuit
• Data rate	7 MHz (μPD3735), 9 MHz (μPD3735A)

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ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD3735D	22-pin ceramic DIP (CERDIP) (400 mil)	Standard
μPD3735AD	22-pin ceramic DIP (CERDIP) (400 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice

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The mark ★ shows revised point.

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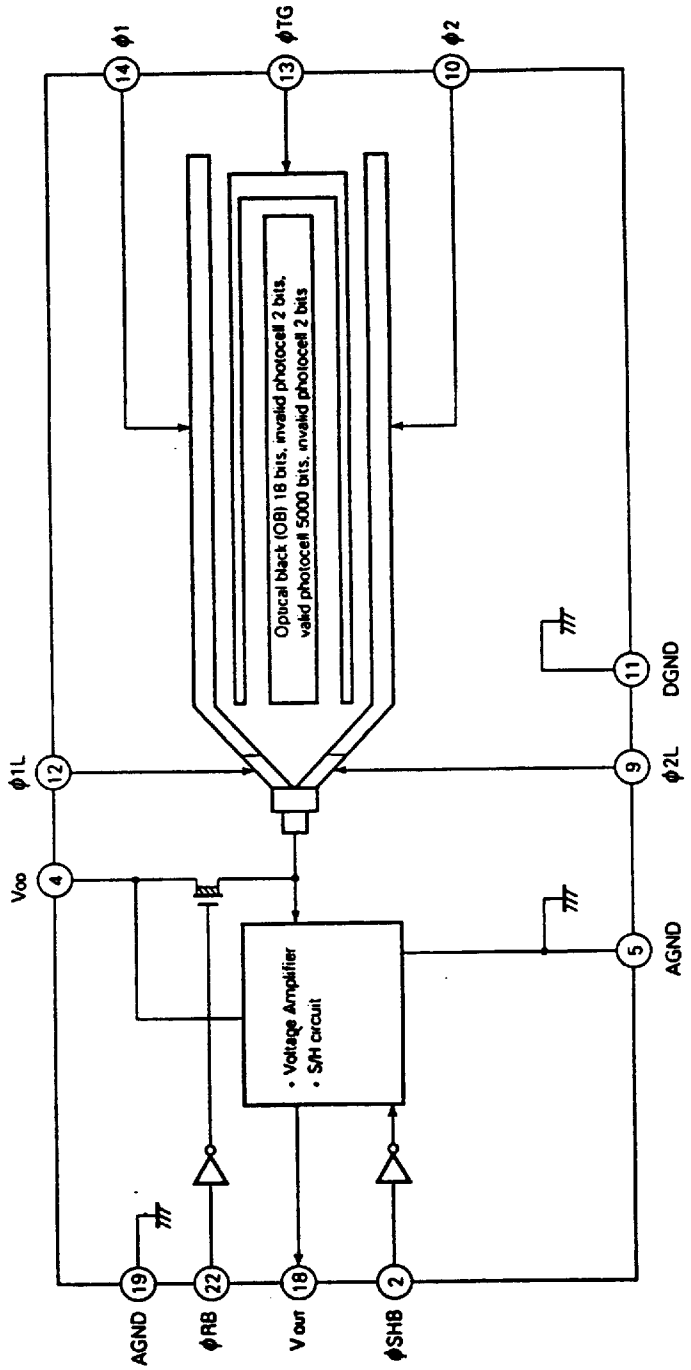
BLOCK DIAGRAM



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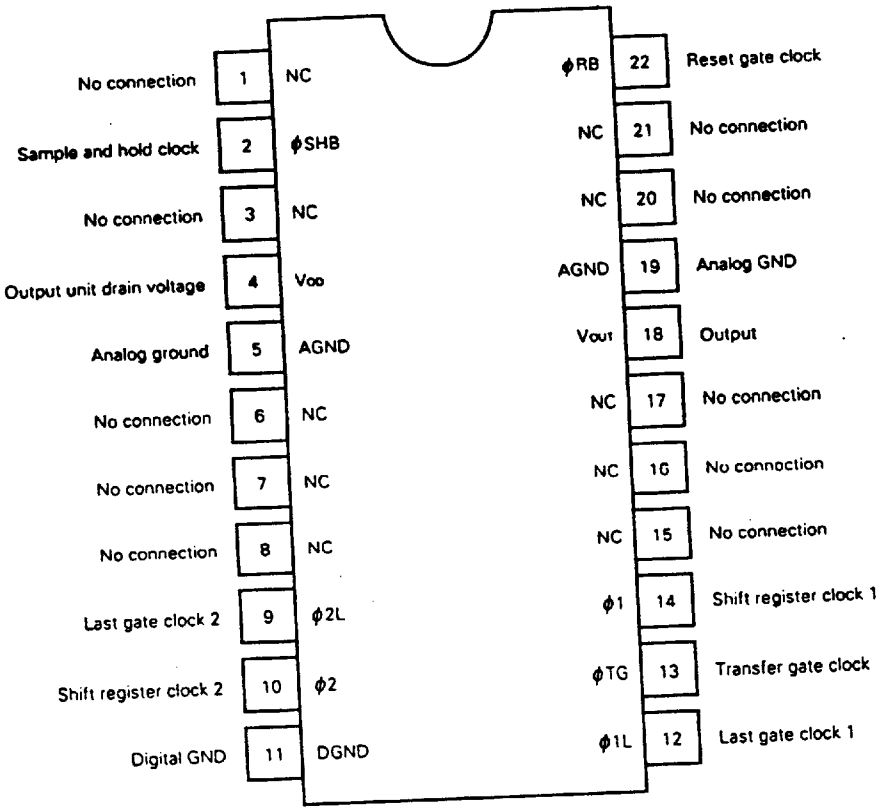
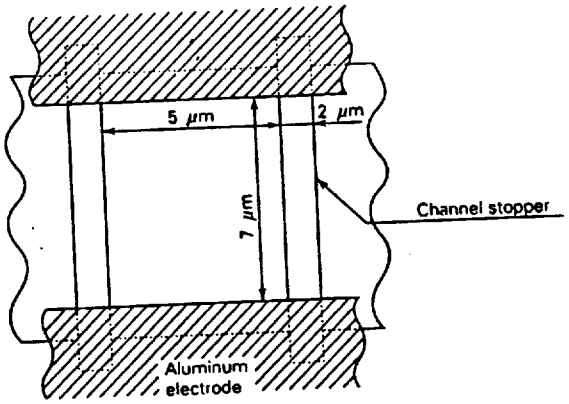
PIN CONFIGURATION (Top View)



PHOTOELEMENT STRUCTURE DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (T_a = +25 °C)

Parameter	Symbol	Ratings	Unit
Output unit drain voltage	V_{OD}	−0.3 to +15	V
Shift register clock voltage	$V_{\phi 1, \phi 2}$	−0.3 to +15	V
Reset signal voltage	$V_{\phi RB}$	−0.3 to +15	V
Transfer gate signal voltage	$V_{\phi TG}$	−0.3 to +15	V
Sample and hold signal voltage	$V_{\phi SHB}$	−0.3 to +15	V
Operating ambient temperature	T_{opt}	−25 to +60	°C
Storage temperature	T_{stg}	−40 to +100	°C

★ RECOMMENDED OPERATING CONDITIONS (T_a = −25 to + 60 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output unit drain voltage	V_{OD}	11.4	12.0	12.6	V
Shift register clock ϕ_1, ϕ_2 signal high level	$V_{\phi 1H}$, ϕ_{2H}	4.5	5.0	5.5	V
Shift register clock ϕ_1, ϕ_2 signal low level	$V_{\phi 1L}$, ϕ_{2L}	−0.3	0	0.5	V
Reset signal ϕ_{RB} high level	$V_{\phi RBH}$	4.5	5.0	5.5	V
Reset signal ϕ_{RB} low level	$V_{\phi RBL}$	−0.3	0	0.5	V
Transfer gate signal high level	$V_{\phi TGH}$	4.5	$V_{\phi 1H}$ Note 1	$V_{\phi 1H}$ Note 1	V
Transfer gate signal low level	$V_{\phi TGL}$	−0.3	0	0.5	V
Sample and hold signal high level	$V_{\phi SHBH}$	4.5	5.0	5.5	V
Sample and hold signal low level	$V_{\phi SHBL}$	−0.3	0	0.5	V
Data rate	$f_{\phi R}$	0.2	1	Note 2	MHz

Notes 1. When $V_{\phi TGH} > V_{\phi 1H}$, image lag increases.

2. 7 MHz (μPD3735), 9 MHz (μPD3735A)

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ELECTRICAL CHARACTERISTICS

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(T_a = +25 °C, V_{DD} = 12 V, $f_{\phi 1}$ = 0.5 MHz, data rate = 1 MHz, storage time = 10 ms
light source: 3200 K halogen lamp + C500 (infrared cut filter), input clock = 5 V_{P-P})

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{SAT}			1.5	2.0		V
Saturation exposure	SE	Daylight color fluorescent lamp	μPD3735		0.16		lx·s
			μPD3735A		0.21		
Photo response non-uniformity	PRNU	V_{OUT} = 500 mV			±2	±10	%
Average dark signal	ADS	Light shielding			0.5	2.0	mV
		μPD3735A: Data rate = 2 MHz, Storage time = 3 ms			0.15	0.6	
Dark signal non-uniformity	DSNU	Light shielding	μPD3735	−2.0	±3	+10	
			μPD3735A	−2.0	±9	+18	
		μPD3735A: Data rate = 2 MHz, Storage time = 3 ms		−0.6	±2.7	+5.4	
Power consumption	P_W				300	450	mW
Output impedance	Z_O				0.5	1	kΩ
Response	R_F	Daylight color fluorescent lamp	μPD3735	8.4	12	15.6	V/lx·s
			μPD3735A	6.7	9.5	12.4	
	R_W	W lamp	μPD3735	25.2	36	46.8	
			μPD3735A	20.0	28.5	37.1	
Response peak wavelength					550		nm
Image lag	IL	V_{OUT} = 1 V			6	11	%
Offset level	V_{OS}			3.0	4.8	6.6	V
Input capacity of shift register clock pin	$C_{\phi 1}$				900		pF
	$C_{\phi 2}$				800		
Input capacity of reset pin	$C_{\phi RB}$				5	10	pF
Input capacity of sample and hold pin	$C_{\phi SHB}$				5	10	pF
Input capacity of last gate clock pin	$C_{\phi 1L}$ $C_{\phi 2L}$				50	100	pF
Input capacity of transfer gate signal pin	$C_{\phi TG}$				100	200	pF
Output rise delay time	t_d		μPD3735		40		ns
			μPD3735A		30		
Register imbalance	RI	V_{OUT} = 500 mV				3	%
Transfer efficiency	TTE	V_{OUT} = 500 mV, $f_{\phi R}$ = 10 MHz		92	98		%
Dynamic range	DR	V_{SAT}/DSNU	μPD3735		666		times
			μPD3735A		222		
Reset feed through noise	RFSN	Light shielding		0	350	600	mV
Sample and hold noise	SHSN	Light shielding		−50	0	50	mV

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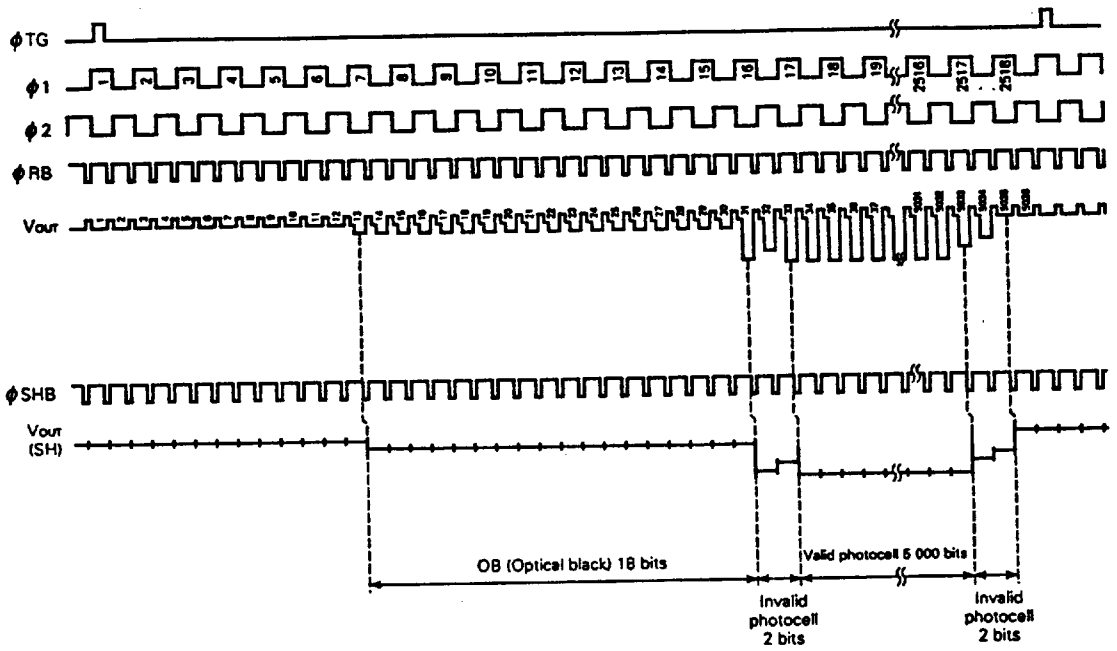
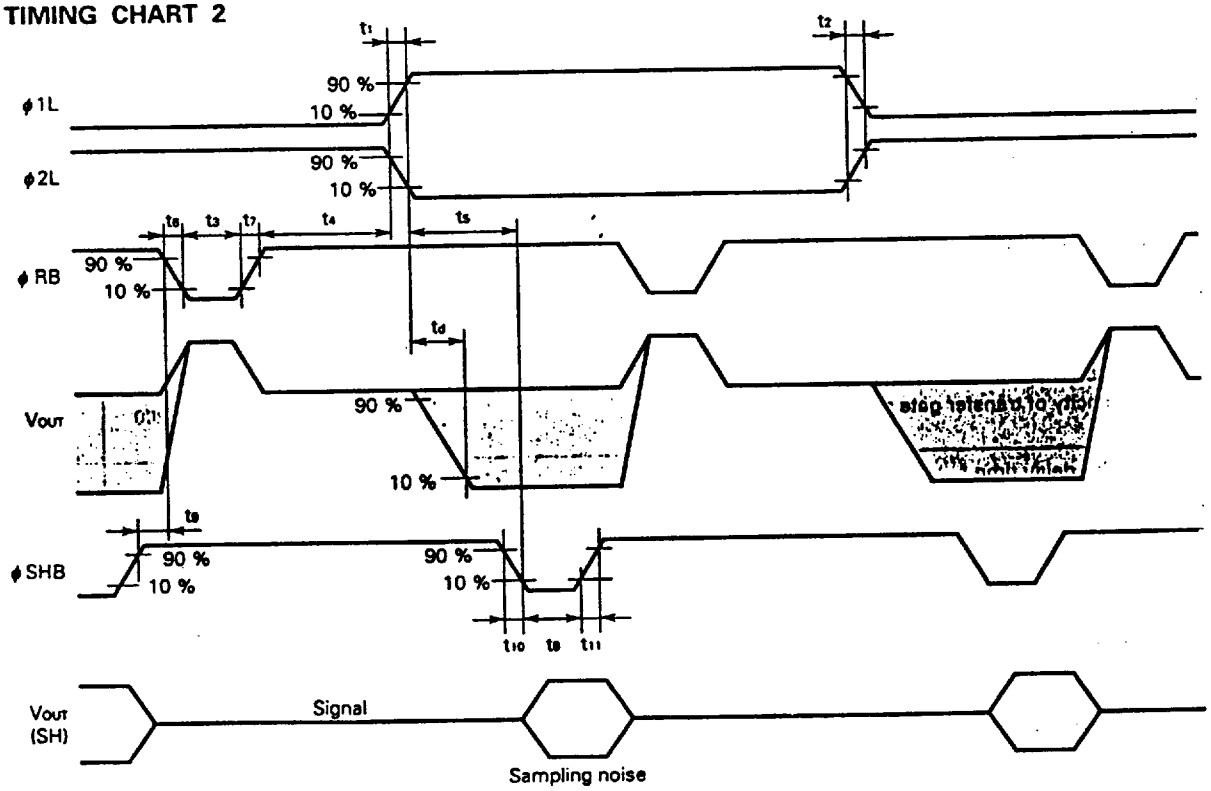
TIMING CHART 1



Remark V_{OUT} = Output when φSHB is not used (When φSHB is not used, connect φSHB pin to GND).
V_{OUT} (SH) = Output when φSHB is used.

★ TIMING CHART 2



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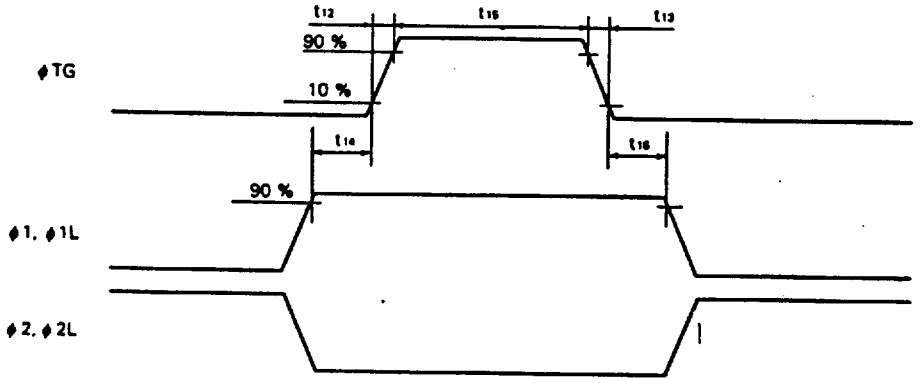
TIMING CHART for φTG, φ1, φ1L, φ2, φ2L ★



μPD3735 (Unit: ns)

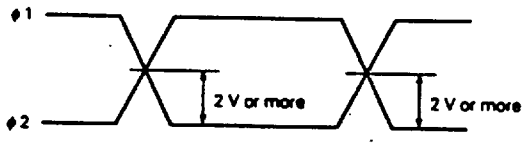
Parameter	MIN.	TYP.	MAX.
t_1, t_2	0	50	150
t_4	30	100	(500)
t_5	40	300	(500)
t_6, t_7	0	50	100
t_3, t_8	35	150	(500)
t_9	0	100	(150)
t_{10}, t_{11}	0	50	100
t_{12}, t_{13}	0	50	100
t_{14}, t_{16}	0	100	(500)
t_{15}	500	1000	(5000)

μPD3735A (Unit: ns)

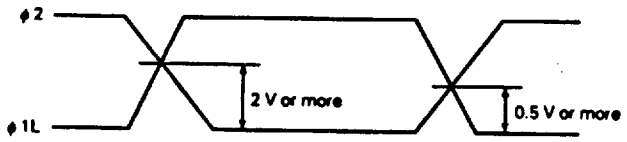
Parameter	MIN.	TYP.	MAX.
t_1, t_2	0	50	150
t_4	25	100	(500)
t_5	30	300	(500)
t_6, t_7	0	50	100
t_3, t_8	25	150	(500)
t_9	0	100	(150)
t_{10}, t_{11}	0	50	100
t_{12}, t_{13}	0	50	100
t_{14}, t_{16}	0	100	(500)
t_{15}	500	1000	(5000)

Remark The MAX. in the table above shows the operation range in which the output characteristics are kept almost enough for genaral purpose, does not show the limit above which the μPD3735 (μPD3735A) is destroied.

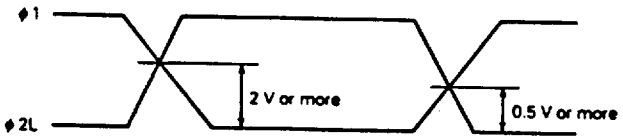
CROSS POINTS for φ1, φ2



CROSS POINTS for φ1L, φ2



CROSS POINTS for φ1, φ2L



Remark Adjust cross point of (φ1, φ2), (φ1L, φ2), (φ1, φ2L) by each pin external input resistor.

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DEFINITIONS OF CHARACTERISTIC ITEMS

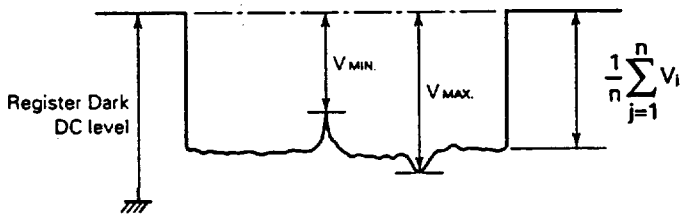
1. Saturation voltage: V_{SAT}
   Output signal voltage at which the response linearity is lost.

2. Saturation exposure: SE
   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

3. Photo response non-uniformity: PRNU
   The peak/bottom ratio to the average output voltage of all the valid bits calculated by the following formula.

$$PRNU\ (\%) = \left(\frac{V_{MAX.} \text{ or } V_{MIN.}}{\frac{1}{n}\sum_{j=1}^{n} V_j} - 1 \right) \times 100$$

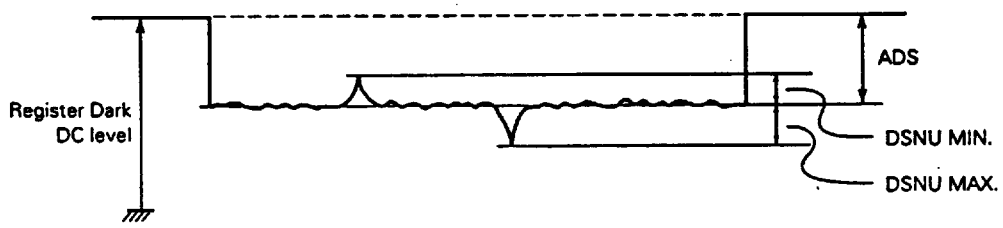
n : Number of valid bits
V_j : Output voltage of each bit



4. Average dark signal: ADS
   Output average voltage in light shielding.

$$ADS(mV) = \frac{1}{n}\sum_{j=1}^{n} V_j$$

5. Dark signal non-uniformity: DSNU
   The difference between peak or bottom output voltage in light shielding and ADS.



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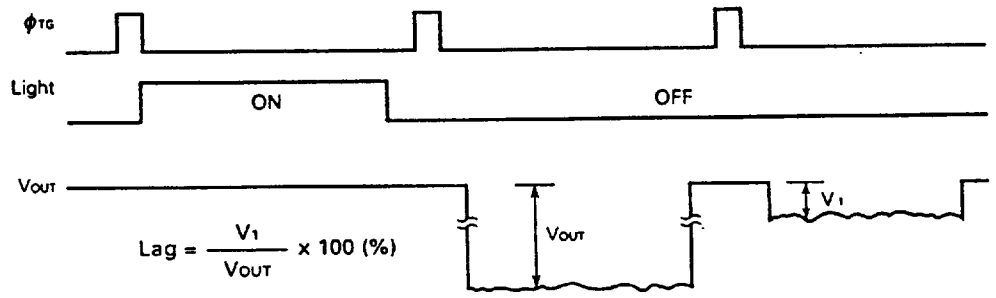
6. Output impedance: Z_o
   Output pin impedance viewed from outside.

7. Response: R
   Output voltage divided by exposure (lx·s).
   Note that the response varies with the light source.

8. Image Lag: IL
   The rate between the last output voltage and the next one after read out the data of a line.



9. Register Imbalance: RI
   The rate of the average voltage which is the difference between the output voltage of Odd and Even bits, against the average output voltage of all the valid bits.

$$RI = \frac{\frac{1}{n}\sum_{j=1}^{n} |V_j - V_{j+1}|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100\ (\%)$$

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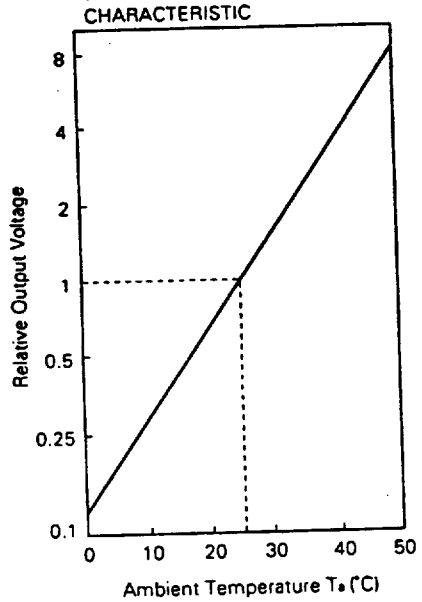
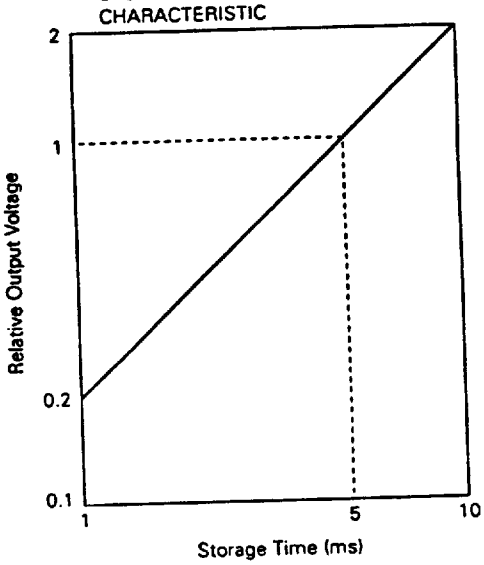
STANDARD CHARACTERISTIC CURVES (T_a = 25 °C)

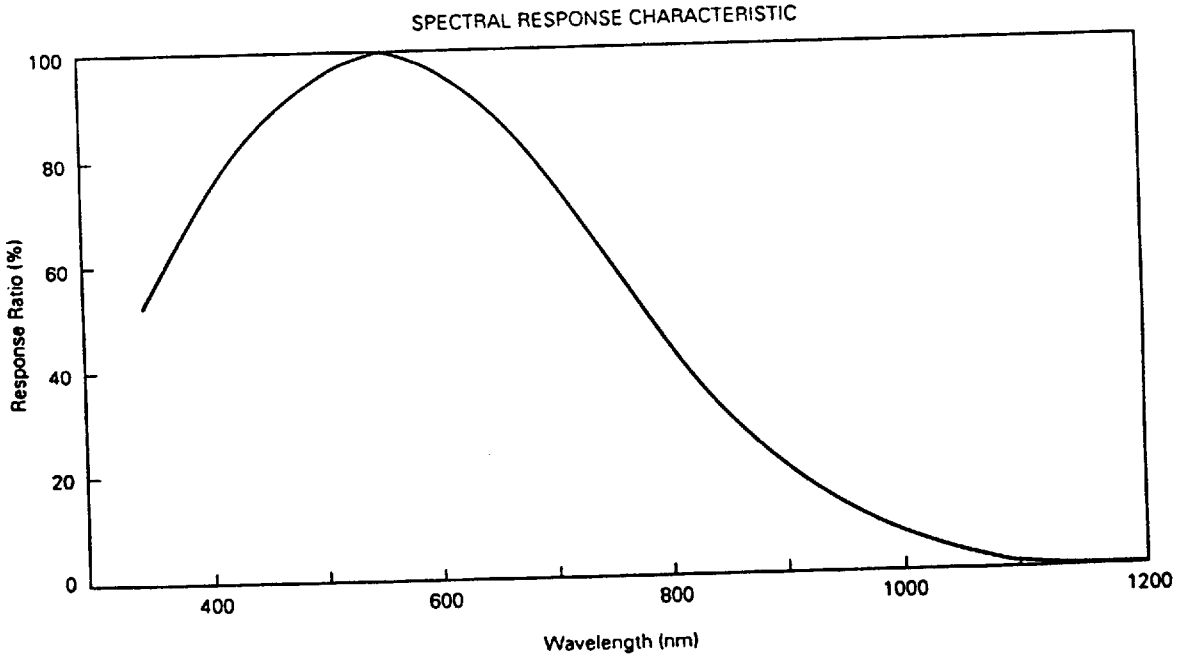
DARK OUTPUT TEMPERATURE CHARACTERISTIC



STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC



SPECTRAL RESPONSE CHARACTERISTIC



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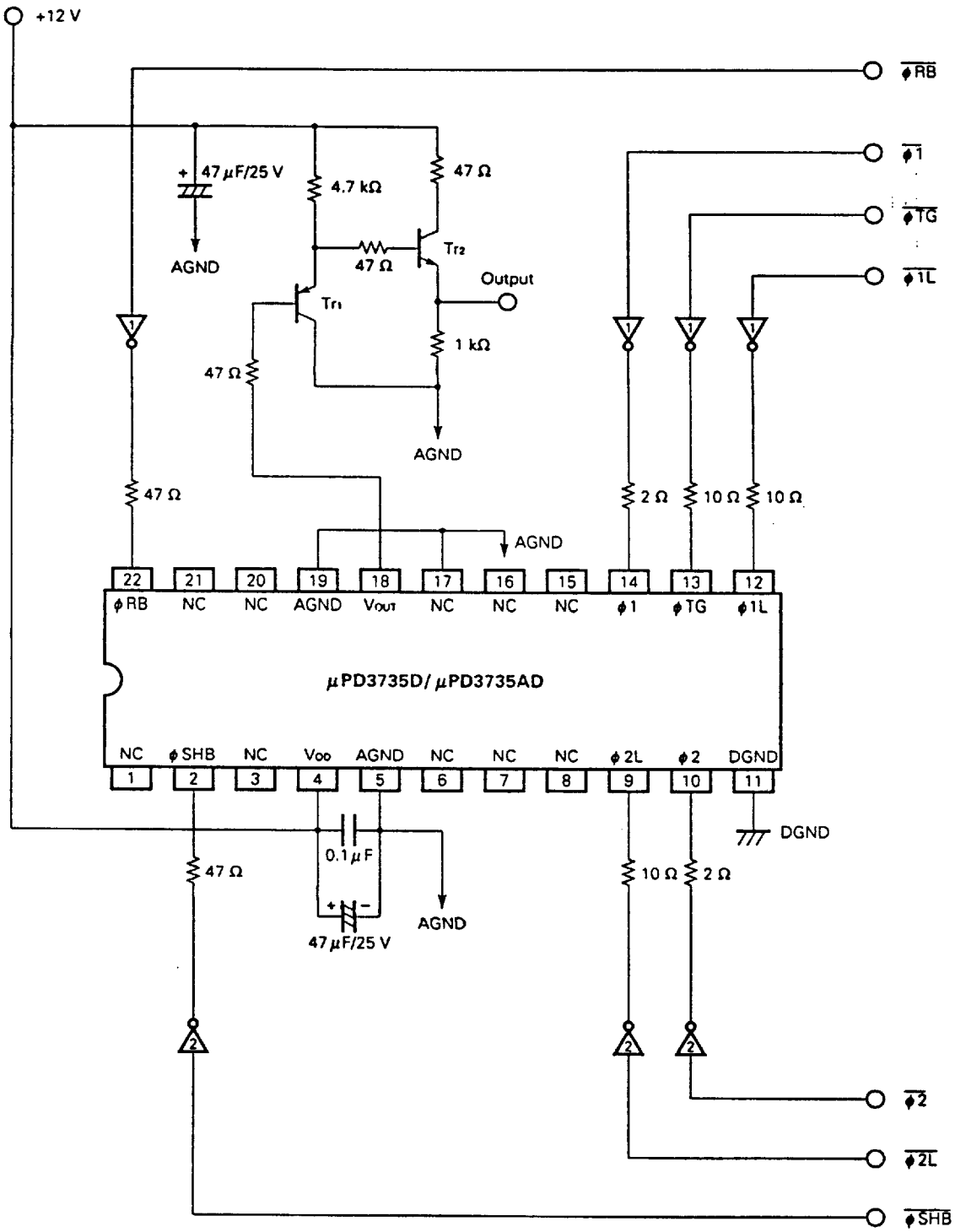
APPLICATION EXAMPLE



1. 74AC04 Tr_1 2SA733
2. 74AC04 Tr_2 2SC945

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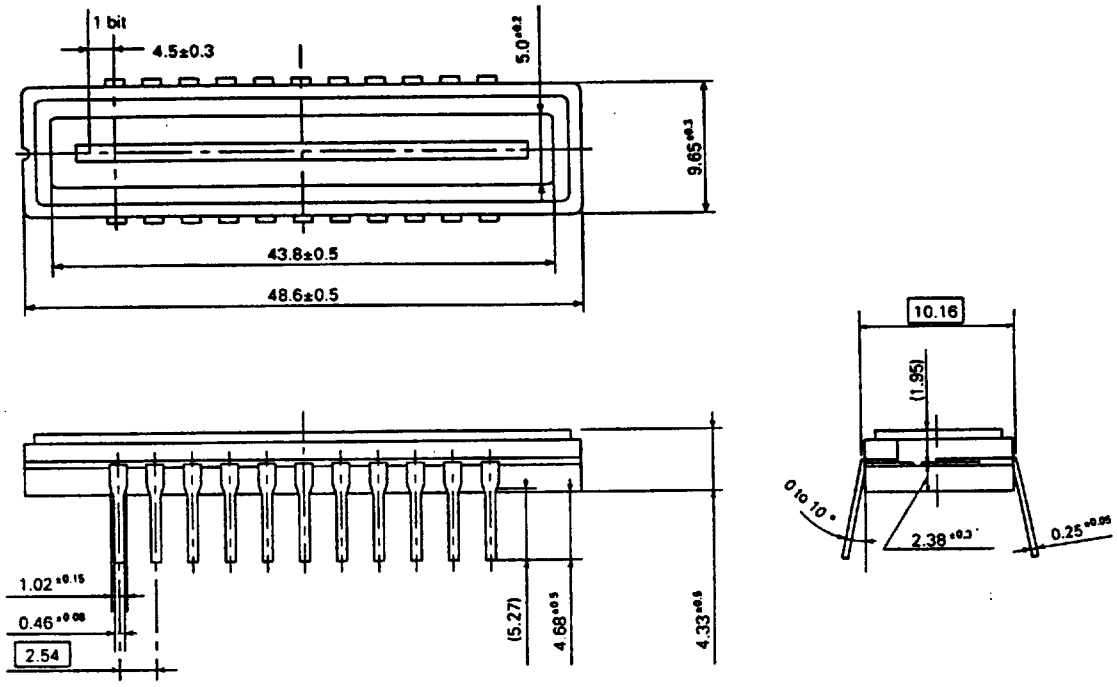
PACKAGE DIMENSIONS (Unit: mm)



Name	Dimensions	Refractive index
Glass cap	47.5 x 9.25 x 0.7	1.5

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RECOMMENDED SOLDERING CONDITIONS ★

The following conditions (see table below) must be met when soldering this product.
For more details, refer to our document "SEMICONDUCTOR DEVICE TECHNOLOGY MANUAL" (IEI-1207).
Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 1 Type of Through Hole Device

μPD3735, 3735A: 22-pin ceramic DIP (CERDIP) (400 mil)

Soldering process	Soldering conditions
Wave soldering (Only lead part)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Partial heating method	Pin temperature: 260 °C or below, Time: 10 seconds or below

Caution Do not jet molten solder on the surface of package.

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