

SANYONo. $\times$ 5084**LC322270J, M-80****2 MEG (131072 words $\times$ 16 bits) DRAM
Fast Page Mode, Byte Write****Preliminary****Overview**

The LC322270J, M is a CMOS dynamic RAM operating on a single 5 V power source and having a 131072 words $\times$ 16 bits configuration. Equipped with large capacity capabilities, high speed transfer rates and low power dissipation, this series is suited for a wide variety of applications ranging from computer main memory and expansion memory to commercial equipment.

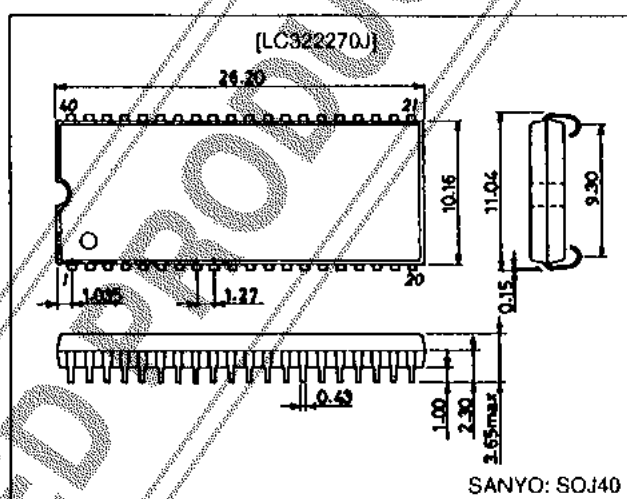
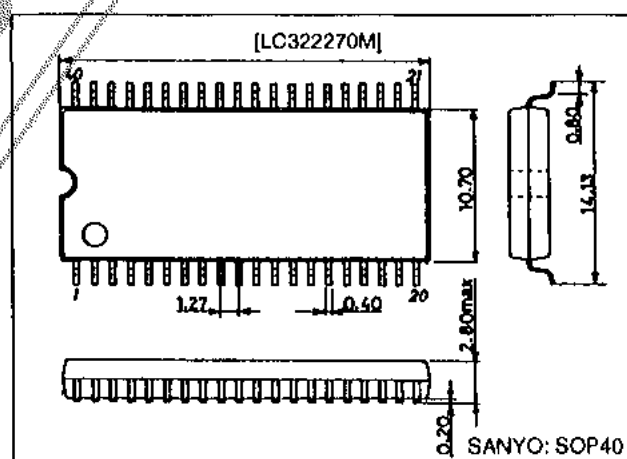
Address input utilizes a multiplexed address bus which permits it to be enclosed in a compact plastic package of 40-pin SOJ and 40-pin SOP. Refresh rates are within 8 ms with 512 row address (A0 to A7, A8R) selection and support Row Address Strobe (RAS)-only refresh, Column Address Strobe (CAS)-before-RAS refresh and hidden refresh settings. There are functions such as fast page mode, read-modify-write and byte write. The pin assignment follows the JEDEC 4M DRAM (262144 words $\times$ 16 bits, 1CAS/2WE type) standard pinouts.

Features

- 131072 words $\times$ 16 bits configuration.
- Single 5 V $\pm$ 10% power supply.
- All input and output (I/O) TTL compatible.
- Supports fast page mode, read-modify-write and byte write.
- Supports output buffer control using early write and Output Enable (OE) control.
- 8 ms refresh using 512 refresh cycles.
- Supports RAS-only refresh, CAS-before-RAS refresh and hidden refresh.
- Follows the JEDEC 4M DRAM (262144 words $\times$ 16 bits, 1CAS/2WE type) standard pinouts.
- Package:
40-pin SOJ plastic package (400 mil): LC322270J
40-pin SOP plastic package (525 mil): LC322270M
- RAS access time/cycle time/power dissipation.
- RAS access time/column address access time/CAS access time/cycle time/power dissipation.

Package Dimensions

unit: mm

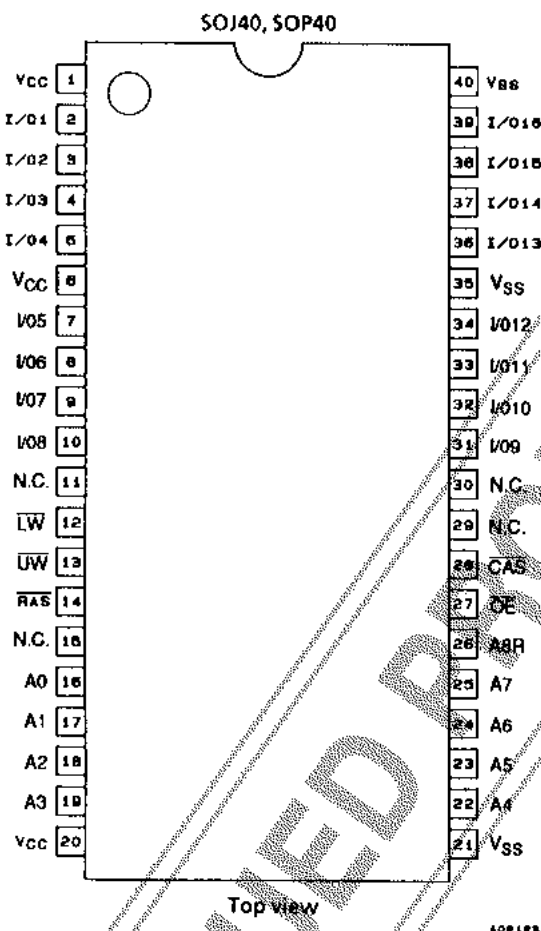
3200-SOJ40**3195-SOP40**

Parameter		LC322270J, M-80
RAS access time		80 ns
Column address access time		45 ns
CAS access time		30 ns
Cycle time		150 ns
Power dissipation (max.)	During operation	633 mW
	During standby	5.5 mW (CMOS level)/11 mW (TTL level)

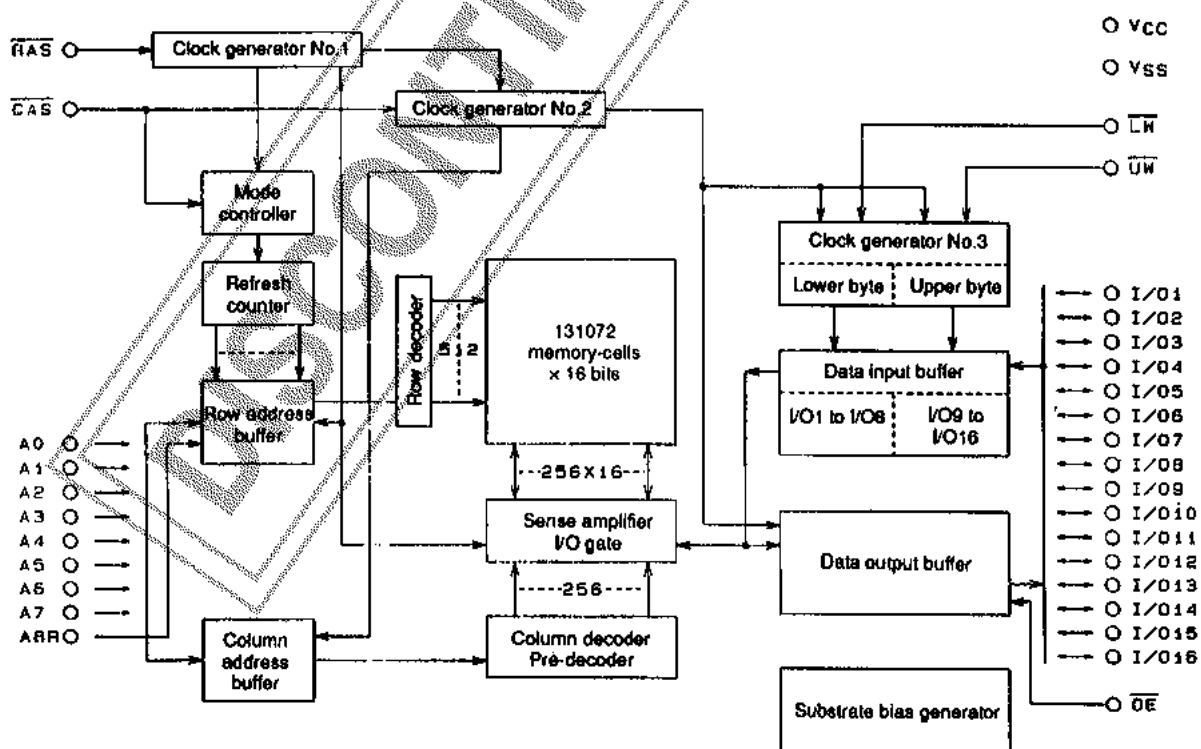
SANYO Electric Co., Ltd. Semiconductor Business Headquarters

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Pin Assignment



Block Diagram



Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Maximum supply voltage	$V_{CC\ max}$	-1.0 to +7.0	V	1
Input voltage	V_{IN}	-1.0 to +7.0	V	1
Output voltage	V_{OUT}	-1.0 to +7.0	V	1
Operating temperature range	T_{opr}	0 to +70	°C	1
Storage temperature range	T_{stg}	-55 to +150	°C	1
Allowable power dissipation	$P_d\ max$	700	mW	1
Output short-circuit current	I_{OUT}	50	mA	1

Note: 1. Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at $T_a = 0$ to +70°C

Parameter	Symbol	min	typ	max	Unit	Note
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	2
Input high level voltage	V_{IH}	2.4		6.5	V	2
Input low level voltage (A0 to A7, A8R, RAS, CAS, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	V_{IL}	-1.0*1		+0.8	V	2
Input low level voltage (I/O1 to I/O16)	V_{IL}	-0.5*1		+0.8	V	2

Note: 2. All voltages are referenced to V_{SS} .

*1: -2.0 V when pulse width is less than 20 ns.

DC Electrical Characteristics at $T_a = 0$ to +70°C, $V_{CC} = 5\ V \pm 10\%$

Parameter	Symbol	Conditions	min	max	Unit	Note
Operating current (Average current during operation)	I_{CC1}	RAS, CAS, address cycling; $I_{RC} = I_{RC\ min}$		115	mA	3, 4, 5
Standby current	I_{CC2}	RAS = CAS = V_{IH}		2	mA	
RAS-only refresh current	I_{CC3}	RAS cycling, CAS = V_{IH} ; $I_{RC} = I_{RC\ min}$		115	mA	3, 5
Fast page mode current	I_{CC4}	RAS = V_{IL} , CAS, address cycling; $I_{RC} = I_{RC\ min}$		90	mA	3, 4, 5
Standby current	I_{CC5}	RAS = CAS = $V_{CC} - 0.2\ V$		1	mA	
CAS-before-RAS refresh current	I_{CC6}	RAS, CAS cycling; $I_{RC} = I_{RC\ min}$		115	mA	3
Input leakage current	I_{IL}	0 V < V_{IN} < 6.5 V, pins other than test pin = 0 V	-10	+10	μA	
Output leakage current	I_{OL}	$\overline{D_{OUT}}$ disable, 0 V < V_{OUT} < 6.5 V	-10	+10	μA	
Output high level voltage	V_{OH}	$I_{OUT} = -2.5\ mA$	2.4		V	
Output low level voltage	V_{OL}	$I_{OUT} = 2.1\ mA$		0.4	V	

Note: 3. All current values are measured at minimum cycle rate. Since current flows immoderately, if cycle time is longer than shown here, current value becomes smaller.

4. I_{CC1} and I_{CC4} are dependent on output loads. Maximum values for I_{CC1} and I_{CC4} represent values with output open.

5. Address change is less than or equal to one time during RAS = V_{IL} . Concerning I_{CC4} , it is less than or equal to one time during 1 cycle (t_{PC}).

AC Electrical Characteristics at $T_a = 0$ to +70°C, $V_{CC} = 5\ V \pm 10\%$ (Notes 6, 7 and 8)

Parameter	Symbol	min	max	Unit	Note
Random read, write cycle time	t_{RC}	150		ns	
Read-write/read-modify-write cycle time	t_{RWC}	200		ns	
Fast page mode cycle time	t_{PC}	55		ns	
Fast page mode read-write/read-modify-write cycle time	t_{PRWC}	100		ns	
RAS access time	t_{RAC}		80	ns	9, 14, 15
CAS access time	t_{CAC}		30	ns	9, 14
Column address access time	t_{AA}		45	ns	9, 15
CAS precharge access time	t_{CPA}		50	ns	9
Output low-impedance time from CAS low	t_{CLZ}	0		ns	9
Output buffer turn-off delay time	t_{OFF}	0	20	ns	10
Rise, fall time	t_T	3	50	ns	
RAS precharge time	t_{RP}	60		ns	
RAS pulse width	t_{RAS}	80	10000	ns	
RAS pulse width for fast page mode cycle only	t_{RASp}	80	100000	ns	

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Parameter	Symbol	min	max	Unit	Note
RAS hold time	t_{RSH}	30		ns	
CAS hold time	t_{CSH}	80		ns	
CAS pulse width	t_{CAS}	30	10000	ns	
RAS to CAS delay time	t_{RCD}	25	50	ns	14
RAS to column address delay time	t_{RAD}	17	35	ns	15
CAS to RAS precharge time	t_{CRP}	10		ns	
CAS precharge time	t_{CP}	10		ns	
Row address setup time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	12		ns	
Column address setup time	t_{ASC}	0		ns	
Column address hold time	t_{CAH}	20		ns	
Column address hold time referenced to RAS	t_{AR}	60		ns	
Column address to RAS lead time	t_{RAL}	45		ns	
Read command setup time	t_{RCS}	0		ns	
Read command hold time referenced to CAS	t_{RCH}	0		ns	11
Read command hold time referenced to RAS	t_{RRH}	0		ns	11
Write command hold time	t_{WCH}	15		ns	
Write command hold time referenced to RAS	t_{WCR}	60		ns	
Write command pulse width	t_{WP}	15		ns	
Write command to RAS lead time	t_{RWL}	25		ns	
Write command to CAS lead time	t_{CWL}	20		ns	
Data input setup time	t_{DS}	0		ns	12
Data input hold time	t_{DH}	20		ns	12
Data input hold time referenced to RAS	t_{DHR}	60		ns	
Refresh time	t_{REF}		8	ms	
Write command setup time	t_{WCS}	0		ns	13
CAS to UW, LW delay time	t_{CWO}	50		ns	13
RAS to UW, LW delay time	t_{RWO}	100		ns	13
Column address to UW, LW delay time	t_{AWO}	65		ns	13
CAS precharge UW, LW delay time for last page mode cycle only	t_{CPWD}	70		ns	13
CAS setup time for CAS-before-RAS	t_{CSR}	10		ns	
CAS hold time for CAS-before-RAS	t_{CHR}	15		ns	
RAS precharge CAS active time	t_{RPC}	10		ns	
CAS precharge time for CAS-before-RAS counter test	t_{CPT}	40		ns	
RAS hold time referenced to OE	t_{ROH}	15		ns	
OE access time	t_{OEA}		25	ns	9
OE delay time	t_{OED}	15		ns	
OE output buffer turn-off delay time	t_{OEZ}	0	15	ns	10
OE command hold time	t_{OEH}	20		ns	
Data input to CAS delay time	t_{DZC}	0		ns	16
Data input to OE delay time	t_{DZO}	0		ns	16
Masked write setup time	t_{MCS}	0		ns	
Masked write hold time referenced to RAS	t_{MRH}	0		ns	
Masked write hold time referenced to CAS	t_{MCH}	0		ns	

Input/Output Capacitance at $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5\text{ V} \pm 10\%$

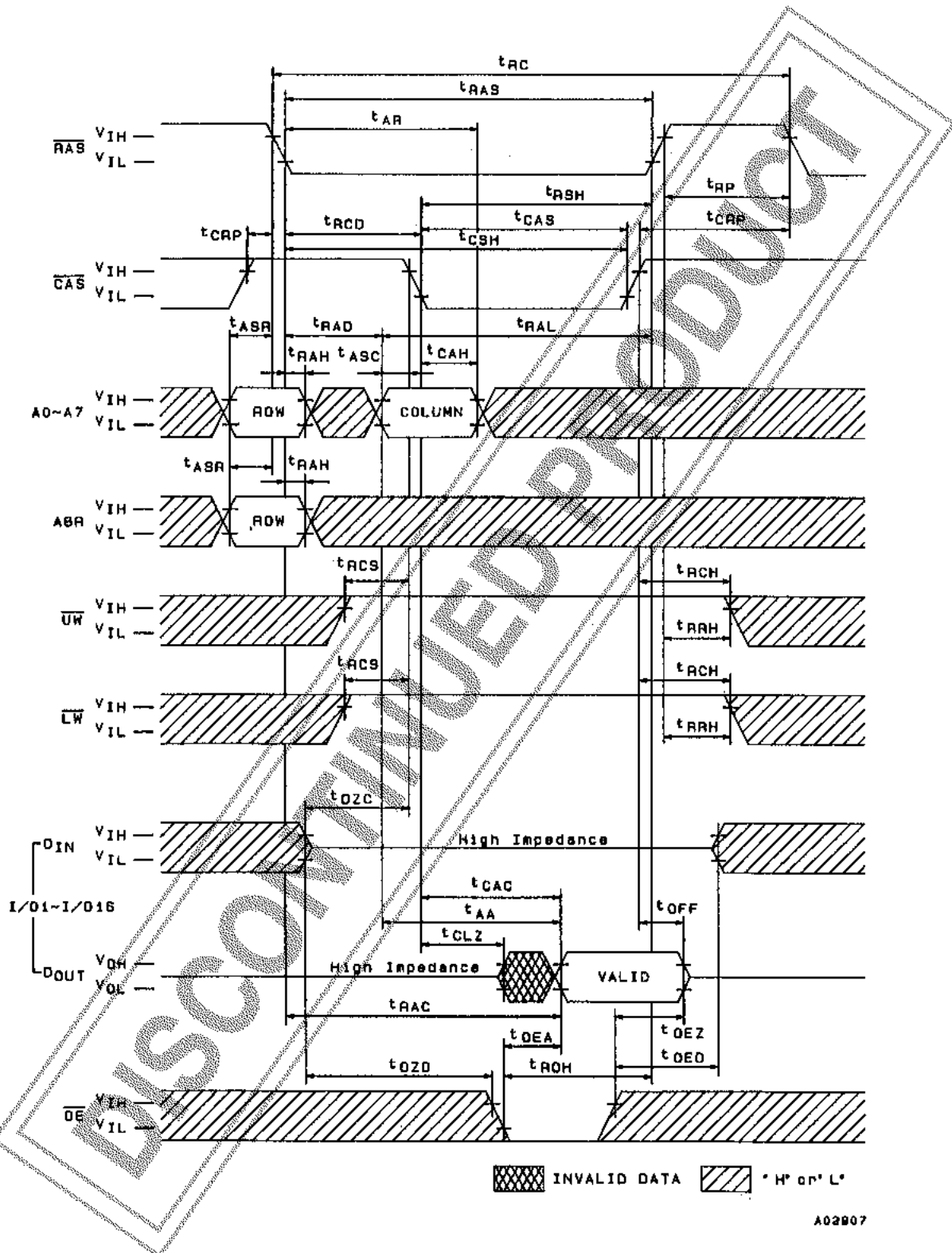
Parameter	Symbol	min	max	Unit	Note
Input capacitance (A0 to A7, ABR, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{UW}}$, $\overline{\text{LW}}$, $\overline{\text{OE}}$)	C_{IN}		7	pF	
Input/Output capacitance (VO1 to VO16)	C_{VO}		7	pF	

- Note:
6. An initial pause of 200 μs is required after power-up followed by eight $\overline{\text{RAS}}$ -only refresh cycles before proper device operation is achieved. In case of using refresh counter, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles instead of eight $\overline{\text{RAS}}$ -only refresh cycles are required.
 7. Measured at $t_T = 5\text{ ns}$.
 8. When measuring input signal timing, V_{IH} (min) and V_{IL} (max) are used for reference points. In addition, rise and fall time are defined between V_{IH} and V_{IL} .
 9. Measured using an equivalent of 50 pF and one standard TTL loads.
 10. t_{OFF} (max) and t_{OEZ} (max) are defined as the time until output voltage can no longer be measured when output switches to a high impedance condition.
 11. Operation is guaranteed if either t_{RRH} or t_{RCH} is satisfied.
 12. These parameters are measured from the falling edge of $\overline{\text{CAS}}$ for an early-write cycle, and from the falling edge of $\overline{\text{UW}}$ and $\overline{\text{LW}}$ for a read-write/read-modify-write cycle.
 13. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters for memory in that they specify the operating mode. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle switches to an early-write cycle and output pins switch to high impedance throughout the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$ for fast page mode cycle only, the cycle switches to a read-write/read-modify-write cycle and data output equal information in the selected cells. If neither of the above timings are satisfied, output pins are in an undefined state.
 14. t_{ACD} (max) is not a restrictive operating parameter but instead represents the point at which the access time t_{RAC} (max) is guaranteed. If $t_{\text{ACD}} \geq t_{\text{ACD}}(\text{max})$, access time is determined according to t_{CAC} .
 15. t_{RAD} (max) is not a restrictive operating parameter but instead represents the point at which the access time t_{RAC} (max) is guaranteed. If $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$, access time is determined according to t_{AA} .
 16. Operation is guaranteed if either t_{QZC} or t_{QZO} is satisfied.

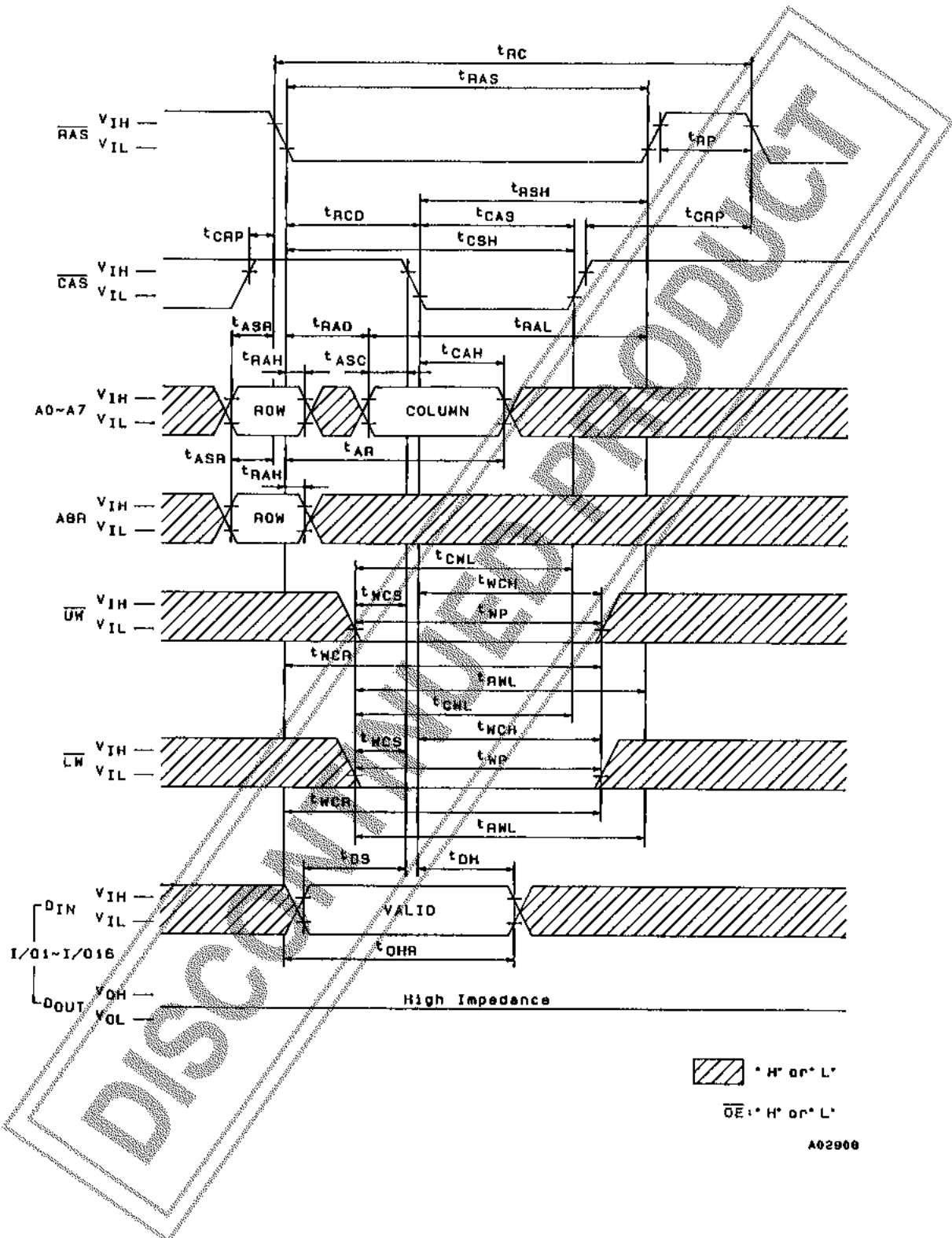
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Timing Chart

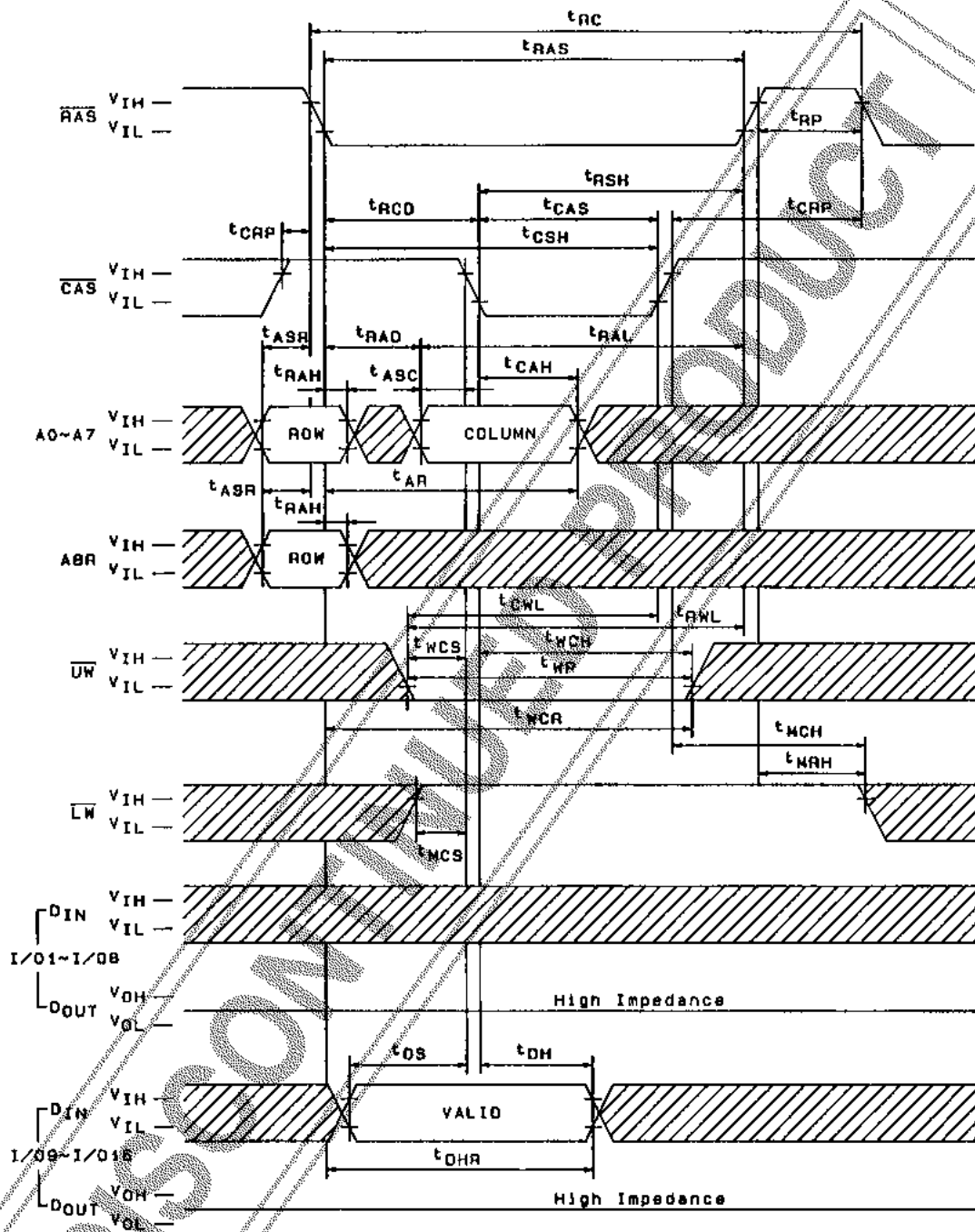
Read Cycle



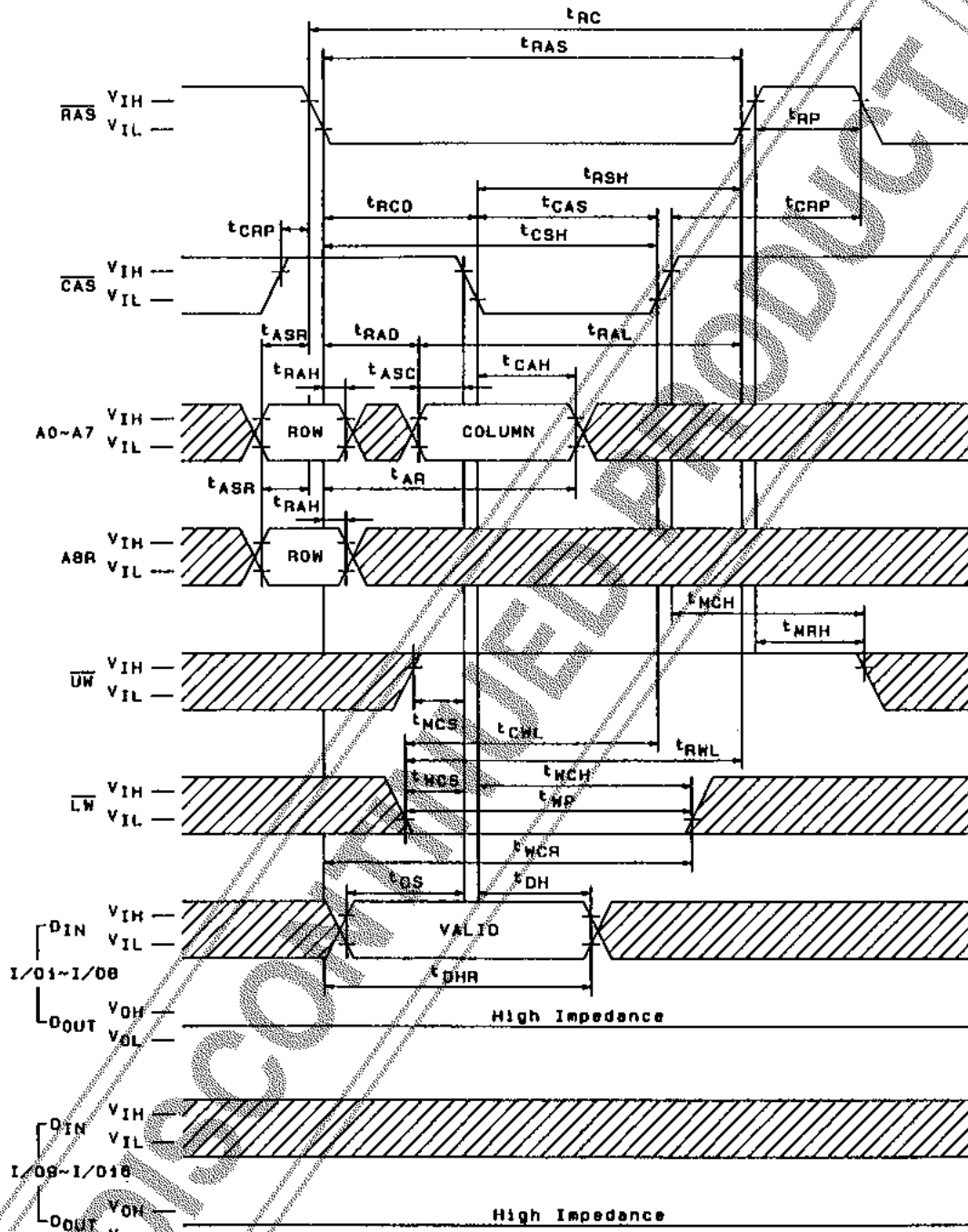
Early Write Cycle



Upper Byte Early Write Cycle



Lower Byte Early Write Cycle

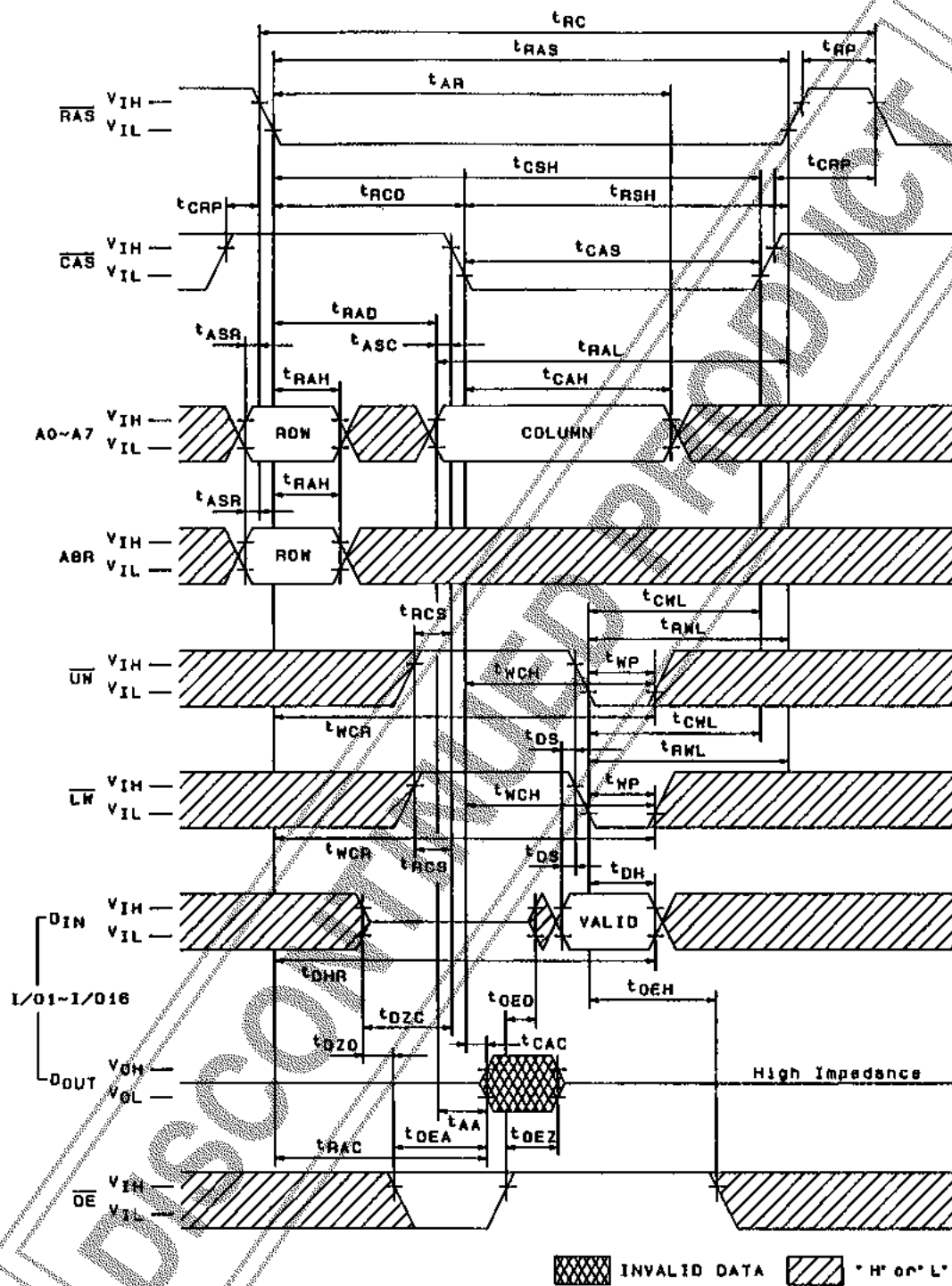


 * H* or * L*

$\overline{DE} \perp H^{\circ} \text{ or } L^{\circ}$

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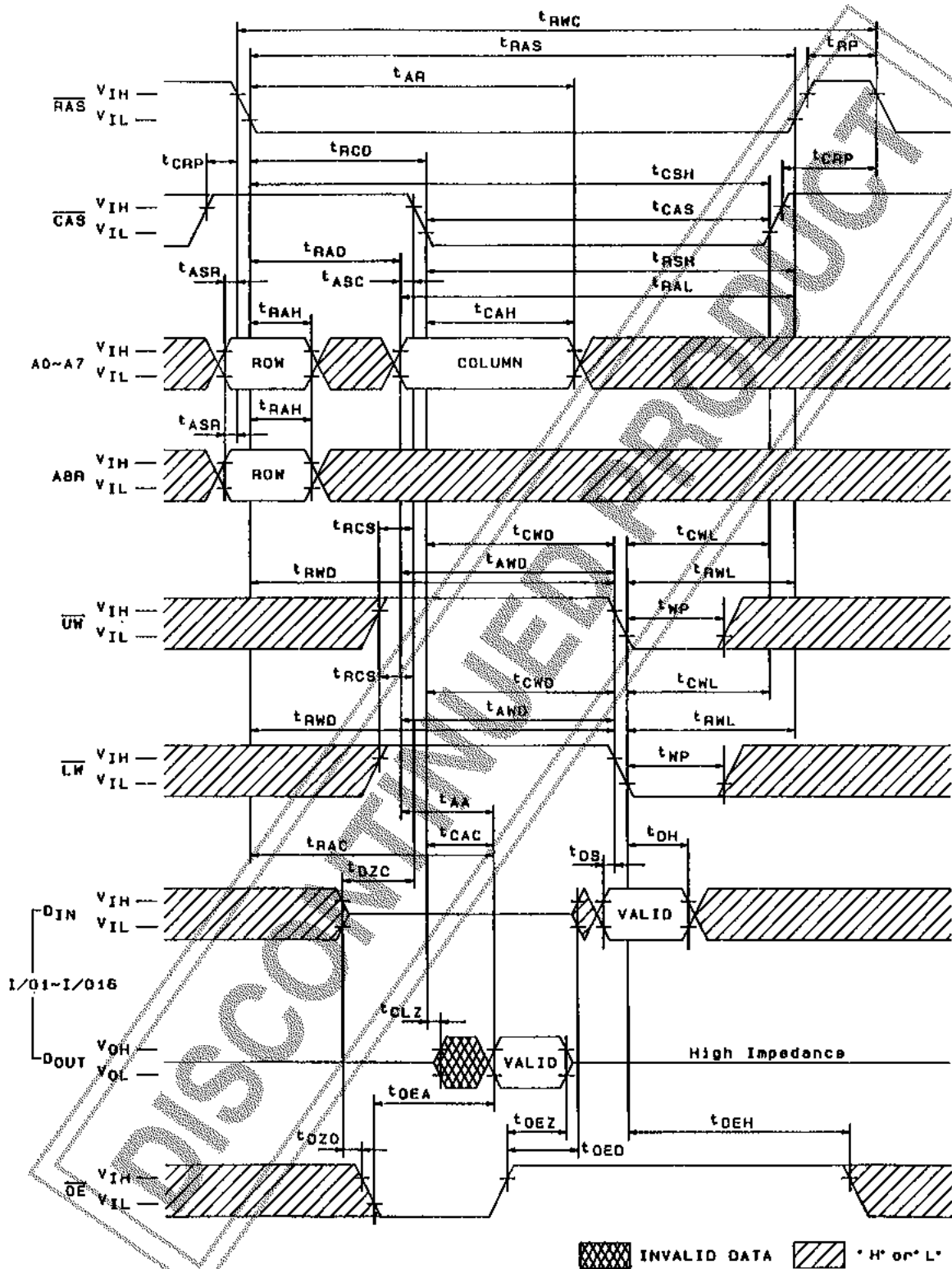
Write Cycle ($\overline{\text{OE}}$ Control)



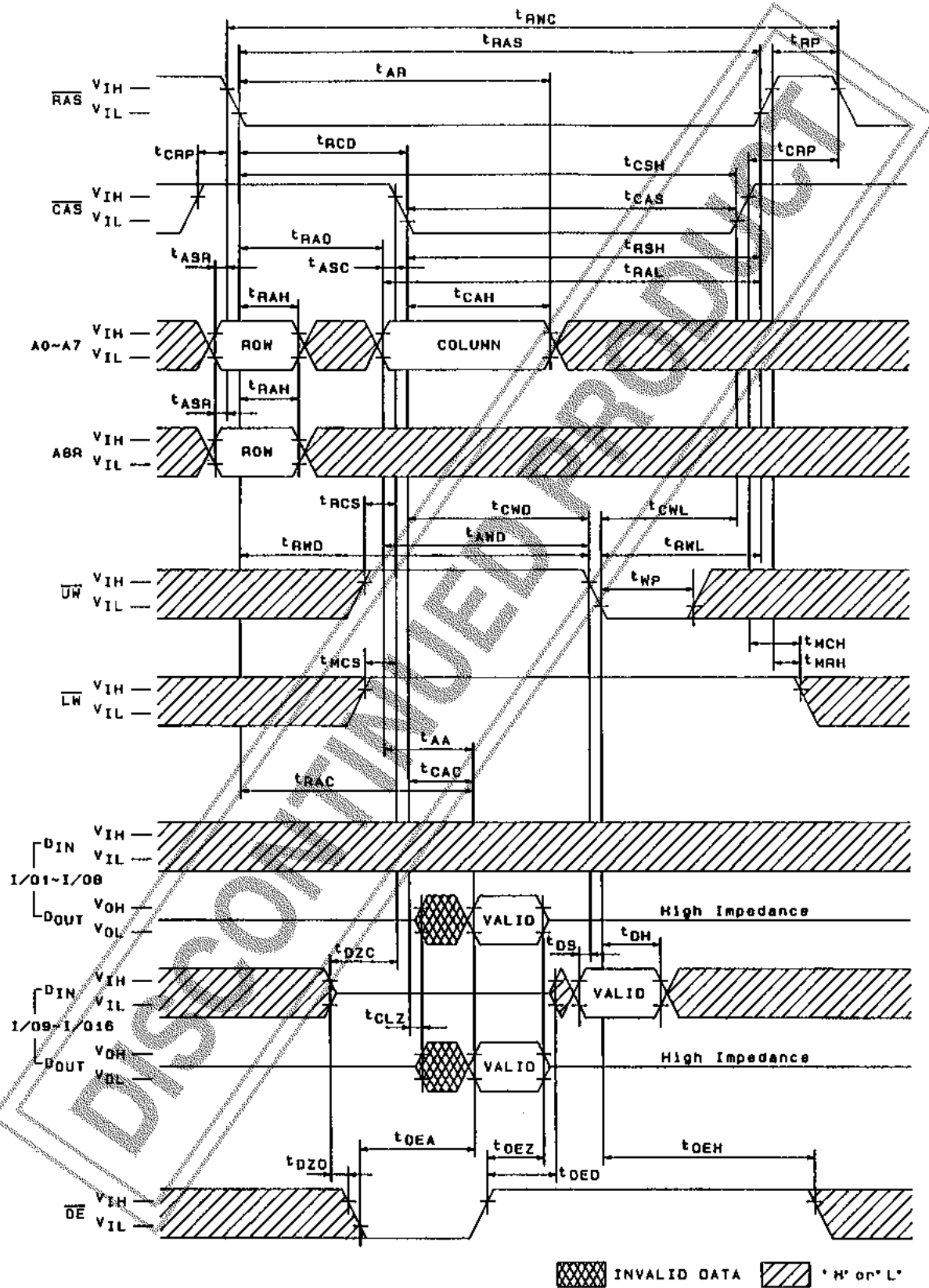
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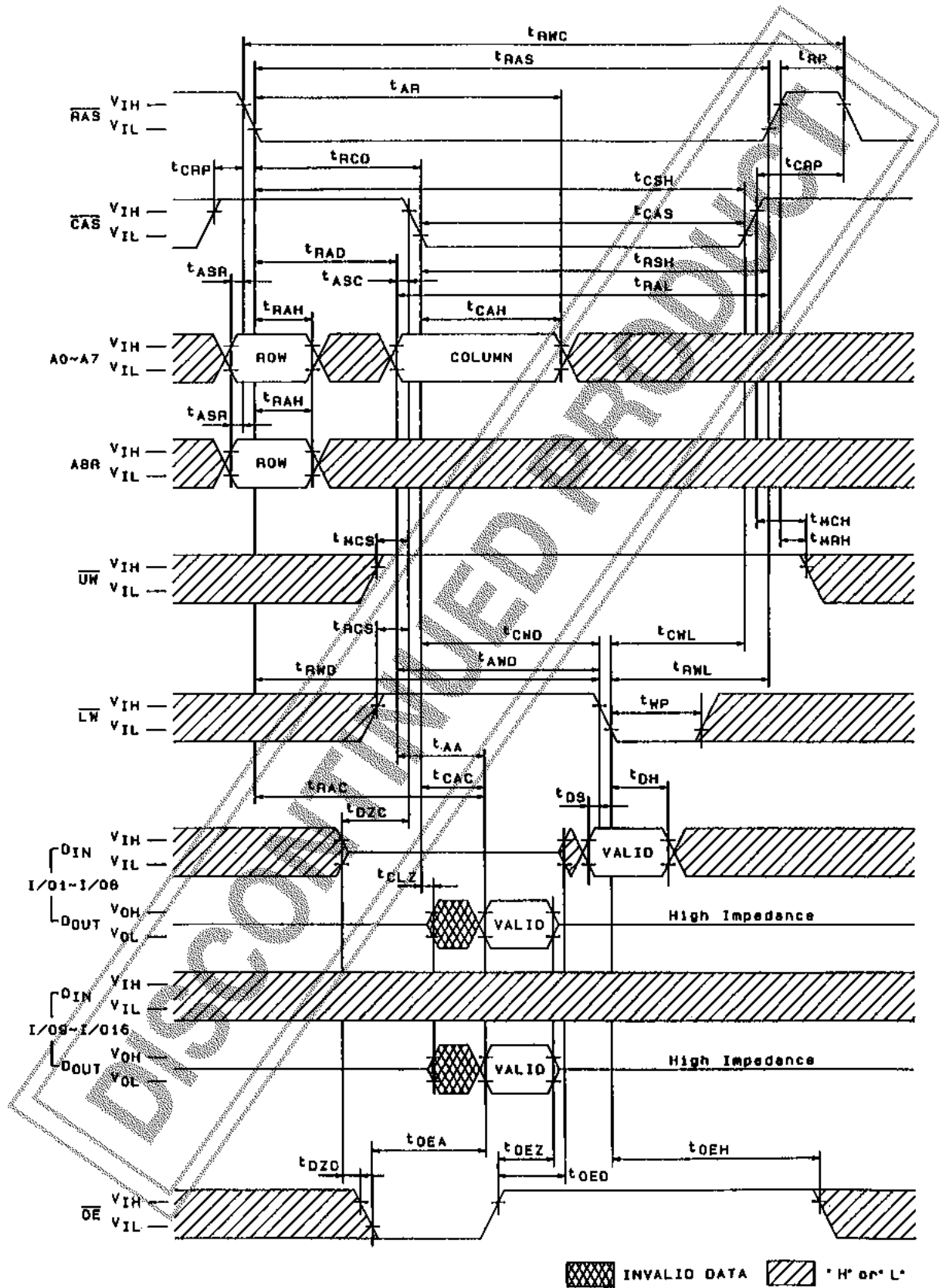
Read-Modify Write Cycle



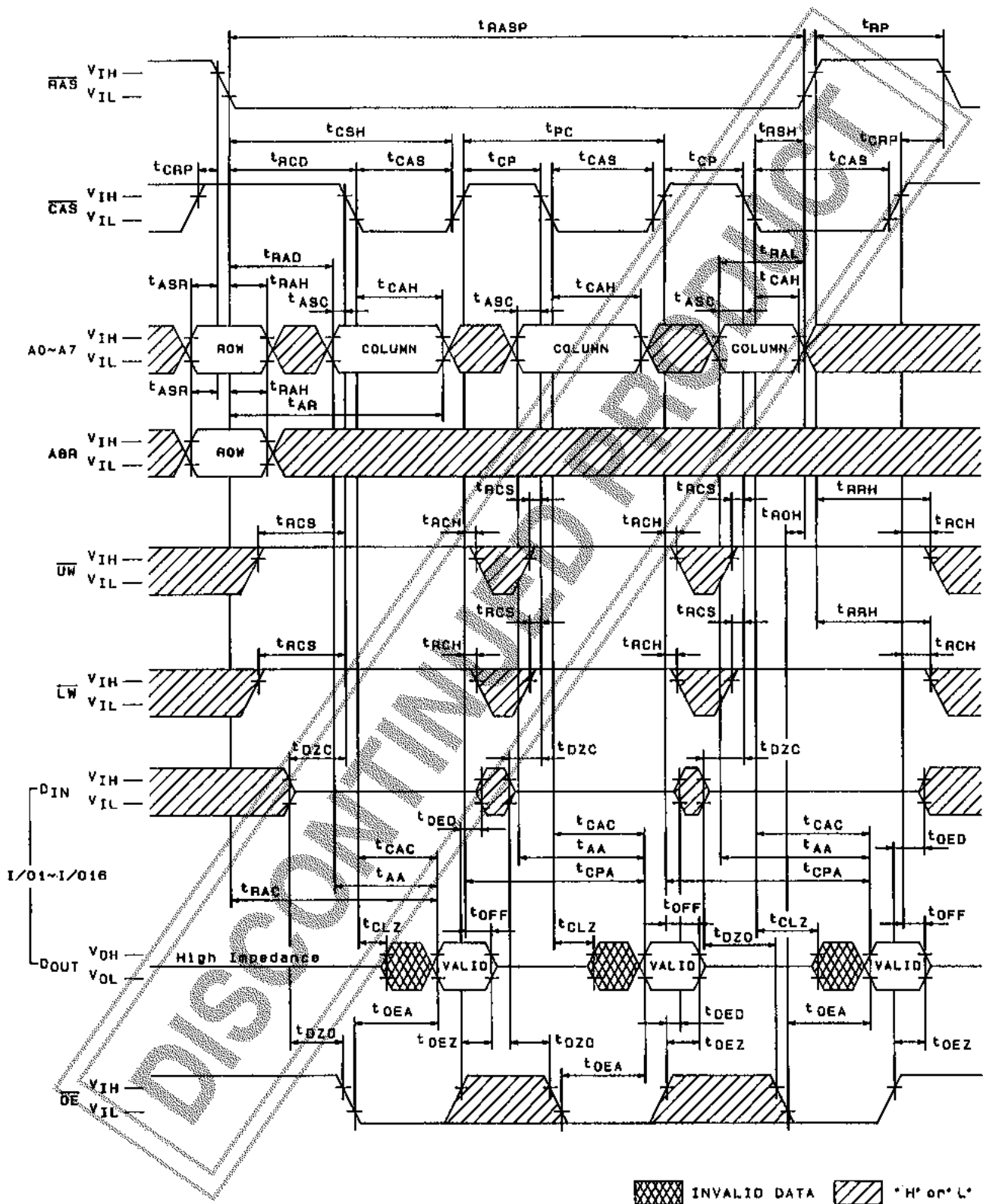
Read-Modify Upper Byte Write Cycle

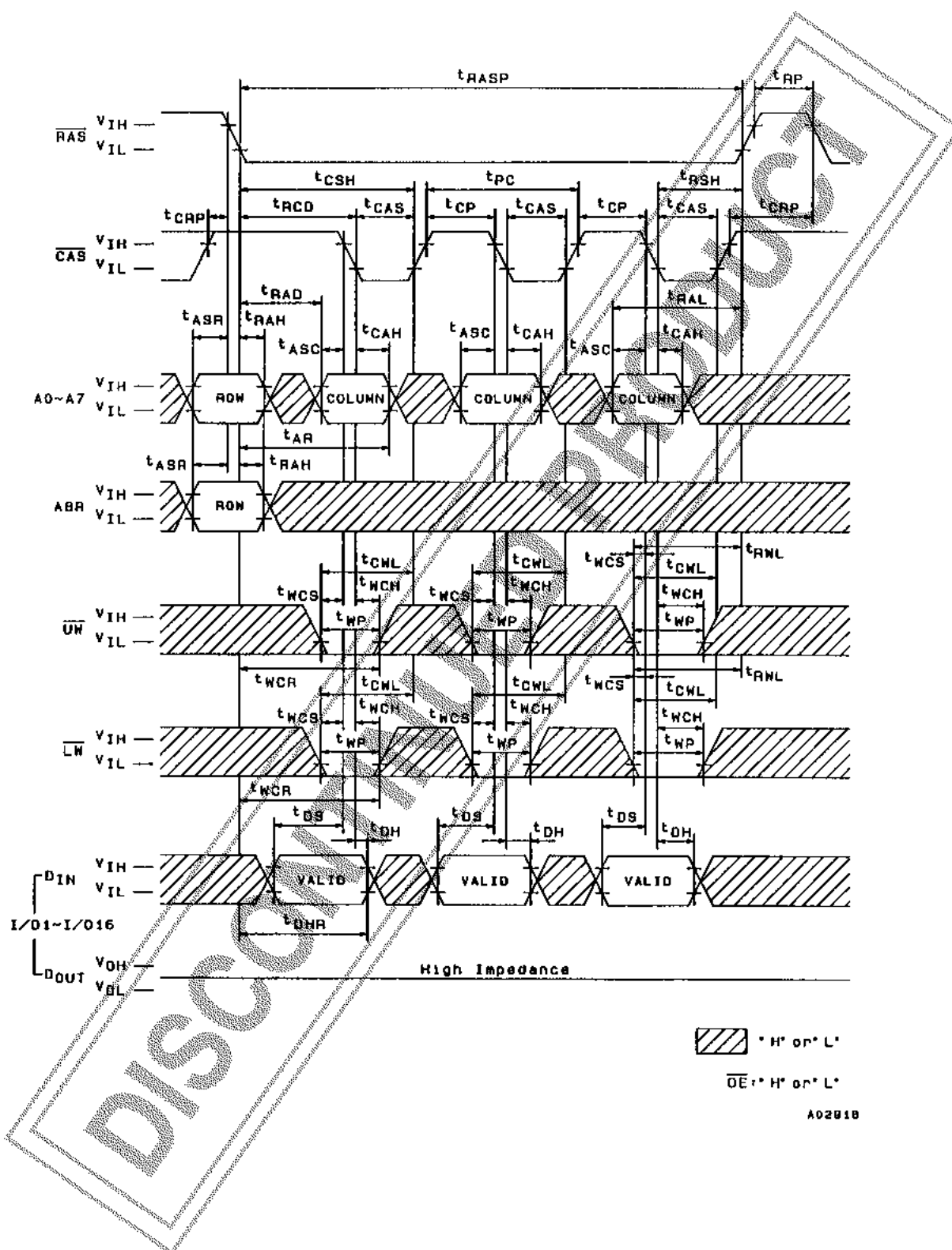


Read-Modify Lower Byte Write Cycle

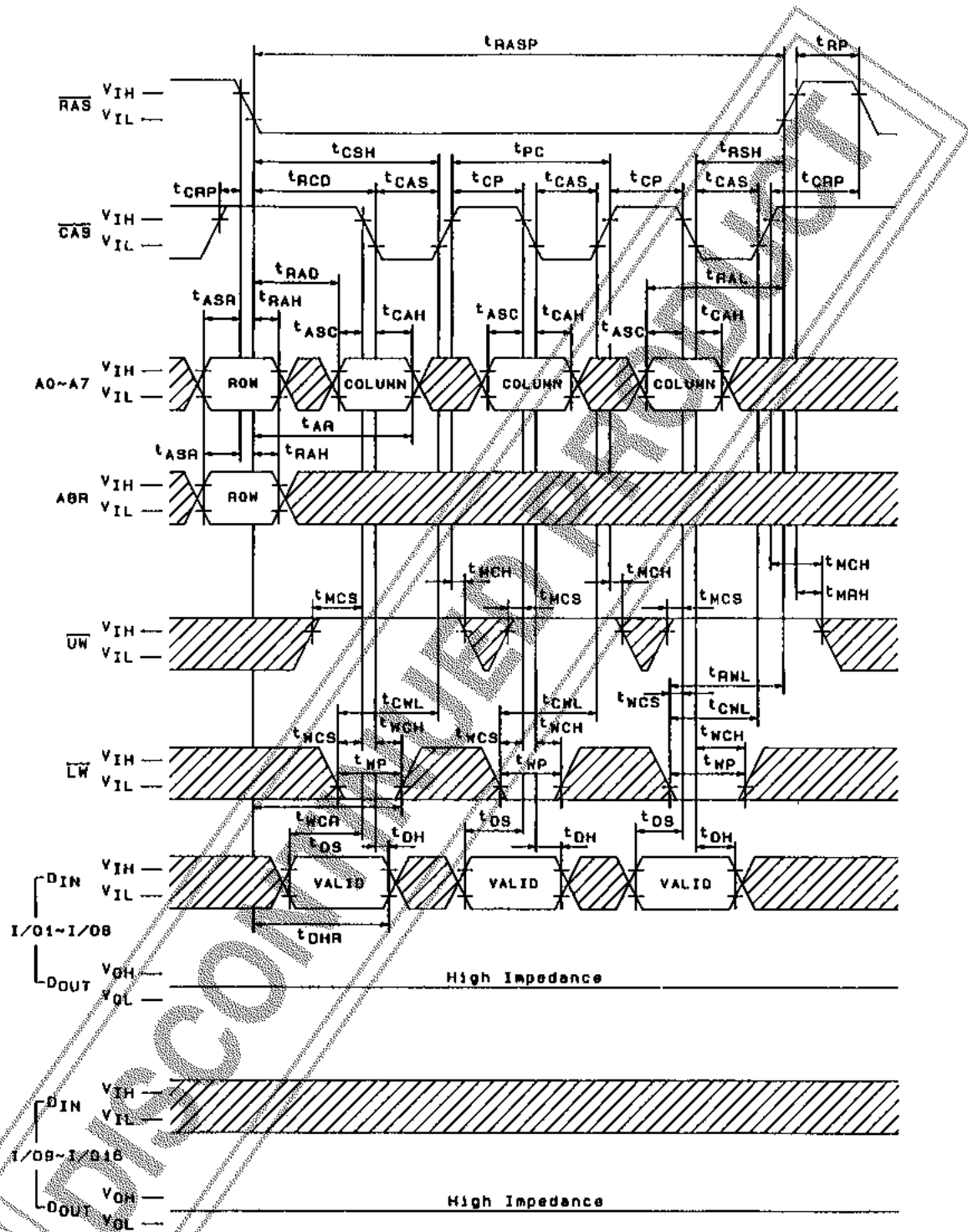


Fast Page Mode Read Cycle





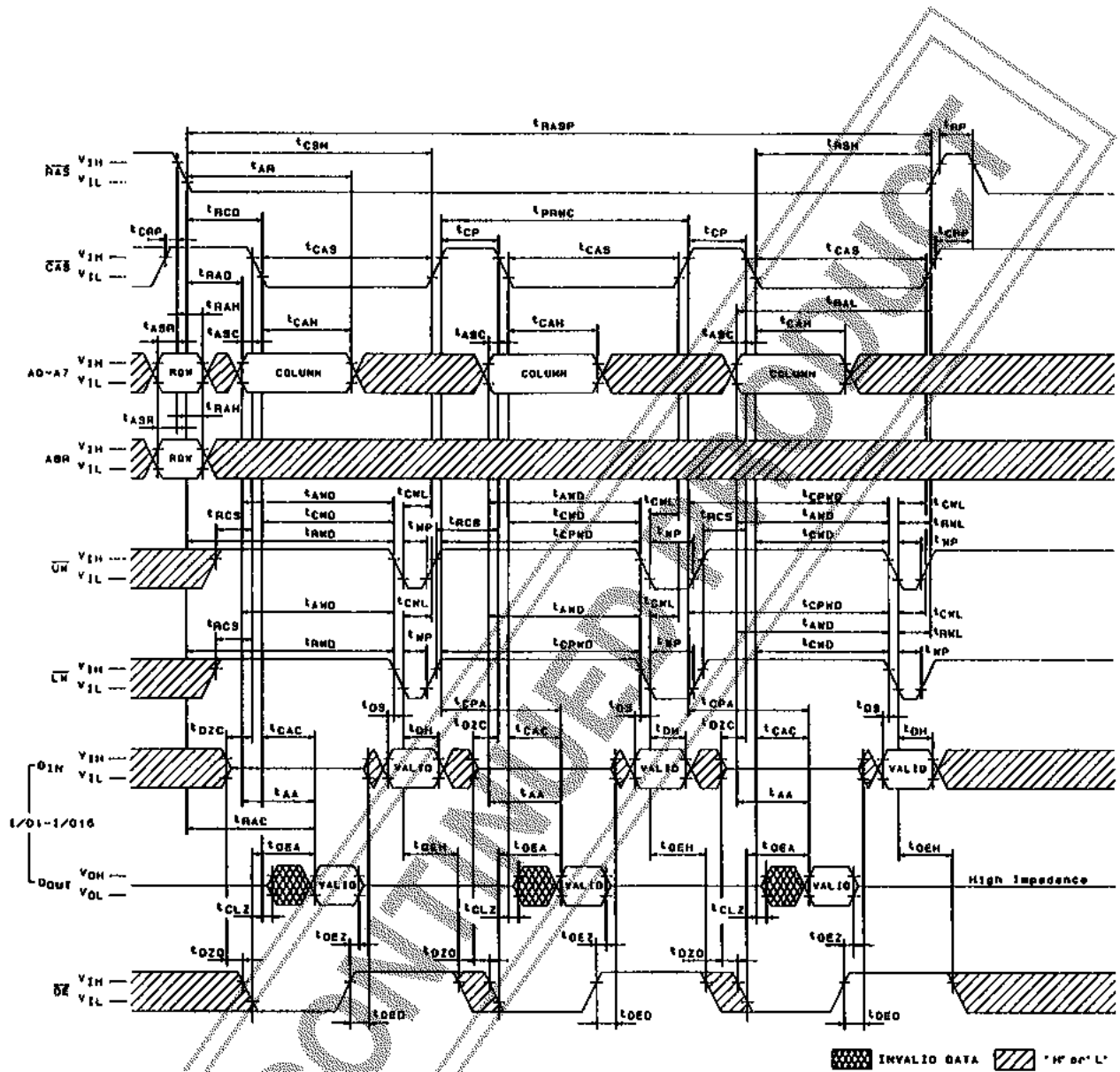
Fast Page Mode Lower Byte Early Write Cycle



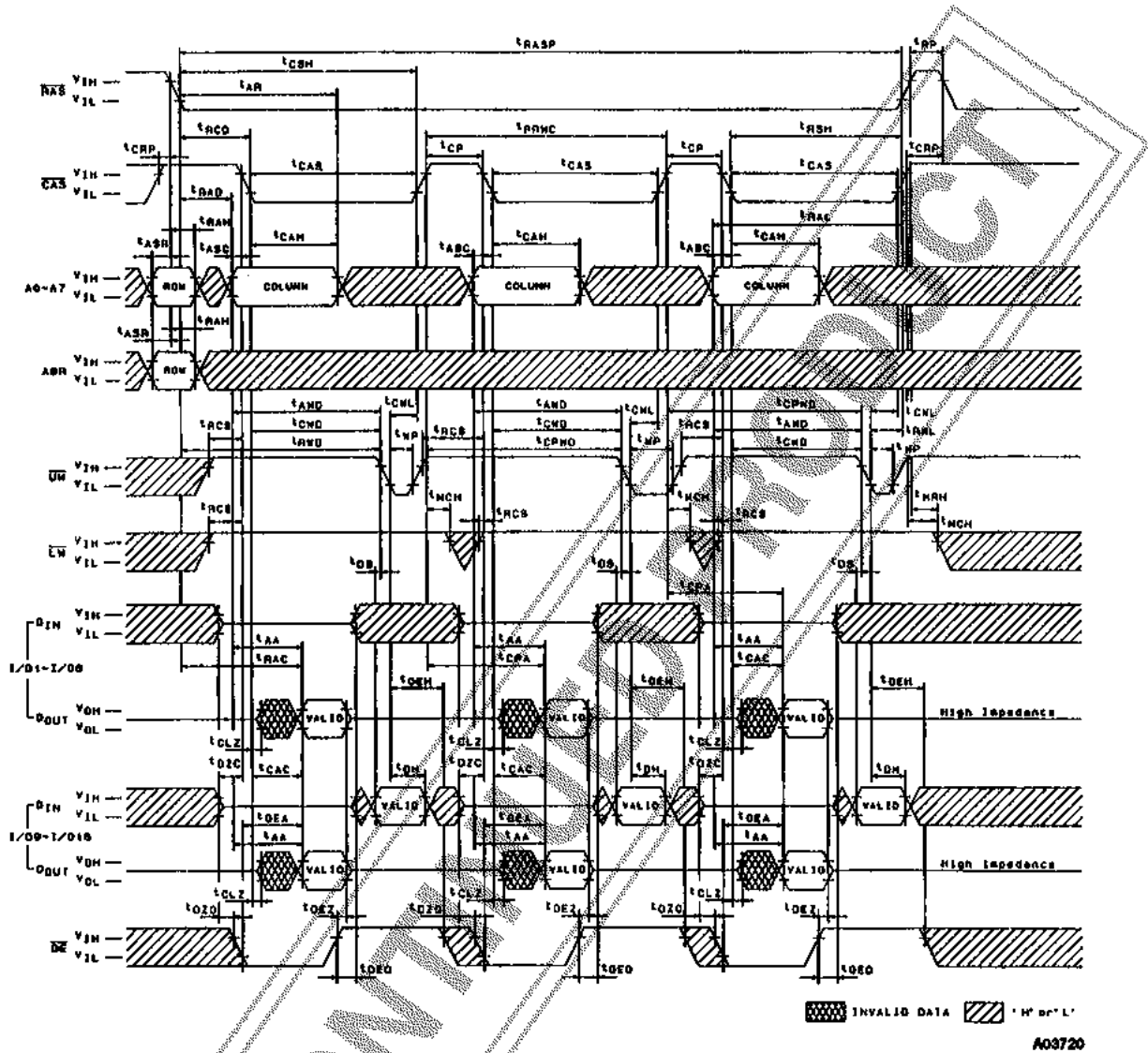
• H* or* L*

OE: H* or* L*

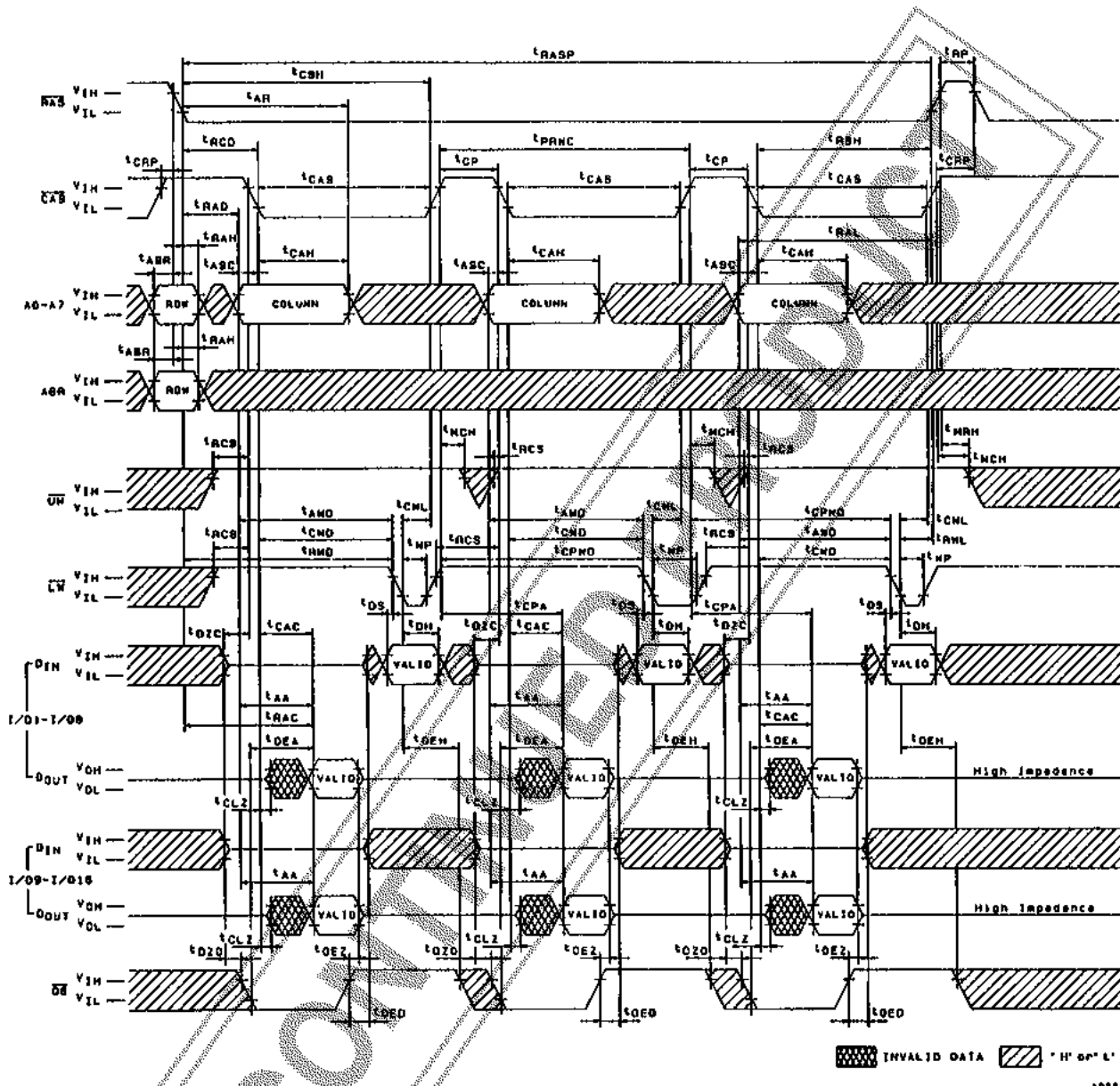
Fast Page Mode Read-Modify-Write Cycle



Fast Page Mode Read-Modify Upper Byte Write Cycle

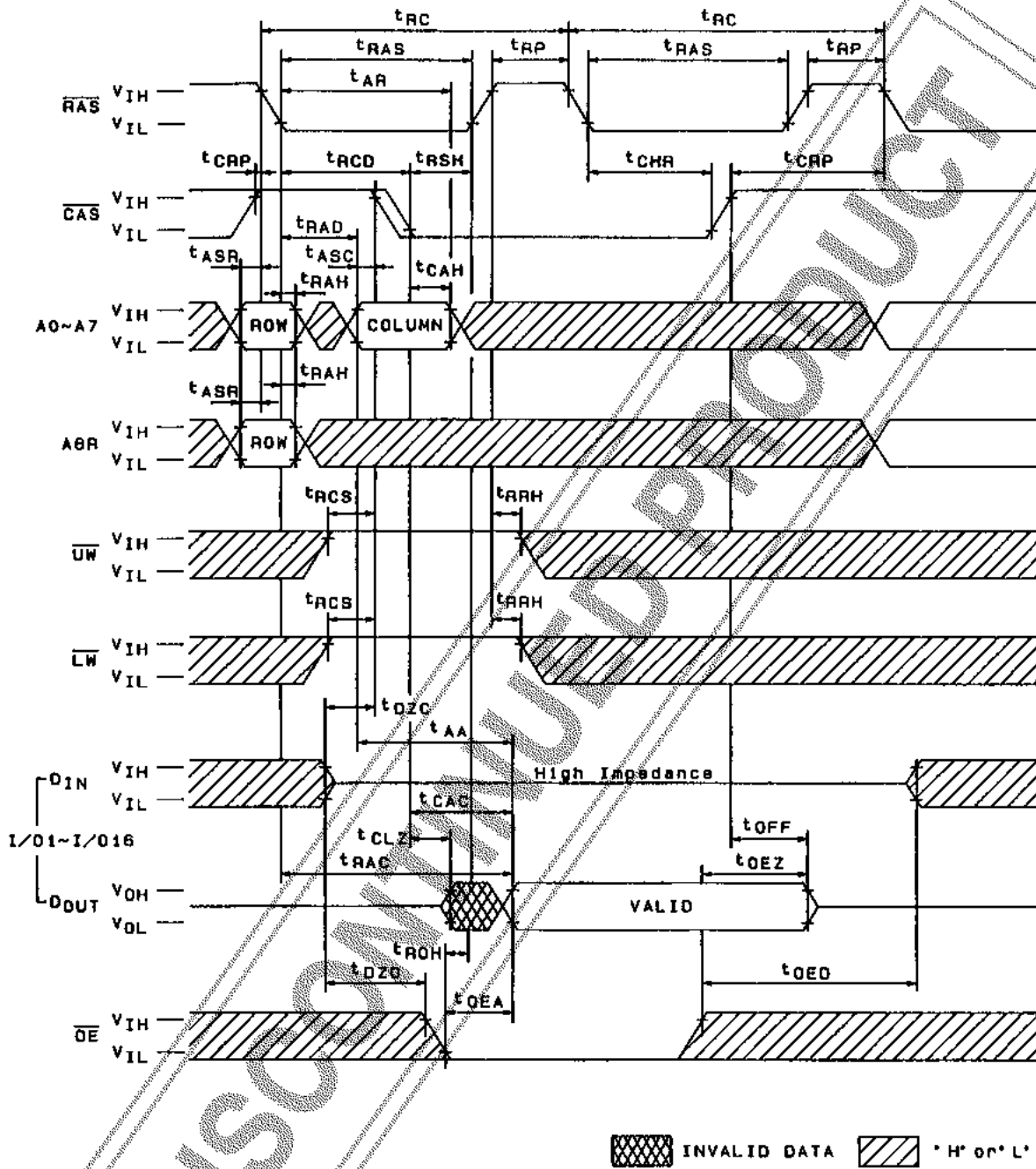


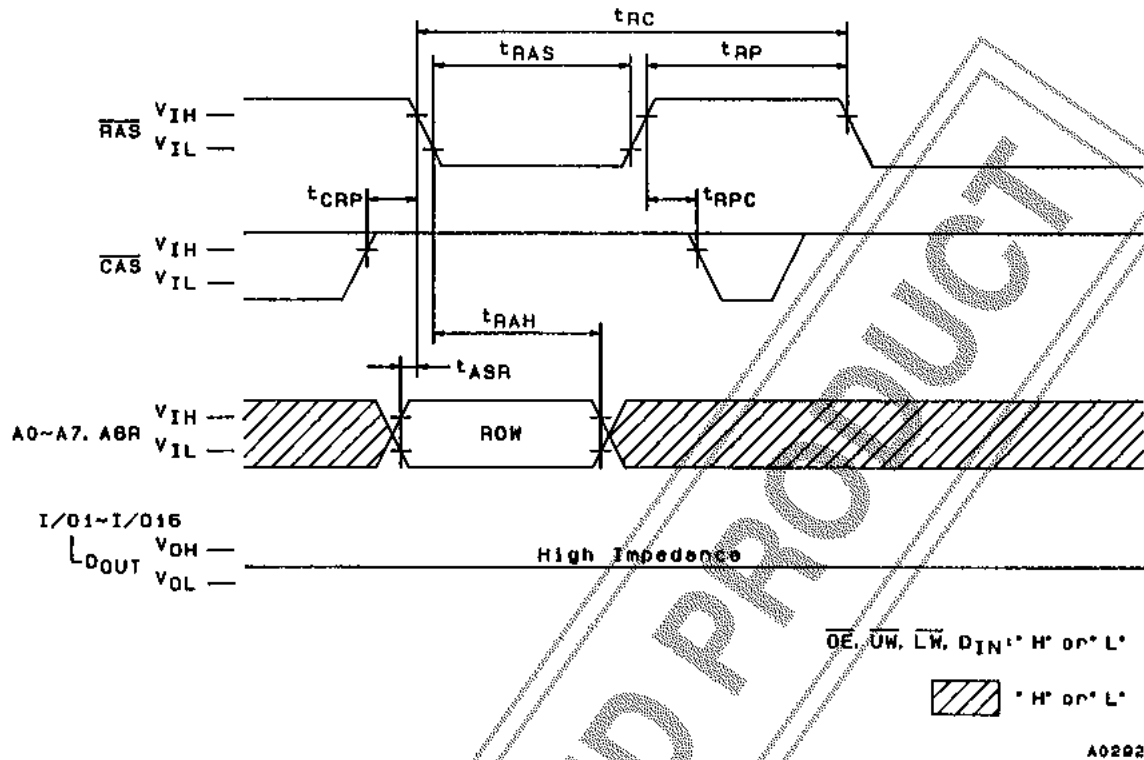
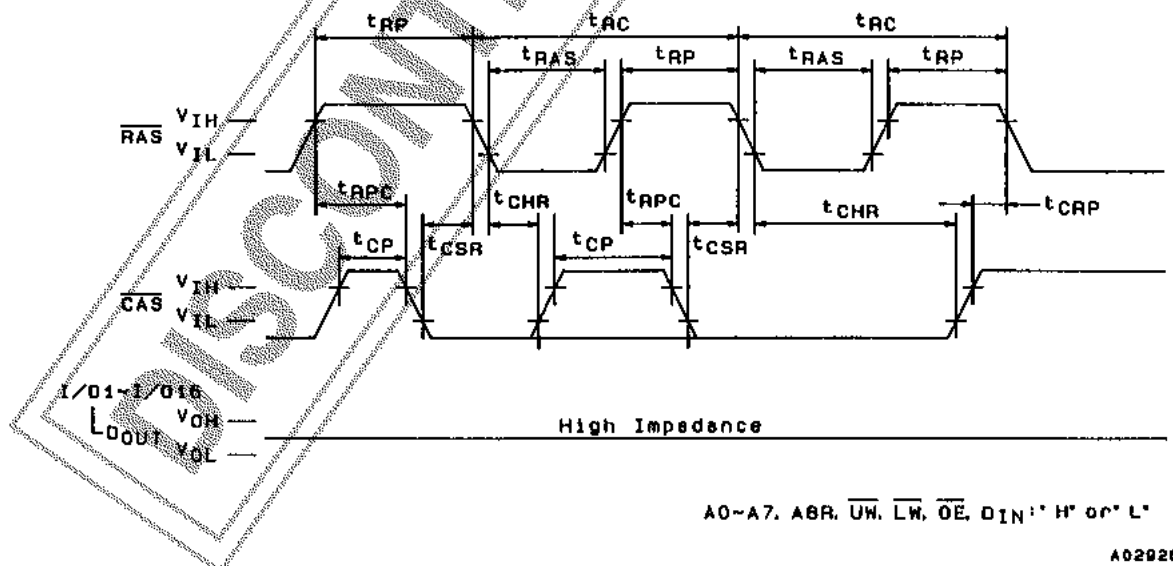
Fast Page Mode Read-Modify Lower Byte Write Cycle



AD3023

Hidden Refresh Cycle



RAS-Only Refresh Cycle**CAS-Before-RAS Refresh Cycle**



CAS-Before-RAS Refresh Counter Test Cycle (Write)

