Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 256K (32K x 9-BIT) SRAM

PRELIMINARY
IDT10509D
IDT100509D
IDT101509D

FEATURES:

- 32,768-words x 9-bit organization
- Address access time: 8/10/12/15
- Wide word for reduced address loading
- Guaranteed Output Hold time
- Differential Write Clock and Single-Ended Write Enable
- Fully compatible with ECL logic levels
- Separate data input and output
- Standard pinouts

DESCRIPTION:

The IDT10509D, IDT100509D and IDT101509D are 294,912-bit high-speed BiCEMOS™ ECL static random access memories organized as 32Kx9, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

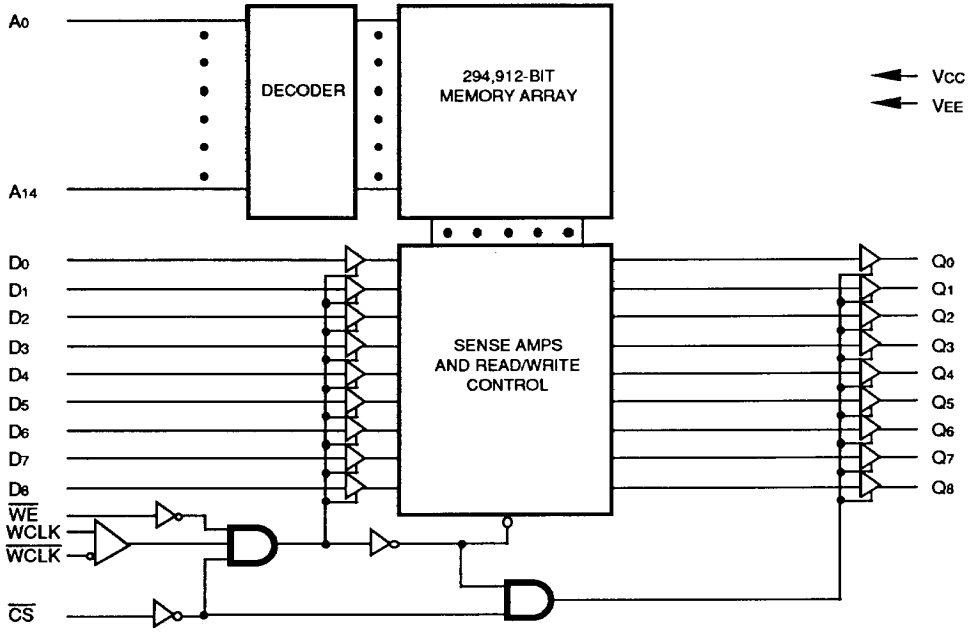
These devices are part of a family of nine-bit-wide ECL SRAMs. The devices have been configured to follow the proposed ECL SRAM JEDEC pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is similar to CMOS devices of equivalent density.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: $Data_{OUT}$ is available an access time after the last change of address.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation.

To write data into this device requires the creation of a Write Pulse, which is the combination of the Write Enable and the Write Clock. The differential Write Clock ensures easy creation of a clean write pulse throughout the memory array, reducing requirements on the skew of Write Enable with respect to addresses. Write cycles can be operated in traditional manner by disabling the Write-Clock and using the Write Enable only. Write cycle disables the output pins in conventional fashion.

FUNCTIONAL BLOCK DIAGRAM



2810 drw 01

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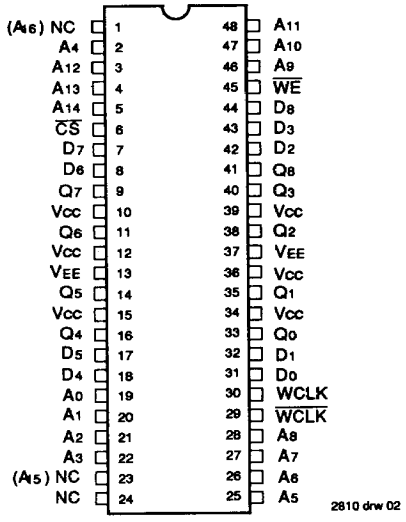
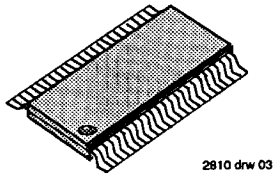
PIN CONFIGURATION



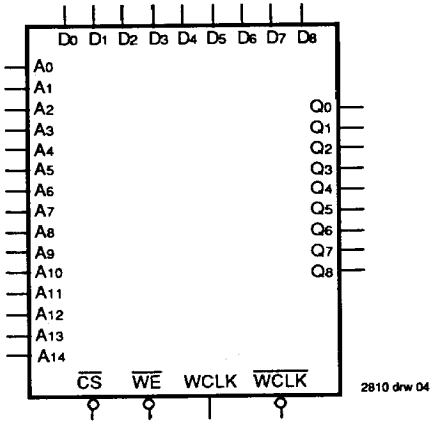
2810 drw 02

TOP VIEW


2810 drw 03

300-Mil-Wide
Plastic SSOP Package
48

LOGIC SYMBOL



2810 drw 04

32Kx9
SRAM

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A14	Address Inputs
D0 through D8	Data Inputs
Q0 through Q8	Data Outputs
$\overline{CS}$	Chip Select Input (Internal pull down)
$\overline{WE}$	Write Enable Input
$\overline{WCLK}$, WCLK	Differential Write Clock Inputs
VEE	More Negative Supply Voltage
Vcc	Less Negative Supply Voltage
NC	No Connect (Not internally bonded)

2810 tbl 01

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2810 tbl 02

NOTE:
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	SSOP Typ.	SSOP Max.	Unit
CIN	Input Capacitance	TBD	–	pF
COUT	Output Capacitance	TBD	–	pF

2810 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	WCLK	$\overline{WCLK}$	Data OUT	Function
H	X	X	X	L	Deselected
L	H	X	X	RAM Data	Read
L	X	L	H	RAM Data	Read
L	L	H	L	L	Write, Diff. Clock
L	L	VEE	L	L	Write, Low Clock
L	L	H	VEE	L	Write, High Clock
L	L	VEE	VEE	L	Write, Single Enable

2810 tbl 04

NOTE:
1. H=High, L=Low, X=Don't Care

ECL-10K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2810 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-280	-220	–	mA	–

2810 tbl 06

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2810 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-260	-200	–	mA

2810 tbl 08

NOTE:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

5

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2810 tbl 09

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

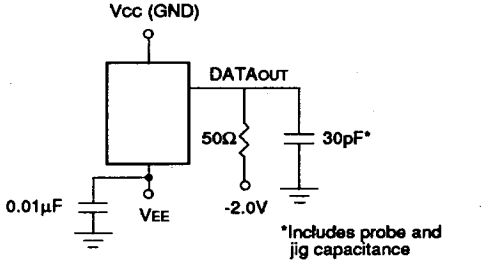
(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Condition		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-280	-220	–	mA

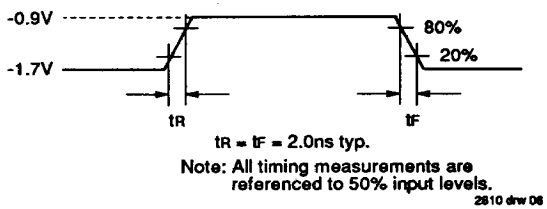
2810 tbl 10

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



AC TEST INPUT PULSE



RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2810 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10509D, IDT100509D, and IDT101509D BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the proposed pinout and functionality for 32Kx9 ECL SRAMs. The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed to control the write to the SRAM array. This device includes on-board logic that provides an internal Write Pulse defined as the logical NOT-AND combination (i.e. NOR, see block diagram) of Write Clock ($\overline{WCLK}$) asserted low and the Write Enable ($\overline{WE}$) asserted low. Note that the Write Clock is a differential input allowing for greater noise rejection and cleaner signal forming over the memory array. This combination of signals is useful for the development of the very short Write Pulse that asynchronous SRAMs need: Write Clock is a carefully formed free-running signal that is de-skewed over the memory array layout; Write Enable is a control signal that can be generated and delivered with the same skew tolerance as address signals.

While $\overline{CS}$, ADDR, and DataIN must be valid when Write Pulse (see definition above) goes low. Data is written to the memory cell at the end of the Write Pulse, and inputs must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

ALTERNATIVE WRITE OPERATION

The device may also be used other Write Pulse modes, if preferred. The Write Clock input may be converted from differential to single-ended operation as described in the Truth Table. The Write Clock may be disabled altogether, and only the Write Enable used to form Write Pulse, by externally connecting both inputs of the differential Write Clock (WCLK and $\overline{WCLK}$) to the VEE supply voltage.

Tying the positive side of the differential Write Clock (WCLK) to the VEE voltage will allow for two single-ended write enables, $\overline{WE}$ and $\overline{WCLK}$. The internal Write Pulse is in Write mode when both are low.

Tying the negative side of the differential Write Clock ($\overline{WCLK}$) to the VEE voltage will allow for two single-ended write enables, $\overline{WE}$ and WCLK. The internal Write Pulse is in Write mode when $\overline{WE}$ is low and WCLK is high.

5

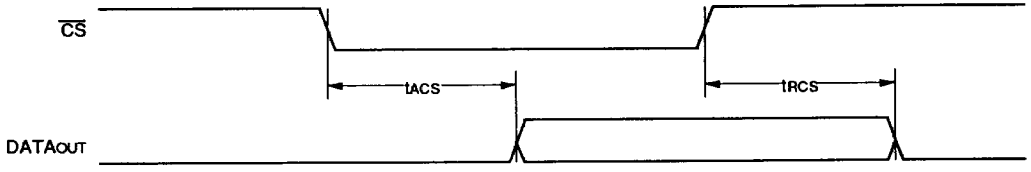
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10509D8 100509D8 101509D8		10509D10 100509D10 101509D10		10509D12 100509D12 101509D12		10509D15 100509D15 101509D15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
tACS	Chip Select Access Time	–	–	5	–	5	–	5	–	5	ns
tRCS	Chip Select Recovery Time	–	–	5	–	5	–	5	–	5	ns
tAA	Address Access Time	–	–	8	–	10	–	12	–	15	ns
tOH	Data Hold from Address Change	–	3	–	3	–	3	–	3	–	ns

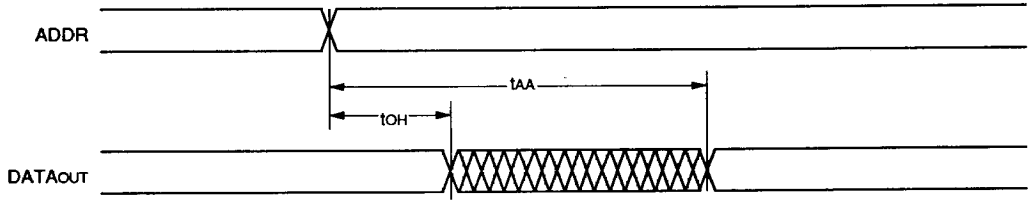
2810 tbl 12

NOTE:
1. Input and Output reference level is 50% point of waveform.

READ CYCLE GATED BY CHIP SELECT



READ CYCLE GATED BY ADDRESS



2810 drw 07

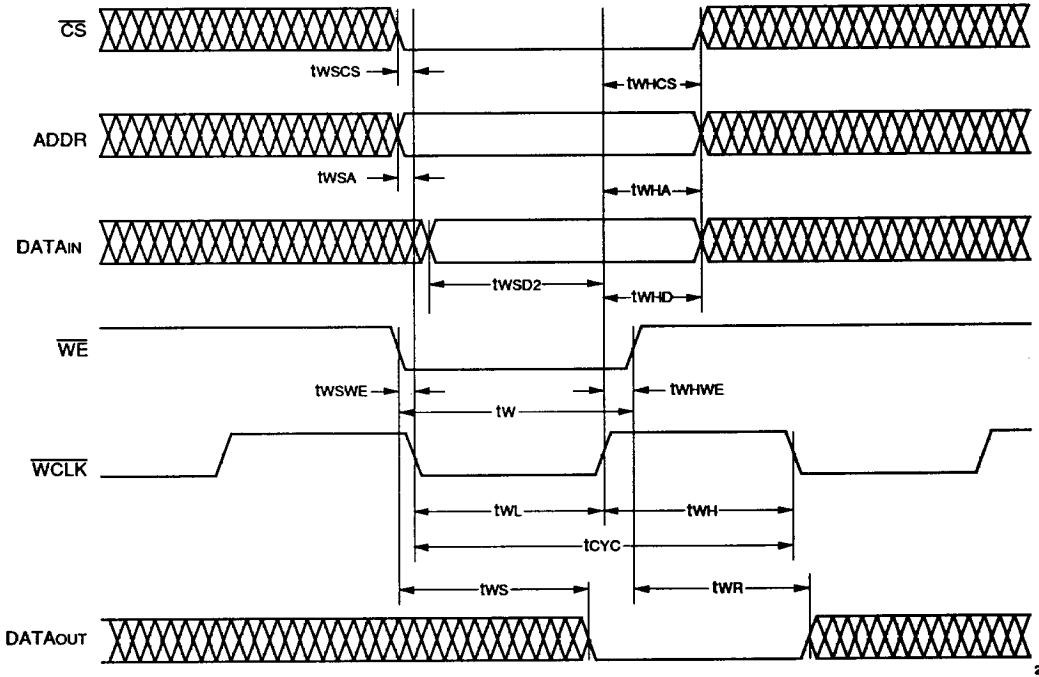
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter (1)	Test Condition	10509D8 100509D8 101509D8		10509D10 100509D10 101509D10		10509D12 100509D12 101509D12		10509D15 100509D15 101509D15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle											
tCYC	Cycle Time	–	8	–	10	–	12	–	15	–	ns
tW	Write Enable Pulse Width	–	6	–	8	–	10	–	13	–	ns
tWL	$\overline{WCLK}$ Low Pulse Width	–	6	–	8	–	10	–	13	–	ns
tWH	$\overline{WCLK}$ High Pulse Width	–	2	–	2	–	2	–	2	–	ns
tWSCS	Chip Select Set-up Time	–	0	–	0	–	0	–	0	–	ns
tWSA	Address Set-up Time	–	0	–	0	–	0	–	0	–	ns
tWSD2	Data Set-up Time	–	6	–	8	–	10	–	13	–	ns
tWSWE	Write Enable Set-up Time	–	0	–	0	–	0	–	0	–	ns
tWHCS(2)	Chip Select Hold Time	–	1	–	1	–	1	–	2	–	ns
tWHA(2)	Address Hold Time	–	1	–	1	–	1	–	2	–	ns
tWHD(2)	Data Hold Time	–	1	–	1	–	1	–	2	–	ns
tWHWE(2)	Write Enable Hold Time	–	0	–	0	–	0	–	0	–	ns
tWS	Write Disable Time	–	–	5	–	5	–	5	–	5	ns
tWR(3)	Write Recovery Time	–	–	5	–	5	–	5	–	5	ns

2810 tbl 13

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Write Pulse Width is the logical NOT-AND of $\overline{WE1}$ and $\overline{WE2}$, that is, when both are logical low.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Q_0 to Q_3) when no new Address Transition occurs.

WRITE CYCLE TIMING DIAGRAM



2810 drw 08

ORDERING INFORMATION