# Agilent HFCT-701XB, 10 Gb Ethernet, 1310 nm, 10 km 10GBASE-LR, XENPAK LAN-PHY

Data Sheet

**Description**

The HFCT-701XB is an "intelligent" optical module which incorporates the complete physical layer functionality from the 10.3125 Gb/s 64B/66B encoded optical interface to a XAUI compliant (4 channel x 3.125 Gb/s) 8B/10B encoded electrical interface and vice versa. The control interface (MDIO) is also integrated.

The HFCT-701XB module includes a transmitter that incorporates an uncooled, directly modulated 1310 nm DFB laser. The receiver subassembly includes a highly reliable PIN photodiode. The MUX/DEMUX, XAUI interface and MDIO management functions are all integrated into the module, as is a precision oscillator that removes any need for an external reference clock.

**Features**

- **IEEE Std 802.3ae type 10GBASE-LR PMD (10 Gigabit Ethernet standard)**
- **Compliant with XENPAK MSA Draft 3.0**
- **Standard SC Duplex fiber optic connector**
- **Standard 70 pin electrical connector**
- **Four wide XAUI Electrical interface**
- **MDIO Management Interface**
- **Only 3.3 V and 1.8 V supplies required (compatible with the XENPAK APS)**
- **5 diagnostic loopback modes**
- **Front panel hot pluggable**
- **Excellent thermal and EMI integrity performance supports high port densities**
- **Hot plug power up circuit removes PSU sequence dependency and reduces inrush current**
- **Precision onboard oscillator - no external clocks required**

**Applications**

- **Enterprise to Metro Uplinks**
- **Campus Trunking**
- **Data Aggregation**
- **Exchange Point-to-Point Links**

**Table of Contents**

## General Specifications

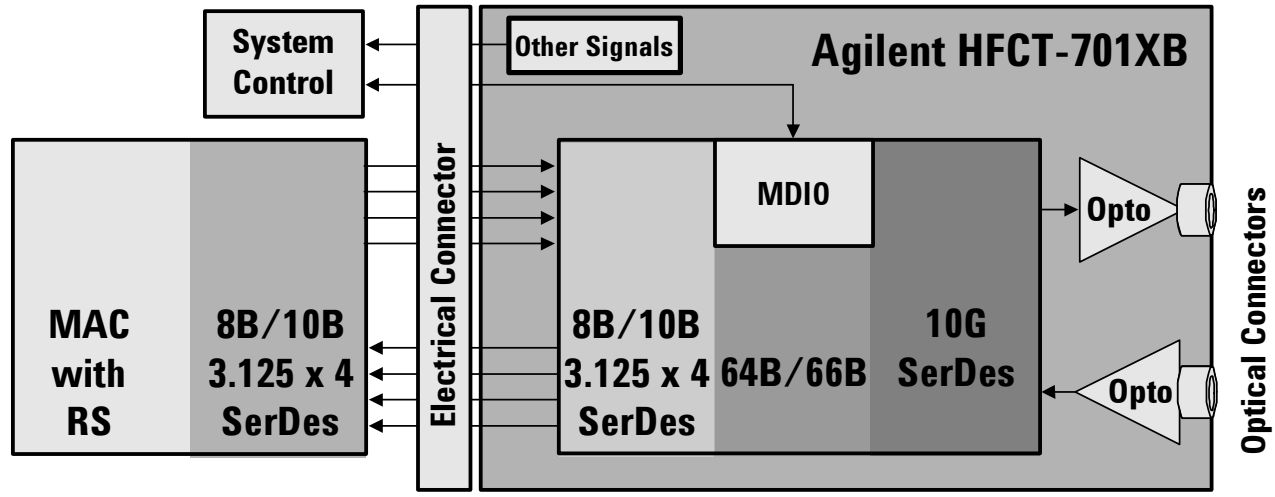



**Figure 1. High level block diagram**

### General Optical Specifications

*Optical Connector:*
SC Duplex
*Optical Line rate:*
10.3125 Gb/s
*Link Length:*
10 km, with G.652 fiber
*Laser:*
1310 nm, directly modulated, uncooled DFB
*Detector:*
PIN diode

### General Electrical Specifications

*Connector:*
70-pin, mates to Tyco/AMP Part No. 1367337-1 or equivalent
*Supply Voltages:*
+1.8 V and +3.3 V
*E->O Coding (Transmit Direction):*
8B/10B coding removed, 64B/66B added
*O->E Coding (Receive Direction):* 64B/66B removed, 8B/10B coding added
*XAUI interface:*
100 Ω Differential, AC- coupled I/O on Tx and Rx, per IEEE 802.3ae Clause 47
*Control interface:*
MDIO, 1.2 V, per IEEE 802.3ae Clause 45.3
*Non Volatile memory:*
48 byte user space

### Environmental Specifications

*Operating temperature:*
0 °C to +70 °C case
*Power consumption:*
6.0 W maximum

## Technical Specifications

### Absolute Maximum Ratings[1]

| Parameter | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|
| Storage Temperature | 0 | | 85 | °C | |
| Operating Temperature | 0 | | 70 | °C | Case temperature |
| Supply Voltage (3.3 V) | | | 3.6 | V | |
| Supply Voltage (1.8 V) | | | 2.0 | V | |
| Voltage on any XAUI pin | | | 2.5 | V | |
| Voltage on any LVCMOS pin | -0.7 | | 4.0 | V | |

### Recommended Operating Conditions[2]

| Parameter | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|
| Stabilization Time | | 0.5 | 5 | sec | |
| Input Voltage | 3.135 | 3.3 | 3.465 | V | |
| Input Voltage (APS) | 1.71 | 1.8 | 1.89 | V | |
| Supply Current (@ 3.3 V) | | 1.5 | 1.6 | A | |
| Supply Current (@ 1.8 V) | | 0.15 | 0.4 | A | |
| Power Consumption | | 5.2 | 6.0 | W | |
| Inrush current during hot plug | | | 50 | mA/ms | |
| Inrush current (per power pin) | | | 0.75 | A | 150% x 0.5A steady state rating |

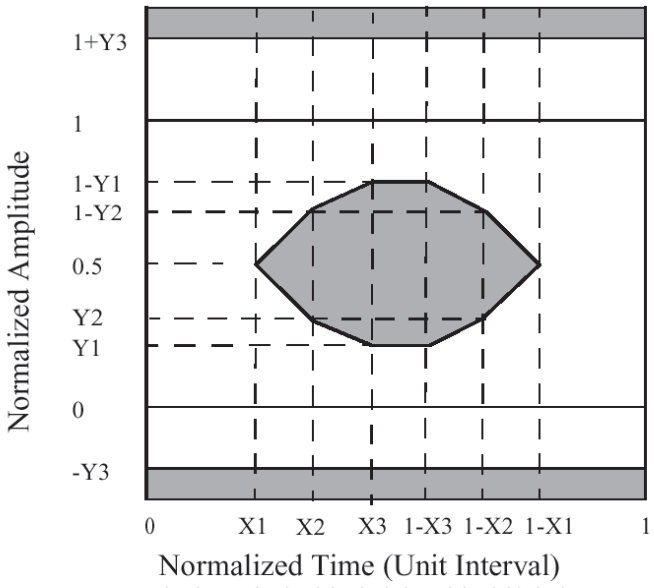
**Notes:**
1. Absolute maximum ratings are those values beyond which functional performance is not intended, device reliability is not implied, and damage to the device may occur.
2. Typical operating conditions are those values for which functional performance and device reliability is implied.

## Optical Specifications

| Parameter | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|
| **Transmitter** | | | | | |
| Laser OMA output power | -5.2 | | | dBm OMA | 1, 2 |
| Laser mean output power | -8.2 | | 0.5 | dBm mean | 1, 2, 3 |
| Extinction ratio | 3.5 | | - | dB | 1, 2 |
| Wavelength | 1260 | | 1355 | nm | |
| Transmitter and dispersion penalty (TDP) | | | 3.2 | dB | 1, 2 |
| Side mode suppression ratio | 30 | | | dB | 1 |
| OMA - TDP | -6.2 | | | dBm OMA | 1, 2 |
| $RIN_{12}OMA$ | | | -128 | dB/Hz | 1 |
| Optical Return Loss | | | 12 | dB | |
| TX eye definition | | | | | See Figure 2 |
| **Receiver** | | | | | |
| Stressed sensitivity | - | | -10.3 | dBm OMA | 1 |
| Nominal sensitivity | - | | -12.6 | dBm OMA | 1, 3 |
| Receive Power Overload | 0.5 | | | dBm mean | 1, 4 |
| Reflectance loss | | | -12 | dB | 1 |
| Wavelength | 1260 | | 1355 | nm | 1 |
| Signal detect On | -30 | | | dBm | |
| Signal detect Off | | | -16 | dBm | |
| Signal detect Hysteresis | 0.5 | | | dB | |

### General Specification Considerations (Notes)

1. IEEE 802.3ae compliant.
2. These parameters are interrelated: see IEEE 802.3ae.
3. Information purposes only.
4. Up to 1.5 dB without damage.




Note: where X1, X2, X3, Y1, Y2, Y3 = 0.25, 0.40, 0.45, 0.25, 0.28, 0.40 respectively

**Figure 2. Transmitter Eye Mask Definition**

### Electrical Control and Sense I/O Parameters

**Table 1 - CMOS DC Parameters (MDC, PRTAD<4:0>, LASI)**

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| Vol | Output low voltage | | | 0.15 | V | ext. Rpullup = 10 kΩ to 1.2 V |
| Voh | Output high voltage | 1.0 | | 1.5 | V | ext. Rpullup = 10 kΩ to 1.2V |
| Vih | Input high voltage | 0.84 | | 1.25 | V | |
| Vil | Input low voltage | | | 0.36 | V | |
| Ipd | Input pad pulldown current | 20 | 40 | 120 | µA | Vin = 1.2 V |
| Trise | Rise time | | | 30 | us | Cload = 300 pF |
| Tfall | Fall time | | 25 | 50 | ns | Cload = 300 pF |

### Electrical MDIO Parameters

**Table 2 - MDIO 1.2 V dc parameters**

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| Voh | Output high voltage | 1.0 | | 1.5 | V | Ioh = -100 uA |
| Vol | Output low voltage | -0.3 | | 0.2 | V | Iol = +100 uA |
| Iol | Output low current | -4 | | | mA | Vin = 0.3 |
| Vih | Input high voltage | 0.84 | | 1.5 | V | |
| Vil | Input low voltage | -0.3 | | 0.36 | V | |
| Cin | Input capacitance | | | 10 | pF | |

**Table 3 - MDIO AC Parameters**

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| Thold | MDIO data hold time | 10 | | | ns | |
| Tsetup | MDIO data setup time | 10 | | | ns | |
| Tdelay | Delay from MDC rising edge to MDIO data change | 0 | | 300 | ns | |
| Fmax | Maximum MDC clock rate | | | 2.5 | MHz | |

## Electrical High Speed I/O Parameters

### Table 4 - 3.125 Gb/s XAUI Input Interface

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| | BAUD rate | | 3.125 | | Gb/s | |
| | BAUD rate tolerance | -100 | | 100 | ppm | |
| | Differential input amplitude | 200 | | 2500 | mVpp | Note 1 |
| | Differential return loss | | | -10 | dB | 100 MHz to 2.5 GHz ref to 100Ω impedance |
| | Common mode return loss | | | -6 | dB | 100 MHz to 2.5 GHz ref to 25Ω |
| | Input Differential Skew | | | 75 | ps P-P | at crossing point, Note 2 |
| | Jitter amplitude tolerance deterministic + random jitter + Sj jitter | | | 0.55 + Sj | UIpp | See Figure 2a for SJ jitter graph |

### Table 5 - 3.125 Gb/s XAUI Driver Characteristics

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| | BAUD rate | | 3.125 | | Gb/s | |
| | BAUD rate variation | -100 | | 100 | ppm | |
| | Differential amplitude | 800 | | 1600 | mVpp | |
| | Transition times (20-80%) | 60 | 90 | 130 | ps | Note 2 |
| | Total output jitter | | | ± 0.175 | UI | no pre-equalization |
| | Output deterministic jitter | | | ± 0.085 | UI | no pre-equalization |
| | Output differential skew | | | 15 | ps | at crossing point |
| | Differential output return loss | | | | dB | 312.5 MHz to 625 MHz: -10 dB<br>625 MHz to 3.125 GHz: as per equation 47-1 IEEE 802.3ae |
| | Electrical eye mask | | | | | See Figure 3 |

**Note:**

1. Maximum amplitude of 2500 mVpp is the combined effect of the driver maximum output signal of 1600 mVpp and the receiver input impedance mismatch.
2. For information only.

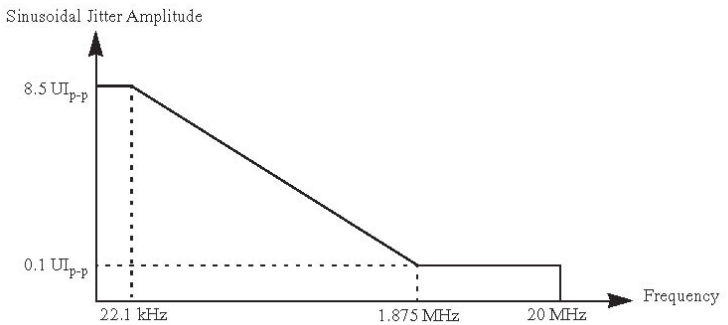



**Figure 2a. Single-tone sinusoidal jitter mask**

### Electrical Eye Mask

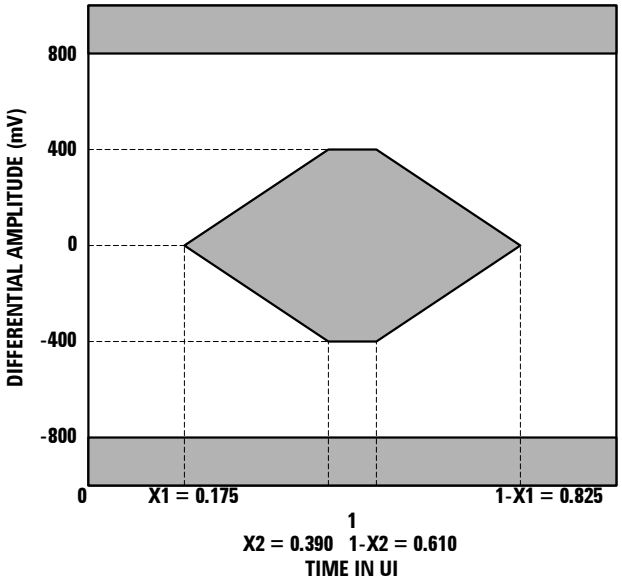



**Figure 3 - XAUI Driver Near End Template**

### General Connector Considerations

1. Ground connections are common for Tx and Rx.
2. $V_{CC}$ contacts are each rated at 0.5 A nominal.
3. See Figure 8 for layout of Host PCB and location of Pin1.

**Table 6 - General I/O Pin Summary**

| Signal Type | Pins | Direction | Function |
|---|---|---|---|
| **Power Supply Pins** | | | |
| Ground | 1:3, 33:37, 40, 43, 46, 49, 52:54, 57, 60, 63, 66, 69:70 | | Electrical ground |
| 3.3 V | 5:6, 30:31 | I | 3.3 V power supply |
| 5.0 V | 4, 32 | I | 5.0 V power supply not used |
| Adaptive power supply | 7:8, 28:29 | I | Adaptive power supply (1.8 V) |
| Adaptive power supply set | 25 | I | APS set ccnnection |
| Adaptive power supply sense | 27 | I | APS sense connection |
| **Control & Sense I/O Pins** | | | |
| LASI | 9 | O | 1.2 V CMOS pull up on host |
| Reset | 10 | I | 1.2 V CMOS pull up on module |
| Transmitter ON/OFF | 12 | I | 1.2 V CMOS pull up on module |
| Port address 4:0 | 19:23 | I | 1.2 V CMOS pull up on module |
| **MDIO Pins** | | | |
| MOD DETECT | 14 | O | 1 kW pull down to ground on module |
| Management data IO | 17 | I/O | 1.2 V per IEEE802.3ae clause 45.3 |
| Management data clock | 18 | I | 1.2 V per IEEE802.3ae clause 45.3 |
| **High Speed I/O Pins** | | | |
| Receiver lane 0:3 + | 41, 44, 47, 50 | O | XAUI per IEEE802.3ae clause 47 |
| Receiver lane 0:3 - | 42, 45, 48, 51 | O | XAUI per IEEE802.3ae clause 47 |
| Transmitter lane 0:3 + | 55, 58, 61, 64 | I | XAUI per IEEE802.3ae clause 47 |
| Transmitter lane 0:3 - | 56, 59, 62, 65 | I | XAUI per IEEE802.3ae clause 47 |
| **Non Connected Pins** | | | |
| Not connected | 4, 11, 13, 15:16, 24, 26, 32, 38:39, 67:68 | | NC on module |

## Electrical Pin Out

| | | | |
|---|---|---|---|
| 70 | GND | 1 | GND |
| 69 | GND | 2 | GND |
| 68 | NOT CONNECTED | 3 | GND |
| 67 | NOT CONNECTED | 4 | 5.0V |
| 66 | GND | 5 | 3.3V |
| 65 | TX LANE3- | 6 | 3.3V |
| 64 | TX LANE3+ | 7 | APS |
| 63 | GND | 8 | APS |
| 62 | TX LANE2- | 9 | LASI |
| 61 | TX LANE2+ | 10 | RESET |
| 60 | GND | 11 | NOT CONNECTED |
| 59 | TX LANE1- | 12 | TX ON/OFF |
| 58 | TX LANE1+ | 13 | NOT CONNECTED |
| 57 | GND | 14 | MOD DETECT |
| 56 | TX LANE0- | 15 | NOT CONNECTED |
| 55 | TX LANE0+ | 16 | NOT CONNECTED |
| 54 | GND | 17 | MDIO |
| 53 | GND | 18 | MDC |
| 52 | GND | 19 | PRTAD4 |
| 51 | RX LANE3- | 20 | PRTAD3 |
| 50 | RX LANE3+ | 21 | PRTAD2 |
| 49 | GND | 22 | PRTAD1 |
| 48 | RX LANE2- | 23 | PRTAD0 |
| 47 | RX LANE2+ | 24 | NOT CONNECTED |
| 46 | GND | 25 | APS SET |
| 45 | RX LANE1- | 26 | NOT CONNECTED |
| 44 | RX LANE1+ | 27 | APS SENSE |
| 43 | GND | 28 | APS |
| 42 | RX LANE0- | 29 | APS |
| 41 | RX LANE0+ | 30 | 3.3V |
| 40 | GND | 31 | 3.3V |
| 39 | NOT CONNECTED | 32 | 5.0V |
| 38 | NOT CONNECTED | 33 | GND |
| 37 | GND | 34 | GND |
| 36 | GND | 35 | GND |

**Figure 4. Electrical Pin Out**

## Electrical Pin Out Definitions

### Table 7 - Pin Function Definitions (Lower Row)

| Pin No | Name | Direction | Function | Note |
|---|---|---|---|---|
| 1 | GND | | Electrical ground | |
| 2 | GND | | Electrical ground | |
| 3 | GND | | Electrical ground | |
| 4 | NOT CONNECTED | | 5.0 V power supply | |
| 5 | 3.3 V | I | 3.3 V power supply | |
| 6 | 3.3 V | I | 3.3 V power supply | |
| 7 | APS | I | Adaptive power supply (1.8 V) | |
| 8 | APS | I | Adaptive power supply (1.8 V) | |
| 9 | LASI | O | Logic high: normal operation<br>Logic low: LASI asserted | See Table 10 |
| 10 | RESET | I | Logic high: normal operatio<br>Logic low: reset | |
| 11 | NOT CONNECTED | | | |
| 12 | TX ON/OFF | I | Pulled up inside module via 10 kΩ<br>Logic high: transmitter on<br>Logic low: transmitter off | |
| 13 | NOT CONNECTED | | | |
| 14 | MOD DETECT | O | Pulled low inside module through 1 k to GND | |
| 15 | NOT CONNECTED | | | |
| 16 | NOT CONNECTED | | | |
| 17 | MDIO | I/O | Management data IO | |
| 18 | MDC | I | Management data clock | |
| 19 | PRTAD4 | I | Port address bit 4 | |
| 20 | PRTAD3 | I | Port address bit 3 | |
| 21 | PRTAD2 | I | Port address bit 2 | |
| 22 | PRTAD1 | I | Port address bit 1 | |
| 23 | PRTAD0 | I | Port address bit 0 | |
| 24 | NOT CONNECTED | | | |
| 25 | APS SET | I | APS set connection | |
| 26 | NOT CONNECTED | | | |
| 27 | APS SENSE | I | APS sense connection | |
| 28 | APS | I | Adaptive Power Supply (1.8 V) | |
| 29 | APS | I | Adaptive Power Supply (1.8 V) | |
| 30 | 3.3 V | I | Power | |
| 31 | 3.3 V | I | Power | |
| 32 | NOT CONNECTED | | 5.0 V Power Supply | |
| 33 | GND | | Electrical Ground | |
| 34 | GND | | Electrical Ground | |
| 35 | GND | | Electrical Ground | |

**Table 8 - Pin Function Definitions (Upper Row)**

| Pin No | Name | Direction | Function | Note |
|---|---|---|---|---|
| 36 | GND | | Electrical Ground | |
| 37 | GND | | Electrical Ground | |
| 38 | NOT CONNECTED | | | |
| 39 | NOT CONNECTED | | | |
| 40 | GND | | Electrical Ground | |
| 41 | RX LANE 0+ | O | Module XAUI Output Lane 0+ | |
| 42 | RX LANE 0- | O | Module XAUI Output Lane 0- | |
| 43 | GND | | Electrical Ground | |
| 44 | RX LANE 1+ | O | Module XAUI Output Lane 1+ | |
| 45 | RX LANE 1- | O | Module XAUI Output Lane 1- | |
| 46 | GND | | Electrical Ground | |
| 47 | RX LANE 2+ | O | Module XAUI Output Lane 2+ | |
| 48 | RX LANE 2- | O | Module XAUI Output Lane 2- | |
| 49 | GND | | Electrical Ground | |
| 50 | RX LANE 3+ | O | Module XAUI Output Lane 3+ | |
| 51 | RX LANE 3- | O | Module XAUI Output Lane 3- | |
| 52 | GND | | Electrical Ground | |
| 53 | GND | | Electrical Ground | |
| 54 | GND | | Electrical Ground | |
| 55 | TX LANE 0+ | I | Module XAUI Input Lane 0+ | |
| 56 | TX LANE 0- | I | Module XAUI Input Lane 0- | |
| 57 | GND | | Electrical Ground | |
| 58 | TX LANE 1+ | I | Module XAUI Input Lane 1+ | |
| 59 | TX LANE 1- | I | Module XAUI Input Lane 1- | |
| 60 | GND | | Electrical Ground | |
| 61 | TX LANE 2+ | I | Module XAUI Input Lane 2+ | |
| 62 | TX LANE 2- | I | Module XAUI Input Lane 2- | |
| 63 | GND | | Electrical Ground | |
| 64 | TX LANE3+ | I | Module XAUI Input Lane 3+ | |
| 65 | TX LANE3- | I | Module XAUI Input Lane 3- | |
| 66 | GND | | Electrical Ground | |
| 67 | NOT CONNECTED | | | |
| 68 | NOT CONNECTED | | | |
| 69 | GND | | Electrical Ground | |
| 70 | GND | | Electrical Ground | |

## Mechanical Specifications

### Package Dimensions

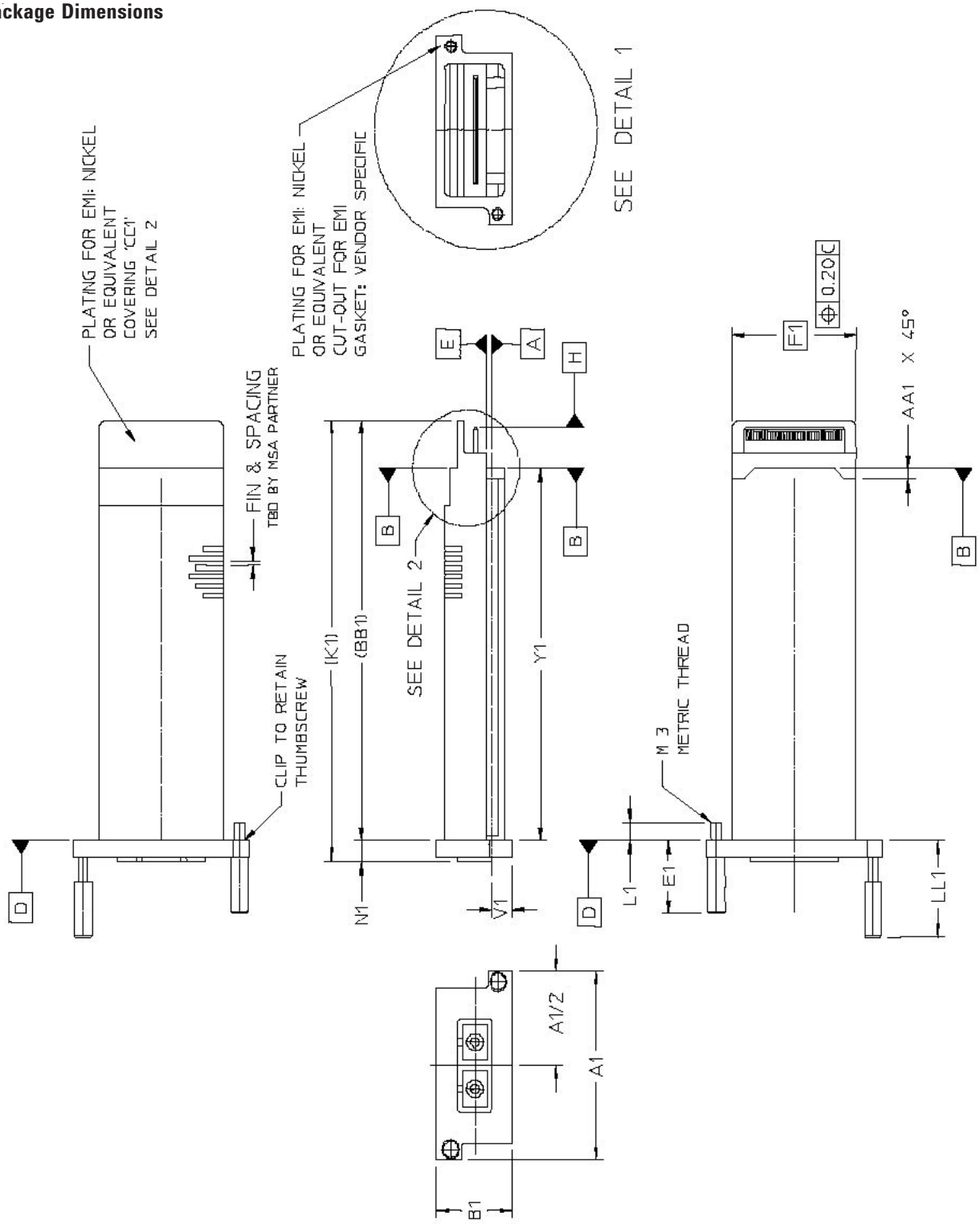



**Figure 5.**

**Note:**
It is recommended that the user refers to the XENPAK MSA at www.xenpak.org for full mechanical detail.

**Dimensions Table (Figure 5)**

| Key | Values | | Tolerance | Comments |
|---|---|---|---|---|
| | mm | inch | mm | |
| A1 | 51.3 | 2.020 | ±0.20 | Width of Bezel overall |
| B1 | 22.4 | 0.882 | ±0.20 | Height of Bezel overall |
| E1 | 20.75 | 0.817 | Maximum | Extension of captive screw |
| F1 | 36.0 | 1.417 | ±0.20 | Width of Transceiver body |
| K1 | (121.0) | 4.764 | REF | Length of Transceiver overall minus protruding captive screw heads |
| L1 | 5.00 | 0.197 | ±0.20 | Length of captive screw from Datum "D" to end of threaded end |
| N1 | 5.8 | 0.228 | ±0.20 | Datum "D" to front of Transceiver Bezel |
| V1 | 7.92 | 0.312 | ±0.20 | Datum "E" to Bottom of Transceiver Bezel |
| Y1 | 102.20 | 4.024 | ±0.20 | Datum "D" to Datum "B" |
| AA1 | 3.0 | 0.118 | ±0.50 | Datum "B" to end of 45° chamfer |
| BB1 | (115.2) | 4.535 | REF | Length of Module from Datum "D" to rear Over-hanging Ledge |
| LL1 | 25.8 | 1.016 | Maximum | Length of Thumbscrew |

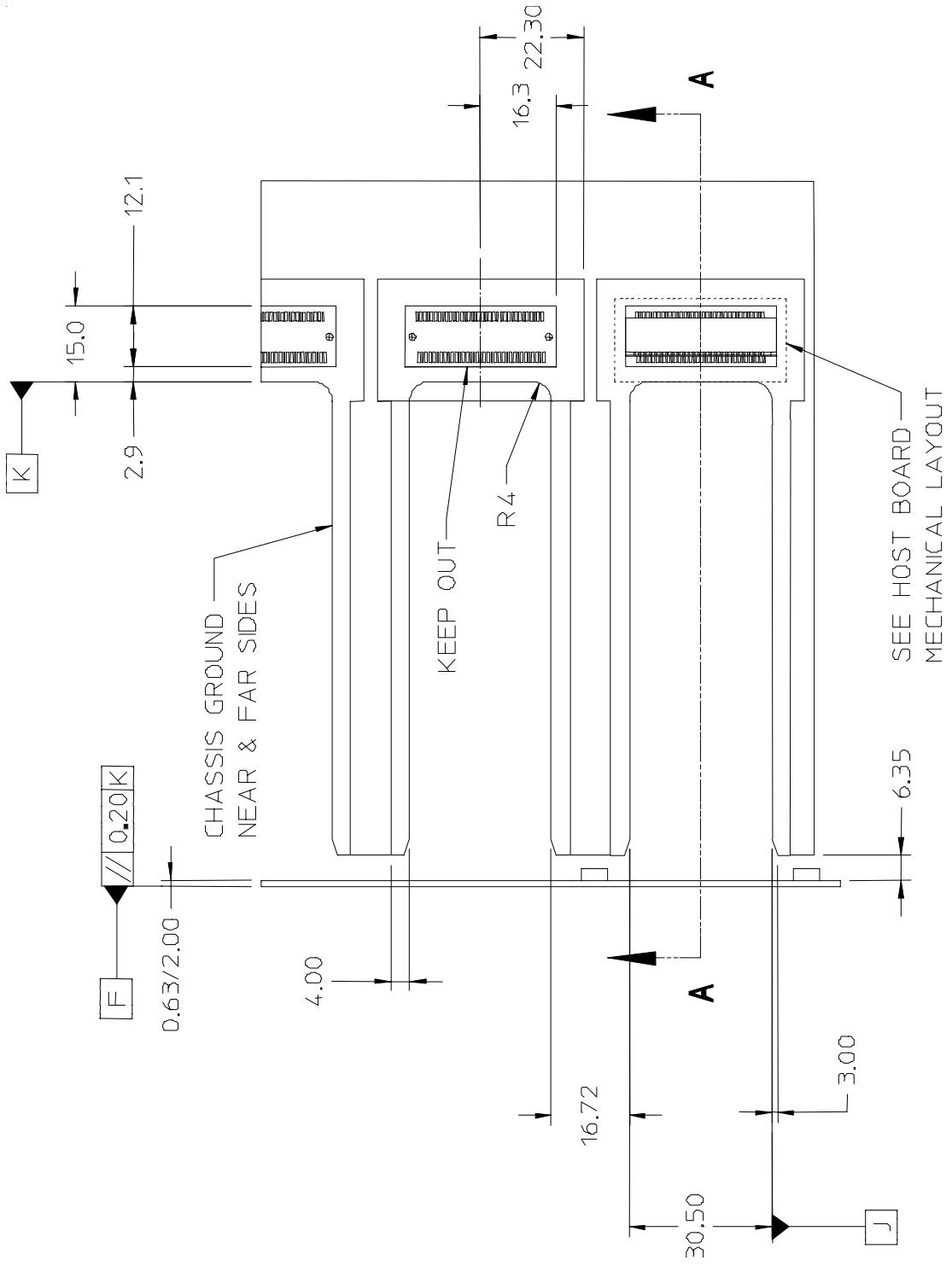
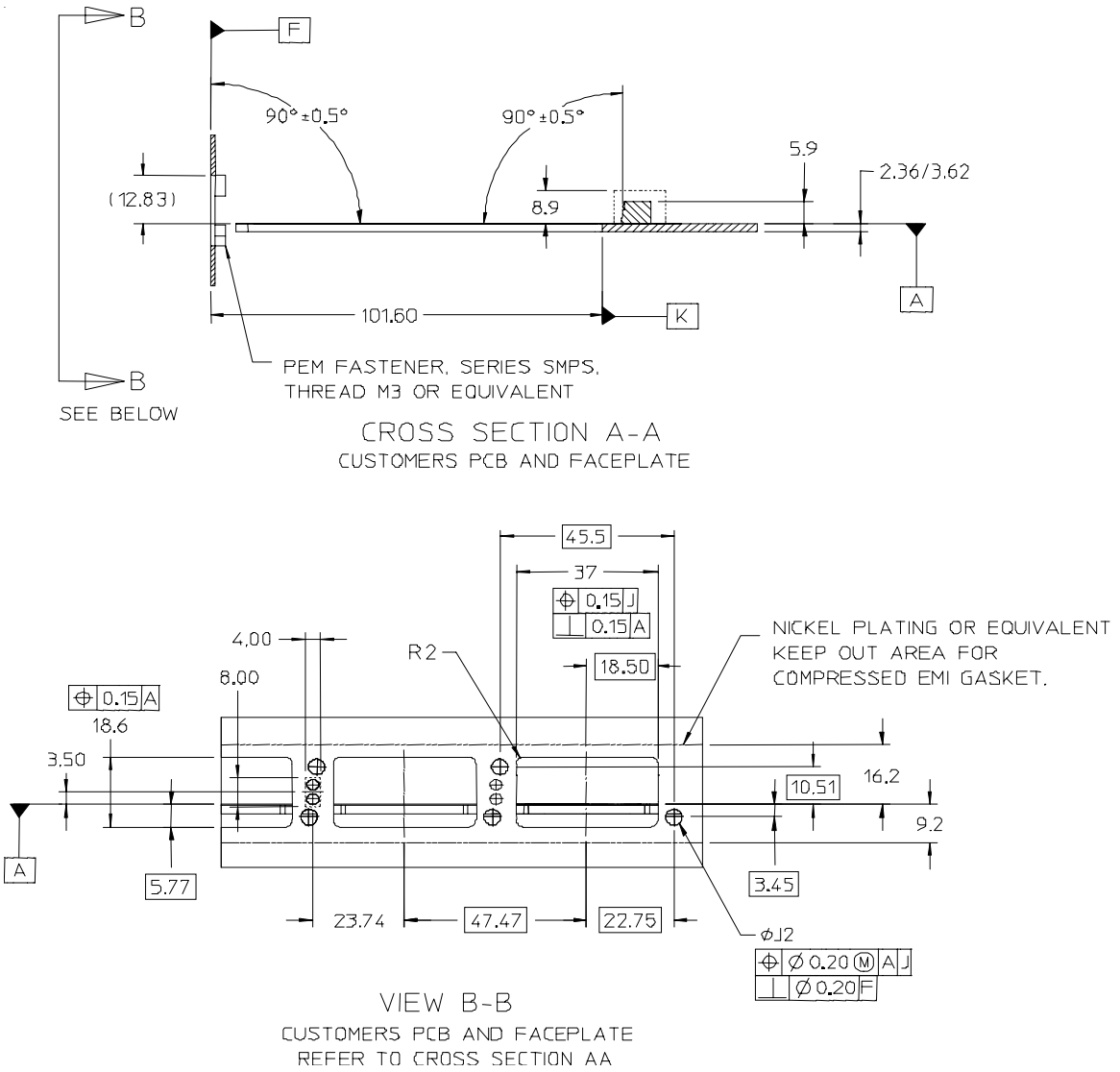

22.30
16.3
A
12.1
15.0
2.9
K
R4
KEEP OUT
CHASSIS GROUND
NEAR & FAR SIDES
SEE HOST BOARD
MECHANICAL LAYOUT
0.20 K
0.63/2.00
F
6.35
4.00
A
3.00
16.72
30.50
J

**Figure 6.**




**Note:**
Case Ground is separated from the common Rx and Tx signal ground

**Figure 7.**

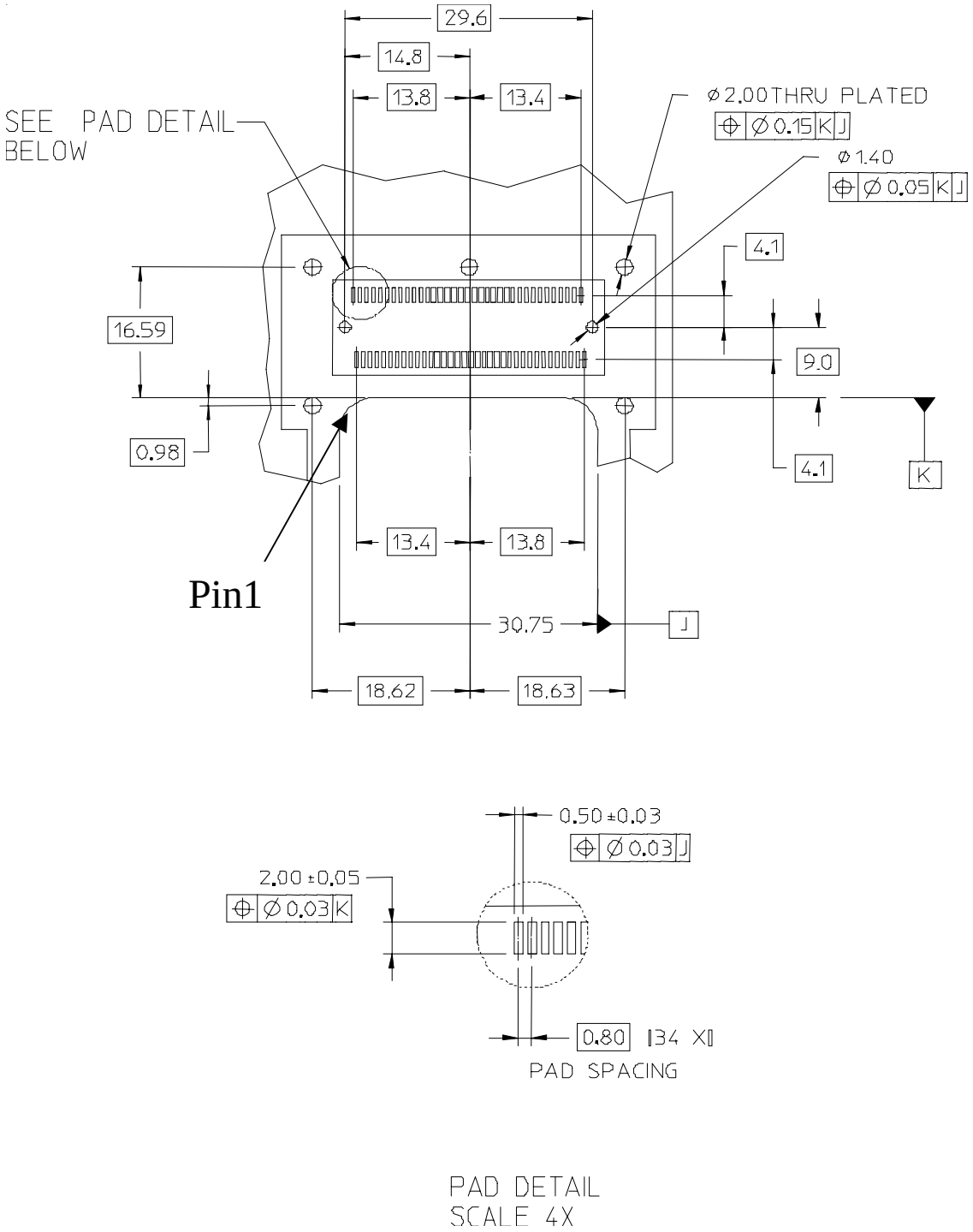



**Figure 8. Host board layout for 70 pin connector**

### Block Diagram

Figure 9 shows a block diagram of the HFCT-701XB. Figures 10 and 11 show greater detail of the transmitter and receiver paths.

### Transmitter Path Summary

Figure 10 shows a block diagram of the transmit path, from the four XAUI differential inputs to the optical output. The incoming 4 x 3.125 Gb/s XAUI differential 8B/10B encoded electrical inputs, are reformatted and transmitted onto the outgoing fiber optic interface at 10.3125 Gb/s, using 64B/66B encoding.

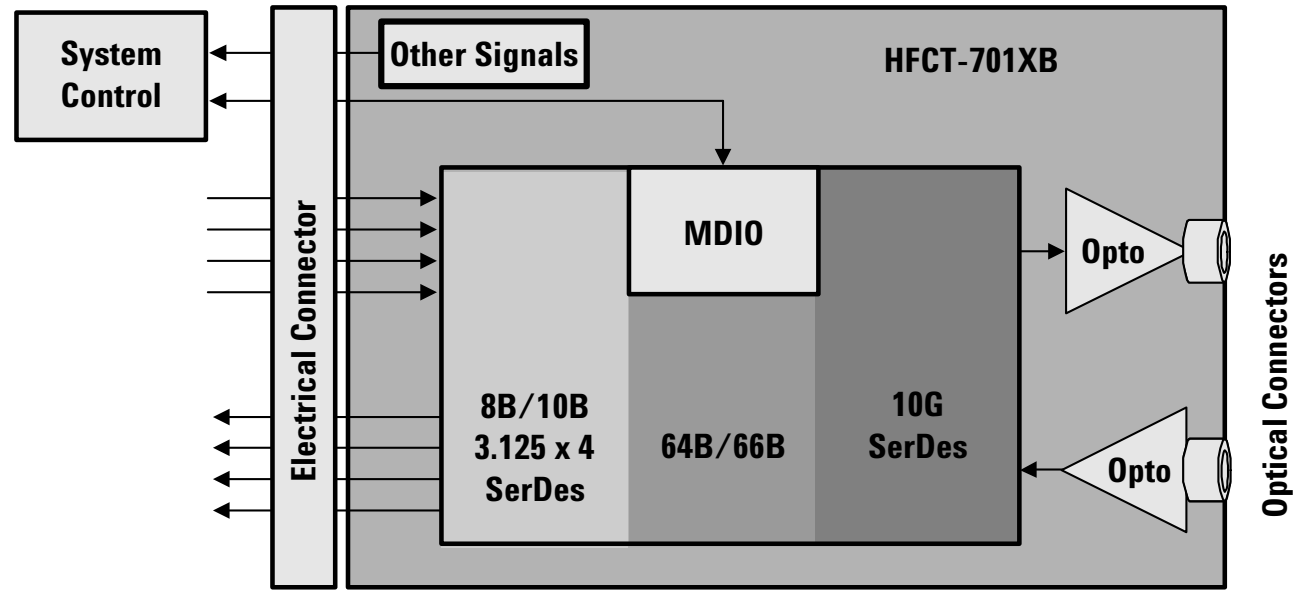



**Figure 9. Block Diagram of HFCT-701XB**

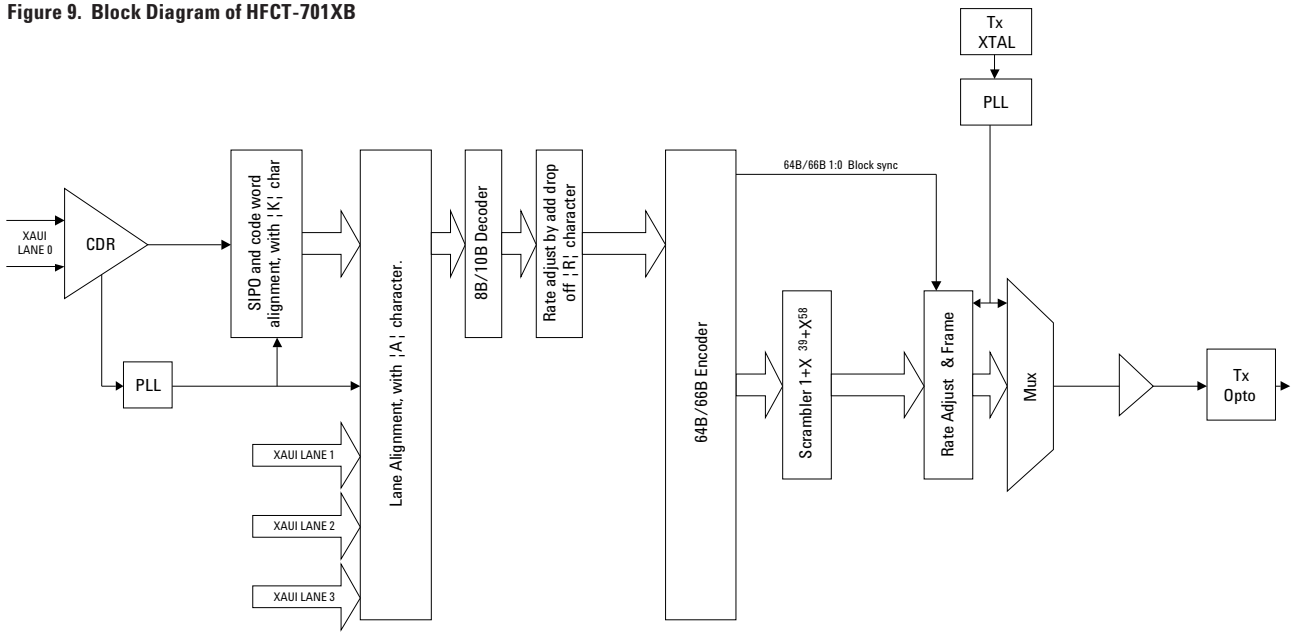



**Figure 10. Transmit Path High Level Overview**

### Receiver Path Summary

Figure 11 shows a block diagram of the receiver path, from the incoming 10.3125 Gb/s, 64B/66B encoded optical interface to the four 3.125 Gb/s differential 8B/10B encoded XAUI electrical output interface. The XAUI output drivers provide low-swing differential output with 100 Ω differential output impedance and are ac coupled.

### Management Data Input/Output (MDIO) Interface

The MDIO interface provides a simple, two wire, serial interface to connect a station management entity (STA) and a managed PHY for the purpose of controlling the PHY and gathering status from the PHY. The management interface consists of the two wire physical interface, a frame format, a protocol specification for exchanging the frames and a register set that can be read and written using these frames. The two wires of the physical interface are the Management Data Clock (MDC) and the Management Data I/O (MDIO).

### Management Data Clock (MDC)

The MDC is sourced by the Station Management entity (STA) to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal that has no maximum high or low times.

### Management Data I/O (MDIO)

MDIO is a bidirectional signal between the PHY (HFCT-701XB) and the STA. It is used to transfer control and status information. Data is always driven and sampled synchronously with respect to MDC. Figure 13 shows that MDIO open drain driver configuration.

### MDIO Timing relationship to MDC

MDIO is a bidirectional signal that can be sourced by the STA or the HFCT-701XB. When the STA sources the MDIO signal, the STA shall provide a minimum of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC (see Figure 12). When the MDIO signal is sourced by the HFCT-701XB, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock output delay from the HFCT-701XB shall be a minimum of 0 ns and a maximum of 300 ns.

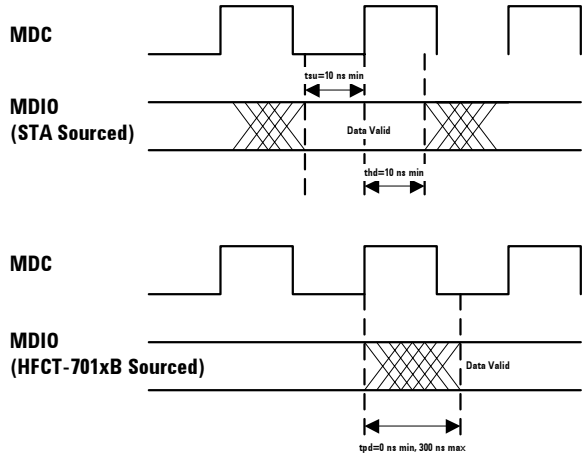



**Figure 12. MDIO/MDC Timing**

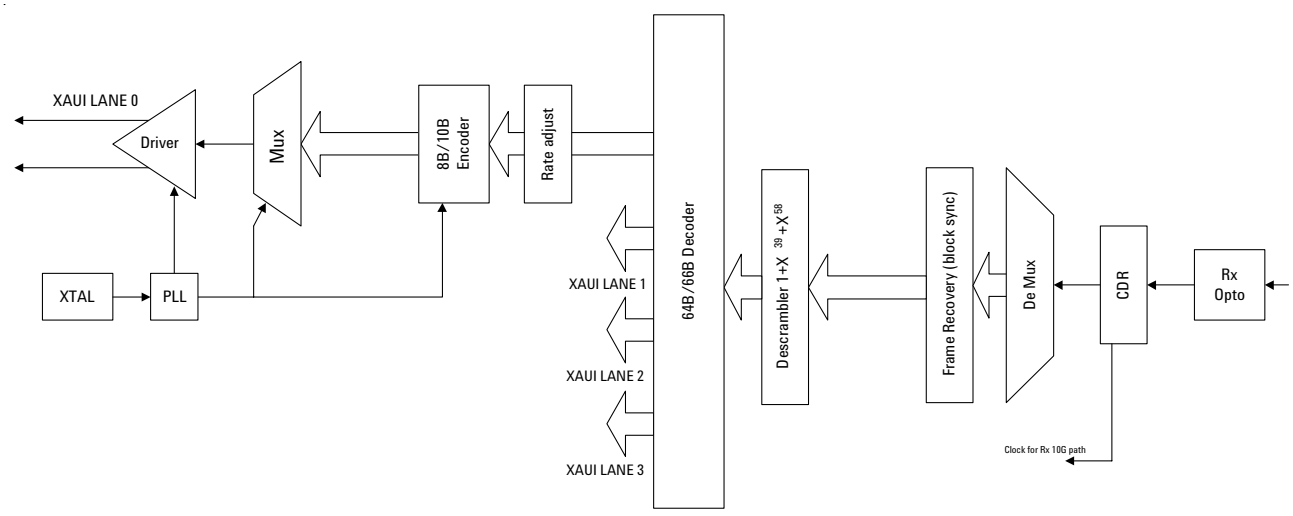



**Figure 11. Receive Path High Level Overview**

### Management Frame Format

The HFCT-701XB has an internal address register which is used to store the address for MDIO reads and writes. This MDIO address register can be set by using an address frame that specifies the register address to be accessed within a particular port device.

The following write, read or a post-read-increment-address frame to the same port device shall access the register whose address is stored in the HFCT-701XB MDIO address register. An address frame should be followed immediately by its associated write, read or post-read-increment-address frame.

Upon receiving a post-read-increment-address frame and having completed the read operation, the HFCT-701XB shall increment and store the address of the register accessed. If no address cycle is received before the next write, read or post-read-increment-address frame, then the HFCT-701XB shall use the stored address for that register access.

The Management Frame Format for Indirect Access is specified in Table 9.

### PRE - Preamble

At the beginning of each transaction the STA shall send a preamble sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC, to provide the HFCT-701XB with a pattern that it can use to establish synchronization. The HFCT-701XB must observe this preamble sequence before it responds to any transaction.

### ST - Start

The Start of Frame is indicated by a <00> pattern. This pattern ensures transitions from the default logic one line to zero and back to one.

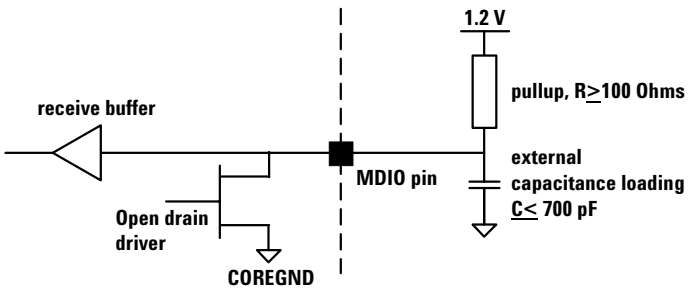



**Figure 13. MDIO open Drain Driver Configuration**

**Table 9. Frame Format**

| | Management Frame Fields | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **FRAME** | **PRE** | **ST** | **OP** | **PRTAD** | **DEVAD** | **TA** | **ADDR/DATA** | **IDLE** |
| ADDRESS | 1...1 | 00 | 00 | PRTAD[4:0] | DA[4:0] | 10 | D[15:0] | Z |
| WRITE | 1...1 | 00 | 01 | PRTAD[4:0] | DA[4:0] | 10 | D[15:0] | Z |
| READ | 1...1 | 00 | 11 | PRTAD[4:0] | DA[4:0] | Z0 | D[15:0] | Z |
| READ INC | 1...1 | 00 | 10 | PRTAD[4:0] | DA[4:0] | Z0 | D[15:0] | Z |

### OP - Operation Code

**Table 10. OP Code Definitions**

| OP Code | Operation |
|---|---|
| 00 | Register Address |
| 01 | Write Data |
| 11 | Read Data |
| 10 | Post Read Data + Increment |

### PRTAD

The Port Address is five bits, allowing 32 unique port addresses. HFCT-701XB's port address is set through pins PRTAD<0:4>.

### DEVAD

The Device Address is five bits, allowing 32 unique devices per port. The HFCT-701XB supports device addresses 1 (PMA/PMD), 3 (PCS) and 4 (PHY XS).

### TA

The Turnaround time is a two bit time spacing between the Register Address field and the Data field of a management frame to avoid contention during a read transaction (see IEEE 802.3ae).

### ADDR/DATA

The Data/Address field is 16 bits. The first bit transmitted/received is bit 15 and the last bit is bit 0.

### IDLE

The idle condition is a high-impedance state. The MDIO line will be pulled to a one.

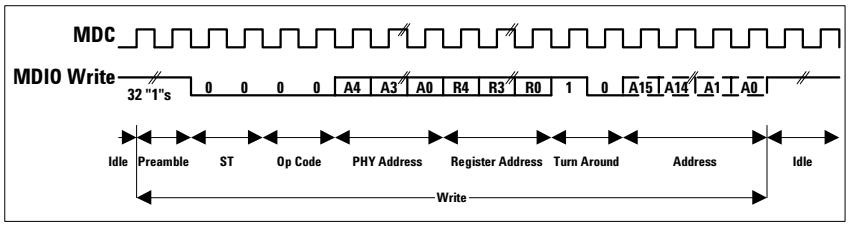
### EEPROM Interface

### NVR

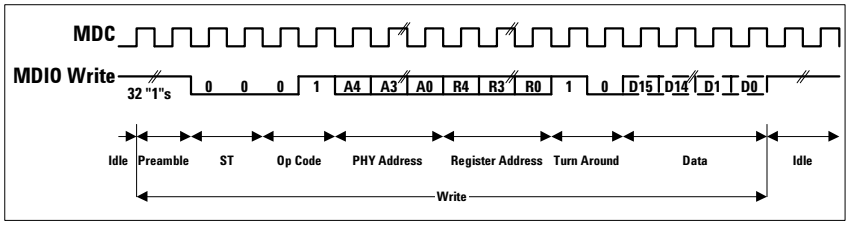
There are two main memory/register types in the HFCT-701XB which comply with the IEEE 802.3ae and XENPAK standard: volatile and nonvolatile. These areas can be further divided into user readable and writeable areas.

At power up the module register space is initialized and, where appropriate, default values are loaded from the non user accessible nonvolatile memory. The user accessible nonvolatile memory is also uploaded entirely into the user accessible volatile memory.

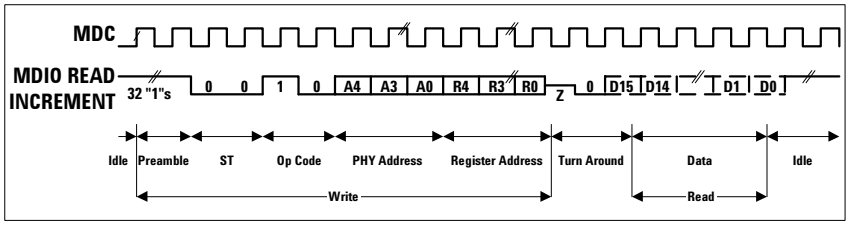
**DEVICE MANAGEMENT INTERFACE - ADDRESS FRAME STRUCTURE**




**DEVICE MANAGEMENT INTERFACE - WRITE FRAME STRUCTURE**




**DEVICE MANAGEMENT INTERFACE - READ INCREMENT FRAME STRUCTURE**




**DEVICE MANAGEMENT INTERFACE - READ FRAME STRUCTURE**

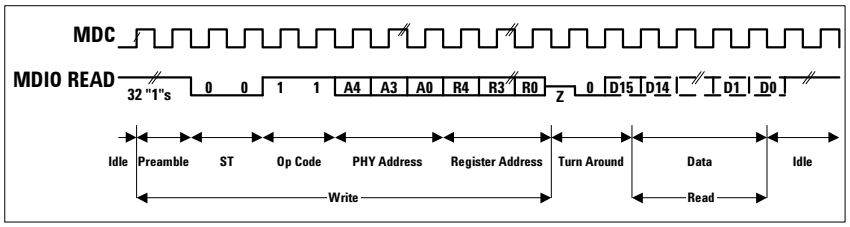



**Figure 14. MDIO Frame Formats**

It is important to note that writes to the user accessible volatile memory are not stored to the corresponding user nonvolatile area and will therefore be lost upon a power down or reset. For such writes to be permanent the data must be written first to the user accessible nonvolatile area and then a reload invoked via the NVR Control/Status register, see Register 1.32768.

**Access**
The XENPAK MSA related Nonvolatile Control/Status register is only needed for performing writes to the nonvolatile user accessible area within the HFCT-701XB because nonvolatile memory cannot be written to by normal MDIO write cycles. Other writes to volatile memory and registers may be performed directly via normal MDIO write cycles. All volatile and nonvolatile locations may be read directly via MDIO read cycles, it is not necessary to use the NVR Control/Status register, other than for status.

**Read/Write Command (bit5)**
The XENPAK MSA related 1.32768.5 register must be set to 1 to perform writes to the NVR and zero (read) otherwise a zero written to bit 5 initiates an NVR read. A 1 written to bit 5 initiates an NVR write.

If the NVR register bit 5 is set to zero and the extended command bits set to 11 forces an upload of all values in the NVR to the volatile areas, including default register values. Such an upload is performed automatically after a hard or soft reset.

**EEPROM Checksum Checking**
The HFCT-701XB will perform a checksum calculation and compare after every successful 256 byte read. The checksum for comparison is in EEPROM register 118 =MDIO register 1.32893.7:0. The checksum is equal to the 8 LSB 's of the sum of bytes 0 to 117 of the EEPROM. The calculated checksum is stored in MDIO register 1.49156.15:8. The result of the calculated checksum compared with the one read from EEPROM is placed in MDIO register 1.49155.7.

**EEPROM 256 Byte Read Cycle**
An EEPROM 256 Byte Read Cycle is initiated by setting MDIO bits 1.32768.0,1 to 0 and 1.32768.5 to 0.

The information to be read from the EEPROM stored in the 256 MDIO registers. A 256 byte read is initiated on hot plug or reset.

**EEPROM Single Byte Read or Write Cycle**
An EEPROM Single Byte Read/ Write Cycle is initiated by setting MDIO EEPROM control register bits 1.32768.1:0 to 10. As for the 256 byte read/write commands, MDIO register 1.32768.5 determines if a read or a write cycle will be performed. The single byte EEPROM address is read from EEPROM control register 1.32768 bit15:8. The data is placed in/read from the associated MDIO register.

**Monitors and Diagnostic Features**
The LASI pin is used to indicate suboptimal performance in either the receive or transmit path. It can be used as an interrupt. It is the OR of the tx_alarm, rx_alarm and the ls_alarm signals each gated with their respective enables. The enables are read from MDIO register 1.36867, LASI control.

LASI ={OR of (reg 1.36869.n 'bit wise AND ' reg 1.36866.n) for n=0 to 15}.

**Table 11. LASI Control Registers**

| Description | MDIO Status Registers | Type | MDIO Enable Registers | Default Value |
|---|---|---|---|---|
| LS_ALARM | 1.36869.0 | RO/LH | 1.36866.0 | 0 |
| TX_ALARM | 1.36869.1 | RO/LH | 1.36866.1 | 0 |
| RX_ALARM | 1.36869.2 | RO/LH | 1.36866.2 | 0 |
| LASI test mode | 1.36869.3 | RW | 1.36866.3 | 0 |
| 1.8 V supply too low | 1.36869.4 | RO/LH | 1.36866.4 | 0 |
| 3.3 V supply too low | 1.36869.5 | RO/LH | 1.36866.5 | 0 |
| MON3P3V_IN voltage too low | 1.36869.6 | RO/LH | 1.36866.6 | 0 |

**ls_alarm**
LS Alarm is latched high each time the link_status signal changes state. LS_ALARM is the output of this latch AND the LS_ALARM enable register (see Figure 15). link_status is an indicator of the link health.

link_status = {PMD signal detect (MDIO 1.10.0) AND PCS block_lock (MDIO 3.32.0) AND PHY_XS lane_alignment (MDIO 4.24.12)}

**tx_alarm**
tx_alarm is used to indicate a problem with the transmit path. tx_alarm is the OR of several transmit path status registers in MDIO registers 1.36868 bit wise AND'd with the TX_ALARM enable register. The ORing of each term is enabled by a companion MDIO register in 1.36865.

tx_alarm = {OR of (reg 1.36868 'bit wise AND' reg 1.36865) for n=0 to 15} AND {TX_ALARM enable (reg 1.36866)}

**Table 12. Receive Alarm Registers**

| Description | MDIO Status Registers (RO) | Mirrors | Type | MDIO Enable Registers (R/W) | Default |
|---|---|---|---|---|---|
| PHY_XS receive local fault | 1.36867.0 | 4.8.10 | RO/LH | 1.36864.0 | 1 |
| PHY_XS receive rate error | 1.36867.1 | 1.49154.3 | RO/LH | 1.36864.1 | 0 |
| PCS receive code violation | 1.36867.2 | | RO/LH | 1.36864.2 | 0 |
| PCS receive local fault | 1.36867.3 | 3.8.11 | RO/LH | 1.36864.3 | 0 |
| PMA receive local fault | 1.36867.4 | 1.8.11 | RO/LH | 1.36864.4 | 1 |
| Receive power error | 1.36867.5 | | RO/LH | 1.36864.5 | 0 |

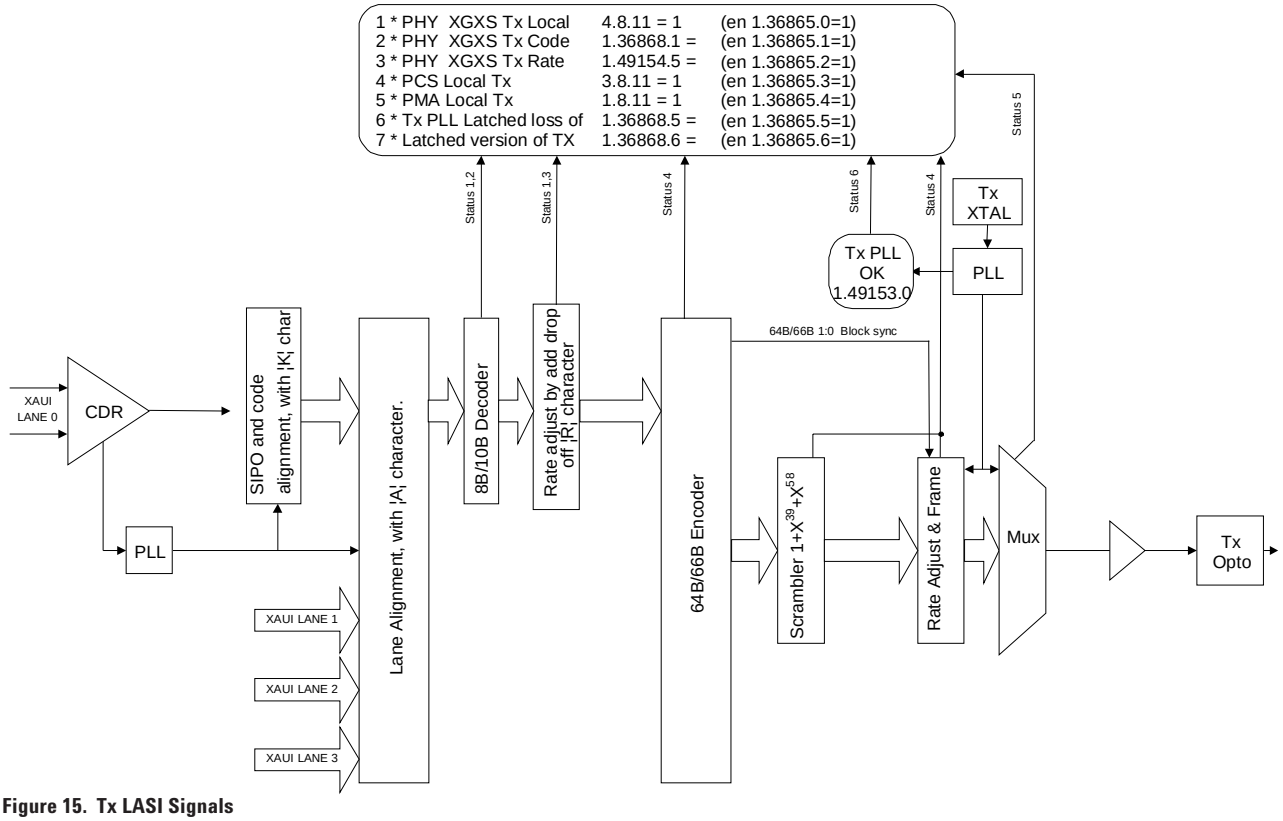



**Figure 15. Tx LASI Signals**

**Rx_alarm**

rx_alarm is used to indicate a problem with the receive path. rx_alarm is the OR of several receive path status registers in MDIO registers 1.36867. The ORing of each term is enabled by a companion MDIO register in 1.36864 and the overall output is enabled by the RX_ALARM enable register (1.36866.2h).

**Table 13. Transmit Alarm Registers**
**rx_alarm ={OR of (reg 1.36867 'bit wise AND ' reg 1.36864..n) for n=0 to 15} AND {RX_ALARM enable (1.36866.2h})**

| Description | MDIO Status Registers (RO) | Mirrors | Type | MDIO Enable Registers (R/W) | Default |
|---|---|---|---|---|---|
| PHY_XS transmit local fault | 1.36868.0 | 4.8.11 | RO/LH | 1.36865.0 | 1 |
| PHY_XS code error | 1.36868.1 | - | RO/LH | 1.36865.1 | 0 |
| PHY_XS transmit rate error | 1.36868.2 | 1.49154.5 | RO/LH | 1.36865.2 | 0 |
| PCS transmit local fault | 1.36868.3 | 3.8.11 | RO/LH | 1.36865.3 | 1 |
| PMA transmit local fault | 1.36868.4 | 1.8.11 | RO/LH | 1.36865.4 | 1 |
| latched version of txlock | 1.36868.5 | 1.49153.0 | RO/LH | 1.36865.5 | 0 |
| latched version of TXFAULT | 1.36868.6 | | RO/LH | 1.36865.6 | 1 |
| laser temperature error | 1.36868.7 | | RO/LH | 1.36865.7 | 0 |
| laser bias error | 1.36868.8 | | RO/LH | 1.36865.8 | 0 |
| Tx output power error | 1.36868.9 | | RO/LH | 1.36865.9 | 0 |

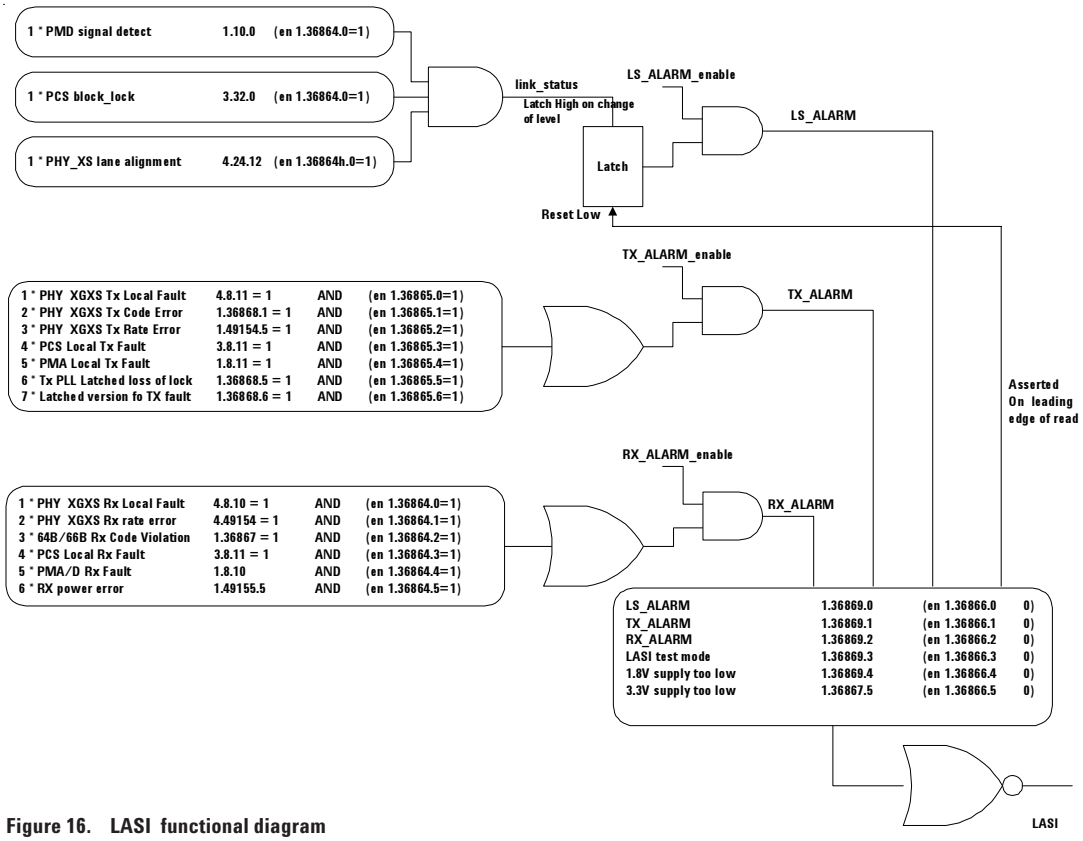



**Figure 16. LASI functional diagram**

**Loopbacks**

When in any system (PMA, PCS or XGXS system) loopback mode the HFCT-701XB shall accept data from the transmit path and return it on the receive path.

During PMA loopback the XENPAK module will transmit the data received at the XAUI i/p's. In XGXS system loopback, the laser will default to mean power but without any modulation. In PCS loopback mode a continuous pattern of 0x0F0F will be output. Transmit data will be output instead if the associated 'loopback data out enable bit ' is set high for the enabled loopback mode.

When in PMA network loopback mode, the recovered and retimed 10.3125 GBd signal is looped to the transmitter. The receive path XAUI output data will be received data. XAUI idle codes will be output instead of the received data if the 'network loopback data out enable bit ' is set high.

In IEEE 802.3ae standard XGXS network loopback the recovered received data is looped back to the transmit path in the XAUI block.

Enabling of more than one loopback path is invalid.

**Reset Operation**

Writing a '1' to any of MDIO registers 1.0.15, 3.0.15 or 4.0.15 causes all the HFCT-701XB registers to be reset to their default values. These bits are all self-clearing after the reset function is complete.

Pulling the RESET pin low causes a full chip reset.

Writes to any bits of the Control register while the RESET is asserted are ignored. All status and control registers are reset to their default states. The NVR read sequence is started when RESET goes high. MDIO register bits 1.0.15, 3.0.15, and 4.0.15 will be held to 1 until the reset sequence is complete.

**Table 14. Loopback Summary**

| loopback name | loopback direction | loopback control register | bypassed path default output | data output enable register | bypassed path output control' =1 |
|---|---|---|---|---|---|
| PMA system loopback | Tx -> Rx | 1.0.0 | transmit data | NA | NA |
| PCS loopback | Tx -> Rx | 3.0.14 | 0F0F | 3.49152.5 | transmit data |
| XGXS network loopback (802.3ae standard) | Rx -> Tx | 4.0.14 | Receive data at Rx Xaui | NA | NA |
| XGXS system loopback | Tx -> Rx 4 | 4.49152.14 | Mean power, no modulation | 4.49152.15 | transmit data |
| PMA network loopback | Rx -> Tx 1 | 1.49153.4 | received data | 1.49153.9 | idle at RxXAUI |

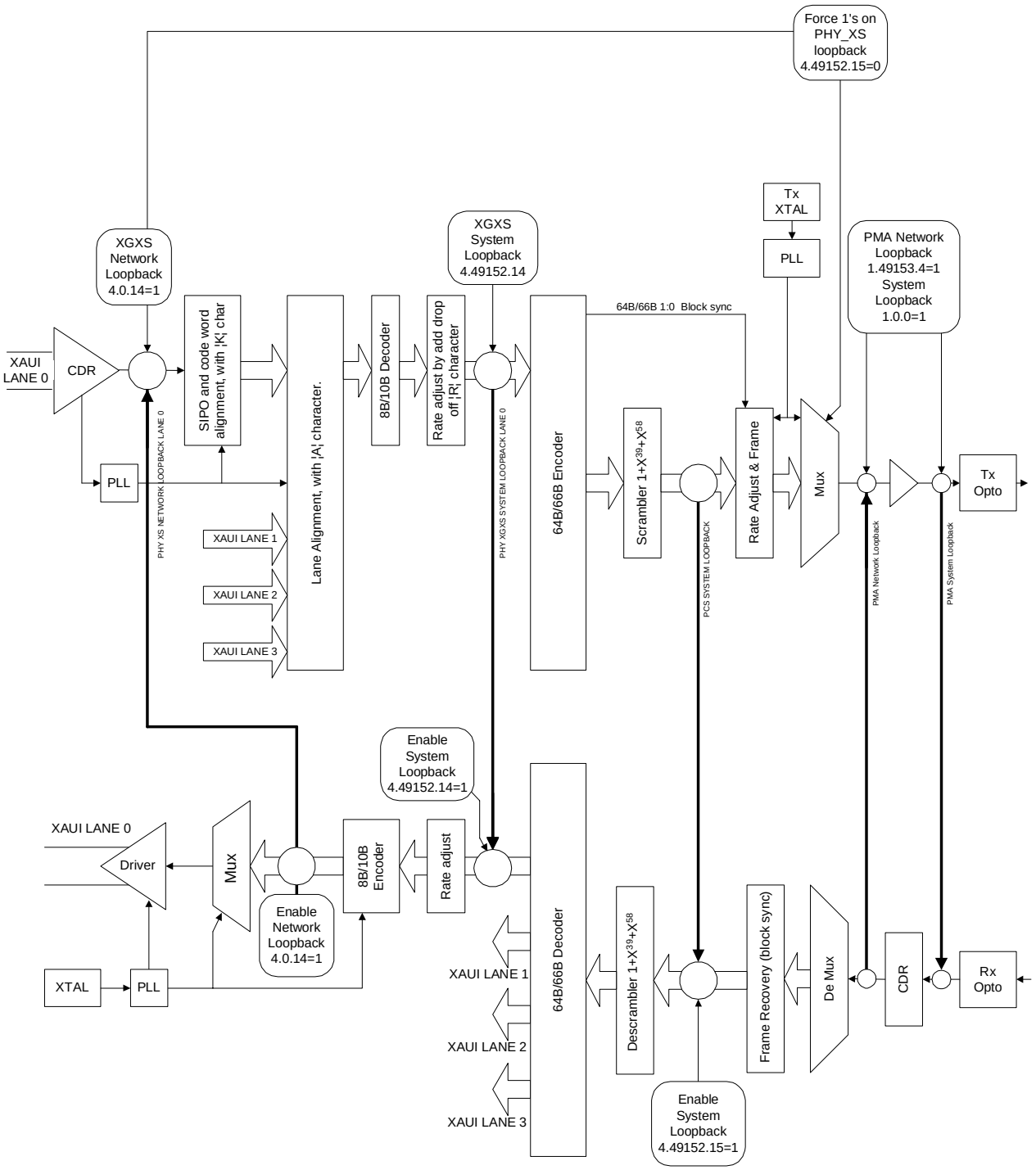



**Figure 17. HFCT-701XB Loopback Modes**

**Internal Clock Functionality**

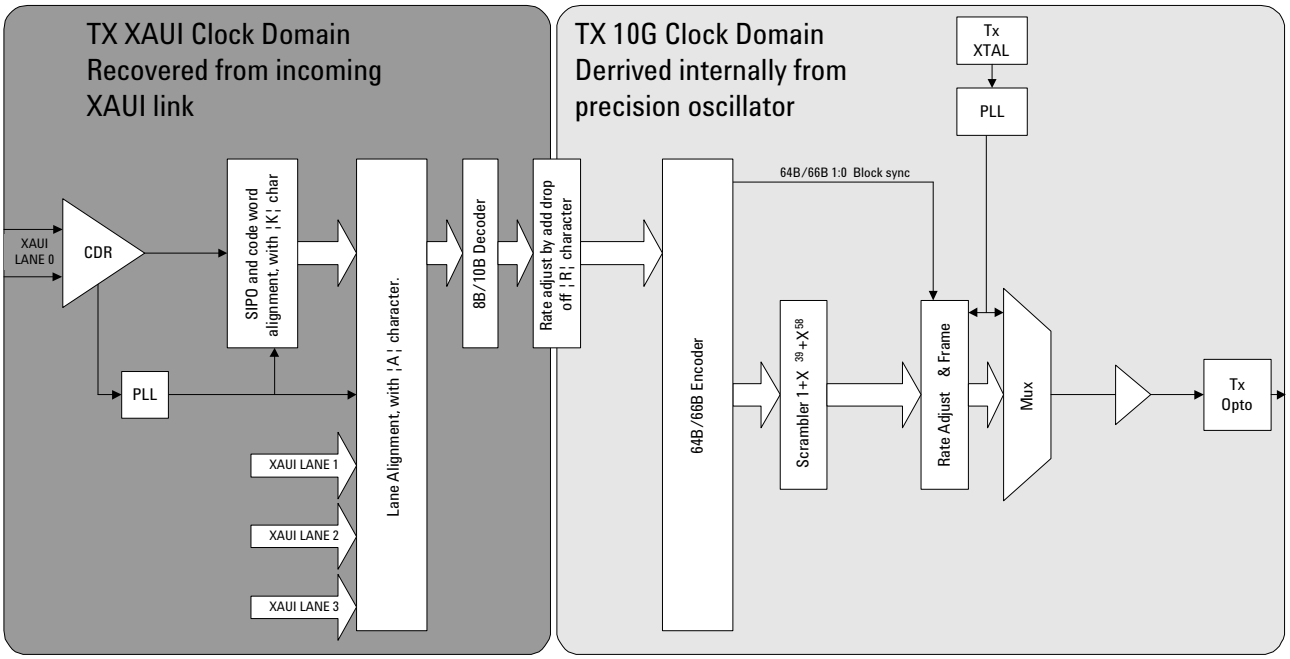



**Figure 18. Transmit Path**

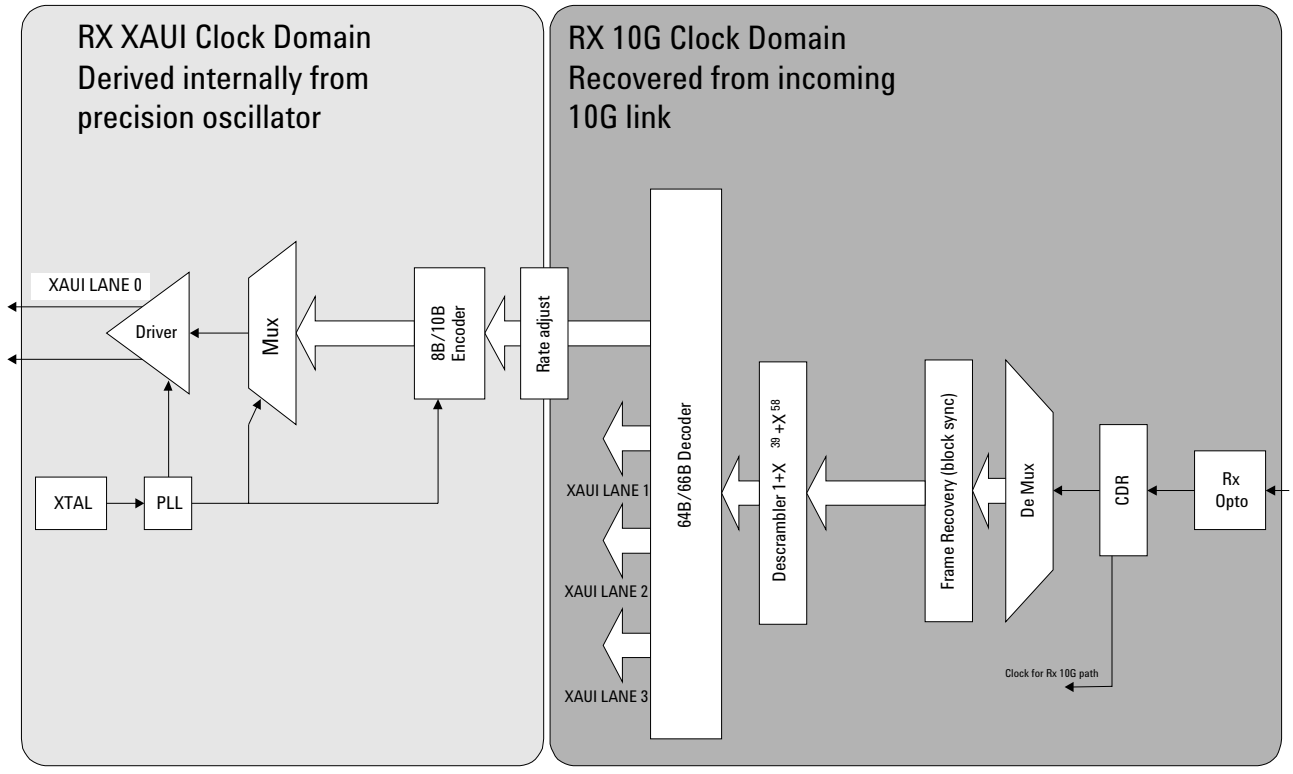



**Figure 19. Receive Path**

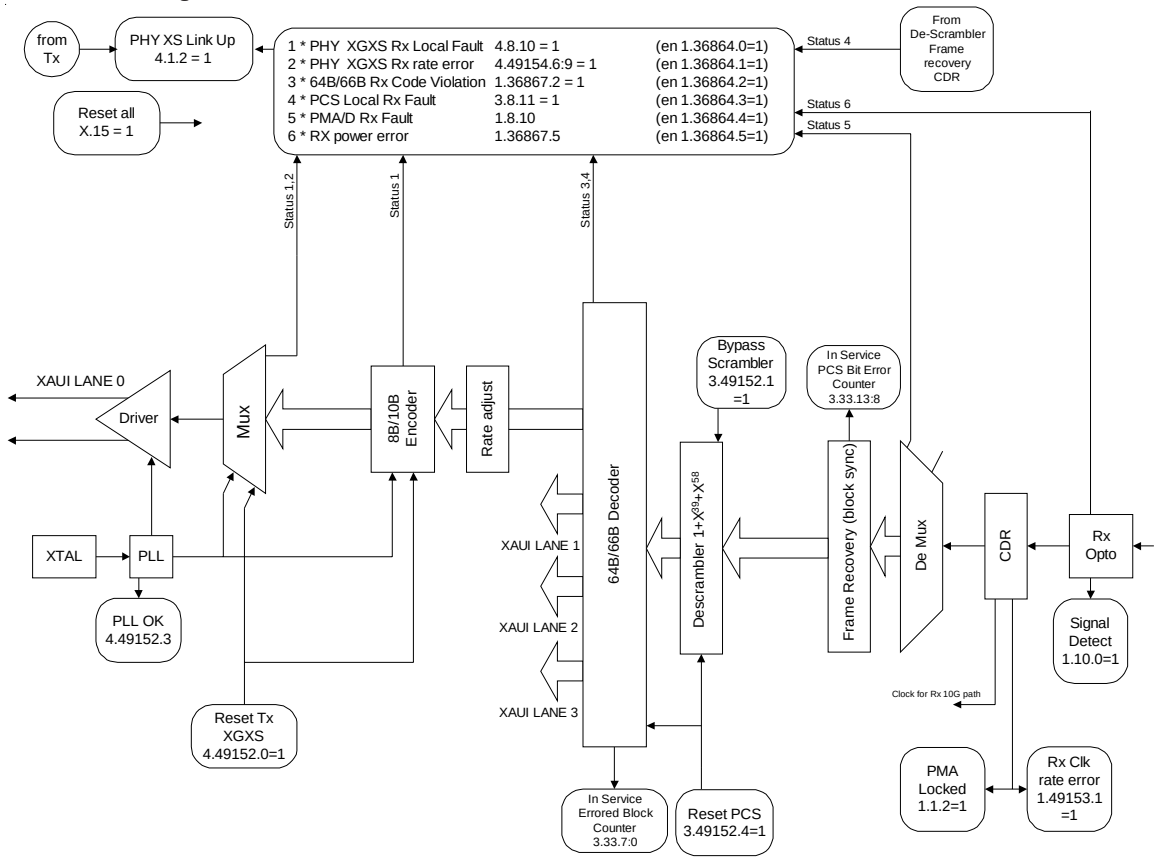



**Figure 20. Summary of Key Receiver Path Registers**

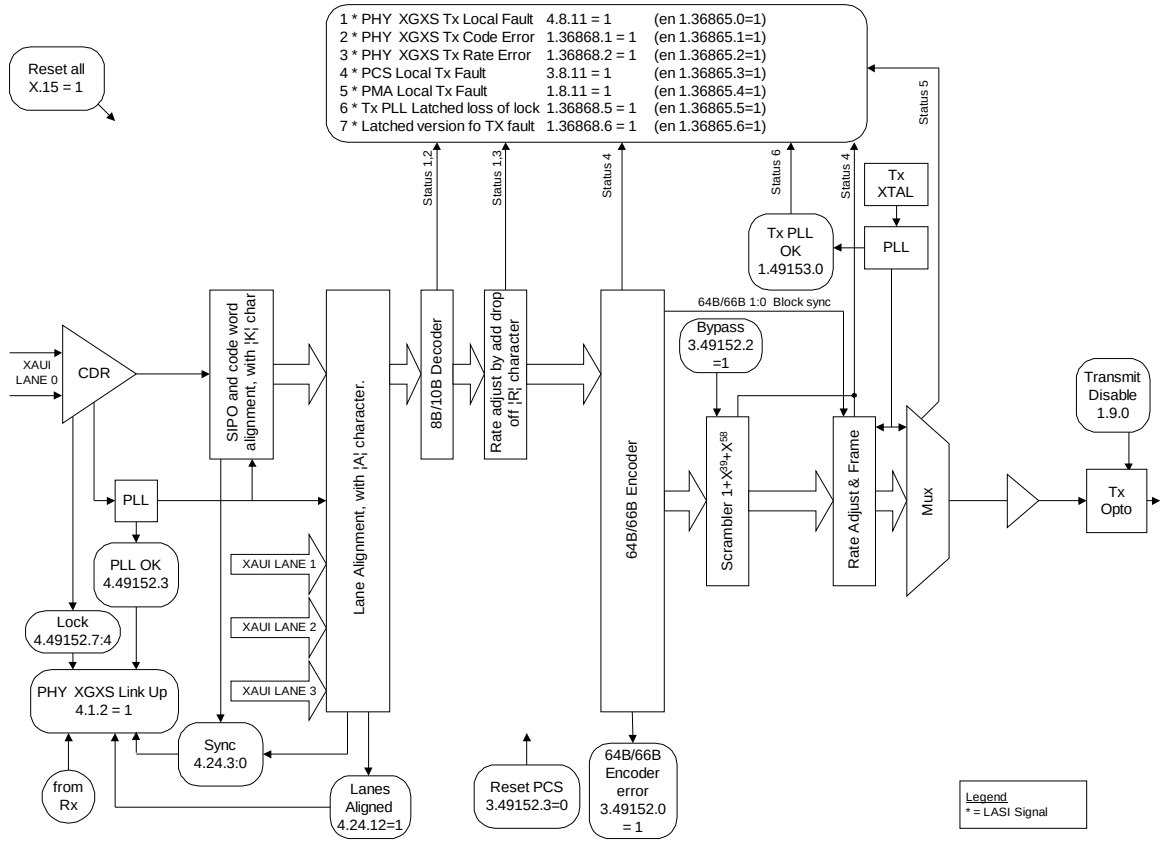



**Figure 21. Summary of Key Transmit Path Registers**

**HFCT-701XB Device 1 PMA/PMD Registers**

| Device | From Decimal | Hex | To Decimal | Hex | Register Name |
|---|---|---|---|---|---|
| 1 | 0 | 0 | | | PMA/PMD Control 1 |
| 1 | 1 | 1 | | | PMA/PMD Status 1 |
| 1 | 2 | 2 | 3 | 3 | Device identifier |
| 1 | 4 | 4 | | | PMA/PMD Speed Ability |
| 1 | 5 | 5 | 6 | 6 | Devices in package |
| 1 | 7 | 7 | | | 10G PMA/PMD Control 2 |
| 1 | 8 | 8 | | | 10G PMA/PMD Status 2 |
| 1 | 9 | 9 | | | 10G PMD transmit disable |
| 1 | 10 | A | | | 10G PMD receive signal detect |
| 1 | 14 | E | 15 | F | Package identifier (OUI) |
| 1 | 32768 | 8000 | | | NVR Control/Status |
| 1 | 32775 | 8007 | | | XENPAK MSA version supported |
| 1 | 32776 | 8008 | 32777 | 8009 | NVR size in bytes |
| 1 | 32778 | 800A | 32779 | 800B | Number of bytes used |
| 1 | 32780 | 800C | | | Basic Field Address |
| 1 | 32781 | 800D | | | Customer Field Address |
| 1 | 32782 | 800E | | | Vendor Field Address |
| 1 | 32783 | 800F | 32784 | 8010 | Extended Vendor Field Address |
| 1 | 32785 | 8011 | | | Reserved |
| 1 | 32786 | 8012 | | | Transceiver type |
| 1 | 32787 | 8013 | | | Optical connector type |
| 1 | 32788 | 8014 | | | Bit encoding |
| 1 | 32789 | 8015 | 32790 | 8016 | Nominal Bit Rate in multiples of 1Mb/s |
| 1 | 32791 | 8017 | | | Protocol Type |
| 1 | 32792 | 8018 | 32801 | 8021 | Standards Compliance Codes 10GbE Code Byte 0 |
| 1 | 32802 | 8022 | 32803 | 8023 | Specifies transmission range in 10 m increments |
| 1 | 32804 | 8024 | 32805 | 8025 | Fibre Type Byte 0 and Byte1 |
| 1 | 32806 | 8026 | 32808 | 8028 | Centre Optical Wavelength in 0.01nm steps - Channel 0 |
| 1 | 32818 | 8032 | 32821 | 8035 | Package Identifier OUI |
| 1 | 32822 | 8036 | 32825 | 8039 | Transceiver Vendor OUI |

| Device | From Decimal | Hex | To Decimal | Hex | Register Name |
|---|---|---|---|---|---|
| 1 | 32826 | 803A | 32841 | 8049 | Transceiver vendor name in ASCII |
| 1 | 32842 | 804A | 32857 | 8059 | Part number provided by transceiver vendor in ASCII |
| 1 | 32858 | 805A | 32859 | 805B | Revision level for part number provided by vendor ASCII |
| 1 | 32860 | 805C | 32875 | 806B | Vendor serial number in ASCII |
| 1 | 32876 | 806C | 32885 | 8075 | Vendor manufacturing date code in ASCII |
| 1 | 32886 | 8076 | | | 5 V stressed environment reference |
| 1 | 32887 | 8077 | | | 3.3 V stressed environment reference |
| 1 | 32888 | 8078 | | | APS stressed environment reference |
| 1 | 32889 | 8079 | | | Nominal APS voltage |
| 1 | 32890 | 807A | | | DOM capability |
| 1 | 32891 | 807B | | | Reserved |
| 1 | 32893 | 807D | | | Basic Field Checksum |
| 1 | 32894 | 807E | 32941 | 80AD | Customer Writeable Area |
| 1 | 32942 | 80AE | 33030 | 8106 | Vendor Specific |
| 1 | 33031 | 8107 | 36863 | 8FFF | Extended Vendor Specific |
| 1 | 36864 | 9000 | | | RX_ALARM Control |
| 1 | 36865 | 9001 | | | TX_ALARM Control |
| 1 | 36866 | 9002 | | | LASI Control |
| 1 | 36867 | 9003 | | | RX_ALARM Status |
| 1 | 36868 | 9004 | | | TX_ALARM Status |
| 1 | 36869 | 9005 | | | LASI Status |
| 1 | 49153 | C001 | | | Extended PMA features |
| 1 | 49155 | C003 | | | PMA/PMD Vendor Specific |
| 1 | 49156 | C004 | | | PMA/PMD Vendor Specific Checksum |
| 1 | 49188 | C024 | | | PMA Vendor Specific |

**Register 1.0 - PMA/PMD Control 1**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.0.15 | Reset | 1 = PMA/PMD reset<br>0 = Normal operation | RW | |
| 1.0.14 | Reserved | Value always 0, writes ignored | RW | |
| 1.0.13 | Speed selection | 1 = Operation at 10 Gb/s and above<br>0 = Unspecified | RW | 1 |
| 1.0.12 | Reserved | Value always 0, writes ignored | RW | |
| 1.0.11 | Low Power | 1 = Low Power mode<br>0 = Normal operation | RW | 0 |
| 1.0.10:7 | Reserved | Value always 0, writes ignored | RW | |
| 1.0.6 | Speed selection | 1 = Operation at 10 Gb/s and above<br>0 = Unspecified | RW | 1 |
| 1.0.5:2 | Speed selection | 5 4 3 2<br>1 x x x = Reserved<br>x 1 x x = Reserved<br>x x 1 x = Reserved<br>0 0 0 1 = Reserved<br>0 0 0 0 = 10 Gb/s | RW | |
| 1.0.1 | Reserved | Values always 0, writes ignored | RW | |
| 1.0.0 | PMA loopback | 1 = Enable PMA loopback mode<br>0 = Disable PMA loopback mode | RW | 0 |

**Register 1.1 - PMA/PMD Status 1**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.1.15:8 | Reserved | N/A | RO | |
| 1.1.7 | Fault | 1 = Local fault condition detected in PMA/PMD<br>0 = Local fault condition not detected in PMA/PMD<br>(Set to a 1 when either 1.8.11 or 1.8.10 set to a one) | RO | N/A |
| 1.1.6:3 | Reserved | N/A | RO/LL | |
| 1.1.2 | Receive link status | 1 = PMA locked to receive signal<br>0 = PMA not locked to receive signal | RO/LL | N/A |
| 1.1.1 | Power down ability | 1 = PMA/PMD supports low power mode<br>0 = PMA/PMD does not support low power mode | RO | 1 |
| 1.1.0 | Reserved | N/A | | |

**Register 1.2 to 1.3 - Device Identifier**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.3.15:0 | PMA Identifier | | RO | |
| 1.2.15:0 | PMA Identifier | | RO | |

**Register 1.4 PMA/PMD Speed Ability**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.4.15:1 | Reserved for future speeds | | RO | N/A |
| 1.4.0 | 10 G capable | 1 = PMA/PMD is capable of operating at 10 Gb/s<br>0 = PMA/PMD is not capable of operating at 10Gb/s | RO | 1 |

**Note:**
1. RW = Read/Write, RO = Read Only, LL = Latching Low

**Register 1.5 to 1.6 - PMA/PMD Devices in Package**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.6.15 | Vendor Specific Device 2 present | 1 = Vendor specific device 2 present in package<br>0 = Vendor specific device 2 not present in package | RO | 1 |
| 1.6.14 | Vendor Specific | Reserved | RO | |
| 1.6.13:0 | Reserved | N/A | RO | |
| 1.5.15:6 | Reserved | N/A | RO | |
| 1.5.5 | DTE XS present | 1 = DTE XS present in package<br>0 = DTE XS not present in package | RO | 0 |
| 1.5.4 | PHY XS present | 1 = PHY XS present in package<br>0 = PHY XS not present in package | RO | 1 |
| 1.5.3 | PCS present | 1 = PCS present in package<br>0 = PCS not present in package | RO | 1 |
| 1.5.2 | WIS present | 1 = WIS present in package<br>0 = WIS not present in package | RO | 0 |
| 1.5.1 | PMD/PMA present | 1 = PMD/PMA present in package<br>0 = PMD/PMA not present in package | RO | 1 |
| 1.5.0 | Clause 22 registers present | 1 = Clause 22 registers present in package<br>0 = Clause 22 registers not present in package | RO | 0 |

**Register 1.7 - 10 G PMA/PMD Control 2**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.7.15:3 | Reserved | N/A | | |
| 1.7.2:0 | PMA/PMD type selection | 2 1 0<br>1 1 1 = 10GBASE-SR PMA/PMD type<br>1 1 0 = 10GBASE-LR PMA/PMD type<br>1 0 1 = 10GBASE-ER PMA/PMD type<br>1 0 0 = 10GBASE-LX4 PMA/PMD type<br>0 1 1 = 10GBASE-SW PMA/PMD type<br>0 1 0 = 10GBASE-LW PMA/PMD type<br>0 0 1 = 10GBASE-EW PMA/PMD type<br>0 0 0 = Reserved | RW | 110 |

**Note:**
1. RW = Read/Write, RO = Read Only,

**Register 1.8 - 10 G PMA/PMA Status 2**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.8.15:14 | Device present | 15 14<br>1 0 = Device responding at this address<br>1 1 = No device responding at this address<br>0 1 = No device responding at this address<br>0 0 = No device responding at this address | RO | 10 |
| 1.8.13 | Transmit local fault ability | 1 = PMA/PMD has the ability to detect a local fault condition on the transmit path<br>0 = PMA/PMD does not have the ability to detect a fault condition on the transmit path | RO | 1 |
| 1.8.12 | Receive local fault ability | 1 = PMA/PMD has the ability to detect a local fault condition on the receive path<br>0 = PMA/PMD does not have the ability to detect a fault condition on the receive path | RO | 1 |
| 1.8.11 | Transmit local fault | 1 = Local fault condition on transmit path<br>0 = No local fault condition on transmit path | RO/LH | N/A |
| 1.8.10 | Receive local fault | 1 = Local fault condition on receive path<br>0 = No local fault condition on receive path | RO/LH | N/A |
| 1.8.9 | Reserved | N/A | RO | |
| 1.8.8 | PMD transmit disable ability | 1 = PMD has the ability to disable the transmit path<br>0 = PMD does not have the ability to disable the transmit path | RO | 1 |
| 1.8.7 | 10GBASE-SR ability | 1 = PMA/PMD is able to perform 10GBASE-SR<br>0 = PMA/PMD is not able to perform 10GBASE-SR | RO | 0 |
| 1.8.6 | 10GBASE-LR ability | 1 = PMA/PMD is able to perform 10GBASE-LR<br>0 = PMA/PMD is not able to perform 10GBASE-LR | RO | 1 |
| 1.8.5 | 10GBASE-ER ability | 1 = PMA/PMD is able to perform 10GBASE-ER<br>0 = PMA/PMD is not able to perform 10GBASE-ER | RO | 0 |
| 1.8.4 | 10GBASE-LX4 ability | 1 = PMA/PMD is able to perform 10GBASE-LX4<br>0 = PMA/PMA is not able to perform 10GBASE-LX4 | RO | 0 |
| 1.8.3 | 10GBASE-SW ability | 1 = PMA/PMD is able to perform 10GBASE-SW<br>0 = PMA/PMD is not able to perform 10GBASE-SW | RO | 0 |
| 1.8.2 | 10GBASE-LW ability | 1 = PMA/PMD is able to perform 10GBASE-SW<br>0 = PMA/PMD is not able to perform 10GBASE-LW | RO | 0 |
| 1.8.1 | 10GBASE-EW ability | 1 = PMA/PMD is able to perform 10GBASE-EW<br>0 = PMA/PMD is not able to perform 10GBASE-EW | RO | 0 |
| 1.8.0 | PMA loopback ability | 1 = PMA has the ability to perform a loopback function<br>0 = PMA does not have the ability to perform a loopback function | RO | 1 |

**Register 1.9 - 10 G PMD Transmit Disable**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.9.15:5 | Reserved | N/A | RW | |
| 1.9.4:1 | LX4 Signal Detect | Not used | RW | 0 |
| 1.9.4:0 | PMD Transmit Disable | 1 = Transmit disable<br>0 = Transmit enable | RW | 0 |

**Note:**

1. RW = Read/Write, RO = Read Only, LH = Latch High, clear on read (note that if the condition exitsts following register read, the bit will not be cleared).

### Register 1.10 - 10 G PMD Receive Signal OK

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.10.15:5 | Reserved | Value always 0, writes ignored | RO | |
| 1.10.4:1 | LX4 Signal Detect | Not used | RO | |
| 1.10.0 | Global PMD Receive signal detect | 1 = Signal detected on receive<br>0 = Signal not detected on receive | RO | |

### Register 1.14 to 1.15 - Package Identifier (OUI)

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.15.15 | Reserved | Reserved | RO | 248 |
| 1.15.14:11 | Revision Number | Revision Number | RO | |
| 1.15.11:8 | NVR Address | NVR DEV Address | RO | |
| 1.15.7:6 | NVR Address | NVR DEV Address | RO | |
| 1.15.5:0 | Package Identifier | XENPAK OUI | RO | |
| 1.14.15:8 | Package Identifier | XENPAK OUI | RO | 34 |
| 1.14.7:0 | Package Identifier | XENPAK OUI | RO | |

### Register 1.32768 - NVR Control/Status

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.32768.15:9 | Vendor Specific | | RW | |
| 1.32768.7:6 | Reserved | N/A | RO | |
| 1.32768.5 | Read/Write Command[3] | 0 = Read NVR<br>1 = Write NVR | RW[2] | |
| 1.32768.4 | Reserved | N/A | RO | |
| 1.32768.3:2 | Command Status | 00 = Idle<br>01 = Command completed successfully<br>10 = Command in progress<br>11 = Command failed | RO/LH | |
| 1.32768.1:0 | Extended Commands | 00 = Reserved<br>01 = Reserved<br>10 = Read/Write 1 byte<br>11 = Read all NVR contents | RW[2] | |

### 1.32775 to 1.32782 - NVR Information

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32775.7:0 | Version | NVR Version number (MSB:LSB) | RO | 30 |
| 1.32776.7:0 | NVR_Size | NVR Size (upper byte) = 256 bytes | RO | 1 |
| 1.32777.7:0 | NVR_Size | NVR Size (lower byte) = 256 bytes | RO | 0 |
| 1.32778.7:0 | Mem_Used | Bytes used (upper byte) = 256 bytes | RO | 1 |
| 1.32779.7:0 | Mem_Used | Bytes used (lower byte) = 256 bytes | RO | 0 |
| 1.32780.7:0 | Basic Addr | Basic Field Address (MSB:LSB) Start | RO | 11 |
| 1.32781.7:0 | Cust Addr | Customer Field Address (MSB:LSB) Start | RO | 119 |
| 1.32782.7:0 | Vend Addr | Vendor Field Address (MSB:LSB) Start | RO | 167 |
| 1.32783.7:0 | Ext Vend Addr | Extended Vendor Field Address Start | RO | 1 |
| 1.32784.7:0 | Ext Vend Addr | Extended Vendor Field Address Start | RO | 0 |
| 1.32785.7:0 | Reserved | | RO | 0 |

**Note:**

1. RW = Read/Write, RO = Read Only, LH = latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).
2. The values of the 'Command' and 'Extended Command' bits are held until a command has been executed.
3. Writes to register 1.32768 ignored during "command in progress". Reads will not clear command status.

**Register 1.32786 - Transceiver Type**

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32786.7:0 | Transceiver type | XENPAK | RO | 1 |

**Register 1.32787 - Optical Connector Type**

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32787.7:0 | Connector | SC Duplex Connector | RO | 1 |

**Register 1.32788 - Bit Encoding**

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32788.7:0 | Bit Encoding | NRZ | RO | 1 |

**Register 1.32789 to 1.32790 - Bit Rate**

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32789.7:0 | Bit rate | Bit 15 (MSB) to Bit 8 | RO | 40 |
| 1.32790.7:0 | Bit rate | Bit 7 to Bit 0 | RO | 72 |

**Register 1.32791 - Protocol Type**

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32791.7:0 | Protocol | Supports 10GbE | RO | 1 |

**Register 1.32792 to 1.32793 - 10GbE Compliance Code**

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32792.7:0 | Standards compliance code | Supports 10GBASE-LR | RO | 2 |
| 1.32793.15:0 | Reserved | N/A | | 0 |

**Register 1.32802 to 1.32803 - Transmission Range**

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32802.7:0 | Transmission Range | Bit 15 (MSB) to Bit 8 | RO | 3 |
| 1.32803.7:0 | Transmission Range | Bit 7 to Bit 0 | RO | 232 |

**Register 1.32804 to 1.32805 - Fiber Type Suitability**

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32804.5 | Fiber Type | SM Generic | RO | 32 |
| 1.32805.0 | Reserved | N/A | | 128 |

**Register 1.32806 to 1.32808 - Center Wavelength**

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32806.7:0 | Wavelength | Bits 23-16 | RO | 1 |
| 1.32807.7:0 | Wavelength | Bits 15-8 | RO | 255 |
| 1.32808.7:0 | Wavelength | Bits 7-0 | RO | 184 |

**Note:**

1. RW = Read/Write, RO = Read Only.

**Register 1.32818 to 1.32821 - Package Identifier (OUI) = Xenpak**

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32818.7:0 | Package Identifier | Package Identifier | RO | 0 |
| 1.32819.7:0 | Package Identifier | Package Identifier | RO | 65 |
| 1.32820.7:2 | Package Identifier | Package Identifier | RO | 244 |
| 1.32820.1:0 | NVR Address | NVR Device Address | RO | |
| 1.32821.7:5 | NVR Address | NVR Device Address | RO | 32 |
| 1.32821.4:1 | Revision Number | Revision Number | RO | |
| 1.32821.0 | Reserved | Reserved | | |

**Register 1.32822 to 1.32825 - Vendor (OUI) = Agilent**

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32822.7:0 | Vendor OUI | Vendor OUI | RO | 0 |
| 1.32823.7:0 | Vendor OUI | Vendor OUI | RO | 0 |
| 1.32824.7:2 | Vendor OUI | Vendor OUI | RO | 48 |
| 1.32824.1:0 | Model No | Model Number | RO | |
| 1.32825.7:4 | Model No | Model Number | RO | 211 |
| 1.32825.3:0 | Rev No | Revision Number | RO | |

**Register 1.32826 to 1.32841 - Vendor Name (ASCII)**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.32826.7:0 | Vendor Name | Vendor Name byte 15 (MSB:LSB) | RO | A (65) |
| 1.32827.7:0 | Vendor Name | Vendor Name byte 14 (MSB:LSB) | RO | G (71) |
| 1.32828.7:0 | Vendor Name | Vendor Name byte 13 (MSB:LSB) | RO | I (73) |
| 1.32829.7:0 | Vendor Name | Vendor Name byte 12 (MSB:LSB) | RO | L (76) |
| 1.32830.7:0 | Vendor Name | Vendor Name byte 11 (MSB:LSB) | RO | E (69) |
| 1.32831.7:0 | Vendor Name | Vendor Name byte 10 (MSB:LSB) | RO | N (78) |
| 1.32832.7:0 | Vendor Name | Vendor Name byte 9 (MSB:LSB) | RO | T (84) |
| 1.32833.7:0 | Vendor Name | Vendor Name byte 8 (MSB:LSB) | RO | SPACE (32) |
| 1.32834.7:0 | Vendor Name | Vendor Name byte 7 (MSB:LSB) | RO | SPACE (32) |
| 1.32835.7:0 | Vendor Name | Vendor Name byte 6 (MSB:LSB) | RO | SPACE (32) |
| 1.32836.7:0 | Vendor Name | Vendor Name byte 5 (MSB:LSB) | RO | SPACE (32) |
| 1.32837.7:0 | Vendor Name | Vendor Name byte 4 (MSB:LSB) | RO | SPACE (32) |
| 1.32838.7:0 | Vendor Name | Vendor Name byte 3 (MSB:LSB) | RO | SPACE (32) |
| 1.32839.7:0 | Vendor Name | Vendor Name byte 2 (MSB:LSB) | RO | SPACE (32) |
| 1.32840.7:0 | Vendor Name | Vendor Name byte 1 (MSB:LSB) | RO | SPACE (32) |
| 1.32841.7:0 | Vendor Name | Vendor Name byte 0 (MSB:LSB) | RO | SPACE (32) |

**Note:**
1. RW = Read/Write, RO = Read Only.

**Register 1.32842 to 1.32857 - Vendor Part Number (ASCII)**

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32842.7:0 | Vendor Part No | Vendor Part No. byte 15 (MSB:LSB) | RO | H (72) |
| 1.32843.7:0 | Vendor Part No | Vendor Part No. byte 14 (MSB:LSB) | RO | F (70) |
| 1.32844.7:0 | Vendor Part No | Vendor Part No. byte 13 (MSB:LSB) | RO | C (67) |
| 1.32845.7:0 | Vendor Part No | Vendor Part No. byte 12 (MSB:LSB) | RO | T (84) |
| 1.32846.7:0 | Vendor Part No | Vendor Part No. byte 11 (MSB:LSB) | RO | - (45) |
| 1.32847.7:0 | Vendor Part No | Vendor Part No. byte 10 (MSB:LSB) | RO | 7 (55) |
| 1.32848.7:0 | Vendor Part No | Vendor Part No. byte 9 (MSB:LSB) | RO | 0 (48) |
| 1.32849.7:0 | Vendor Part No | Vendor Part No. byte 8 (MSB:LSB) | RO | 1 (49) |
| 1.32850.7:0 | Vendor Part No | Vendor Part No. byte 7 (MSB:LSB) | RO | X (88) |
| 1.32851.7:0 | Vendor Part No | Vendor Part No. byte 6 (MSB:LSB) | RO | B (66) |
| 1.32852.7:0 | Vendor Part No | Vendor Part No. byte 5 (MSB:LSB) | RO | SPACE (32) |
| 1.32853.7:0 | Vendor Part No | Vendor Part No. byte 4 (MSB:LSB) | RO | SPACE (32) |
| 1.32854.7:0 | Vendor Part No | Vendor Part No. byte 3 (MSB:LSB) | RO | SPACE (32) |
| 1.32855.7:0 | Vendor Part No | Vendor Part No. byte 2 (MSB:LSB) | RO | SPACE (32) |
| 1.32856.7:0 | Vendor Part No | Vendor Part No. byte 1 (MSB:LSB) | RO | SPACE (32) |
| 1.32857.7:0 | Vendor Part No | Vendor Part No. byte 0 (MSB:LSB) | RO | SPACE (32) |

**Register 1.32858 to 1.32859 - Vendor Revision (ASCII)**

| Bit(s) | Name | Description | R/W[1] | Default Value (dec) |
|---|---|---|---|---|
| 1.32858.7:0 | Vendor Rev | Revision Upper Byte (MSB:LSB) | RO | 0 |
| 1.32859.7:0 | Vendor Rev | Revision Lower Byte (MSB:LSB) | RO | 0 |

**Register 1.32860 to 1.32875 - Vendor Serial Number (ASCII)**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.32860.7:0 | Vendor Serial No | Vendor Serial No. byte 15 (MSB:LSB) | | |
| 1.32861.7:0 | Vendor Serial No | Vendor Serial No. byte 14 (MSB:LSB) | | |
| 1.32862.7:0 | Vendor Serial No | Vendor Serial No. byte 13 (MSB:LSB) | RO | - |
| 1.32863.7:0 | Vendor Serial No | Vendor Serial No. byte 12 (MSB:LSB) | RO | - |
| 1.32864.7:0 | Vendor Serial No | Vendor Serial No. byte 11 (MSB:LSB) | RO | - |
| 1.32865.7:0 | Vendor Serial No | Vendor Serial No. byte 10 (MSB:LSB) | RO | - |
| 1.32866.7:0 | Vendor Serial No | Vendor Serial No. byte 9 (MSB:LSB) | RO | - |
| 1.32867.7:0 | Vendor Serial No | Vendor Serial No. byte 8 (MSB:LSB) | RO | - |
| 1.32868.7:0 | Vendor Serial No | Vendor Serial No. byte 7 (MSB:LSB) | RO | - |
| 1.32869.7:0 | Vendor Serial No | Vendor Serial No. byte 6 (MSB:LSB) | RO | - |
| 1.32870.7:0 | Vendor Serial No | Vendor Serial No. byte 5 (MSB:LSB) | RO | - |
| 1.32871.7:0 | Vendor Serial No | Vendor Serial No. byte 4 (MSB:LSB) | RO | - |
| 1.32872.7:0 | Vendor Serial No | Vendor Serial No. byte 3 (MSB:LSB) | RO | - |
| 1.32873.7:0 | Vendor Serial No | Vendor Serial No. byte 2 (MSB:LSB) | RO | - |
| 1.32874.7:0 | Vendor Serial No | Vendor Serial No. byte 1 (MSB:LSB) | RO | - |
| 1.32875.7:0 | Vendor Serial No | Vendor Serial No. byte 0 (MSB:LSB) | RO | - |

**Note:**
1. RW = Read/Write, RO = Read Only.

**Register 1.32876 to 1.32885 - Date Code (ASCII)**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.32876.7:0 | Year (1000's) | Year in 1000's (bit 7=MSB, bit 0=LSB) | | |
| 1.32877.7:0 | Year (100's) | Year in 100's (bit 7=MSB, bit 0=LSB) | | |
| 1.32878.7:0 | Year (10's) | Year in 10's (bit 7=MSB, bit 0=LSB) | RO | - |
| 1.32879.7:0 | Year (1's) | Year Units (bit 7=MSB, bit 0=LSB) | RO | - |
| 1.32880.7:0 | Month (10's) | Month in 10's (bit 7=MSB, bit 0=LSB) | RO | - |
| 1.32881.7:0 | Month (1's) | Month in units (bit 7=MSB, bit 0=LSB) | RO | - |
| 1.32882.7:0 | Day (10's) | Day in 10's (bit 7=MSB, bit 0=LSB) | RO | - |
| 1.32883.7:0 | Day (1's) | Day in Units (bit 7=MSB, bit 0=LSB) | RO | - |
| 1.32884.7:0 | Lot Code (10's) | Lot code in 10's (bit 7=MSB, bit 0=LSB) | RO | - |
| 1.32885.7:0 | Lot Code (1's) | Lot code in units (bit 7=MSB, bit 0=LSB) | RO | - |

**Register 1.32886 - 5 V Stressed Environment**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.32886.7:0 | 5V Supply | 5 V stressed environment reference | RO | 0 |

**Register 1.32887 - 3.3 V Stressed Environment**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.32887.7:0 | 3.3V Supply | 3.3 V stressed environment reference | RO | 16 |

**Register 1.32888 - APS Stressed Environment**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.32888.7:0 | APS Supply | APS stressed environment reference | RO | 1 |

**Register 1.32889 - APS Voltage**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.32889.7:0 | APS Voltage | Nominal APS voltage (1.8V) | RO | 16 |

**Register 1.32890 - DOM Capability**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.32890.7 | Status | DOM Control/Status Register:<br>0 = not implemented<br>1 = implemented | RO | 0 |
| 1.32890.6 | DOM set | Set when DOM implemented | RO | 0 |
| 1.32890.5 | WDM capability | WDM lane by lane DOM capability: setting this bit indicates that registers A0CO-A0FF are valid. Setting this bit will NOT override indications placed in register A06F (DOM capability) | RO | 0 |
| 1.32890.4 | Laser bias scale | Laser bias scale factor:<br>0 = 2 µA<br>1 = 10 µA | RO | 0 |
| 1.32890.3 | | Reserved | RO | 0 |
| 1.32890.2:0 | External DOM | Address of external DOM device | RO | 0 |

**Register 1.32891 - Reversed**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.32891.7:0 | DOM Control/Status | DOM Control/Status | RO | |

**Register 1.32894 - 1.32941 Customer Writeable Area**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.32894.7:0 | Start of writeable area | Start of customer writeable Area | RO | |
| 1.32941.7:0 | End of writeable area | End of customer writeable area | RO | |

**Note:**

1. RW = Read/Write, RO = Read Only.

**Register 1.32942 to 1.33030 - Vendor Specific**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.32942.7:0 to 1.33030.7:0 | | Vendor Specific | RO | |

**Register 1.33030 - Extended Vendor Specific**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.33031.7:0 | | Extended Vendor Specific | RO | |

**Register 1.36864 RX_ALARM Control (see also Table 1.36867 RX_ALARM Status)**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.36864. 15:11 | Reserved | Reserved | RO | 0 |
| 1.36864. 6 | PHY_XS receive buffer error enable | 1 = PHY_XS receive buffer over/underflow error enable<br>0 = disabled | RW | 0 |
| 1.36864. 5 | Receive optical power fault | 1 = Receive Optical Power Fault Enable<br>0 = Receive Optical Power Fault Disable | | |
| 1.36864. 4 | PMA/PMD local fault | 1 = PMA/PMD Receiver Local Fault Enable<br>0 = PMA/PMD Receiver Local Fault Disable | | 1 |
| 1.36864. 3 | PCS local fault | 1 = PCS Receiver Local Fault Enable<br>0 = PCS Receiver Local Fault Disable | RW | 1 |
| 1.36864.2 | PCS Receive Code | 1 = Violation Enable<br>0 = Violation Disable | | |
| 1.36864.1 | RX Flag | 1 = Enabled<br>0 = Disabled | RW | 0 |
| 1.36864.0 | PHY XS Receive local fault | 1 = PHY XS Receive Local Fault Enable<br>0 = PHY XS Receive Local Fault Disable | RW | 1 |

**Register 1.36865 TX_ALARM Control (see also Table 1.36868 TX_ALARM Status)**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.36865. 15:11 | Reserved | Reserved | RO | 0 |
| 1.36865. 10 | PHY_XS code violation error | 1 = PHY_XS code violation error enabled<br>0 = PHY_XS code violation error disabled | RW | Note 3 |
| 1.36865. 9 | Laser bias current fault | 1 = Laser Bias Current Fault Enable<br>0 = Laser Bias Current Fault Disable | Note 2 | 0<br>Note 2 |
| 1.36865. 8 | Laser temp fault | 1 = Laser Temperature Fault Enable<br>0 = Laser Temperature Fault Disable | Note 2 | 0 |
| 1.36865. 7 | Laser output fault | 1 = Laser Output Power Fault Enable<br>0 = Laser Output Power Fault Disable | Note 2 | 0 |
| 1.36865. 6 | Transmitter Fault | 1 = Transmitter Fault Enable<br>0 = Transmitter Fault Disable | RW | 1 |
| 1.36865. 5 | Transmitter Loss of Lock | 1 = Transmitter Loss of Lock enabled<br>0 = Transmitter Loss of Lock disabled | RW | Note 3 |
| 1.36865. 4 | PMA/PMD transmit fault | 1 = PMA/PMD Transmitter Local Fault Enable<br>0 = PMA/PMD Transmitter Local Fault Disable | Note 2 | 1 |
| 1.36865.3 | PCS transmit fault | 1 = PCS Transmit Local Fault Enable<br>0 = PCS Transmit Local Fault Disable | RW | 1 |
| 1.36865.2 | PCS buffer over/underflow | 1 = PCS buffer over/underflow enabled<br>0 = PCS buffer over/underflow disabled | RW | 0 |
| 1.36865.1 | TX Flag | 1 = TX flag enabled<br>0 = TX flag disabled | RW | 0 |
| 1.36865.0 | PHY XS transmit fault | 1 = PHY XS Transmit Local Fault Enable<br>0 = PHY XS Transmit Local Fault Disable | RW | 1 |

**Note:**

1. RW = Read/Write, RO = Read Only.
2. Optional features that are not implemented shall have their enable bit forced to zero. When implemented, the default value for the control bit shall be 1.
3. The default value for a vendor specific bit shall be vendor specific.

**Register 1.36866 - LASI Control (see also Table 1.36869 LASI Status)**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.36866.15:8 | Reserved | Reserved | RO | 0 |
| 1.36866. 6 | MON3P3V_IN supply too low | 1 = Enable detection of supply too low<br>0 = Disable detection of supply too low | RW | |
| 1.36866.5 | 3.3V supply too low | 1 = Enable detection of supply too low<br>0 = Disable detection of supply too low | RW | 0 |
| 1.36866.4 | 1.8V supply too low | 1 = Enable detection of supply too low<br>0 = Disable detection of supply too low | RW | 0 |
| 1.36866.3 | LASI test data | 1 = Enable LASI test data<br>0 = Disable LASI test data | RW | 0 |
| 1.36866. 2 | RX alarm | 1 = RX_ALARM enable<br>0 = RX ALARM disable | RW | 0 |
| 1.36866. 1 | TX alarm | 1 = TX_ALARM enable<br>0 = TX ALARM disable | RW | 0 |
| 1.36866. 0 | LS alarm | 1 = LS_ALARM enable<br>0 = LS ALARM disable | RW | 0 |

**Register 1.36867 - RX_ALARM Status (see also Table 1.36864 - RX_ALARM Control)**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.36867.15:11 | Reserved | Reserved | RO/RW | |
| 1.36867.6 | PHY_XS receive buffer error enable | 1 = PHY XS receive buffer over/underflow enabled<br>0 = PHY XS receive buffer over/underflow disabled | RO/LH | |
| 1.36867.5 | Receive optical power fault | Local fault condition detected in optical power fault | RO/LH | |
| 1.36867.4 | PMA/PMD Receive local fault | PMA/PMD receive local fault ( A mirror of 1.8.10) | RO/LH | |
| 1.36867.3 | PCS Receive local fault | PCS receive local fault (A mirror of 3.8.10) | RO/LH | |
| 1.36867.2 | PCS receive code violation | Local fault condition detected in code violation | RO/LH | |
| 1.36867.1 | RX flag | | RO/LH | |
| 1.36867.0 | PHY-XS Receive local fault | PHY_XS receive local fault. (A mirror of 4.8.10) | RO/LH | |

**Register 1.36868 - TX_ALARM Status (see also Table 1.36865 TX_ALARM Control)**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.36868. 15:11 | Reserved | Reserved | RO | |
| 1.36868. 10 | PHY_XS code violation enable | PHY_XS code violation error enable | RO/LH | |
| 1.36868. 9 | Laser bias fault | ADC channel 2<br>Laser Bias Current Fault | RO/LH | |
| 1.36868. 8 | Laser temp fault | ADC channel 1<br>Laser Temperature Fault | RO/LH | |
| 1.36868. 7 | Laser power fault | ADC channel 0<br>Laser Output Power Fault | RO/LH | |
| 1.36868. 6 | Transmitter fault | Transmitter Fault | RO/LH | |
| 1.36868. 5 | Transmitter loss of lock | | RO/LH | |
| 1.36868. 4 | PMA/PMD transmit local fault | PMA/PMD Transmitter Local Fault (linked to 1.8.11) | RO/LH | |
| 1.36868.3 | PCS transmit local fault | PCS Transmit Local Fault (linked to 3.8.11) | RO/LH | |
| 1.36868.2 | PCS buffer over/underflow error | Linked to 4.49154.8:9 | RO/LH | |
| 1.36868.1 | TX_flag | | RO/LH | |
| 1.36868.0 | PHY XS transmit local fault | PHY XS Transmit Local Fault (linked to 4.8.11) | RO/LH | |

**Note:**

1. RW = Read/Write, RO = Read Only, LH = Latch High, clear on read (note that if the condition exists following register read, the bit will not be cleared).

**Register 1.36869 - LASI Status (see also Table 1.36866 LASI Control)**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.36869.15:7 | Reserved | Reserved | RO | |
| 1.36869.6 | MON3P3V_IN supply alarm | 1 = 1.8V supply too low<br>0 = no alarm | RO/LH | |
| 1.36869.5 | 3.3V supply alarm | 1 = 1.8V supply too low<br>0 = no alarm | RO/LH | |
| 1.36869.4 | 1.8V supply alarm | 1 = 1.8V supply too low<br>0 = no alarm | RO/LH | |
| 1.36869.3 | LASI test data | Local fault condition detected in test data | RW | |
| 1.36869.2 | RX_ALARM | 1 = Local fault condition detected in RX_ALARM<br>0 = No alarm | RO[2] | |
| 1.36869.1 | TX_ALARM | 1 = Local fault condition detected in TX_ALARM<br>0 = No alarm | RO[2] | |
| 1.36869.0 | LS_ALARM | 1 = Local fault condition detected in status change<br>0 = No status change | LH | |

**Register 1.49153 - Extended PMA Features**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.49153.15:11 | Reserved | N/A | | |
| 1.49153.10 | RXLOSB_I override | 1 = RXLOSB_I override<br>0 = no override | RW | 0 |
| 1.49153.9 | PMA Network loopback data out | 1 = Transmit all idles at RxXAUI when in network loopback mode<br>0 = Receive data at RxXAUI when in network loopback mode | RW | |
| 1.49153.8:5 | Reserved | N/A | | |
| 1.49153.4 | PMA Network loopback mode | 1 = Enable network loopback<br>0 = Disable network loopback | RW | |
| 1.49153.3 | Reserved | N/A | | |
| 1.49153.2 | refmon | 0 = REFCLK present | RO | 1 |
| 1.49153.1 | syn_err | 1 = Recovered clock rate error | RO | 1 |
| 1.49153.0 | txlock | 1 = Fiber transmit PLL in lock | RO | 1 |

**Notes**:

1. RW = Read/Write, RO = Read Only, LH = Latch High, clear on read (note that if the condition exists following register read, the bit will not be cleared.
2. The RX_ALARM and TX_ALARM indications are the logic OR of the contents of registers 0x9003 and 0x9004 respectively. Therefore, these alarms will persist until the bit(s) reflecting the source of interrupt are cleared.

**Register 1.49155 - PMA/PMD Vendor Specific**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.49155.15:14 | EEPROM test mode | 00 = 37kHz<br>01 = high frequency test mode<br>10 = debug mode - do not use<br>11 = debug mode - do not use | RW | |
| 1.49155.13 | EEPROM detect | 1 = Detected | RO | |
| 1.49155.12 | EEPROM error | 1 = EEPROM error | RO/LH | |
| 1.49155.11 | EEPROM active | 1 = EEPROM access in progress, MDIO writes to EEPROM registers ignored | RO | |
| 1.49155.10:8 | Reserved | | RO | |
| 1.49155.7 | EEPROM checksum OK | 1 = OK | RO/LH | |
| 1.49155.6 | Reserved | | RO | |
| 1.49155.5:4 | EEPROM 256 byte read cycle burst size | Size Bit1 Bit0<br>1 0 0<br>8 0 1<br>16 1 0<br>256 1 1 | RW | 11 |
| 1.49155.3:2 | Reserved | | RO | |
| 1.49155.1:0 | EEPROM 256 byte write cycle burst size | Size Bit1 Bit0<br>1 0 0<br>8 0 1<br>16 1 0<br>1 1 1 | RW | 01 |

**Register 1.49156 - PMA/PMD Vendor Specific Checksum**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.49156.15:8 | EEPROM calculated checksum | | RO | |
| 1.49156.7:4 | Reserved | | RO | |
| 1.49156.3:2 | EEPROM 256 byte write cycle burst size | Size Bit1 Bit0<br>1 0 0<br>8 0 1<br>16 1 0<br>1 1 1 | RW | 01 |
| 1.49156.1:0 | DOM write command | Bit1 Bit0 Command<br>0 0 Reserved<br>0 1 Reserved<br>1 0 Reserved<br>1 1 Write 256 bytes | RW | |

**Register 1.49188 - PMA Vendor Specific**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 1.49188.15:4 | Reserved | | RO | |
| 1.49188.3 | TXPLLOUT frequency selection | 1 = 10 GHz<br>0 = 156 MHz | RW | 0 |
| 1.49188.2 | Reserved | | RO | |
| 1.49188.1 | TXPLLOUT enable | 1 = enabled<br>0 = disabled | RW | 0 |
| 1.49188.0 | EEPROM_SCL tristate | 1 = tristate<br>0 = not tristate | RW | 0 |

**Notes**:

1. RW = Read/Write, RO = Read Only, LH = Latch High, clear on read (note that if the condition exists following register read, the bit will not be cleared.

**HFCT-701XB Device 3 PCS Registers**

| Device | From Decimal | Hex | To Decimal | Hex | Register Name |
|---|---|---|---|---|---|
| 3 | 0 | 0 | | | PCS Control 1 |
| 3 | 1 | 1 | | | PCS Status 1 |
| 3 | 2 | 2 | 3 | 3 | PCS Device identifier |
| 3 | 4 | 4 | | | PCS Speed Ability |
| 3 | 5 | 5 | 6 | 6 | PCS Devices in package |
| 3 | 7 | 7 | | | 10G PCS Control 2 |
| 3 | 8 | 8 | | | 10G PCS Status 2 |
| 3 | 32 | 20 | | | 10GBASE-R PCS Status 1 |
| 3 | 33 | 21 | | | 10GBASE-R PCS Status 2 |
| 3 | 34 | 22 | 37 | 25 | 10GBASE-R PCS Test Pattern Seed A |
| 3 | 38 | 26 | 41 | 29 | 10GBASE-R PCS Test Pattern Seed B |
| 3 | 42 | 2A | | | 10GBASE-R PCS Test Pattern Control |
| 3 | 43 | 2B | | | 10GBASE-R PCS Test Pattern Error Counter |
| 3 | | | | | |
| 3 | | | | | |
| 3 | 49152 | C000 | | | PCS extended features |
| 3 | 49153 | C0001 | 49157 | C005 | |
| 3 | 49158 | C006 | 49169 | C011 | PCS Vendor Specific |

### Register 3.0 - PCS Control 1

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.0.15 | PCS 64/66 Reset | 1 = PCS reset<br>0 = Normal operation | RW/SC | |
| 3.0.14 | PCSLoopback | 1 = Enable loopback mode<br>0 = Disable loopback mode | RW | 0 |
| 3.0.13 | Speed Selection | 1 = Operation at 10 Gb/s and above<br>0 = Unspecified | RW | |
| 3.0.12 | Reserved | | RW | |
| 3.0.11 | Low power | 1 = Low power mode<br>0 = Normal operation | RW | |
| 3.0.10:7 | Reserved | | RW | |
| 3.0.6 | Speed selection | 1 = Operation at 10 Gb/s and above<br>0 = Unspecified | RW | |
| 3.0.5:2 | Speed selection | 5 4 3 2<br>0 0 0 0 = 10 Gb/s | RW | 0000 |
| 3.0.1:0 | Reserved | | RW | |

### Register 3.1 - PCS Status 1

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.1.15:8 | Reserved | | RO | |
| 3.1.7 | Local fault | 1 = Local fault condition detected<br>0 = Local fault condition not detected<br>(Set to 1 when either 3.8.11 or 3.8.10 set to 1) | RO | |
| 3.1.6:3 | Reserved | N/A | | |
| 3.1.2 | PCS receive link status | 1 = PCS receive link up<br>0 = PCS receive link down | RO/LL | |
| 3.1.1 | Low Power ability | 1 = PCS supports low power mode<br>0 = PCS does not support low power mode | RO | |
| 3.1.0 | Reserved | N/A | RO | |

### Register 3.2 to 3.3 - PCS Device Identifier

A mirror of Registers 1.2 to 1.3.

### Register 3.4 - PCS Speed Ability

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.4.15:1 | Reserved | | RO | N/A |
| 3.4.0 | 10 G capable | 1 = PCS capable of operating at 10 Gb/s<br>0 = PCS is not capable of operating at 10 Gb/s | RO | 1 |

### Register 3.5 to 3.6 - PCS Devices in Package

A mirror of Registers 1.5 to 1.6.

**Note:**

1. RW = Read/Write, SC = Self Clearing, RO = Read Only, LL = Latching Low.

**Register 3.7 - 10 G PCS Control 2**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.7.15:2 | Reserved | N/A | | |
| 3.7.1:0 | PCS type selection | 1 0<br>0 0 = Select 10GBASE-R PCS type | RW | 00 |

**Register 3.8 - 10 G PCS Status 2**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.8.15:14 | Device present | 15 14<br>1 0 = Device responding at this address<br>1 1 = No device responding at this address<br>0 1 = No device responding at this address<br>0 0 = No device responding at this address | RO | |
| 3.8.13:12 | Reserved | N/A | RO | |
| 3.8.11 | Transmit local fault | 1 = Local fault condition on transmit path<br>0 = No local fault condition on transmit path | RO/LH | |
| 3.8.10 | Receive local fault | 1 = Local fault condition on receive path<br>0 = No local fault condition on receive path | RO/LH | |
| 3.8.9:3 | Reserved | N/A | RO | |
| 3.8.2 | 10GBASE-W capable | 1 = PCS is able to support 10GBASE-W PCS type<br>0 = PCS is not able to support 10GBASE-W PCS type | RO | |
| 3.8.1 | 10GBASE-X capable | 1 = PCS is able to support 10GBASE-X PCS type<br>0 = PCS is not able to support 10GBASE-X PCS type | RO | |
| 3.8.0 | 10GBASE-R capable | 1 = PCS is able to support 10GBASE-R PCS type<br>0 = PCS is not able to support 10GBASE-R PCS type | RO | |

**Register 3.32 - 10GBASE-R PCS Status 1**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.32.15:13 | Reserved | | RO | |
| 3.32.12 | 10GBASE-R receive link status | 1 = 10GBASE-R PCS receive link up<br>0 = 10GBASE-R PCS receive link down | RO | |
| 3.32.11:3 | Reserved | | RO | |
| 3.32.2 | PRBS31 pattern testing ability | 1 = PCS is able to support PRBS31 pattern testing<br>0 = PCS is not able to support PRBS31 pattern testing | RO | |
| 3.32.1 | 10GBASE-R PCS high BER | 1 = 10GBASE-R PCS reporting a high BER<br>0 = 10GBASE-R PCS not reporting a high BER | RO | |
| 3.32.0 | 10GBASE-R PCS block lock | 1 = 10GBASE-R PCS locked to received blocks<br>0 = 10GBASE-R PCS not locked to received blocks | RO | |

**Notes**:
1. RW = Read/Write, RO = Read Only, LH = Latch High, clear on read (note that if the condition exists following register read, the bit will not be cleared.

**Register 3.33 - 10GBASE-R PCS Status 2**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.33.15 | Latched block lock | 1 = PCS has reported block lock since last read<br>0 = PCS has not reported block lock since last read | RO/LL | |
| 3.33.14 | Latched high BER | 1 = PCS has reported high BER since last read<br>0 = PCS has not reported high BER since last read | RO/LH | |
| 3.33.13:8 | BER | BER counter | RO/NR | |
| 3.33.7:0 | Errored blocks | Jitter pattern checker | RO/NR | |

**Register 3.34 to 3.37 - 10GBASE-R PCS Test Pattern Seed A**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.37.15:10 | Reserved | Value always 0, writes ignored | RW | |
| 3.37.9:0 | Test pattern seed A 3 | Test pattern seed A bits 48-57 | RW | |
| 3.36.15:0 | Test pattern seed A 2 | Test pattern seed A bits 32-47 | RW | |
| 3.35.15:0 | Test pattern seed A 1 | Test pattern seed A bits 16-31 | RW | |
| 3.34.15:0 | Test pattern seed A 0 | Test pattern seed A bits 0-15 | RW | |

**Register 3.38 to 3.41 - 10GBASE-R PCS Test Pattern Seed B**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.41.15:10 | Reserved | Value always 0, writes ignored | RW | |
| 3.41.9:0 | Test pattern seed B 3 | Test pattern seed B bits 48-57 | RW | |
| 3.40.15:0 | Test pattern seed B 2 | Test pattern seed B bits 32-47 | RW | |
| 3.39.15:0 | Test pattern seed B 1 | Test pattern seed B bits 16-31 | RW | |
| 3.38.15:0 | Test pattern seed B 0 | Test pattern seed B bits 0-15 | RW | |

**Register 3.42 - 10GBASE-R PCS Test Pattern Control**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.42.15:6 | Reserved | Value always 0, writes ignored | RW | |
| 3.42.5 | PRBS31 receive test pattern | 1 = Enable PRBS31 test pattern mode on the receive path<br>0 = Disable PRBS31 test pattern mode on the receive path | RW | 0 |
| 3.42.4 | PRBS31 transmit test pattern | 1 = Enable PRBS31 test pattern mode on the transmit path<br>0 = Disable PRBS31 test pattern mode on the transmit path | RW | 0 |
| 3.42.3 | Transmit test pattern | 1 = Enable transmit test pattern testing<br>0 = Disable transmit test pattern testing | RW | |
| 3.42.2 | Receive test pattern | 1 = Enable receive test pattern testing<br>0 = Disable receive test pattern testing | RW | |
| 3.42.1 | Test pattern select | 1 = Square wave test pattern<br>0 = Pseudo random test pattern | RW | |
| 3.42.0 | Data pattern select | 1 = Zeros data pattern<br>0 = LF data pattern | RW | |

**Notes**:

1. RW = Read/Write, RO = Read Only, LL = Latching Low, LH = Latch High, clear on read (note that if the condition exists following register read, the bit will not be cleared, NR = Non Roll-Over.

**Register 3.43 - 10GBASE-R PCS Test Pattern Error Counter**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.43.15:0 | Test pattern error counter | Error counter<br>LSB = bit 0<br>MSB = bit 15 | RO/NR | |

**Register 3.49152 - PCS Extended Features**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.49152.15:8 | Diagnostic Register | Diagnostic register | RO | |
| 3.49152.7:6 | Reserved | N/A | | |
| 3.49152.5 | PCS loopback data out | 1 = Transmit data at TXOUT when in PCS loopback mode<br>0 = Transmit a square wave when in PCS loopback mode | RW | 0 |
| 3.49152.4 | Reset transmit PCS | 1 = Not reset<br>0 = ResetNote: not self clearing | RW | 1 |
| 3.49152.3 | Reset receive PCS | 1 = Not reset<br>0 = ResetNote: not self clearing | RW | 1 |
| 3.49152.2 | TX scrambler bypass | 1 = Bypass | RW | 0 |
| 3.49152.1 | RX scrambler bypass | 1 = Bypass | RW | 0 |
| 3.49152.0 | 64/66 encoder error | 1 = Error | RO/LH | 0 |

**Register 3.49152 - 3.49157 - PCS Vendor Specific**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.49152.15:0 | Diagnostic registers | | | |
| 3.49153.15:0 | | | | |
| 3.49154.15:0 | | | | |
| 3.49155.15:0 | | | | |
| 3.49156.15:0 | | | | |
| 3.49157.15:0 | | | | |

**Register 3.49158 - PCS Vendor Specific**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.49158.15:7 | Vendor Specific | Reserved | RO | |
| 3.49158.6:0 | Receive Frame Offset | | RO | |

**Register 3.49159 - PCS Vendor Specific Receive Path PACKET Checker**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.49159.15:0 | First 16 bits of XGMII bus error flag | 1 = error at this bit location | RO/LH | |

**Register 3.49160 - PCS Vendor Specific Receive Path PACKET Checker**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.49160.15:0 | Second 16 bits of XGMII bus error flag | 1 = error at this bit location | RO/LH | |

**Register 3.49161 - PCS Vendor Specific Receive Path PACKET Checker**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.49161.15:6 | Vendor Specific | Reserved | RO | |
| 3.49161.5 | rx_idle_err_flag | Received a full packet but with start or idle errors | RO/LH | |
| 3.49161.4 | rx_start_err_flag | Received a full packer but with preamble errors | RO/LH | |
| 3.49161.3 | rx_data_err_flag | Received a full packet but long packet | RO/LH | |
| 3.49161.2 | rx_long_pkt_flag | Received a full packet but long packet | RO/LH | |
| 3.49161.1 | rx_short_pkt_flag | Received a full packet but short packet | RO/LH | |
| 3.49161.0 | rx_term_err_flag | Set if terminate received but the next byte is not an idle | RO/LH | |

**Notes**:

1. RW = Read/Write, RO = Read Only, LH = Latch High, clear on read (note that if the condition exists following register read, the bit will not be cleared, NR = Non Roll-Over.

**Register 3.49162 - PCS Vendor Specific Transmit Path PACKET Checker**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.49162.15:0 | First 16 bits of XGMII bus error flag | 1 = error at this bit location | RO/LH | |

**Register 3.49163 - PCS Vendor Specific Transmit Path PACKET Checker**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.49163.15:0 | Second 16 bits of XGMII bus error flag | 1 = error at this bit location | RO/LH | |

**Register 3.49164 - PCS Vendor Specific PACKET Generator/Checker**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.49164.15:6 | Packet generator idle size | | RW | |
| 3.49164.5 | tx_idle_err_flag | Received a full packet but with start or idle errors | RO/LH | |
| 3.49164.4 | tx_start_err_flag | Received a full packet but with preamble errors | RO/LH | |
| 3.49164.3 | tx_data_err_flag | Received a full packet but with long packet | RO/LH | |
| 3.49164.2 | tx_long_pkt_flag | Received a full packet but with long packet | RO/LH | |
| 3.49164.1 | tx_short_pkt_flag | Received a full packet but with short packet | RO/LH | |
| 3.49164.0 | tx_term_err_flag | Set if terminate received but the next byte is not an idle | RO/LH | |

**Register 3.49165 - PCS Vendor Specific PACKET Generator**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.49165.15:0 | Fixed pattern | First 16 bits of XGMII | RW | |

**Register 3.49166 - PCS Vendor Specific PACKET Generator**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.49166.15:0 | Fixed pattern | Second 16 bits of XGMII | RW | |

**Register 3.49167 - PCS Vendor Specific PACKET Generator**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.49167.15:14 | Vendor Specific | Reserved | RO | |
| 3.49167.13 | Tx path pattern checker | 1 = enabled<br>0 = disabled | RW | 0 |
| 3.49167.12 | Tx path pattern generator | 1 = enabled<br>0 = disabled | RW | 0 |
| 3.49167.11 | Rx path pattern checker | 1 = enabled<br>0 = disabled | RW | 0 |
| 3.49167.10 | Rx path pattern generator | 1 = enabled<br>0 = disabled | RW | 0 |
| 3.49167.9 | Packet type | 1 = increment pattern<br>0 = fixed pattern | RW | |
| 3.49167.8:0 | Data packet size divided by 4 | | RW | |

**Notes**:

1. RW = Read/Write, RO = Read Only, LH = Latch High, clear on read (note that if the condition exists following register read, the bit will not be cleared.

**Register 3.49169 - PCS Vendor Specific**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 3.49169.15:2 | Reserved | | RO | |
| 3.49169.1 | Gearbox FIFO error | Diagnostic register | RO | |
| 3.49169.0 | Frame sync FIFO error | Diagnostic register | RO | |

**Note:**
1. RW = Read/Write, RO = Read Only.

**HFCT-701XB Device 4 PHYXS Registers**

| Device | From Decimal | Hex | To Decimal | Hex | Register Name |
|---|---|---|---|---|---|
| 4 | 0 | 0 | | | PHY XS Control 1 |
| 4 | 1 | 1 | | | PHY XS Status 1 |
| 4 | 2 | 2 | 3 | 3 | PHY XS Device identifier |
| 4 | 4 | 4 | | | PHY XS Speed Ability |
| 4 | 5 | 5 | 6 | 6 | PHY XS Devices in package |
| 4 | 8 | 8 | | | PHY XS Status 2 |
| 4 | 14 | E | 15 | F | PHY XS Package identifier |
| 4 | 24 | 18 | | | 10G PHY XGXS Lane Status |
| 4 | 25 | 19 | | | 10G PHY XGXS Test Control |
| 4 | 49152 | C000 | | | PHY_XS Extended Features |
| 4 | 49153 | C001 | | | PHY_XS Extended Features |
| 4 | 49154 | C002 | 49160 | C008 | PHY_XS Vendor Specific |

**Register 4.0 - PHY_XS Control 1**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.0.15 | Global Reset | 1 = reset<br>0 = Normal operation | RW/SC | |
| 4.0.14 | Loopback | 1 = Enable PHY XS loopback mode<br>0 = Disable PHY XS loopback mode | RW | 0 |
| 4.0.13 | Speed selection | 1 = Operation at 10 Gb/s and above<br>0 = Unspecified | RW | |
| 4.0.12 | Reserved | | RW | |
| 4.0.11 | Low power | 1 = Low power mode<br>0 = Normal operation | RW | |
| 4.0.10:7 | Reserved | | RW | |
| 4.0.6 | Speed selection | 1 = Operation at 10 Gb/s and above<br>0 = Unspecified | RW | |
| 4.0.5:2 | Speed selection | 5 4 3 2<br>0 0 0 0 = 10 Gb/s | RW | 0000 |
| 4.0.1:0 | Reserved | Value always 0, writes ignored | RW | |

**Register 4.1 - PHY_XS Status 1**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.1.15:8 | Reserved | N/A | RO | |
| 4.1.7 | Local fault | 1 = Local fault condition detected on PHY XS<br>0 = Local fault condition not detected on PHY XS | RO | |
| 4.1.6:3 | Reserved | N/A | RO | |
| 4.1.2 | PHY XS transmit link status | 1 = The PHY XS transmit link is up<br>0 = The PHY XS transmit link is down | RO/LL | |
| 4.1.1 | Low Power ability | 1 = PHYXS supports low power mode<br>0 = PHYXS does not support low power mode | RO | 1 |
| 4.1.0 | Reserved | N/A | RO | |

**Register 4.2 to 4.3 - Device Identifier**

A mirror of Registers 1.2 to 1.3.

**Register 4.4 - PHY_XS Speed Ability**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.4.15:1 | Reserved for future speeds | | RO | |
| 4.4.0 | 10 G capable | 1 = PHYXS is capable of operating at 10 Gb/s<br>0 = PHYXS is not capable of operating at 10 Gb/s | RO | 1 |

**Register 4.5 to 4.6 - Device in Package**

A mirror of Registers 1.5 to 1.6.

**Notes**:

1. RW = Read/Write, SC = Self Clearing, RO = Read Only, LL = Latching Low.

**Register 4.8 - PHY_XS Status 2**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.8.15:14 | Device present | 15 14 | RO | 10 |
| | | 1 0 = Device responding at this address | | |
| | | 1 1 = No device responding at this address | | |
| | | 0 1 = No device responding at this address | | |
| | | 0 0 = No device responding at this address | | |
| 4.8.13:12 | Reserved | N/A | | |
| 4.8.11 | Transmit local fault | 1 = Local fault condition on transmit path of PHY XS | RO/LH | |
| | | 0 = No local fault condition on transmit path of PHY XS | | |
| 4.8.10 | Receive local fault | 1 = Fault condition on receive path of PHY XS | RO/LH | |
| | | 0 = No fault condition on receive path of PHY XS | | |
| 4.8.9:0 | Reserved | N/A | RO | |

**Register 4.14 to 4.15 - Package Identifier (OUI)**

A mirror of Registers 1.32818 to 1.32821.

**Register 4.24 - 10G PHY_XGXS Lane Status**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.24.15:13 | Reserved | N/A | RO | |
| 4.24.12 | PHY XGXS lane alignment status | 1 = PHY XGXS transmit lanes aligned<br>0 = PHY XGXS transmit lanes not aligned | RO | |
| 4.24.11 | Pattern testing ability | 1 = PHY XGXS is able to generate test patterns<br>0 = PHY XGXS is not able to generate test patterns | RO | 1 |
| 4.24.10 | PHY XGXS loopback ability | 1 = PHY XGXS has the ability to perform a loopback function<br>0 = PHY XGXS does not have the ability to perform a loopback function | RO | 1 |
| 4.24.9:4 | Reserved | N/A | RO | |
| 4.24.3 | Lane 3 sync | 1 = Lane 3 is synchronized<br>0 = Lane 3 is not synchronized | RO | N/A |
| 4.24.2 | Lane 2 sync | 1 = Lane 2 is synchronized<br>0 = Lane 2 is not synchronized | RO | N/A |
| 4.24.1 | Lane 1 sync | 1 = Lane 1 is synchronized<br>0 = Lane 1 is not synchronized | RO | N/A |
| 4.24.0 | Lane 0 sync | 1 = Lane 0 is synchronized<br>0 = Lane 0 is not synchronized | RO | N/A |

**Register 4.25 - 10 G PHY_XGXS Test Control**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.25.15:3 | Reserved | N/A | RW | |
| 4.25.2 | Receive test pattern enable | 1 = Receive test pattern enabled<br>0 = Receive test pattern not enabled | RW | 0 |
| 4.25.1:0 | Test pattern select | 1 0<br>1 1 = Reserved<br>1 0 = Mixed frequency test pattern<br>0 1 = Low frequency test pattern<br>0 0 = High frequency test pattern | RW | |

**Notes**:

1. RW = Read/Write, RO = Read Only, LH = Latch High, clear on read (note that if the condition exists following register read, the bit will not be cleared.

**Register 4.49152 - PHY_XS Extended Features**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.49152.15 | XAUI system loopback data out enable | 1 = Transmit data at TXOUT when in PHY_XS loopback mode<br>0 = Transmit all 1's when in PHY_XS loopback mode | RW | 0 |
| 4.49152.14 | XAUI system loopback (Tx - >Rx path) enable | 1 = Enable XAUI loopback | RW | 0 |
| 4.49152.13 | XAUI PRBS enable | 1 = Enable PRBS | RW | 0 |
| 4.49152.12 | XAUI analog monitor point control | 1 = XAUI lane 3 recovered data<br>0 = XAUI lane 3 recovered clock | | |
| 4.49152.11:8 | Reserved | N/A | | |
| 4.49152.7 | Lane 3 locked | 1 = lane 3 in lock | RO | N/A |
| 4.49152.6 | Lane 2 locked | 1 = lane 2 in lock | RO | N/A |
| 4.49152.5 | Lane 1 locked | 1 = lane 1 in lock | RO | N/A |
| 4.49152.4 | Lane 0 locked | 1 = lane 0 in lock | RO | N/A |
| 4.49152.3 | XAUI PLL locked | 1 = XAUI PLL locked | RO | N/A |
| 4.49152.2 | XAUI external reference clock mode | 1 = external clock<br>0 = internal reference clock | RW | 0 |
| 4.49152.1 | Receive XGXS reset | 1 = Not reset<br>0 = Reset<br>Note: not self clearing | RW | 1 |
| 4.49152.0 | Transmit XGXS reset | 1 = Not reset<br>0 = Reset<br>Note: not self clearing | RW | 1 |

**Register 4.49153 - PHY_XS Extended Features**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.49153.15:8 | Reserved | N/A | RO | |
| 4.49153.7 | XAUI lane 7 PRBS error | 1 = error | RO/LH | |
| 4.49153.6 | XAUI lane 6 PRBS error | 1 = error | RO/LH | |
| 4.49153.5 | XAUI lane 5 PRBS error | 1 = error | RO/LH | |
| 4.49153.4 | XAUI lane 4 PRBS error | 1 = error | RO/LH | |
| 4.49153.3 | XAUI lane 3 PRBS error | 1 = error | RO/LH | - |
| 4.49153.2 | XAUI lane 2 PRBS error | 1 = error | RO/LH | - |
| 4.49153.1 | XAUI lane 1 PRBS error | 1 = error | RO/LH | - |
| 4.49153.0 | XAUI lane 0 PRBS error | 1 = error | RO/LH | - |

**Notes**:
1. RW = Read/Write, RO = Read Only.

**Register 4.49154 - PHY_XS Vendor Specific**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.49154.15:10 | Vendor Specific | Reserved | RO | |
| 4.49154.9 | XGXS Tx rate adjust overflow | 1 = Overflow(linked to 1.36868.2) | RO/LH | Note 2 |
| 4.49154.8 | XGXS Tx rate adjust underflow | 1 = Underflow(linked to 1.36868.2) | RO/LH | Note 2 |
| 4.49154.7 | XGXS Rx rate overflow | 1 = Overflow(linked to 1.36867.6) | RO/LH | Note 2 |
| 4.49154.6 | XGXS Rx rate adjust underflow | 1 = Underflow(linked to 1.36867.6) | RO/LH | Note 2 |
| 4.49154.5:0 | Vendor Specific | Reserved | RO | - |

**Register 4.49155 - PHY_XS Vendor Specific**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.49155.15:12 | Sync offset XAUI channel 3 | | RO | |
| 4.49155.11:8 | Sync offset XAUI channel 2 | | RO | |
| 4.49155.7:4 | Sync offset XAUI channel 1 | | RO | |
| 4.49155.3:0 | Sync offset XAUI channel 0 | | RO | |

**Register 4.49156 - PHY_XS Vendor Specific**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.49156.15:12 | Align offset XAUI channel 3 | | RO | |
| 4.49156.11:8 | Align offset XAUI channel 2 | | RO | |
| 4.49156.7:4 | Align offset XAUI channel 1 | | RO | |
| 4.49156.3:0 | Align offset XAUI channel 0 | | RO | |

**Register 4.49157 - PHY_XS Vendor Specific**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.49157.15 | PHY_XS phase_err3 | XAUI lane 3 clock phase error, clear on read | RO | |
| 4.49157.14 | PHY_XS phase_err2 | XAUI lane 2 clock phase error, clear on read | RO | |
| 4.49157.13 | PHY_XS phase_err1 | XAUI lane 1 clock phase error, clear on read | RO | |
| 4.49157.12 | PHY_XS phase_err0 | XAUI lane 0 clock phase error, clear on read | RO | |
| 4.49157.11:0 | Vendor Specific | Reserved | RO | |

**Notes**:
1. RW = Read/Write, RO = Read Only, LH = Latch High, clear on read (note that if the condition exists following register read, the bit will not be cleared.
2. This bit is linked to an MDIO latched high diagnostic alarm register bit. When either register is read, both bits will be cleared.

**Register 4.49158 - PHY_XS Vendor Specific**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.49158.15:8 | Vendor Specific | Reserved | RO | |
| 4.49158.7 | Lane 3 upper byte | 10B/8B decode error | RO/LH | |
| 4.49158.6 | Lane 2 upper byte | 10B/8B decode error | RO/LH | |
| 4.49158.5 | Lane 1 upper byte | 10B/8B decode error | RO/LH | |
| 4.49158.4 | Lane 0 upper byte | 10B/8B decode error | RO/LH | |
| 4.49158.3 | Lane 3 lower byte | 10B/8B decode error | RO/LH | |
| 4.49158.2 | Lane 2 lower byte | 10B/8B decode error | RO/LH | |
| 4.49158.1 | Lane 1 lower byte | 10B/8B decode error | RO/LH | |
| 4.49158.0 | Lane 0 lower byte | 10B/8B decode error | RO/LH | |

**Register 4.49160 - PHY_XS Vendor Specific**

| Bit(s) | Name | Description | R/W[1] | Default Value |
|---|---|---|---|---|
| 4.49160.15:0 | PHY_XS receive code violation counter | Clear on read<br>Bit0 = LSB<br>Bit15 = MSB<br>Note: in Tx path | RO/NR | |

**Notes**:

1. RW = Read/Write, RO = Read Only, LH = Latch High, clear on read (note that if the condition exists following register read, the bit will not be cleared, NR = Non Roll-Over.

**Regulatory Compliance**
The HFCT-701XB is intended to enable commercial system designers to develop equipment that complies with the various regulations governing Certification of Information Technology equipment (see Table 15).

**Electrostatic Discharge (ESD)**
There are two design cases in which immunity to ESD damage is important. The first case is during handling of the transceiver prior to plugging into the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches and floor mats in ESD controlled areas. The second case to consider is static charges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the SC duplex connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level criteria that the equipment is intended to meet.

**Electromagnetic Interference (EMI)**
Most equipment design utilizing these high speed transceivers from Agilent will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. Performance of the HFCT-701XB transceiver is dependent upon customer board and chassis design.

**Immunity**
Equipment utilizing these transceivers will be subject to radio frequency electromagnetic fields in some environments. These transceivers have been characterized without the benefit of the normal equipment chassis enclosure and results are reported below. Performance of a system containing these transceivers within a well-designed chassis enclosure is expected to be better than the results of these tests without a chassis enclosure.

**Glossary**
PHY = Module = Used interchangeably with HFCT-701XB in this document.

Network = Used to indicate elements that are on the optical side of the module.

Network loopback = A signal path within the module from the optical input of the module to the optical output of the module.

System = Used to indicate elements that are on the electrical side of the module.

System loopback = A signal path within the module from the electrical input of the module to the electrical output of the module.

**Table 15. Regulatory Compliance - Typical Performance**

| Feature | Test Method | Performance |
|---|---|---|
| General | Telcordia GR-468-CORE | Qualified in accordance with Remote terminal requirements |
| Electrostatic Discharge - Human Body Model | MIL STD 883 Method 3015 | 500 V |
| Electrostatic Discharge - Charged Device Model | JEDEC JES D22-C101 | 500 V |
| Electrostatic Discharge - Contact Discharge | IEC 61000-4-2 | 8000 V |
| Electromagnetic Interference | FCC Class BCENELEC EN55022 Class B (CISPR 22B) VCCI Class 2 | Margins are dependant on customer board and chassis design |
| Immunity | Variation of IEC 61000-4-3 | A BER of better than 1E-12 was observed from a 10 V/m field swept from 27 MHz to 1 GHz. |
| Eye Safety | IEC 60825/CDRH Class 1 | CDRH: 9521220-51<br>TUV: 933/510230/01 |

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