16, 14 & 12-Bit, Self-Calibrating A/D Converters

Features

- Monolithic CMOS A/D Converters
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 12, 14 and 16-Bit Precision
- Conversion Times:
  - CS5016 16.25 µs
  - CS5014 14.25 µs
  - CS5012A 7.20 µs
- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 150 mW
- Low Distortion

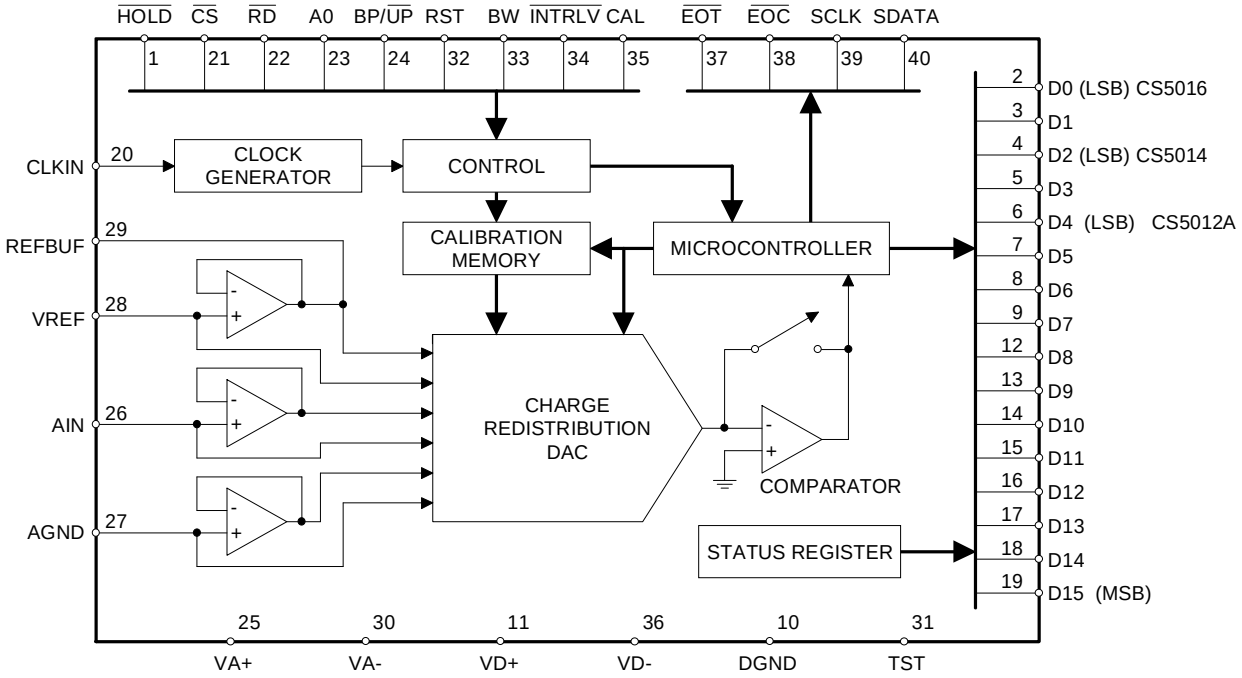
General Description

The CS5012A/14/16 are 12, 14 and 16-bit monolithic analog to digital converters with conversion times of 7.2µs, 14.25µs and 16.25µs. Unique self-calibration circuitry insures excellent linearity and differential non-linearity, with no missing codes. Offset and full scale errors are kept within 1/2 LSB (CS5012A/14) and 1 LSB (CS5016), eliminating the need for calibration. Unipolar and bipolar input ranges are digitally selectable.

The pin compatible CS5012A/14/16 consist of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the devices' sampling architecture, acquires the input signal after each conversion using a fast slewing on-chip buffer amplifier. This allows throughput rates up to 100 kHz (CS5012A), 56 kHz (CS5014) and 50 kHz (CS5016).

An evaluation board (CDB5012/14/16) is available which allows fast evaluation of ADC performance.

ORDERING INFORMATION: Pages 2-45, 2-46, & 2-47



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CS5012A ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 2.5V to 4.5V; f_{clk} = 6.4 MHz for -7, 4 MHz for -12; Analog Source Impedance = 200Ω)

Parameter*		CS5012A-B Min	Typ	Max		Units
Specified Temperature Range			-40 to +85			°C
Accuracy						
Linearity Error	(Note 1)		±1/4	±1/2		LSB_{12}
Drift	(Note 2)		±1/8			ΔLSB_{12}
Differential Linearity	(Note 1)		±1/4	±1/2		LSB_{12}
Drift	(Note 2)		±1/32			ΔLSB_{12}
Full Scale Error	(Note 1)		±1/4	±1/2		LSB_{12}
Drift	(Note 2)		±1/16			ΔLSB_{12}
Unipolar Offset	(Note 1)		±1/4	±1/2		LSB_{12}
Drift	(Note 2)		±1/16			ΔLSB_{12}
Bipolar Offset	(Note 1)		±1/4	±1/2		LSB_{12}
Drift	(Note 2)		±1/16			ΔLSB_{12}
Bipolar Negative Full-Scale Error	(Note 1)		±1/4	±1/2		LSB_{12}
Drift	(Note 2)		±1/16			ΔLSB_{12}
Total Unadjusted Error	(Note 1)		±1/4			LSB_{12}
Drift	(Note 2)		±1/4			ΔLSB_{12}
Dynamic Performance (Bipolar Mode)						
Peak Harmonic or Spurious Noise	(Note 1)					
Full Scale, 1 kHz Input		84	92			dB
Full Scale, 12 kHz Input		84	88			dB
Total Harmonic Distortion			0.008			%
Signal-to-Noise Ratio	(Note 1)					
1 kHz, 0 dB Input		72	73			dB
1 kHz, -60 dB Input			13			dB
Noise	(Note 3)					
Unipolar Mode			45			μV_{rms}
Bipolar Mode			90			μV_{rms}

Notes: 1. Applies after calibration at any temperature within the specified temperature range.
2. Total drift over specified temperature range since calibration at power-up at 25 °C
3. Wideband noise aliased into the baseband. Referred to the input.

* Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

CS5012A ANALOG CHARACTERISTICS (continued)

Parameter*		CS5012A-B Min	Typ	Max		Units
Specified Temperature Range			-40 to +85			°C
Analog Input						
Aperture Time			25			ns
Aperture Jitter			100			ps
Input Capacitance	(Note 4)					
Unipolar Mode						pF
CS5012A			103	137		pF
Bipolar Mode						pF
CS5012A			72	96		pF
Conversion & Throughput						
Conversion Time -7	(Notes 5 and 6)			7.2		µs
Acquisition Time -7	(Note 6)		2.5	2.8		µs
Throughput -7	(Note 6)	100				kHz
Power Supplies						
DC Power Supply Currents	(Note 7)					
I_{A+}			12	19		mA
I_{A-}			-12	-19		mA
I_{D+}			3	6		mA
(CS5012A) I_{D+}			6	7.5		mA
I_{D-}			-3	-6		mA
Power Dissipation	(Note 7)		150	250		mW
Power Supply Rejection	(Note 8)					
Positive Supplies			84			dB
Negative Supplies			84			dB

Notes:
4. Applies only in track mode. When converting or calibrating, input capacitance will not exceed 15 pF.
5. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
6. Conversion, acquisition, and throughput times depend on CLKIN, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CS5012A/14/16 's conversion clock, interleave calibrate is disabled, and operation is from the full-rated, external clock. Refer to the section *Conversion Time/Throughput* for a detailed discussion of conversion timing.
7. All outputs unloaded. All inputs CMOS levels.
8. With 300 mV p-p, 1 kHz ripple applied to each analog supply separately in bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB. Figure 13 shows a plot of typical power supply rejection versus frequency.

CS5014 ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; CLKIN = 4 MHz for -14, 2 MHz for -28; Analog Source Impedance = 200Ω)

Parameter*		CS5014-B Min	CS5014-B Typ	CS5014-B Max		Units
Specified Temperature Range			-40 to +85			°C
Accuracy						
Linearity Error	(Note 1)		±1/4	±1/2		LSB_{14}
						LSB_{14}
Drift	(Note 2)		±1/8			ΔLSB_{14}
Differential Linearity	(Note 1)		±1/4	±1/2		LSB_{14}
Drift	(Note 2)		±1/32			ΔLSB_{14}
Full Scale Error	(Note 1)		±1/2	±1		LSB_{14}
Drift	(Note 2)		±1/4			ΔLSB_{14}
Unipolar Offset	(Note 1)		±1/4	±3/4		LSB_{14}
						LSB_{14}
Drift	(Note 2)		±1/4			ΔLSB_{14}
Bipolar Offset	(Note 1)		±1/4	±3/4		LSB_{14}
						LSB_{14}
Drift	(Note 2)		±1/2			ΔLSB_{14}
Bipolar Negative Full-Scale Error	(Note 1)		±1/2	±1		LSB_{14}
						LSB_{14}
Drift	(Note 2)		±1/4			ΔLSB_{14}
Total Unadjusted Error	(Note 1)		±1			LSB_{14}
Drift	(Note 2)		±1			ΔLSB_{14}
Dynamic Performance (Bipolar Mode)						
Peak Harmonic or Spurious Noise	(Note 1)					
Full Scale, 1 kHz Input		94	98			dB
						dB
Full Scale, 12 kHz Input		84	87			dB
						dB
Total Harmonic Distortion			0.003			%
Signal-to-Noise Ratio	(Notes 1 and 9)					
1 kHz, 0 dB Input		82	84			dB
						dB
1 kHz, -60 dB Input			23			dB
Noise	(Note 3)					
Unipolar Mode			45			μV_{rms}
Bipolar Mode			90			μV_{rms}

Notes: 9. A detailed plot of S/(N+D) vs. input amplitude appears in Figure 26 for the CS5014 and Figure 28 for the CS5016.

* Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

CS5014 ANALOG CHARACTERISTICS (continued)

Parameter*		CS5014-B Min	Typ	Max		Units
Specified Temperature Range			-40 to +85			°C
Analog Input						
Aperture Time			25			ns
Aperture Jitter			100			ps
Input Capacitance	(Note 4)					
Unipolar Mode			275	375		pF
Bipolar Mode			165	220		pF
Conversion & Throughput						
Conversion Time -14	(Notes 5 and 6)			14.25		µs
Acquisition Time -14	(Note 6)		3.0	3.75		µs
Throughput -14	(Note 6)	55.6				kHz
Power Supplies						
DC Power Supply Currents	(Note 7)					
I_{A+}			9	19		mA
I_{A-}			-9	-19		mA
I_{D+}			3	6		mA
I_{D-}			-3	-6		mA
Power Dissipation	(Note 7)		120	250		mW
Power Supply Rejection	(Note 8)					
Positive Supplies			84			dB
Negative Supplies			84			dB

CS5016 ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; CLKIN = 4 MHz for -16, 2 MHz for -32; Analog Source Impedance = 200Ω; Synchronous Sampling.)

Parameter*			CS5016-J, K Min	CS5016-J, K Typ	CS5016-J, K Max	CS5016-A, B Min	CS5016-A, B Typ	CS5016-A, B Max	CS5016-S, T Min	CS5016-S, T Typ	CS5016-S, T Max	Units
Specified Temperature Range				0 to +70			-40 to +85			-55 to +125		°C
Accuracy												
Linearity Error	J, A, S	(Note 1)		0.002	0.003		0.002	0.003		0.002	0.0076	%FS
	K, B, T			0.001	0.0015		0.001	0.0015		0.001	0.0015	%FS
Drift		(Note 2)		±1/4			±1/4			±1/4		ΔLSB_{16}
Differential Linearity		(Note 10)	16			16			16			Bits
Full Scale Error	J, A, S	(Note 1)		±2	±3		±2	±3		±2	±4	LSB_{16}
	K, B, T			±2	±3		±2	±3		±2	±3	LSB_{16}
Drift		(Note 2)		±1			±1			±2		ΔLSB_{16}
Unipolar Offset	J, A, S	(Note 1)		±1	±2		±1	±3		±1	±4	LSB_{16}
	K, B, T			±1	±3/2		±1	±3		±1	±3	LSB_{16}
Drift		(Note 2)		±1			±1			±2		ΔLSB_{16}
Bipolar Offset	J, A, S	(Note 1)		±1	±2		±1	±2		±1	±4	LSB_{16}
	K, B, T			±1	±3/2		±1	±2		±1	±2	LSB_{16}
Drift		(Note 2)		±1			±2			±2		ΔLSB_{16}
Bipolar Negative Full-Scale Error		(Note 1)										
	J, A, S			±2	±3		±2	±3		±2	±5	LSB_{16}
	K, B, T			±2	±3		±2	±3		±2	±3	LSB_{16}
Drift		(Note 2)		±1			±2			±2		ΔLSB_{16}
Dynamic Performance (Bipolar Mode)												
Peak Harmonic or Spurious Noise		(Note 1)										
Full Scale, 1 kHz Input	J, A, S		96	100		96	100		92	100		dB
	K, B, T		100	104		100	104		100	104		dB
Full Scale, 12 kHz Input	J, A, S		85	88		85	88		82	88		dB
	K, B, T		85	91		85	91		85	91		dB
Total Harmonic Distortion	J, A, S			0.002			0.002			0.002		%
Full Scale, 1 kHz Input	K, B, T			0.001			0.001			0.001		%
Signal-to-Noise Ratio		(Notes 1 and 9)										
1 kHz, 0 dB Input	J, A, S		87	90		87	90		84	90		dB
	K, B, T		90	92		90	92		90	92		dB
1 kHz, -60 dB Input	J, A, S			30			30			30		dB
	K, B, T			32			32			32		dB
Noise		(Note 3)										
Unipolar Mode				35			35			35		μV_{rms}
Bipolar Mode				70			70			70		μV_{rms}

Notes: 10. Minimum resolution for which no missing codes is guaranteed

* Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

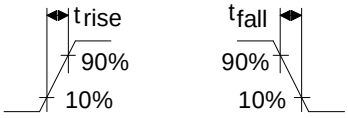
CS5016 ANALOG CHARACTERISTICS (continued)

Parameter*	CS5016-J, K Min	CS5016-J, K Typ	CS5016-J, K Max	CS5016-A, B Min	CS5016-A, B Typ	CS5016-A, B Max	CS5016-S, T Min	CS5016-S, T Typ	CS5016-S, T Max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Analog Input										
Aperture Time		25			25			25		ns
Aperture Jitter		100			100			100		ps
Input Capacitance (Note 4)										
Unipolar Mode		275	375		275	375		275	375	pF
Bipolar Mode		165	220		165	220		165	220	pF
Conversion & Throughput										
Conversion Time -16 (Notes 5 and 6)			16.25			16.25			16.25	µs
-32			32.5			32.5			32.5	µs
Acquisition Time -16 (Note 6)		3.0	3.75		3.0	3.75		3.0	3.75	µs
-32		4.5	5.25		4.5	5.25		4.5	5.25	µs
Throughput -16 (Note 6)	50			50			50			kHz
-32	26.5			26.5			26.5			kHz
Power Supplies										
DC Power Supply Currents (Note 7)										
I_{A+}		9	19		9	19		9	19	mA
I_{A-}		-9	-19		-9	-19		-9	-19	mA
I_{D+}		3	6		3	6		3	6	mA
I_{D-}		-3	-6		-3	-6		-3	-6	mA
Power Dissipation (Note 7)		120	250		120	250		120	250	mW
Power Supply Rejection (Note 8)										
Positive Supplies		84			84			84		dB
Negative Supplies		84			84			84		dB

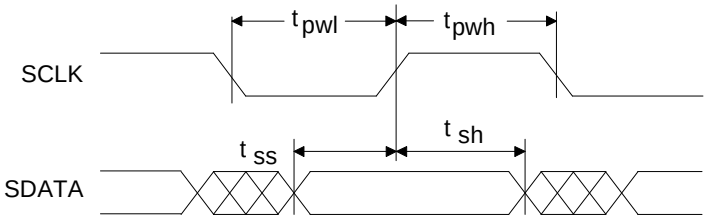
SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V ±10%; VA-, VD- = -5V ±10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF, BW = VD+)

Parameter			Symbol	Min	Typ	Max	Units
CS5012A CLKIN Frequency:			f_{CLK}				
	Internally Generated:			1.75	-	-	MHz
	Externally Supplied:	-7		100 kHz	-	6.4	MHz
CS5014/5016 CLKIN Frequency:			f_{CLK}				
	Internally Generated:	-14, -16		1.75	-	-	MHz
		-14, -32		1	-	-	MHz
	Externally Supplied:	-14, -16		100 kHz	-	4	MHz
		-14, -32		100 kHz	-	2	MHz
CLKIN Duty Cycle				40	-	60	%
Rise Times:		Any Digital Input	t_{rise}	-	-	1.0	µs
		Any Digital Output		-	20	-	ns
Fall Times:		Any Digital Input	t_{fall}	-	-	1.0	µs
		Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width			t_{hpw}	$1/f_{CLK}$+50	-	t_c	ns
Conversion Time:		CS5012A	t_c	$49/f_{CLK}$+50	-	$53/f_{CLK}$+235	ns
		CS5014		$57/f_{CLK}$	-	$61/f_{CLK}$+235	ns
		CS5016		$65/f_{CLK}$	-	$69/f_{CLK}$+235	ns
Data Delay Time			t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width		(Note 11)	t_{epw}	$4/f_{CLK}$-20	-	-	ns
Set Up Times:	CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low		t_{cs}	20	10	-	ns
	A0 to $\overline{CS}$ and $\overline{RD}$ Low		t_{as}	20	10	-	ns
Hold Times:	$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid		t_{ah}	50	30	-	ns
	$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid		t_{ch}	50	30	-	ns
Access Times:	$\overline{CS}$ Low to Data Valid	A, B, J, K	t_{ca}	-	90	120	ns
		S, T		-	115	150	ns
	$\overline{RD}$ Low to Data Valid	A, B, J, K	t_{ra}	-	90	120	ns
		S, T		-	90	150	ns
Output Float Delay:		K, B	t_{fd}	-	90	110	ns
	$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z	T		-	90	140	ns
Serial Clock	Pulse Width Low		t_{pwl}	-	$2/f_{CLK}$	-	ns
	Pulse Width High		t_{pwh}	-	$2/f_{CLK}$	-	ns
Set Up Times:	SDATA to SCLK Rising		t_{ss}	$2/f_{CLK}$-50	$2/f_{CLK}$	-	ns
Hold Times:	SCLK Rising to SDATA		t_{sh}	$2/f_{CLK}$-100	$2/f_{CLK}$	-	ns

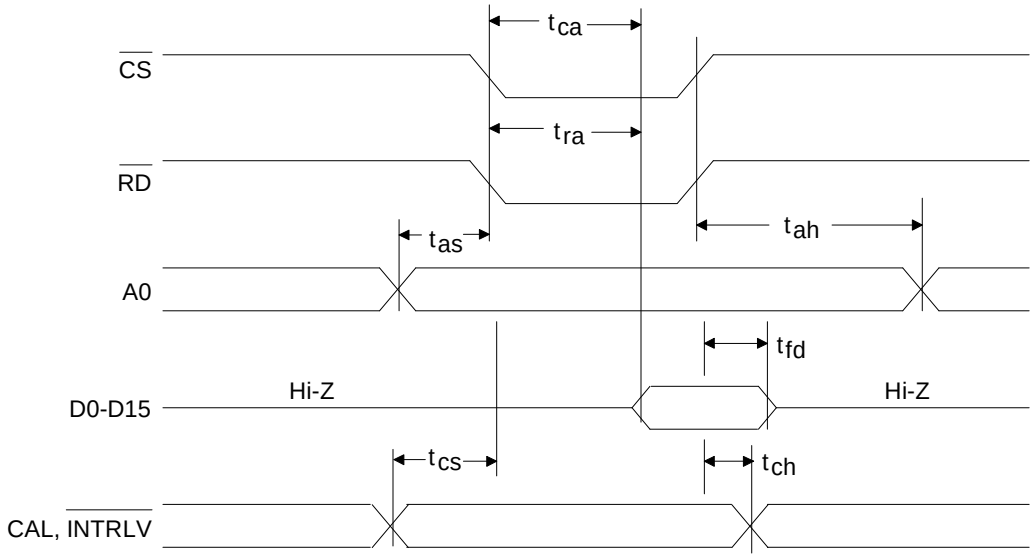
Notes: 11. $\overline{EOC}$ remains low 4 CLKIN cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, it returns high within 4 CLKIN cycles from the start of a data read operation or a conversion cycle.



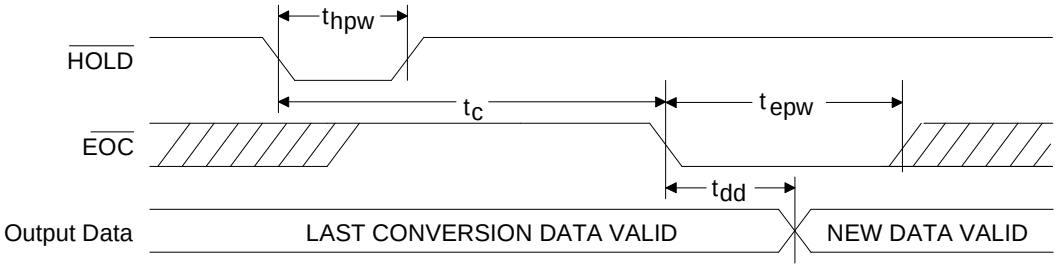
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V ±10%; VA-, VD- = -5V ±10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 12)	V_{OH}	(VD+) - 1.0V	-	-	V
Low-Level Output Voltage I_{out} = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Notes: 12. I_{out} = -100 µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{out} = -40 µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 13)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	-4.5	-5.0	-5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	-4.5	-5.0	-5.5	V
Analog Reference Voltage		VREF	2.5	4.5	(VA+) - 0.5	V
Analog Input Voltage: (Note 14)						
Unipolar		V_{AIN}	AGND	-	VREF	V
Bipolar		V_{AIN}	-VREF	-	VREF	V

Notes: 13. All voltages with respect to ground.
14. The CS5012A/14/16 can accept input voltages up to the analog supplies (VA+ and VA-). It will output all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with repect to ground.)

WARNING: Operation at or beyond these limits may reult in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter			Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	(Note 15)	VD+	-0.3	6.0	V
	Negative Digital		VD-	0.3	-6.0	V
	Positive Analog		VA+	-0.3	6.0	V
	Negative Analog		VA-	0.3	-6.0	V
Input Current, Any Pin Except Supplies		(Note 16)	I_{in}	-	±10	mA
Analog Input Voltage	(AIN and VREF pins)		V_{INA}	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage			V_{IND}	-0.3	(VA+) + 0.3	V
Ambient Operating Temperature			T_A	-55	125	°C
Storage Temperature			T_{stg}	-65	150	°C

Notes: 15. In addition, VD+ should not be greater than (VA+) + 0.3V.
16. Transient currents of up to 100 mA will not cause SCR latch-up.

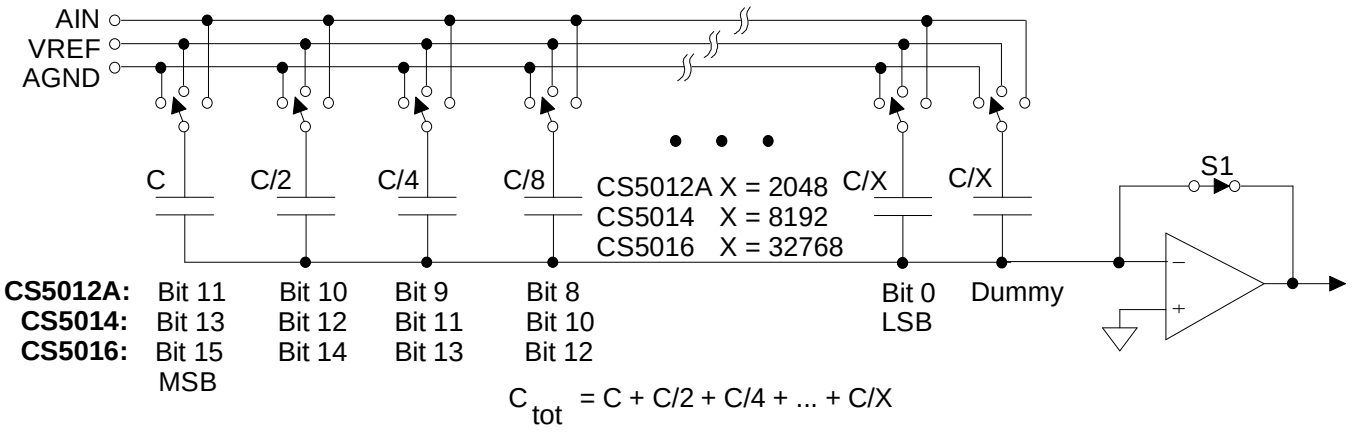


Figure 1. Charge Redistribution DAC

THEORY OF OPERATION

The CS5012A/14/16 family utilize a successive approximation conversion technique. The analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the analog input to the DAC output which is set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of full scale. This procedure continues until all bits have been exercised.

A unique charge redistribution architecture is used to implement the successive approximation algorithm. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the array share a common node at the comparator's input. Their other terminals are capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all capacitors are tied to AIN forming C_{tot}. Switch S1 is closed and the charge on the array, Q_{in}, tracks the input signal V_{in} (Figure 2a).

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps charge Q_{in} on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory

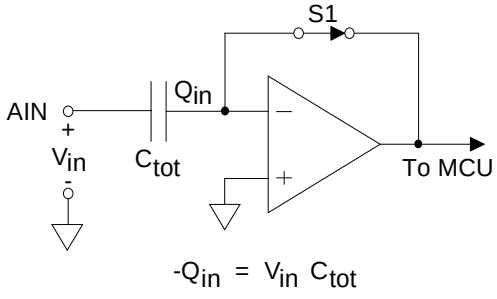


Figure 2a. Tracking Mode

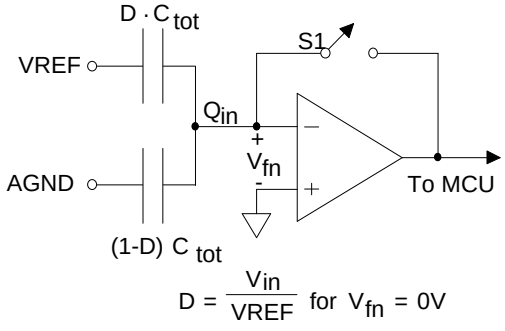


Figure 2b. Convert Mode

during conversion much like a hold capacitor in a sample/hold amplifier.

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which when connected to the reference will drive the voltage at the floating node (V_{fn}) to zero. That binary fraction of capacitance represents the converter's digital output.

This charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range is doubled and is offset half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

Calibration

The ability of the CS5012A/14/16 to convert accurately clearly depends on the accuracy of their comparator and DAC. The CS5012A/14/16 utilize an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve complete accuracy from the DAC, the CS5012A/14/16 use a novel self-calibration scheme. Each bit capacitor, shown in Figure 1, actually consists of several capacitors which can be manipulated to adjust the overall bit weight. An on-chip microcontroller adjusts the subarrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). Calibration resolution for the array is a small fraction of an LSB resulting in nearly ideal differential and integral linearity.

DIGITAL CIRCUIT CONNECTIONS

The CS5012A/14/16 can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the devices' conversion time and throughput. The devices also feature on-chip 3-state output buffers and a complete interface for connecting to 8-bit and 16-bit digital systems. Output data is also available in serial format.

Master Clock

The CS5012A/14/16 operate from a master clock (CLKIN) which can be externally supplied or internally generated. The internal oscillator is activated by externally tying the CLKIN input low. Alternatively, the CS5012A/14/16 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

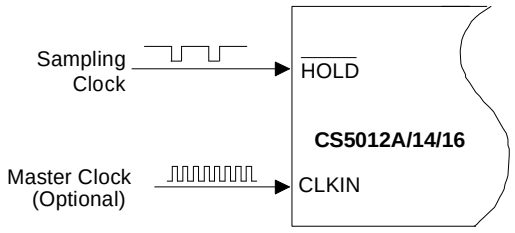


Figure 3a. Asynchronous Sampling

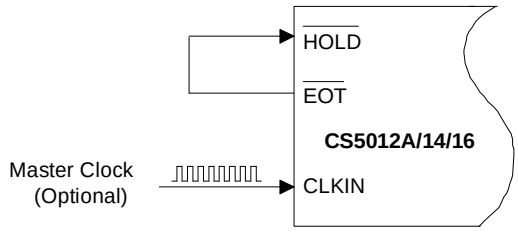


Figure 3b. Synchronous Sampling

All calibration, conversion, and throughput times directly scale to CLKIN frequency. Thus, throughput can be precisely controlled and/or maximized using an external CLKIN signal. In contrast, the CS5012A/14/16's internal oscillator will vary from unit-to-unit and over temperature. The CS5012A/14/16 can typically convert with CLKIN as low as 10 kHz at room temperature.

Initiating Conversions

A falling transition on the $\overline{\text{HOLD}}$ pin places the input in the hold mode and initiates a conversion cycle. Upon completion of the conversion cycle, the CS5012A/14/16 automatically return to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{\text{HOLD}}$ input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one CLKIN cycle plus 50 ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

Microprocessor-Controlled Operation

Sampling and conversion can be placed under microprocessor control (Figure 4) by simply gating the devices' decoded address with the write strobe for the $\overline{\text{HOLD}}$ input. Thus, a write cycle to the CS5012A/14/16's base address will initiate a conversion. However, the write cycle must be to the odd address (A0 high) to avoid initiating a software controlled reset (see *Reset* below).

The calibration control inputs, CAL, and $\overline{\text{INTRLV}}$ are inputs to a set of transparent latches. These signals are internally latched by $\overline{\text{CS}}$ returning high. They must be in the appropriate state whenever the chip is selected during a read or write cycle. Address lines A1 and A2 are shown connected to CAL and $\overline{\text{INTRLV}}$ in Figure 4 placing calibration under microprocessor control as well. Thus, any read or write cycle to the CS5012A/14/16's base address will initiate or terminate calibration. Alternatively, A0, $\overline{\text{INTRLV}}$, and CAL may be connected to the microprocessor data bus.

Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the CS5012A/14/16 require time to acquire the analog input signal before another conversion can be initiated. The acquisition time is specified as six CLKIN cycles plus 2.25 µs (1.32 µs for the CS5012A -7 version only). This adds to the conversion time to define the converter's maximum throughput. The conversion time of the CS5012A/14/16, in turn, depends on the sampling, calibration, and CLKIN conditions.

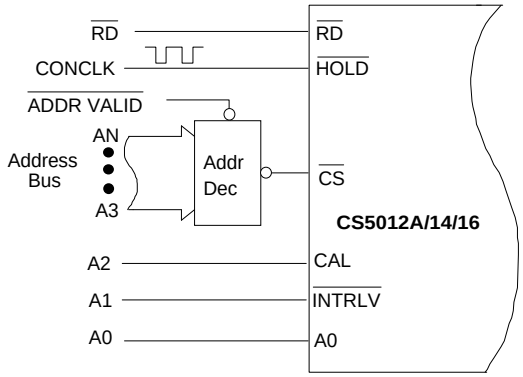


Figure 4a. Conversions Asynchronous to CLKIN

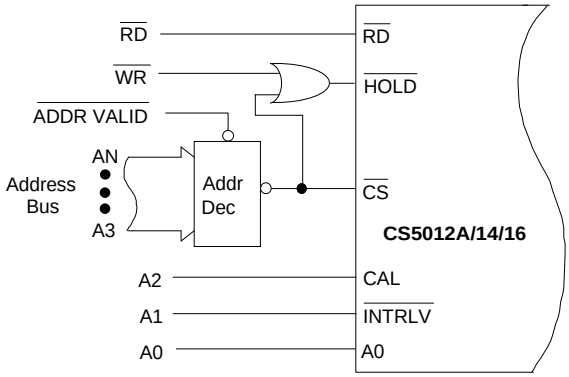


Figure 4b. Conversions under Microprocessor Control

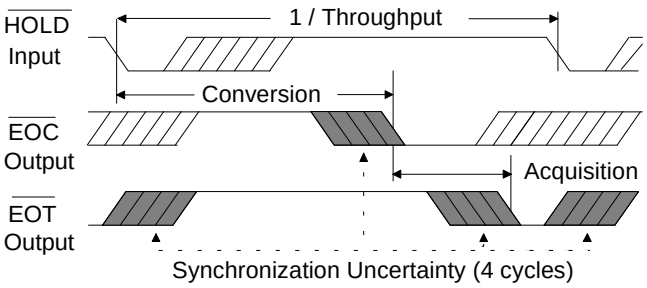


Figure 5a. Asynchronous Sampling (External Clock)

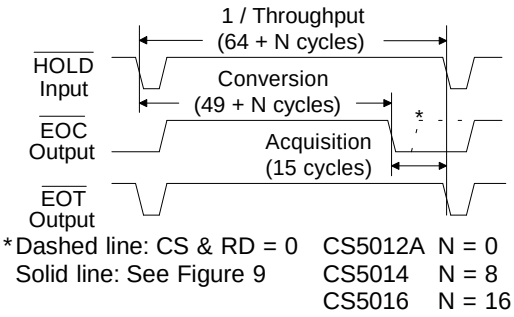


Figure 5b. Synchronous (Loopback Mode)

Asynchronous Sampling

The CS5012A/14/16 internally operate from a clock which is delayed and divided down from CLKIN ($f_{CLK}/4$). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after $\overline{HOLD}$ goes low *even though the charge is trapped immediately.* In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 49, 57 and 65 clock cycles (for the CS5012A/14/16 respectively) to define the maximum conversion time (see Figure 5a and Table 1).

Synchronous Sampling

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track ($\overline{EOT}$) output to $\overline{HOLD}$ (Figure 3b). The $\overline{EOT}$ output falls 15 CLKIN cycles after $\overline{EOC}$ indicating the analog input has been acquired to the CS5012A/14/16's specified accuracy. The $\overline{EOT}$ output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at $[1/64]f_{CLK}$ for the CS5012A, $[1/72]f_{CLK}$ for CS5014 and $[1/80]f_{CLK}$ for CS5016 where f_{CLK} is the CLKIN frequency (see Figure 5b and Table 1).

Sampling Mode	Conversion Time Min	Conversion Time Max	Throughput Time Min	Throughput Time Max
CS5012A				
Synchronous (Loopback)	49 t_{clk}	49 t_{clk}	64 t_{clk}	64 t_{clk}
Asynchronous -7	49 t_{clk}	53 t_{clk} + 235 ns	N/A	59 t_{clk} + 1.32 µs
Asynchronous -12,-24	49 t_{clk}	53 t_{clk} + 235 ns	N/A	59 t_{clk} + 2.25 µs
CS5014				
Synchronous (Loopback)	57 t_{clk}	57 t_{clk}	72 t_{clk}	72 t_{clk}
Asynchronous	57 t_{clk}	61 t_{clk} + 235 ns	N/A	67 t_{clk} + 2.25 µs
CS5016				
Synchronous (Loopback)	65 t_{clk}	65 t_{clk}	80 t_{clk}	80 t_{clk}
Asynchronous	65 t_{clk}	69 t_{clk} + 235 ns	N/A	75 t_{clk} + 2.25 µs

Table 1. Conversion and Throughput Times (t_{clk} = Master Clock Period)

Also, the CS5012A/14/16's internal RC oscillator exhibits jitter (typically ± 0.05% of its period), which is high compared to crystal oscillators. If the CS5012A/14/16 is configured for synchronous sampling while operating from its internal oscillator, this jitter will directly affect sampling purity. The user can obtain best sampling purity while synchronously sampling by using an external crystal-based clock.

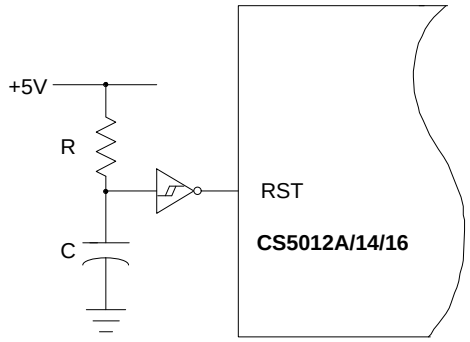


Figure 6. Power-on Reset Circuit

Reset

Upon power up, the CS5012A/14/16 must be reset to guarantee a consistent starting condition and initially calibrate the devices. Due to the CS5012A/14/16's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 5%, 1% or 0.25% of its final value, for the CS5012A/14/16 respectively, before RST falls to guarantee an accurate calibration. Later, the CS5012A/14/16 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CS5012A/14/16 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

Resets can be initiated in hardware or software. The simplest method of resetting the CS5012A/14/16 involves strobing the RST pin high for at least 100 ns. When RST is brought high all internal logic clears. When it returns low, a full calibration begins which takes 58,280 CLKIN cycles for the CS5012A (approximately 9.1 ms with a 6.4 MHz clock) and 1,441,020 CLKIN cycles for the CS5016, CS5014 and CS5012 (approximately 360 ms with a 4 MHz CLKIN). A simple power-on reset circuit can be built using a resistor and capacitor, and a Schmitt-trigger inverter to prevent oscillation (see Figure 6). The CS5012A/14/16 can also be reset in software when under microprocessor control. The CS5012A/14/16 will reset whenever $\overline{CS}$, A0, and $\overline{HOLD}$ are taken low simultaneously. See the *Microprocessor Interface* section (below) to eliminate the possibility of inadvertent software reset. The $\overline{EOC}$ output remains high throughout the calibration operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the CS5012A/14/16 is ready for operation. While calibrating, the $\overline{HOLD}$ input is ignored until $\overline{EOC}$ falls. After $\overline{EOC}$ falls, six CLKIN cycles plus 2.25 µs (1.32 µs for the CS5012A -7 version only) must be allowed for signal acquisition before $\overline{HOLD}$ is activated. Under microprocessor-independent operation ($\overline{CS}$, $\overline{RD}$ low; A0 high) the CS5014's and CS5016's $\overline{EOC}$ output will not fall at the completion of the calibration cycle, but $\overline{EOT}$ will fall 15 CLKIN cycles later.

Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the CS5012A/14/16's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is normally only required once, after power-up.

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, "burst" cal, allows control of partial calibration cycles. *Due to an unforeseen condidtion inside the part, asynchronous termination of calibration may result in a sub-optimal result. Burst cal should not be used.*

The reset calibration always works perfectly, and should be used instead of burst mode. The CS5012's and CS5012A/14/16's very low drift over temperature means that, under most circumstances, calibration will only need to be performed at power-up, using reset.

The CS5012A/14/16 feature a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The CS5012A/14/16 gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 2,014 conversions in the CS5012A and one calibration per 72,051 conversions in the CS5012, CS5014 and CS5016). Initiated by bringing both the $\overline{\text{INTRLV}}$ input and $\overline{\text{CS}}$ low (or hard-wiring $\overline{\text{INTRLV}}$ low), interleave extends the CS5012A/14/16's effective conversion time by 20 CLKIN cycles. Other than reduced throughput, interleave is totally transparent to the user. Interleave calibration should not be used intermittently.

The fact that the CS5012A/14/16 offer several calibration modes is not to imply that the devices need to be recalibrated often. The devices are very stable in the presence of large temperature changes. Tests have indicated that after using a single reset calibration at 25 °C most devices exhibit very little change in offset or gain when exposed to temperatures from -55 to +125 °C. The data indicated 30 ppm as the typical worst case total change in offset or gain over this temperature range. Differential linearity remained virtually unchanged. System error sources outside of the A/D converter, whether due to changes in temperature or to long-term aging, will generally dominate total system error.

Microprocessor Interface

The CS5012A/14/16 feature an intelligent microprocessor interface which offers detailed status information and allows software control of the self-calibration functions. Output data is available in either 8-bit or 16-bit formats for easy interfacing to industry-standard microprocessors.

Strobing both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low enables the CS5012A/14/16's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected to A0 as shown in Figure 4b thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ($\overline{\text{CS}}$ and $\overline{\text{RD}}$ strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while $\overline{\text{HOLD}}$ is low, or a software reset will result* (see *Reset* above).

Alternatively, the End-of-Convert ($\overline{\text{EOC}}$) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The $\overline{\text{EOC}}$ pin falls as each conversion cycle is completed and data is valid at the output. It returns high within four CLKIN cycles of the first subsequent data read operation or after the start of a new conversion cycle.

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	END OF CONVERSION	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/HIGH BYTE	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	END OF TRACK	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the input.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Pin Definitions

To interface with a 16-bit data bus, the BW input to the CS5012A/14/16 should be held high and all data bits (12, 14 and 16 for the CS5012A, CS5014 and CS5016 respectively) read in parallel on pins D4-D15 (CS5012A), D2-D15 (CS5014), or D0-D15 (CS5016). With an 8-bit bus, the converter's result must be read in two portions. In this instance, BW should be held low and the 8 MSB's obtained on the first read cycle following a conversion. The second read cycle will yield the remaining LSB's (4, 6 or 8 for the CS5012A/14/16 respectively) with 4, 2 or 0 trailing zeros. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next conversion finishes. Status bit S2 indicates which byte will appear on the next data read operation.

The CS5012A/14/16 internally buffer their output data, so data can be read while the devices are tracking or converting the next sample. Therefore, retrieving the converters' digital output requires no reduction in ADC throughput. Enabling the 3-state outputs while the CS5012A/14/16 is converting will not introduce conversion errors. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

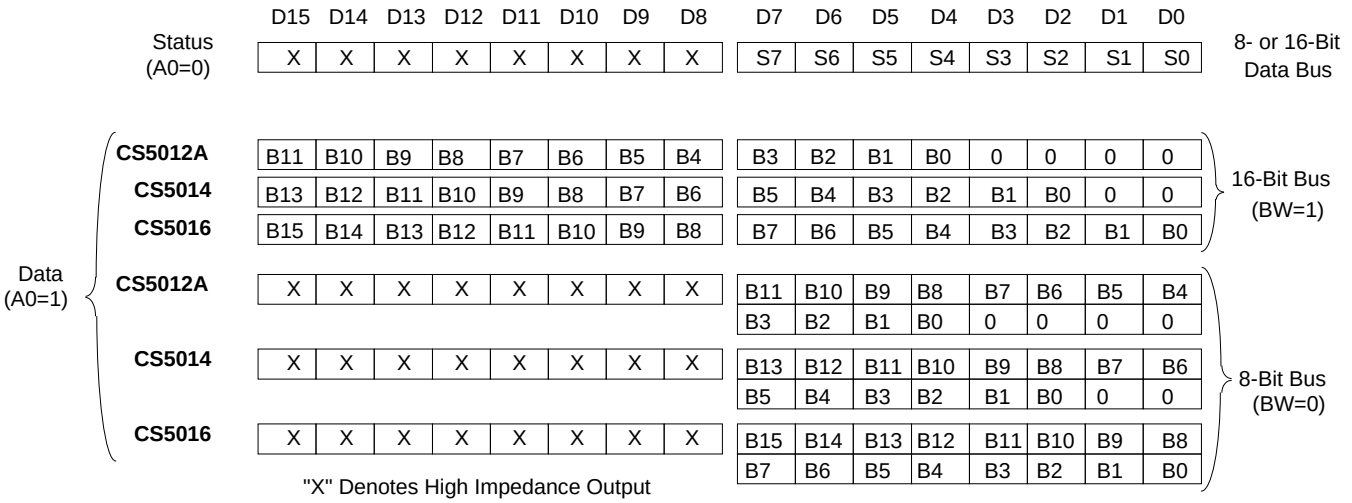


Figure 7. CS5012A/14/16 Data Format

Microprocessor Independent Operation

The CS5012A/14/16 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{CS}$ and $\overline{RD}$ are hard-wired low. This permanently enables the 3-state output buffers and allows transparent latch inputs (CAL and $\overline{INTRLV}$) to be active. A free-running condition is established when BW is tied high, CAL is tied low, and $\overline{HOLD}$ is continually strobed low or tied to $\overline{EOT}$. The CS5012A/14/16's $\overline{EOC}$ output can be used to externally latch the output data if desired. With $\overline{CS}$ and $\overline{RD}$ hard-wired low, $\overline{EOC}$ will strobe low for four CLKIN cycles after each conversion. Data will be unstable up to 100 ns after $\overline{EOC}$ falls, so it should be latched on the rising edge of $\overline{EOC}$.

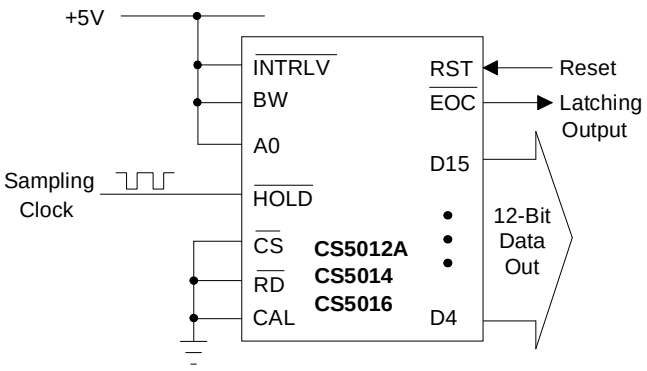


Figure 8. Microprocessor-Independent Connections

Serial Output

All successive-approximation A/D converters derive their digital output serially starting with the MSB. The CS5012A/14/16 present each bit to the SDATA pin four CLKIN cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the CS5012A/14/16 (See Figure 9).

ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5012A/14/16 internally buffer all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage References for the CS501X Series of A/D Converters*" is available for the CS5012A/14/16. In addition to working through a reference circuit design example, it offers several built-and-tested reference circuits.

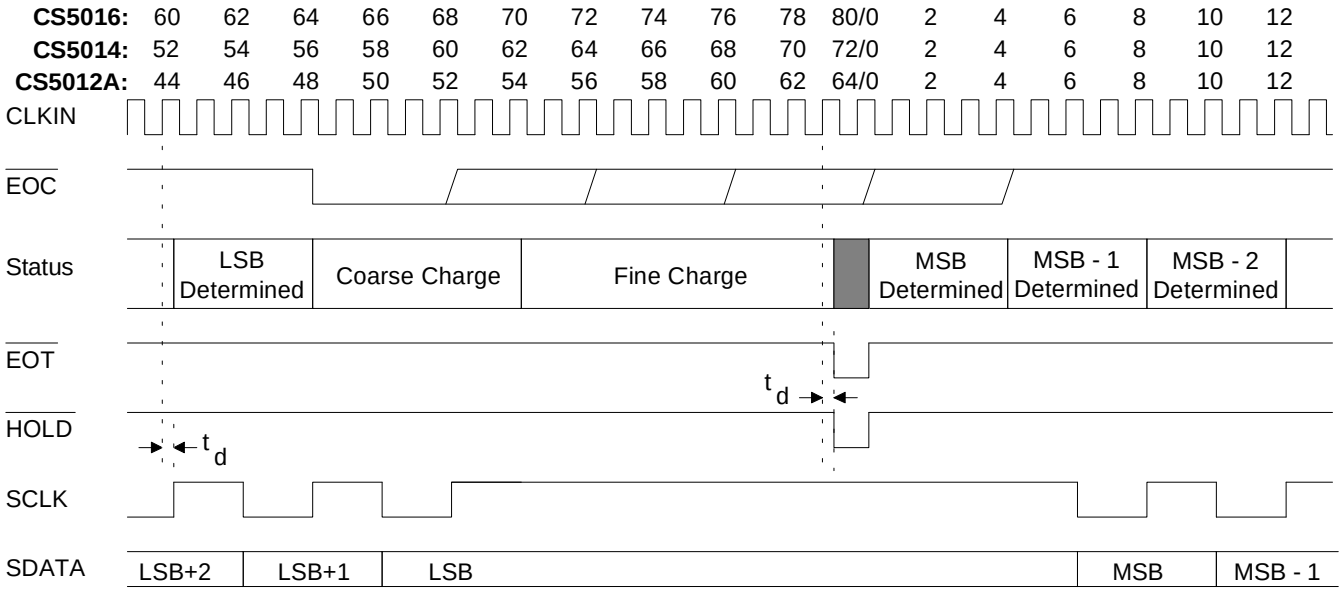
During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CS5012A/14/16 include an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the CS5012A/14/16 sequence through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant

peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc.

The magnitude of the current load on the external reference circuitry will scale to the CLKIN frequency. At full speed, the reference must supply a maximum load current of 10 µA peak-to-peak (1 µA typical). For the CS5012A an output impedance of 15 Ω will therefore yield a maximum error of 150 mV. With a 2.5V reference and LSB size of 600 mV, this would insure better than 1/4 LSB accuracy. A 1 µF capacitor exhibits an impedance of less than 15 Ω at frequencies greater than 10 kHz. Similarly, for the CS5014 with a 4.5V reference (275µV/LSB), better than 1/4 LSB accuracy can be insured with an output impedance of 4Ω or less (maximum error of 40 µV). A 2.2 µF capacitor exhibits an impedance of less than 4Ω at frequencies greater than 5kHz. For the CS5016 with a 4.5V reference (69µV/LSB), better than 1/4 LSB accuracy can be insured with an output impedance of less than 2Ω (maximum error of 20 µV). A 20 µF capacitor exhibits an impedance of less than 2Ω at frequencies greater than 16 kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.



Notes: 1. Synchronous (loopback) mode is illustrated. After $\overline{EOC}$ falls the converter goes into coarse charge mode for 6 CLKIN cycles, then to fine charge mode for 9 cycles, then $\overline{EOT}$ falls. In loopback mode, $\overline{EOT}$ trips $\overline{HOLD}$ which captures the analog sample. Conversion begins on the next rising edge of CLKIN. If operated asynchronously, $\overline{EOT}$ will remain low until after $\overline{HOLD}$ is taken low. When $\overline{HOLD}$ occurs the analog sample is captured immediately, but conversion may not begin until four CLKIN cycles later. $\overline{EOT}$ will return high when conversion begins.

2. Timing delay t_d (relative to CLKIN) can vary between 135 ns to 235 ns over the military temperature range and over ± 10% supply variation

3. $\overline{EOC}$ returns high in 4 CLKIN cycles if A0 = 1 and $\overline{CS}$ = $\overline{RD}$ = 0 (Microprocessor Independent Mode); within 4 CLKIN cycles after a data read (Microprocessor Mode); or 4 CLKIN cycles after $\overline{HOLD}$ = 0 is recognized on a rising edge of CLKIN/4.

Figure 9. Serial Output Timing

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

The CS5012A/14/16 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is between 2.5 and 4.5 V for the CS5012A and 4.5 V for the CS5014/16. The CS5012A/14/16 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1 µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult the application note: Voltage References for the CS501X Series of A/D Converters. For an example of using the CS5012A/14/16 with a 5 volt reference, see the application note: A Collection of Application Hints for the CS501X Series of A/D Converters.

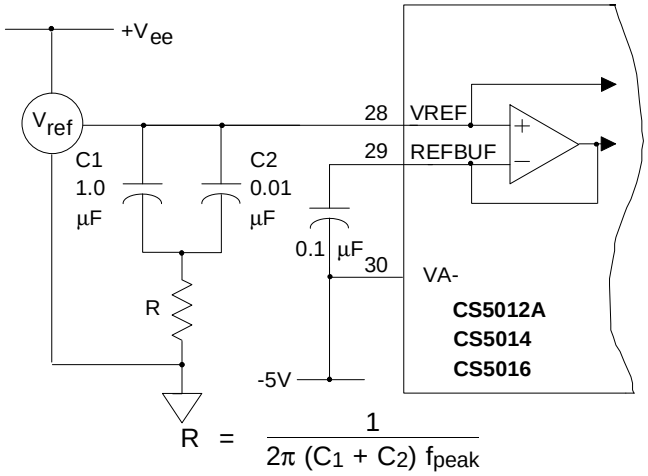


Figure 10. Reference Connections

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six CLKIN cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is required for fine-charging directly from AIN to

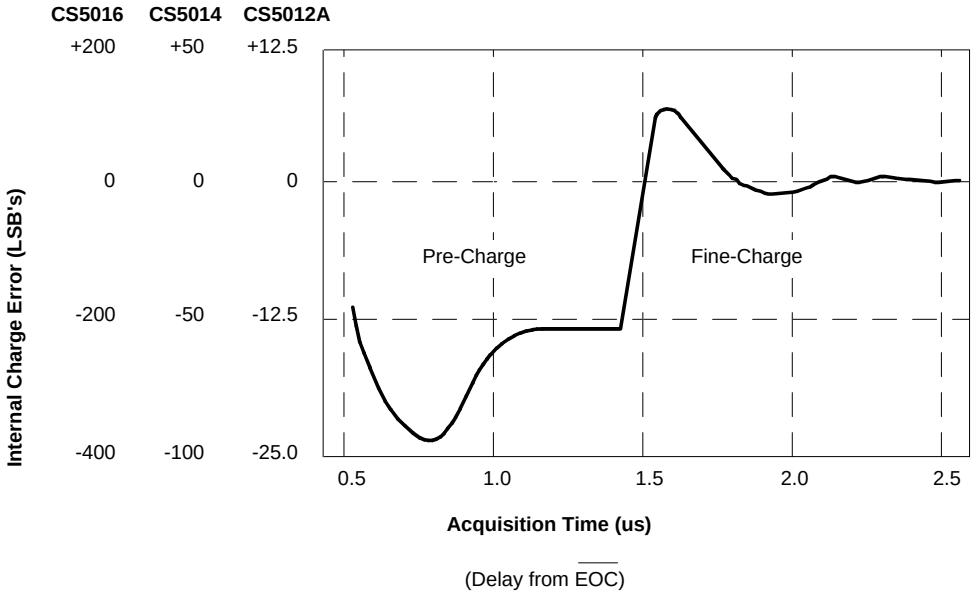


Figure 11. Internal Acquisition Time

obtain the specified accuracy. Figure 11 illustrates this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

The acquisition time of the CS5012A/14/16 depends on the CLKIN frequency. This is due to a fixed pre-charge period. For instance, operating the CS5012A -12, CS5014 -14 or CS5016 -16 version with an external 4 MHz CLKIN results in a 3.75 µs acquisition time: 1.5 µs for pre-charging (6 clock cycles) and 2.25 µs for fine-charging. Fine-charge settling is specified as a maximum of 2.25 µs for an analog source impedance of less than 200 Ω. (For the CS5012A -7 version it is specified as 1.32 µs.) In addition, the comparator requires a source impedance of less than 400 Ω around 2 MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN to ground (typically 200 pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time. For more information on input applications, consult the application note: *Input Buffer Amplifiers for the CS501X Family of A/D Converters*.

During the first six clock cycles following a conversion (pre-charge) in unipolar mode, the CS5012A is capable of slewing at 20V/µs and the CS5014/16 can slew at 5V/µs. In bipolar mode, only half the capacitor array is connected to the analog input so the CS5012A can slew at 40V/µs, and the CS5014/16 can slew at 10V/µs. After the first six CLKIN cycles, the CS5012A will slew at 1.25V/µs in unipolar mode and 3.0V/µs in bipolar mode, and the CS5014/16 will slew at 0.25V/µs in unipolar mode and 0.5V/µs in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the CS5012A/14/16 is converting (see Figure 12). Multiplexer settling is thereby removed from the overall throughput equation, and the CS5012A/14/16 can convert at full speed.

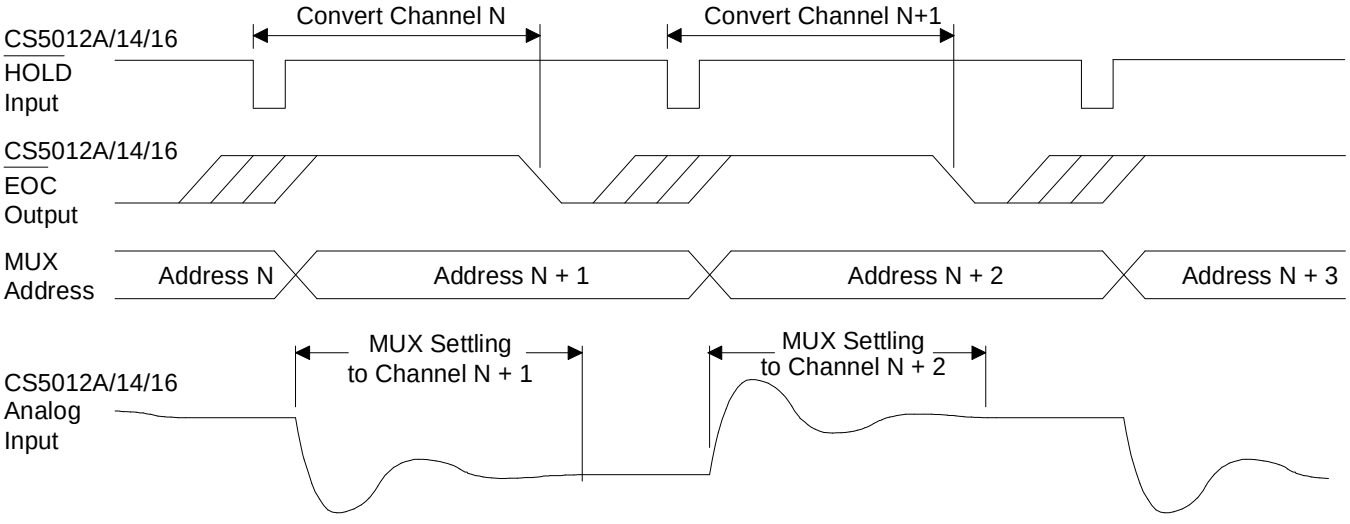


Figure 12. Pipelined MUX Input Channels

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of all ones, and negative full scale gives a digital output of all zeros.

The BP/$\overline{UP}$ mode pin may be switched after calibration without having to recalibrate the converter. However, the BP/$\overline{UP}$ mode should be changed during the previous conversion cycle, that is, between $\overline{HOLD}$ falling and $\overline{EOC}$ falling. If BP/$\overline{UP}$ is changed at any other time, one dummy conversion cycle must be allowed for proper acquisition of the input.

Grounding and Power Supply Decoupling

The CS5012A/14/16 use the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground reference point.

The digital and analog supplies to the CS5012A/14/16 are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 µF ceramic capacitors. If significant low-frequency noise is present on the supplies, 1 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CS5012A/14/16 must never exceed the positive analog supply by more than a diode drop or the device could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram in Figure 36 shows a decoupling scheme which allows the CS5012A/14/16 to be powered from a single set of ± 5V rails.

As with any high-precision A/D converter, the CS5012A/14/16 require careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the device. The CDB5012/14/16 evaluation board is available for the CS5012A/14/16, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5012A/14/16, and can be quickly reconfigured to simulate any combination of sampling, calibration, CLKIN, and analog input range conditions.

Power Supply Rejection

The CS5012A/14/16's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CS5012A/14/16's accuracy. This is because the CS5012A/14/16 adjust their offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 13 shows power supply rejection of the CS5012A/14/16 in the bipolar mode with the analog input grounded and a 300 mVp-p ripple applied to each supply. Power supply rejection improves by 6 dB in the unipolar mode.

The plot in Figure 13 shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode.

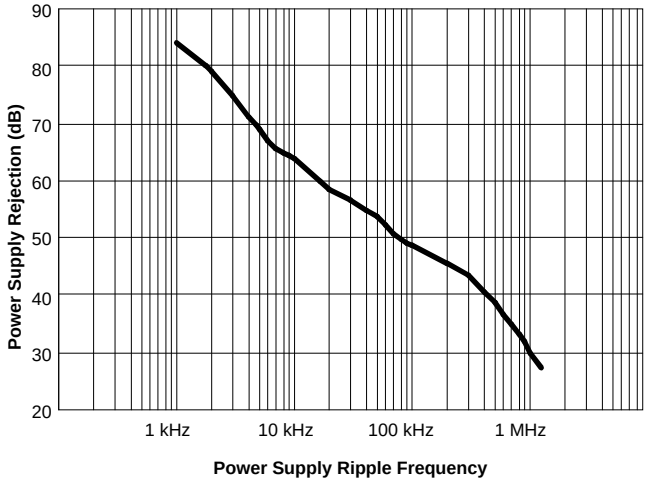


Figure 13. Power Supply Rejection

CS5012A/14/16 PERFORMANCE

Differential Nonlinearity

One source of nonlinearity in A/D converters is bit weight errors. These errors arise from the deviation of bits from their ideal binary-weighted ratios, and lead to nonideal widths for each code. If DNL errors are large, and code widths shrink to zero, it is possible for one or more codes to be entirely missing. The CS5012A/14/16 calibrate all bits in the capacitor array to a small fraction of an LSB resulting in nearly ideal DNL. Histogram plots of typical DNL of the CS5012A/14/16 can be seen in Figures 14, 16, 17. Figure 15 illustrates the DNL of the CS5012 for comparison with the CS5012A (Figure 14).

A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A code with more or less occurrences than average will appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

Integral Nonlinearity

Integral Nonlinearity (INL; also termed Relative Accuracy or just Nonlinearity) is defined as the deviation of the transfer function from an ideal straight line. Bows in the transfer curve generate harmonic distortion. The worst-case condition of bit-weight errors (DNL) has traditionally also defined the point of maximum INL.

Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal.

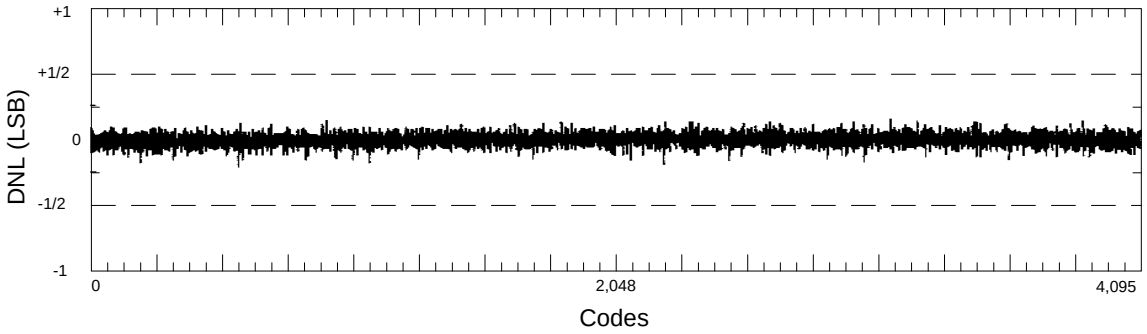


Figure 14. CS5012A Differential Nonlinearity Plot

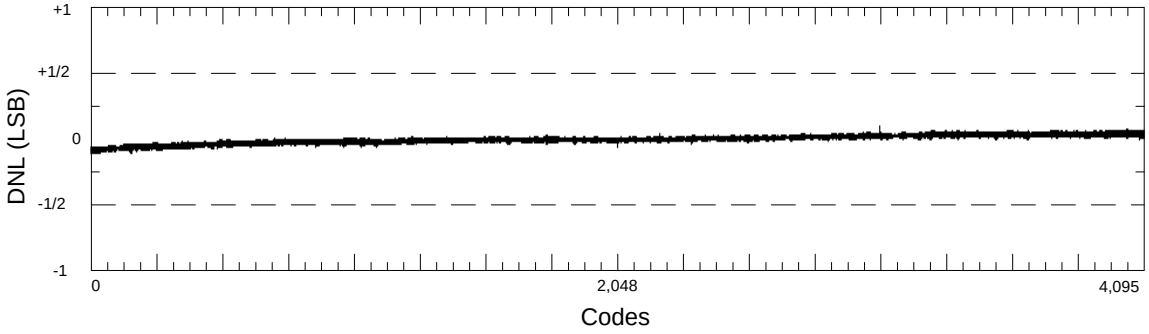


Figure 15. CS5012 Differential Nonlinearity Plot

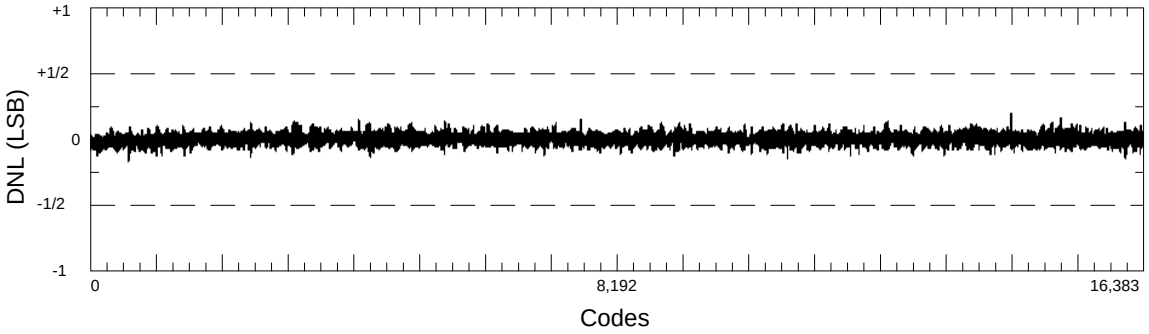


Figure 16. CS5014 Differential Nonlinearity Plot

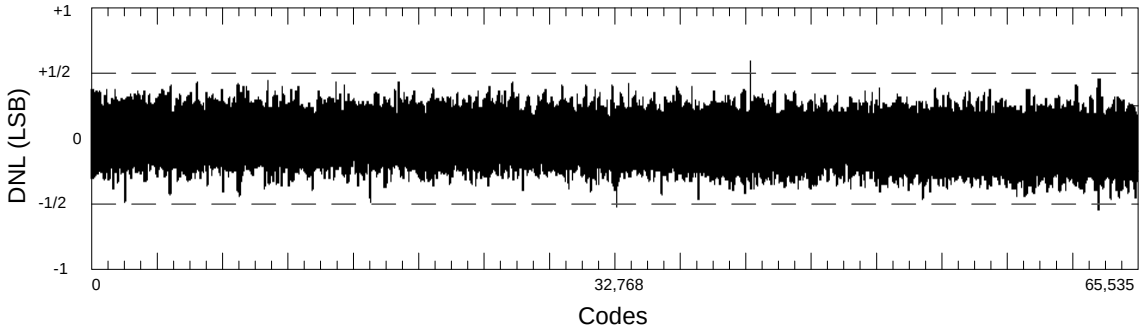


Figure 17. CS5016 Differential Nonlinearity Plot

Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions. Designing a system around characterization data is risky since transfer curves can differ drastically unit-to-unit and lot-to-lot.

The CS5012A/14/16 achieves repeatable signal-to-noise and harmonic distortion performance using an on-chip self-calibration scheme. The CS5012A calibrates its bit weight errors to a small fraction of an LSB at 12-bits yielding peak distortion below the noise floor (see Figure 19). The CS5014 calibrates its bit weights to within ±1/16 LSB at 14-bits (±0.0004% FS) yielding peak distortion as low as -105 dB (see Figure 22). The CS5016 calibrates its bit weights to within ±1/4 LSB at 16-bits (±0.0004% FS) yielding peak distortion as low as -105 dB (see Figure 24). Unlike traditional ADC's, the linearity of the CS5012A/14/16 are not limited by bit-weight errors; their performance is therefore extremely repeatable and independent of input signal conditions.

Quantization Noise

The error due to quantization of the analog input ultimately dictates the accuracy of any A/D converter. The continuous analog input must be represented by one of a finite number of digital codes, so the best accuracy to which an analog input can be known from its digital code is ±1/2 LSB. Under circumstances commonly encountered in signal processing applications, this quantization error can be treated as a random variable. The magnitude of the error is limited to ±1/2 LSB, but any value within this range has equal probability of occurrence. Such a probability distribution leads to an error "signal" with an rms value of 1 LSB/$\sqrt{12}$. Using an rms signal value of FS/$\sqrt{8}$ (amplitude = FS/2), this relates to ideal 12, 14 and 16-bit signal-to-noise ratios of 74, 86 and 98 dB respectively.

Equally important is the spectral content of this error signal. It can be shown to be approximately white, with its energy spread uniformly over the band from dc to one-half the sampling rate. Advantage of this characteristic can be made by judicious use of filtering. If the signal is bandlimited, much of the quantization error can be filtered out, and improved system performance can be attained.

FFT Tests and Windowing

In the factory, the CS5012A/14/16 are tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sinewave is applied to the CS5012A/14/16, and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5012A/14/16.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

Figure 18 shows an FFT computed from an ideal 12-bit sinewave. The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used for testing the CS5014 and CS5016 has a maximum side-lobe level of -92 dB. Fig-

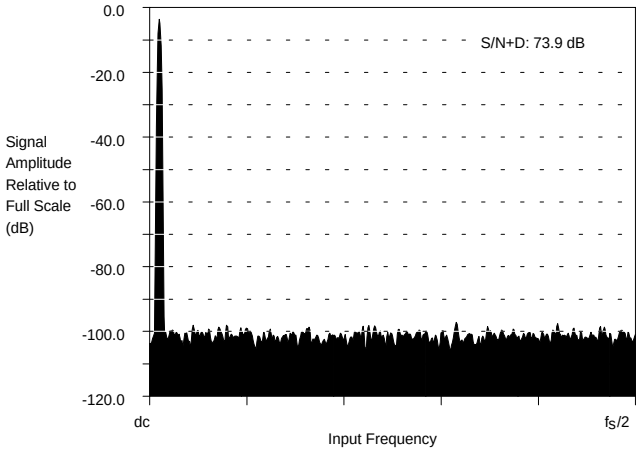


Figure 18. Plot of Ideal 12-bit ADC

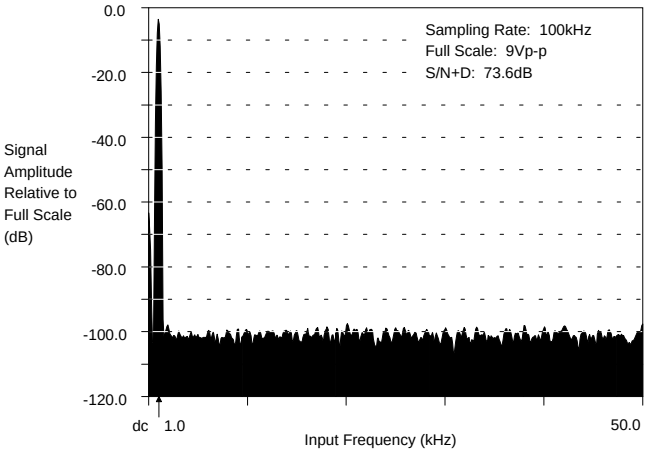


Figure 19. Plot of CS5012A with 1 kHz Full Scale Input

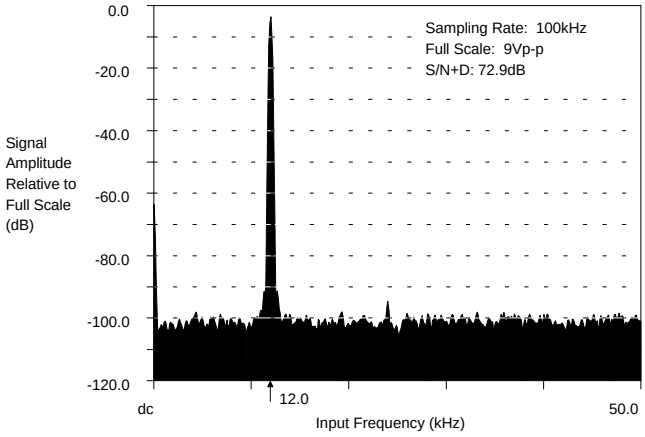


Figure 20. FFT Plot of CS5012A with 12 kHz Full-Scale Input

ures 21 and 23 show FFT plots computed from an ideal 14 and 16-bit sinewave multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten 1024 point time records. This filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics which exist above the noise floor and the -92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic

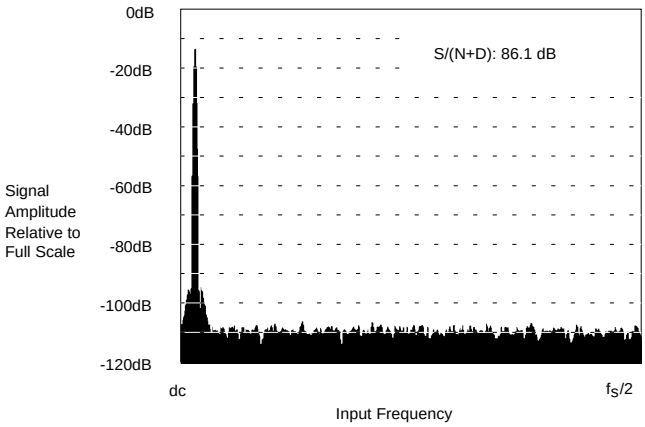


Figure 21. Plot of Ideal 14-bit ADC

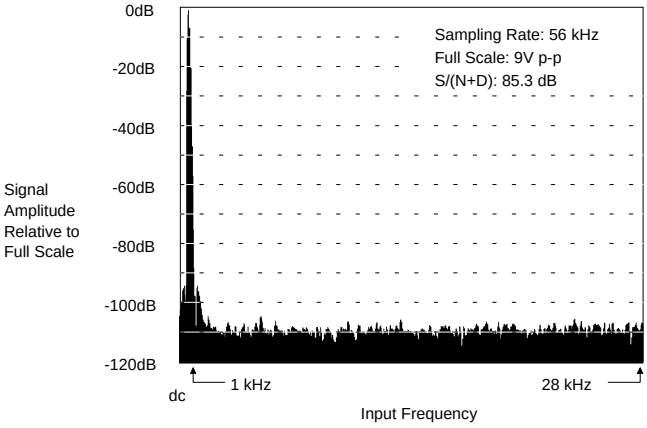


Figure 22. CS5014 FFT plot with 1 kHz Full Scale Input

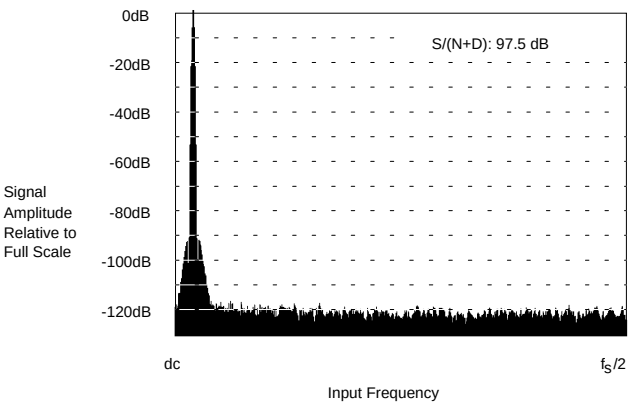


Figure 23. Plot of Ideal 16-bit ADC

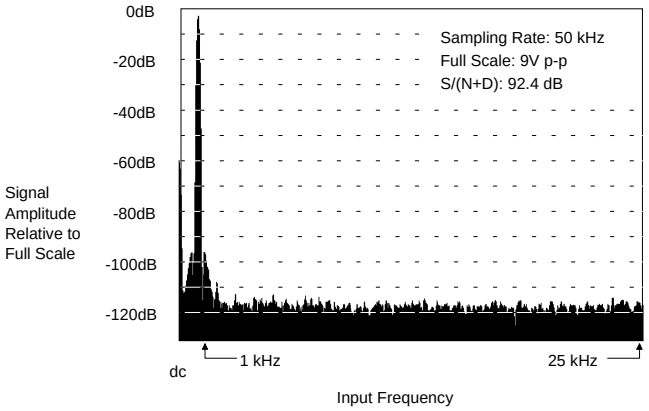


Figure 24. CS5016 FFT plot with 1 kHz Full Scale Input

analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83. This is available on request from Crystal Semiconductor.

Figures 19, 22, and 24 show the performance of the CS5012A/14/16 with 1kHz full scale inputs. Figure 20 shows CS5012A performance with 12kHz full scale inputs. Notice that the performance CS5012A/14/16 closely approaches that of the corresponding ideal ADC.

CS5012A High Frequency Performance

The CS5012A performs very well over a wide range of input frequencies as shown in Figure 25. The figure depicts the CS5012A-KP7 tested under four different conditions. The conditions include tests with the voltage reference set at 4.5 and at 2.5 volts with input signals at 0.5 dB down from full scale and 6.0 dB down from full scale. The sample rate is at 100 kHz for all cases. The plots indicate that the part performs very well even with input frequencies above the Nyquist rate. Best performance at the higher frequencies is achieved with a 2.5 volt reference.

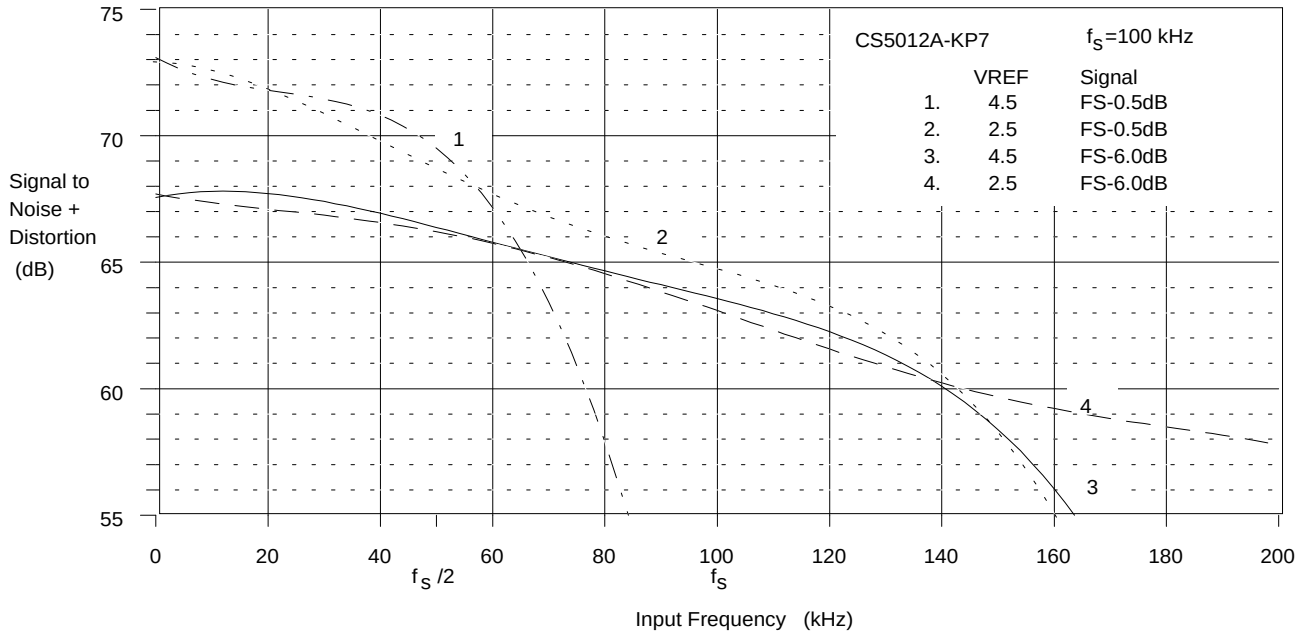


Figure 25. CS5012A High Frequency Input Performance

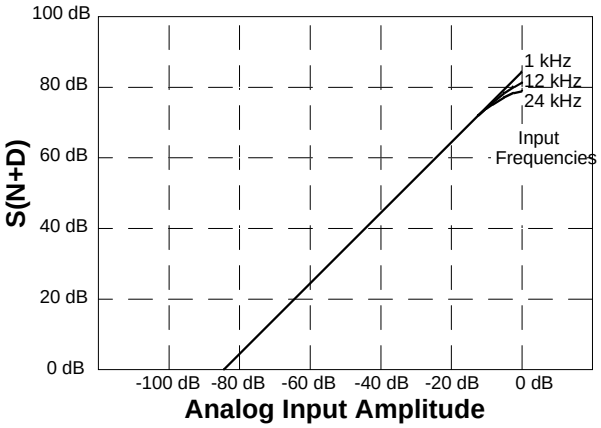


Figure 26. CS5014 S/(N+D) vs. Input Amplitude (9Vp-p Full-Scale Input)

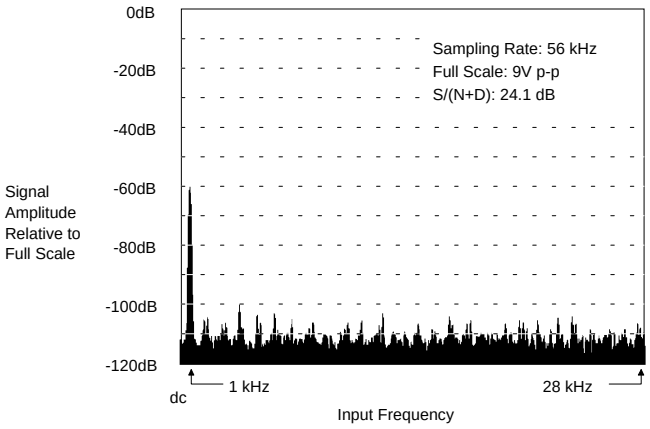


Figure 27. CS5014 FFT plot with 1 kHz -60 dB Input

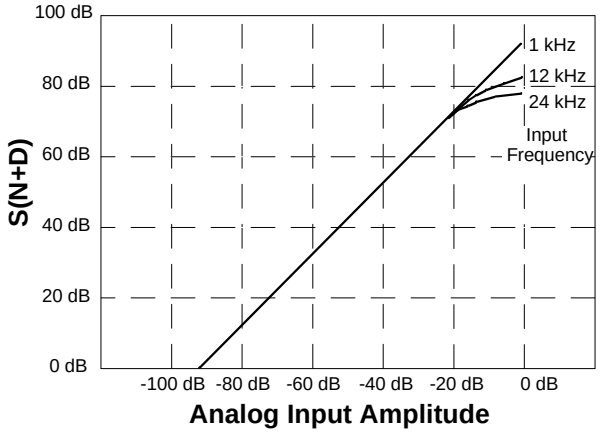


Figure 28. CS5016 S/(N+D) vs. Input Amplitude (9Vp-p Full-Scale Input)

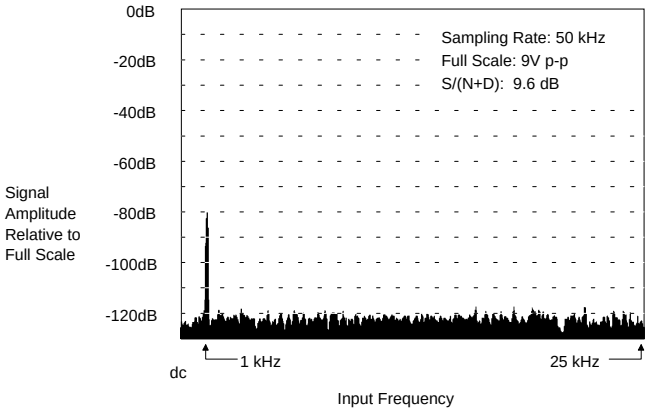


Figure 29. CS5016 FFT plot with 1 kHz -80 dB Input

Signal to Noise + Distortion vs Signal Level

As illustrated in Figures 26 - 29, the CS5014/16's on-chip self-calibration provides very accurate bit weights which yield no degradation in quantization noise with low-level input signals. In fact, quantization noise remains below the noise floor in the CS5016, which dictates the converter's signal-to-noise performance.

CS5016 Noise Considerations

All analog circuitry in the CS5016 is wideband in order to achieve fast conversions and high throughput. Wideband noise in the CS5016 integrates to 35 µV rms in unipolar mode (70 µV rms in bipolar mode). This is approximately 1/2 LSB rms with a 4.5V reference in both modes. Figure 30 shows a histogram plot of output code occurrences obtained from 5000 samples taken from a CS5016 in the bipolar mode. Hexadecimal code 80CD was arbitrarily selected and the analog input was set close to code center. With a noiseless converter, code 80CD would always appear. The histogram plot of the CS5016 has a "bell" shape with all codes other than 80CD due to internal noise.

In a sampled data system all information about the analog input applied to the sample/hold appears in the baseband from dc to one-half the sampling rate. This includes high-frequency components which alias into the baseband. Low-pass (anti-alias) filters

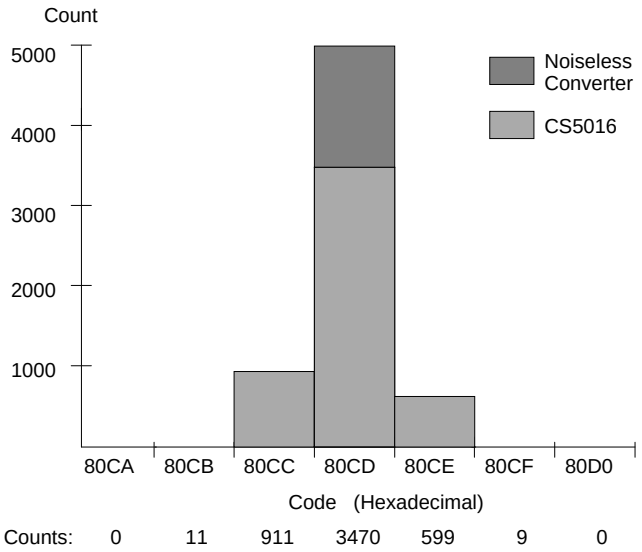


Figure 30. Histogram Plot of 5000 Conversion Inputs from the CS5016

are therefore used to remove frequency components in the input signal which are above one-half the sample rate. However, all wideband noise introduced by the CS5016 still aliases into the baseband. This "white" noise is evenly spread from dc to one-half the sampling rate and integrates to 35 μV rms in unipolar mode.

Noise can be reduced by sampling at higher than the desired word rate and averaging multiple samples for each word. Oversampling spreads the CS5016's noise over a wider band (for lower noise density), and averaging applies a low-pass response which filters noise above the desired signal bandwidth. In general, the CS5016's noise performance can be maximized in any application by always sampling at the maximum specified rate of 50 kHz (for lowest noise density) and digitally filtering to the desired signal bandwidth.

CS5014 and CS5016 Sampling Distortion

The ultimate limitation on the CS5014/16's linearity (and distortion) arises from nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the $\overline{\text{HOLD}}$ command is given. The charge on the array is ideally related to the analog input voltage by $Q_{in} = -V_{in} \times C_{tot}$ as shown in Figure 2. Any deviation from this ideal relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between charge Q_{in} and the analog input voltage V_{in} and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figures 22 and 24).

The ideal relationship between Q_{in} and V_{in} can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency as shown in Figures 26 and 28 since the magnitude of the steady state current increases. First noticeable at 1 kHz, this distortion assumes a linear relationship with input frequency. With signals 20 dB or more below full-scale, it no longer dominates the converter's overall S/(N+D) performance (Figures 31-34).

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to allow the array's charge current to decay, thereby eliminating any voltage drop across the switches. Since the CS5014/16 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter's $\overline{\text{HOLD}}$ input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

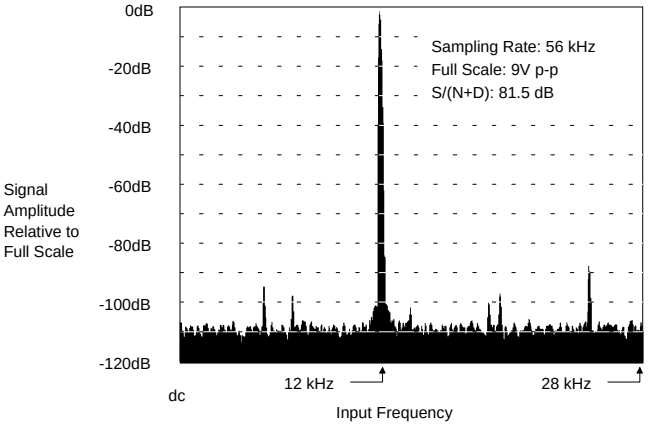


Figure 31. CS5014 FFT plot with 12 kHz Full Scale Input

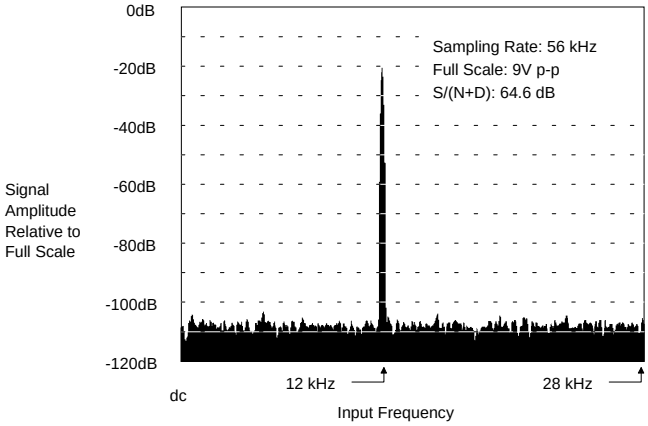


Figure 32. CS5014 FFT plot with 12 kHz -20 dB Input

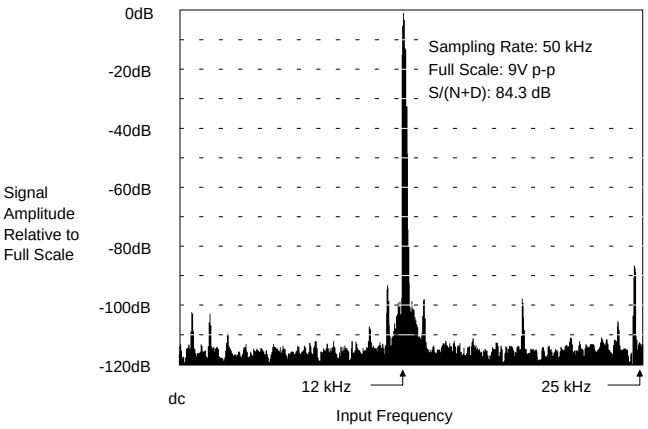


Figure 33. CS5016 FFT plot with 12 kHz Full Scale Input

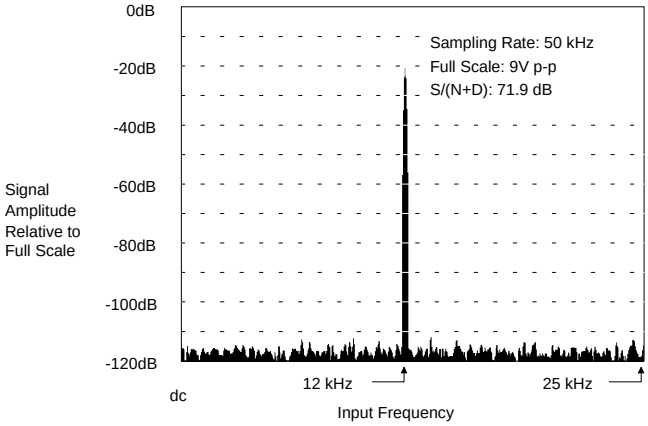


Figure 34. CS5016 FFT plot with 12 kHz -20 dB Input

Clock Feedthrough in the CS5014 and CS5016

Maintaining the integrity of analog signals in the presence of digital switching noise is a difficult problem. The CS5014/16 can be synchronized to the digital system using the CLKIN input to avoid conversion errors due to asynchronous interference. However, digital interference will still affect sampling purity due to coupling between the CS5014/16's analog input and master clock.

The effect of clock feedthrough depends on the sampling conditions. If the sampling signal at the $\overline{\text{HOLD}}$ input is synchronized to the master clock, clock feedthrough will appear as a dc offset at the CS5014/16's output. The offset could theoretically reach the peak coupling magnitude (Figure 35), but the probability of this occurring is small since the peaks are spikes of short duration.

Master Clock		Analog Input	Clock Feedthrough	
Int/Ext	Freq	Source Impedance	RMS	Peak-to-Peak
Internal	2MHz	50 Ω	15uV	70uV
External	2MHz	50 Ω	25uV	110uV
External	4MHz	50 Ω	40uV	150uV
External	4MHz	25 Ω	25uV	110uV
External	4MHz	200 Ω	80uV	325uV

Figure 35. Examples of Measured Clock Feedthrough

If sampling is performed asynchronously with the master clock, clock feedthrough will appear as an ac error at the CS5014/16's output. With a fixed

sampling rate, a tone will appear as the clock frequency aliases into the baseband. The tone frequency can be calculated using the equation below and could be selectively filtered in software using DSP techniques.

$$f_{tone} = (N\ f_s - f_{clk})$$

where $N = f_{clk}/f_s$ rounded to the nearest integer

The magnitude of clock feedthrough depends on the master clock conditions and the source impedance applied to the analog input. When operating with the CS5014/16's internally generated clock, the CLKIN input is grounded and the dominant source of coupling is through the device's substrate. As shown in Figure 35, a typical CS5014/16 operating with their internal oscillator at 2 MHz and 50 Ω of analog input source impedance will exhibit only 15 µV rms of clock feedthrough. However, if a 2 MHz external clock is applied to CLKIN under the same conditions, feedthrough increases to 25 µV rms. Feedthrough also increases with clock frequency; a 4 MHz clock yields 40 µV rms.

Clock feedthrough can be reduced by limiting the source impedance applied at the analog input. As shown in Figure 35, reducing source impedance from 50 Ω to 25 Ω yields a 15 µV rms reduction in feedthrough. Therefore, when operating the CS5014/16 with high-frequency external master clocks, it is important to minimize source impedance applied to the CS5014/16's input.

Also, the overall effect of clock feedthrough can be minimized by maximizing the input range and LSB size. The reference voltage applied to VREF can be maximized, and the CS5014/16 can be operated in bipolar mode which inherently doubles the LSB size over the unipolar mode.

Differences between the CS5012A and the CS5012

The differences between the CS5012A and the CS5012 are tabulated in Table 3. The CS5012 is a short-cycled version of the CS5016 A/D converter and includes the same 18-bit calibration circuitry. This calibration circuitry sets the calibration resolution of the CS5012 at 1/64th of an LSB and achieves the near perfect differential linearity performance illustrated by the CS5012 DNL plot in Figure 15. The CS5012A calibration circuitry was modified to provide calibration to 15-bit resolution therefore achieving calibration to 1/8 of an LSB. This reduction in calibration resolution for the CS5012A reduces the time required to calibrate the device (see Table 3) and reduces the size of the total array capacitance. The reduced array capacitance improves the high frequency performance by allowing higher slew rate in the input circuitry.

Table 3 documents some other improvements included in the CS5012A. The burst mode calibration was made functional, although it should not be used. The device was also modified so the $\overline{EOC}$ signal goes low at the end of a reset calibration in either microprocessor or microprocessor-independent mode. The CS5012A was modified to maintain a throughput rate of 64 CLKIN cycles in loopback mode for all frequencies of CLKIN.

	CS5012A	CS5012
Calibration resolution	15 bits. Results in DNL calibration to 1/8 LSB at 12 bits.	18 bits. Results in DNL calibration to 1/64 LSB at 12 bits.
Calibration time reset: interleave: burst:	 58,280 CLKIN cycles 2,014 conversions fully functional	 1,441,020 CLKIN cycles 72,051 conversions not functional
End of calibration indicator	$\overline{EOC}$ falls in either microprocessor or microprocessor-independent mode at the completion of a RESET calibration cycle.	$\overline{EOC}$ falls at the completion of a RESET calibration cycle in microprocessor mode only. In microprocessor-independent mode $\overline{EOT}$ must be used. $\overline{EOT}$ falls 15 CLKIN cycles after completion of a RESET calibration.
Throughput rate in loopback mode	The device acquires and converts a sample in 64 CLKIN cycles for all CLKIN frequencies when in loopback.	The device acquires and converts in 64 CLKIN cycles for CLKIN=4MHz, but will require 68 CLKIN cycles at 100kHz through-put. This is due to excess delay on $\overline{EOT}$.
Input capacitance in fine-charge mode	103pF typical, unipolar mode 72pF typical, bipolar mode	275pF typical, unipolar mode 165pF typical, bipolar mode
Slew Rate Unipolar Coarse charge Fine charge Bipolar Coarse charge Fine charge	 20V/us 1.5V/us 40V/us 3.0V/us	 5V/us 0.25V/us 10V/us 0.5V/us

Table 3. Differences Between the CS5012A and CS5012

$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

Table 4. CS5012A/14/16 Truth Table

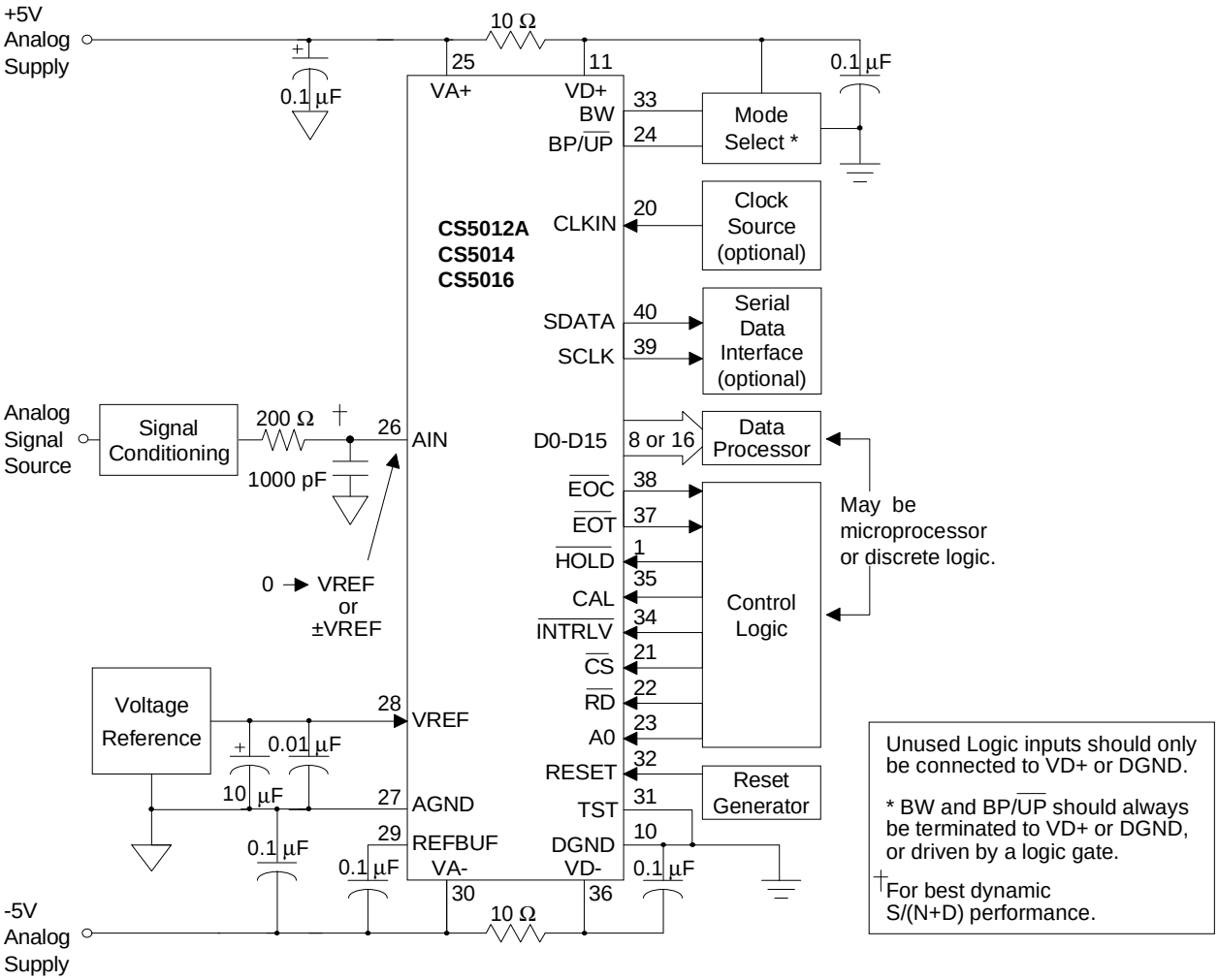
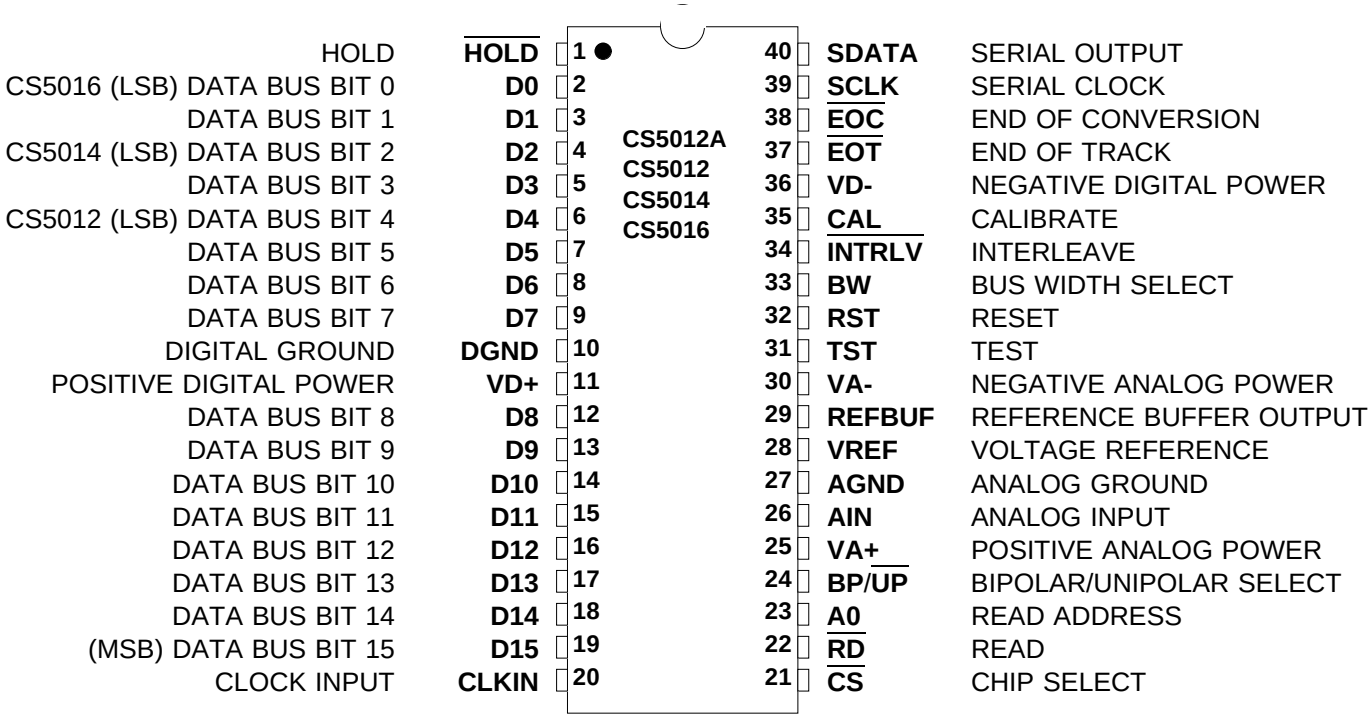
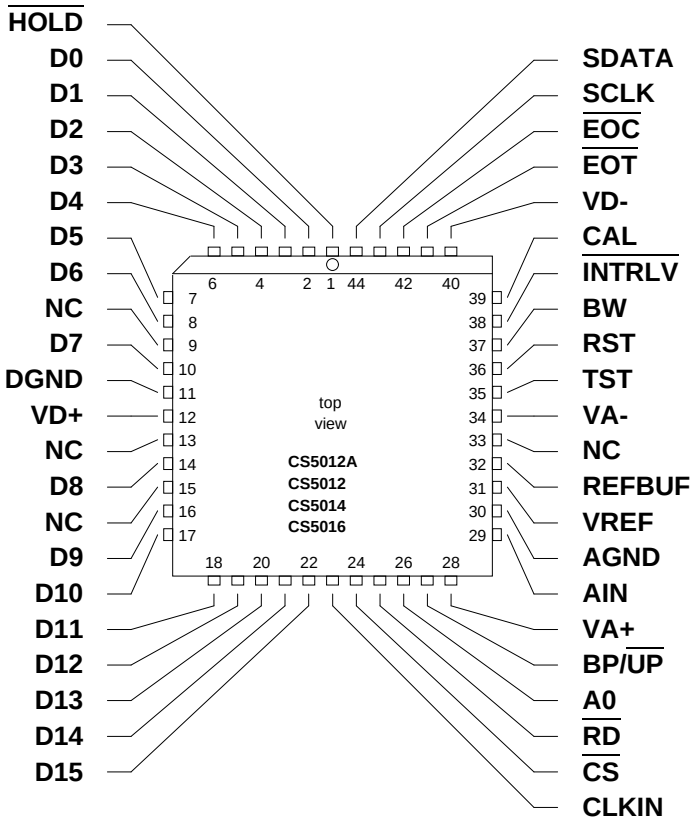


Figure 36. CS5012A/14/16 System Connection Diagram





NOTE: All pin references in this data sheet refer to the 40-pin DIP package numbering. Use this figure to determine pin numbers for 44-pin package.

PIN DESCRIPTIONS

Power Supply Connections

VD+ – Positive Digital Power, PIN 11.
Positive digital power supply. Nominally +5 volts.

VD- – Negative Digital Power, PIN 36.
Negative digital power supply. Nominally -5 volts.

DGND – Digital Ground, PIN 10.
Digital ground.

VA+ – Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- – Negative Analog Power, PIN 30.
Negative analog power supply. Nominally -5 volts.

AGND – Analog Ground, PIN 27.
Analog ground.

Oscillator

CLKIN – Clock Input, PIN 20.
All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

Digital Inputs

$\overline{\text{HOLD}}$ – Hold, PIN 1.
A falling transition on this pin sets the CS5012A/14/16 to the hold state and initiates a conversion. This input must remain low at least one CLKIN cycle plus 50 ns.

$\overline{\text{CS}}$ – Chip Select, PIN 21.
When high, the data bus outputs are held in a high impedance state and the input to CAL and $\overline{\text{INTRLV}}$ are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and $\overline{\text{INTRLV}}$) and a rising transition latches both the CAL and $\overline{\text{INTRLV}}$ inputs. If $\overline{\text{RD}}$ is low, the data bus is driven as indicated by BW and A0.

$\overline{\text{RD}}$ – Read, PIN 22.
When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

A0 – Read Address, PIN 23.

Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

BP/$\overline{\text{UP}}$ – Bipolar/Unipolar Input Select, PIN 24.

When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF. Unipolar encoding is in straight binary format. Once calibration has been performed, either bipolar or unipolar mode may be selected without the need to recalibrate.

RST – Reset, PIN 32.

When taken high for at least 100 ns, all internal digital logic is reset. Upon being taken low, a full calibration sequence is initiated.

BW – Bus Width Select, PIN 33.

When hard-wired high, all 12 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D0-D7. A second read cycle places the four LSB's with four trailing zeros on D0-D7. Subsequent reads will toggle the higher/lower order byte. Regardless of BW's status, a read cycle with A0 low yields the status information on D0-D7.

$\overline{\text{INTRLV}}$ – Interleave, PIN 34.

When latched low using $\overline{\text{CS}}$, the device goes into interleave calibration mode. A full calibration will complete every 2,014 conversions in the CS5012A, and every 72,051 conversions in the CS5014/16. The effective conversion time extends by 20 clock cycles.

CAL – Calibrate, PIN 35. (See Addendum appending this data sheet))

When latched high using $\overline{\text{CS}}$, burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 58,280 CLKIN cycles in the CS5012A, and every 1,441,020 CLKIN cycles in the CS5014/16 . If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning.

Analog Inputs

AIN – Analog Input, PIN 26.

Input range in the unipolar mode is zero volts to VREF. Input range in bipolar mode is -VREF to +VREF. The output impedance of buffer driving this input should be less than or equal to 200 Ω.

VREF – Voltage Reference, PIN 28.

The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode.

Digital Outputs

D0 through D15 – Data Bus Outputs, PINS 2 thru 9, 12 thru 19.

3-state output pins. Enabled by $\overline{CS}$ and $\overline{RD}$, they offer the converter's output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer status register data.

$\overline{EOT}$ – End Of Track, PIN 37.

If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal.

$\overline{EOC}$ – End Of Conversion, PIN 38.

This output indicates the end of a conversion or calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

SDATA – Serial Output, PIN 40.

Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

SCLK – Serial Clock Output, PIN 39.

Used to clock converted output data serially from the CS5012A/14/16. Serial data is stable on the rising edge of SCLK.

Analog Outputs

REFBUF – Reference Buffer Output, PIN 29.

Reference buffer output. A 0.1 µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

TST – Test, PIN 31.

Allows access to the CS5012A/14/16's test functions which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Linearity Error

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in % Full-Scale.

Differential Linearity

Minimum resolution for which no missing codes is guaranteed. Units in bits.

Full Scale Error

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSB's.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Negative Full-Scale Error

The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise)

The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion

The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-Noise Ratio

The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Aperture Time

The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

NOTE: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

CS5012A Ordering Guide

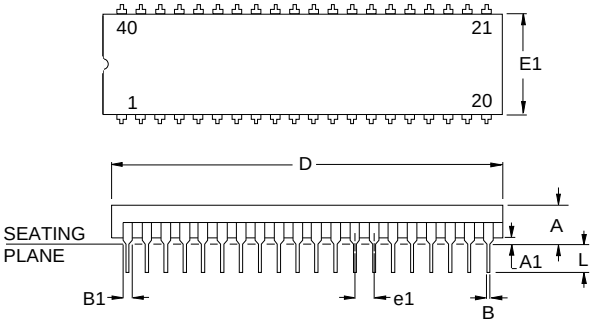
Model	Throughput	Conversion Time	Maximum DNL	Temp. Range	Package
CS5012A-BP7	100 kHz	7.20 µs	±1/2 LSB	-40 to +85 °C	40-Pin Plastic DIP
CS5012A-BL7	100 kHz	7.20 µs	±1/2 LSB	-40 to +85 °C	44-Pin PLCC

CS5016 Ordering Guide

Model	Linearity	Signal to Noise Ratio	Conversion Time	Temp. Range	Package
CS5016-JP32	.0030%	87 dB	32.50 µs	0 to 70 °C	40-Pin Plastic DIP
CS5016-JP16	.0030%	87 dB	16.25 µs	0 to 70 °C	40-Pin Plastic DIP
CS5016-KP32	.0015%	90 dB	32.50 µs	0 to 70 °C	40-Pin Plastic DIP
CS5016-KP16	.0015%	90 dB	16.25 µs	0 to 70 °C	40-Pin Plastic DIP
CS5016-JL32	.0030%	87 dB	32.50 µs	0 to 70 °C	44-Pin PLCC
CS5016-JL16	.0030%	87 dB	16.25 µs	0 to 70 °C	44-Pin PLCC
CS5016-KL32	.0015%	90 dB	32.50 µs	0 to 70 °C	44-Pin PLCC
CS5016-KL16	.0015%	90 dB	16.25 µs	0 to 70 °C	44-Pin PLCC
CS5016-AP32	.0030%	87 dB	32.50 µs	-40 to +85 °C	40-Pin Plastic DIP
CS5016-AP16	.0030%	87 dB	16.25 µs	-40 to +85 °C	40-Pin Plastic DIP
CS5016-BP32	.0015%	90 dB	32.50 µs	-40 to +85 °C	40-Pin Plastic DIP
CS5016-BP16	.0015%	90 dB	16.25 µs	-40 to +85 °C	40-Pin Plastic DIP
CS5016-AL32	.0030%	87 dB	32.50 µs	-40 to +85 °C	44-Pin PLCC
CS5016-AL16	.0030%	87 dB	16.25 µs	-40 to +85 °C	44-Pin PLCC
CS5016-BL32	.0015%	90 dB	32.50 µs	-40 to +85 °C	44-Pin PLCC
CS5016-BL16	.0015%	90 dB	16.25 µs	-40 to +85 °C	44-Pin PLCC
CS5016-SD16	.0076%	87 dB	16.25 µs	-55 to +125 °C	40-Pin CerDIP
CS5016-TD16	.0015%	90 dB	16.25 µs	-55 to +125 °C	40-Pin CerDIP
CS5016-SE16	.0076%	87 dB	16.25 µs	-55 to +125 °C	44-Pin Ceramic LCC
CS5016-TE16	.0015%	90 dB	16.25 µs	-55 to +125 °C	44-Pin Ceramic LCC
5962-8967601QA	.0076%	87 dB	16.25 µs	-55 to +125 °C	40-Pin CerDIP
5962-8967602QA	.0015%	90 dB	16.25 µs	-55 to +125 °C	40-Pin CerDIP
5962-8967601XA	.0076%	87 dB	16.25 µs	-55 to +125 °C	44-Pin Ceramic LCC
5962-8967602XA	.0015%	90 dB	16.25 µs	-55 to +125 °C	44-Pin Ceramic LCC

The following is a list of upgraded part numbers.

Discontinued Part Number	Equivalent Recommended Device
CS5016-SD16B	5962-8967601QA
CS5016-TD16B	5962-8967602QA
CS5016-SE16B	5962-8967601XA
CS5016-TE16B	5962-8967602XA

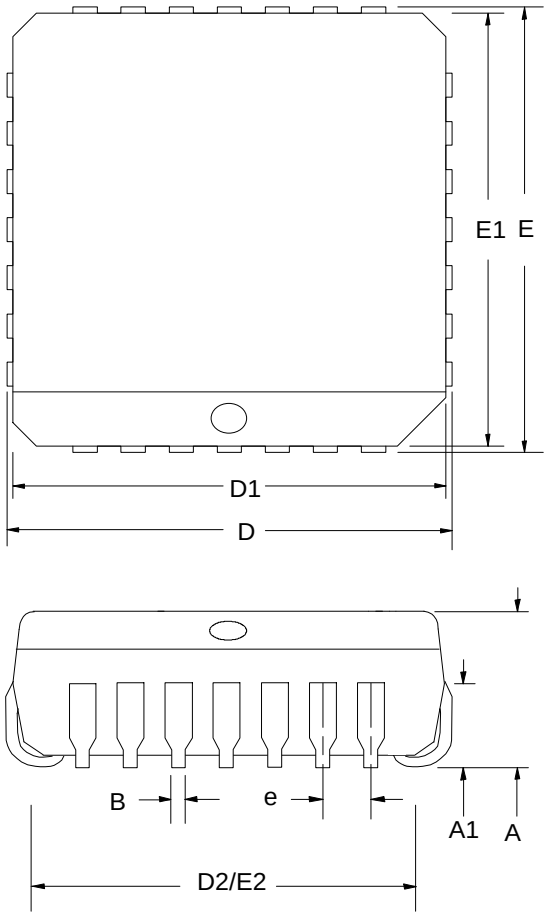


40 pin
Plastic DIP

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	3.94	4.32	5.08	0.155	0.170	0.200
A1	0.51	0.76	1.02	0.020	0.030	0.040
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.02	1.27	1.65	0.040	0.050	0.065
C	0.20	0.25	0.38	0.008	0.010	0.015
D	51.69	52.20	52.71	2.035	2.055	2.075
E1	13.72	13.97	14.22	0.540	0.550	0.560
e1	2.41	2.54	2.67	0.095	0.100	0.105
eA	15.24	-	15.87	0.600	-	0.625
L	3.18	-	3.81	0.125	-	0.150
∝	0°	-	15°	0°	-	15°

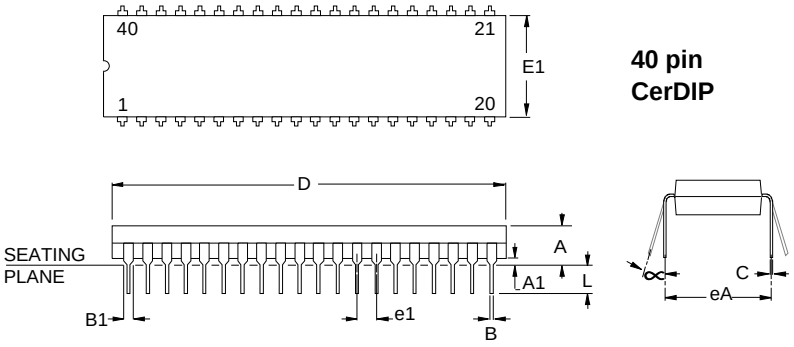
NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION eA TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION E1 DOES NOT INCLUDE MOLD FLASH.



44 pin
PLCC

DIM	NO. OF TERMINALS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.20	4.45	4.57	0.165	0.175	0.180
A1	2.29	2.79	3.04	0.090	0.110	0.120
B	0.33	0.41	0.53	0.013	0.016	0.021
D/E	17.40	17.53	17.65	0.685	0.690	0.695
D1/E1	16.51	16.59	16.66	0.650	0.653	0.656
D2/E2	14.99	15.50	16.00	0.590	0.610	0.630
e	1.19	1.27	1.35	0.047	0.050	0.053

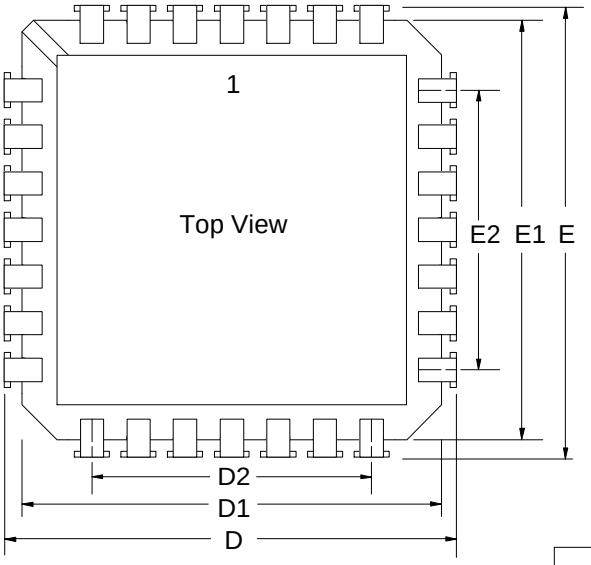


40 pin
CerDIP

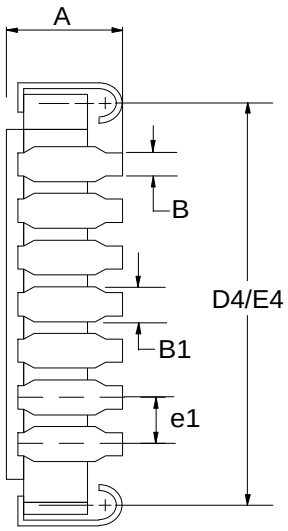
	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	4.06	—	5.84	0.160	—	0.230
A1	0.51	—	1.27	0.020	—	0.050
B	0.38	0.46	0.56	0.015	0.018	0.022
B1	1.27	—	1.65	0.050	—	0.065
C	0.20	0.25	0.30	0.008	0.010	0.012
D	50.29	52.32	52.57	1.980	2.060	2.070
E1	12.70	14.73	15.37	0.500	0.580	0.605
e1	2.41	2.54	2.67	0.095	0.100	0.105
eA	15.11	15.24	15.37	0.595	0.600	0.605
L	2.92	3.81	4.06	0.115	0.150	0.160
∝	5°	—	15°	5°	—	15°

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13mm (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION eA TO CENTER OF LEADS WHEN FORMED PARALLEL.



28/44 pin CLCC



DIM	NO. OF TERMINALS											
	28						44					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
A	2.54	3.05	3.43	0.100	0.120	0.135	2.54	3.05	3.43	0.100	0.120	0.135
B	0.33	0.46	0.58	0.013	0.018	0.023	0.33	0.46	0.58	0.013	0.018	0.023
B1	0.51	0.64	0.81	0.02	0.025	0.032	0.51	0.64	0.81	0.02	0.025	0.032
D/E	12.19	12.46	12.70	0.480	0.490	0.500	17.27	17.53	17.78	0.680	0.690	0.700
D1/E1	11.18	11.43	11.68	0.440	0.450	0.460	16.26	16.51	16.76	0.640	0.650	0.660
D2/E2	7.49	7.62	7.75	0.295	0.300	0.305	12.57	12.70	12.83	0.495	0.500	0.505
D4/E4	10.80	10.92	11.05	0.425	0.430	0.435	15.88	16.00	16.13	0.625	0.630	0.635
e1	1.14	1.27	1.40	0.045	0.050	0.055	1.14	1.27	1.40	0.045	0.050	0.055