Clock Synchronizer and Multiplier

Features

- On-chip PLL for clock synchronization
- On-chip loop filter for clock generation
- Recovery of poor duty cycle clocks
- Synchronizes output frequencies up to 100 MHz
- Low skew (±1 ns, maximum) between input and output clocks
- 20 MHz to 100 MHz output clock range (Versions A and C)
- 5 MHz to 25 MHz output clock range (Versions B and D)
- Drop-in replacement for AV9170
- CMOS technology in 8-pin PDIP (300 mil) and SOIC (150 mil)
- 5V power supply

Description

CH9070 is a PLL clock generator designed to generate clocks for high speed systems with very low skew (±1 ns, maximum). CH9070 synchronizes the output clock to the input clock signal with zero delay, and is able to generate multiples or divisions of the input clock with the same accuracy, using the frequency select pins, FS[1:0].

CH9070 is also useful in recovering poor duty cycle clocks. For example, a 50 MHz clock with a 20/80% duty cycle can be regenerated with an improved 48/52% duty cycle.

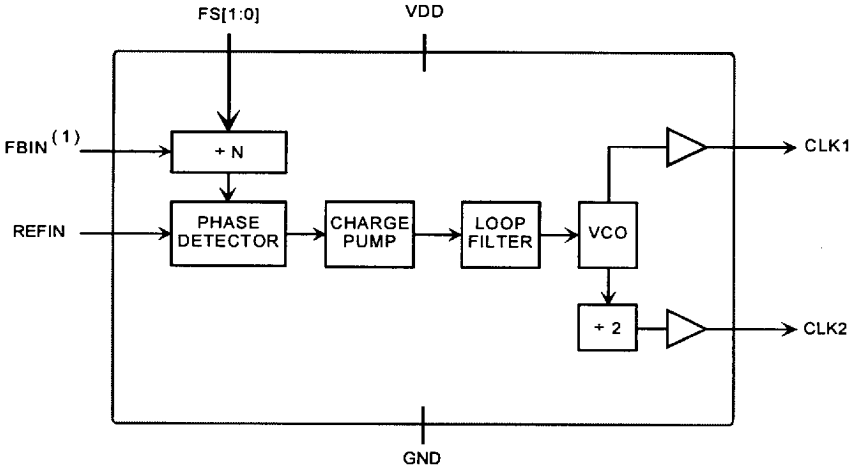

Figure 1: Block Diagram

(1) FBIN is externally connected to either CLK1 or CLK2, not both

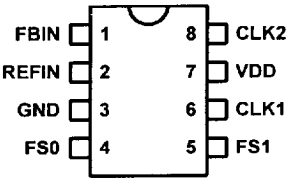

Figure 2: CH9070

Table 1 • Pin Description

Pin	Type	Symbol	Description
1	In	FBIN	Feedback input
2	In	REFIN	Reference clock input
3	Power	GND	Ground
4,5	In	FS0, FS1	Frequency select inputs
6	Out	CLK1	Clock1 output
7	Power	VDD	5V supply
8	Out	CLK2	Clock2 output

Note: The frequency of CLK1 is always twice the frequency of CLK2

Table 2 • Frequencies for CH9070 (FBIN with respect to REFIN)

Frequency Select Inputs		f_{FBIN}			
FS1	FS0	Version A	Version B	Version C	Version D
0	0	2 x fREFIN	2 x fREFIN	3 x fREFIN	3 x fREFIN
0	1	4 x fREFIN	4 x fREFIN	5 x fREFIN	5 x fREFIN
1	0	1 x fREFIN	1 x fREFIN	6 x fREFIN	6 x fREFIN
1	1	8 x fREFIN	8 x fREFIN	10 x fREFIN	10 x fREFIN

Note: FBIN and REFIN are synchronized through the rising edges. Falling edges are not lined up.

Table 3 • CLK1 Output Frequency Ranges

CH9070	f_{CLK1}
Version A	20 MHz – 100 MHz
Version B	5 MHz – 25 MHz
Version C	20 MHz – 100 MHz
Version D	5 MHz – 25 MHz

By connecting CLK1 to FBIN a feedback loop is formed, as shown in **Figure 3**. This connection aligns CLK1 to the input reference clock, REFIN, on the rising edges. Either the rising or falling edges of CLK2 are aligned to REFIN's rising edges.

Table 4 • Frequencies with CLK1 Feedback for CH9070A and B

FS1	FS0	CLK1	CLK2
0	0	2 x fREFIN	fREFIN
0	1	4 x fREFIN	2 x fREFIN
1	0	fREFIN	fREFIN ÷ 2
1	1	8 x fREFIN	4 x fREFIN

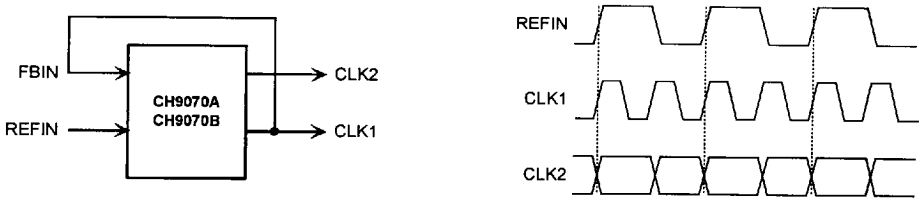

Figure 3: Timing Diagrams with CLK1 Feedback for CH9070A and B

By connecting CLK2 to FBIN a feedback loop is formed, as shown in **Figure 4**. This connection aligns the rising edges of the input and output clock signals.

Table 5 • Frequencies with CLK2 Feedback for CH9070A and B

FS1	FS0	CLK1	CLK2
0	0	4 x fREFIN	2 x fREFIN
0	1	8 x fREFIN	4 x fREFIN
1	0	2 x fREFIN	fREFIN
1	1	16 x fREFIN	8 x fREFIN

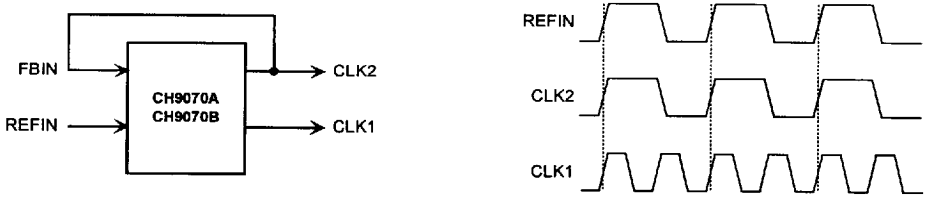

Figure 4: Timing Diagrams with CLK2 Feedback for CH9070A and B

By connecting CLK1 to FBIN a feedback loop is formed, as shown in **Figure 5** . This connection aligns CLK1 to the input reference clock, REFIN, on the rising edges. Either the rising or falling edges of CLK2 are aligned to REFIN's rising edges.

Table 6 • Frequencies with CLK1 Feedback for CH9070C and D

FS1	FS0	CLK1	CLK2
0	0	3 x fREFIN	1.5 x fREFIN
0	1	5 x fREFIN	2.5 x fREFIN
1	0	6 x fREFIN	3 x fREFIN
1	1	10 x fREFIN	5 x fREFIN

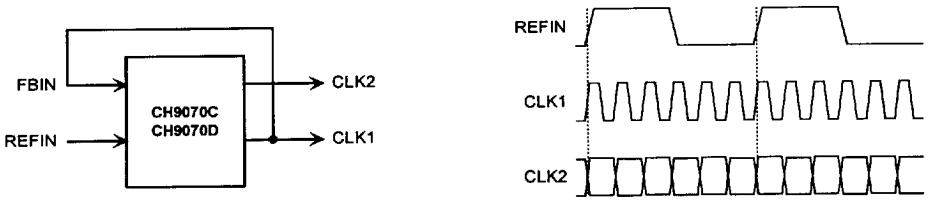

Figure 5: Timing Diagrams with CLK1 Feedback for CH9070C and D

By connecting CLK2 to FBIN a feedback loop is formed, as shown in **Figure 6**. This connection aligns the rising edges of the input and output clock signals.

Table 7 • Frequencies with CLK2 Feedback for CH9070C and D

FS1	FS0	CLK1	CLK2
0	0	6 x fREFIN	3 x fREFIN
0	1	10 x fREFIN	5 x fREFIN
1	0	12 x fREFIN	6 x fREFIN
1	1	20 x fREFIN	10 x fREFIN

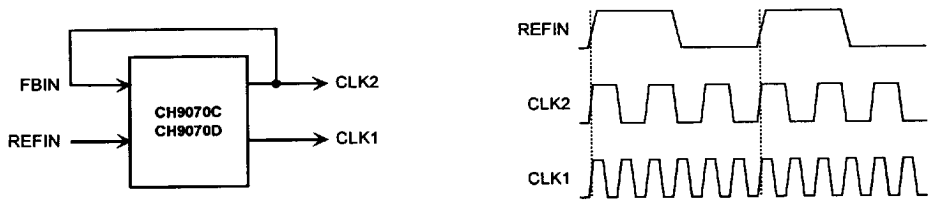

Figure 6: Timing Diagrams with CLK2 Feedback for CH9070C and D

Table 8 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
V_{DD}	Power supply voltage with respect to GND	–0.5 to +7.0	V
V_{IN}	Input voltage on any pin with respect to GND	–0.5 to V_{DD}+0.5	V
T_{STOR}	Storage temperature	–55 to +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 9 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
V_{OH}	Output high voltage	I_{OH} = –1mA, V_{DD} = 5V	V_{DD} – 0.4			V
V_{OH}	Output high voltage	I_{OH} = –4mA, V_{DD} = 5V	V_{DD} – 0.8			µA
V_{OH}	Output high voltage	I_{OH} = –8mA	2.4			V
V_{OL}	Output low voltage	I_{OL} = 8mA			0.4	V
V_{IH}	Input high voltage	V_{DD} = 5V	2.0			V
V_{IL}	Input low voltage	V_{DD} = 5V			0.8	V
I_{IL}	Input low current	V_{IN} = 0V	–5		5	µA
I_{IH}	Input high current	V_{IN} = V_{DD}	–5		5	µA
C_I	Input capacitance				10	pF
I_{DD}	Operating current	V_{DD} = 5V, No load, 100 MHz		20		mA

Table 10 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
T_{IR}	Input clock rise time				10	ns
T_{IF}	Input clock fall time				10	ns
T_R	Output rise time, 0.8V – 2.0V	15 pF load		1	2	ns
T_R	Rise time, 20% – 80% V_{DD}	15 pF load		2	4	ns
T_F	Output fall time, 2.0V – 0.8V	15 pF load		1	2	ns
T_F	Rise time, 80% – 20% V_{DD}	15 pF load		2	4	ns
T_{DC}	Output duty cycle, CH9070A, C	15 pF load. **Note 2**	40	48 / 52	60	%
T_{DC}	Output duty cycle, CH9070B, D	15 pF load. **Note 2**	45	49 / 51	55	%
T_{1S}	Jitter, 1 sigma		–500	±120	300	ps
T_{ABS}	Jitter, absolute	For CLK1 > 10 MHz	–2%	±250	500	ps
T_{ABS}	Jitter, absolute	For CLK1 < 10 MHz			2	%
F_{REFIN}	Input frequency	**Note 1**	1		100	MHz
F_{CLK1}	Output frequency CLK1	CH9070A, CH9070C	20		100	MHz
F_{CLK1}	Output frequency CLK1	CH9070B, CH9070D	5		25	MHz
T_{SKEW1}	FBIN to REFIN skew	Input rise time <5ns. **Note 3**	–1	0.4	1	ns
T_{SKEW1}	FBIN to REFIN skew	Input rise time <10ns. **Note 3**	–2	0.6	2	ns
T_{SKEW2}	CLK1 to CLK2 skew	**Note 3**	–1	0.4	1	ns

Notes:
1. It may be possible to operate CH9070 outside these ranges. Consult Chrontel for details.
2. Duty cycle measured at 1.5V.
3. Skew measured at 1.5V on rising edges.

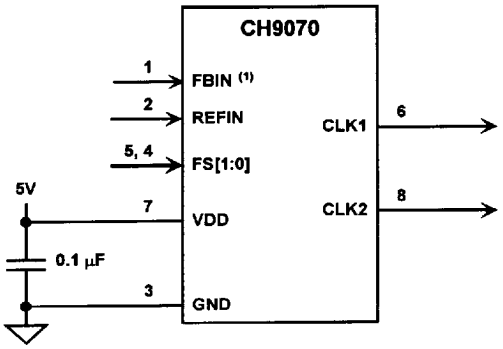

Figure 7: Application Schematic

(1) FBIN is externally connected to either CLK1 or CLK2, not both

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9070x-N	300 mil PDIP	8	5V
CH9070x-S	150 mil SOIC	8	5V
Note: x = frequency table version			