28F016SA/DD28F032SA
ERRATA INFORMATION

The following errata information sheet affects all samples and production of the Intel 28F016SA and DD28F032SA FlashFile™ Memory devices manufactured between October 27, 1993 through the end of the first quarter of 1994*. This errata supersedes the first one published in October 1993.

The list of features affected by the errata is divided into three sections:

1.0 Errata on Operational Specifications

2.0 Errata on Device Features

3.0 Errata on Documentation

1.0 ERRATA ON OPERATIONAL SPECIFICATIONS

1.1 Standby and Deep Power-Down Currents (same information as on the first errata, with order number 297408-001):

The V_{CC} Standby current (I_{CCS}) and Deep Power-Down current (I_{CCD}) exceed the maximum specification values published in the 28F016SA Data Sheet.

The maximum specifications for I_{CCS} and I_{CCD} are changed to the following values for the above described material :

V_{CC}=3.3V± 0.3V

	I_{CCS} Max		I_{CCD} Max	
Inputs	**Spec**	**New**	**Spec**	**New**
CMOS	100 µA	500 µA	5 µA	200 µA
TTL	4 mA	4 mA	5 µA	200 µA

V_{CC}=5.0V± 0.5V

	I_{CCS} Max		I_{CCD} Max	
Inputs	**Spec**	**New**	**Spec**	**New**
CMOS	100 µA	1 mA	5 µA	500 µA
TTL	4 mA	4 mA	5 µA	500 µA

*Call Intel Sales Office for exact details.

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Please note that the Reset functionality of RP# pin is preserved and customers should still be using this pin to do the following:

- Write Protection during system power transitions
- Device Reset to read array mode upon exit from deep power-down mode
- Termination of Write State Machine operations upon entry into deep power-down mode

1.2 Device Performance at V_{CC}=3.3V:

The 28F016SA access times at V_{CC}=3.3V have been characterized and the following speeds are available for the above described material:

- 120 ns @ V_{CC} = 3.3V ± 0.3V with Output Loading Capacitance of 50 pF
  This speed offering is exactly as specified in the 28F016SA Data Sheet.

- 150 ns @ V_{CC} = 3.3V ± 0.15V with Output Loading Capacitance of 50 pF
  Note that the 150 ns access time is only guaranteed with ±0.15V V_{CC} tolerance.

2.0 ERRATA ON DEVICE FEATURES

2.1 Erase Interruptability:

The following 28F016SA/DD28F032SA features are affected by this errata:

- Write During Erase: Queueing a Write command when an Erase command is in progress
- Queueing Multiple Block Erase Commands

Both of these features are not fully functional on the above described material and will be fixed in a coming stepping.

Write During Erase:
When issued a Write command during the execution of an Erase operation, the Write command will queue, but will not interrupt the Erase operation. Upon completion of the Erase operation, the state machine will commence the Write Operation.

Queueing Multiple Block Erase Commands:
Up to three Single Block Erase commands can be queued. In the future stepping of the device, the Single Block Erase queue will extend up to the total number of erase blocks (32). If more than three Single Block Erase commands are desired, the Erase All Unlocked Blocks command should be used. Queueing can still be used with all other queueable commands as described in Chapter 11, Section 11.1, of the 28F016SA 16-Mbit FlashFile™ Memory User's Manual.

Note that the Erase Suspend command to go read other memory blocks works as documented.

2.2 Standby Current Mode when Reading the Page Buffer:

When de-selecting the 28F016SA, there is one condition under which the device power consumption will not decrease to the Standby current level. This condition occurs when the last operation before putting the chip in standby mode is reading the page buffer. In this case, the device still consumes active power. It is therefore recommended to default back to either read array or read status register modes before putting the 28F016SA in standby mode.

3.0 ERRATA ON DOCUMENTATION

This category of errata information represents permanent changes to the device specifications and to the appropriate documentation which will be updated in the future.

3.1 Global Status Register Bits 0 and 1 (refer to 28F016SA User's Manual, Chapter 5, Table 5-2, Global Status Register):

GSR.0: Page Buffer Select Status bit
GSR.1: Page Buffer Status bit

To update the status of these bits the software needs to issue an additional Extended Status Register read command (71H) if the GSR has been updated just prior to reading the status of GSR.0 and GSR.1.

3.2 Device Current Consumption during Sleep Mode:

When the software issues a Sleep command to the 28F016SA, the system expects the device power consumption to reach the Deep Power-Down current level. To insure that the 28F016SA's power consumption reaches the Deep Power-Down current level, the system also needs to de-select the chip by taking either or both CE_0# or CE_1# high. If the chip is not de-selected after the Sleep is issued, the power consumption stays at the Active current level of the last operation prior to executing the Sleep command.

3.3 BYTE# Level during Deep Power-Down Mode:

The BYTE# pin voltage level during the deep power-down mode of operation must be at a CMOS input level in order to meet the current specification for I_{CCD}. Therefore, either BYTE# = V_{CC} ± 0.2V or GND ± 0.2V are acceptable.

3.4 t_{AVEL} Timing Parameter (refer to 28F016SA Data Sheet, Section 5.6):

t_{AVEL} = 0 ns is the new specification. Note 4 is therefore no longer valid.

ADDITIONAL INFORMATION

28F016SA Data Sheet, order number 290489
28F016SA 16-Mbit FlashFile™ Memory User's Manual, order number 297372
DD28F032SA 32-Mbit (2 Mbit x 16, 4 Mbit x 8) FlashFile™ Memory Data Sheet, order number 290490