

# UT54ACS245/UT54ACTS245

## Radiation-Hardened

## Octal Bus Transceivers with Three-State Outputs

### FEATURES

- Three-state outputs drive bus line directly
- 1.2 $\mu$  radiation-hardened CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 20-pin DIP
  - 20-lead flatpack

### DESCRIPTION

The UT54ACS245 and the UT54ACTS245 are non-inverting octal bus transceivers designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ( $\bar{G}$ ) disables the device so that the buses are effectively isolated.

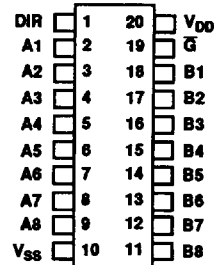
The devices are characterized over full military temperature range of -55°C to +125°C.

### FUNCTION TABLE

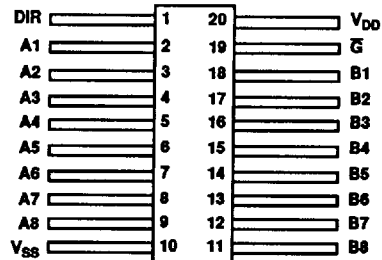
| ENABLE<br>$\bar{G}$ | DIRECTION<br>CONTROL DIR | OPERATION       |
|---------------------|--------------------------|-----------------|
| L                   | L                        | B Data To A Bus |
| L                   | H                        | A Data To B Bus |
| H                   | X                        | Isolation       |

### PINOUTS

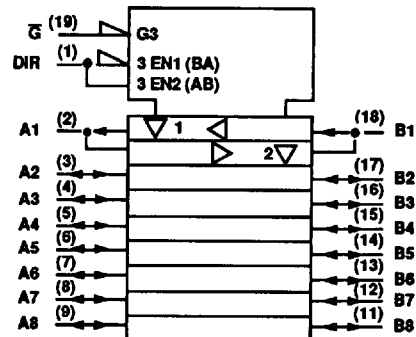
20-Pin DIP  
Top View



20-Lead Flatpack  
Top View



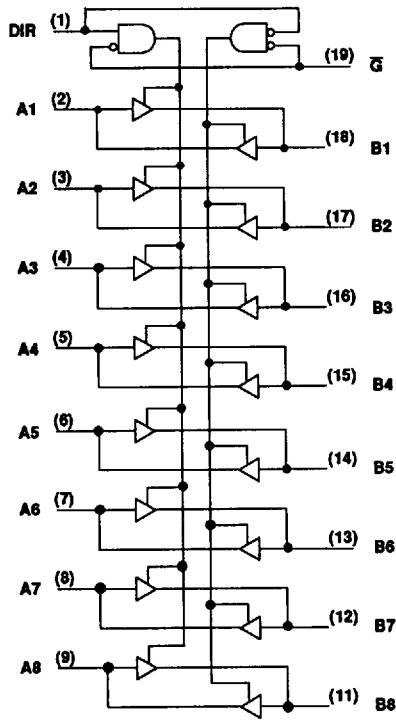
### LOGIC SYMBOL



Note:

1. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



**RADIATION HARDNESS SPECIFICATIONS <sup>1</sup>**

| PARAMETER                        | LIMIT  | UNITS                   |
|----------------------------------|--------|-------------------------|
| Total Dose                       | 1.0E6  | rads(Si)                |
| SEU & SEL Threshold <sup>2</sup> | 80     | MeV-cm <sup>2</sup> /mg |
| Neutron Fluence                  | 1.0E14 | n/cm <sup>2</sup>       |

**Notes:**

- 1. Logic will not latchup during radiation exposure within the limits defined in the table.
- 2. Device storage elements are immune to SEU effects.

**ABSOLUTE MAXIMUM RATINGS**

| SYMBOL           | PARAMETER                              | LIMIT                    | UNITS |
|------------------|--|--------------------------|-------|
| V <sub>DD</sub>  | Supply voltage                         | -0.3 to 7.0              | V     |
| V <sub>I/O</sub> | Voltage any pin                        | -3 to V <sub>DD</sub> +3 | V     |
| T <sub>STG</sub> | Storage Temperature range              | -65 to +150              | °C    |
| T <sub>J</sub>   | Maximum junction temperature           | +175                     | °C    |
| T <sub>LS</sub>  | Lead temperature (soldering 5 seconds) | +300                     | °C    |
| θ <sub>JC</sub>  | Thermal resistance junction to case    | 20                       | °C/W  |
| I <sub>I</sub>   | DC input current                       | ±10                      | mA    |
| P <sub>D</sub>   | Maximum power dissipation              | 1                        | W     |

**Note:**

- 1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

| SYMBOL          | PARAMETER             | LIMIT                | UNITS |
|-----------------|-----------------------|----------------------|-------|
| V <sub>DD</sub> | Supply voltage        | 4.5 to 5.5           | V     |
| V <sub>IN</sub> | Input voltage any pin | 0 to V <sub>DD</sub> | V     |
| T <sub>C</sub>  | Temperature range     | -55 to + 125         | °C    |

**DC ELECTRICAL CHARACTERISTICS <sup>7</sup>**

( $V_{DD} = 5.0V \pm 10\%$ ;  $V_{SS} = 0V$ <sup>6</sup>,  $-55^{\circ}C < T_C < +125^{\circ}C$ )

| SYMBOL      | PARAMETER   | CONDITION                                  | MIN                            | MAX                | UNIT    |
|-------------|---|--|--------------------------------|--------------------|---------|
| $V_{IL}$    | Low-level input voltage <sup>1</sup><br>ACTS<br>ACS     |  |                                | 0.8<br>.3 $V_{DD}$ | V       |
| $V_{IH}$    | High-level input voltage <sup>1</sup><br>ACTS<br>ACS    |  | .5 $V_{DD}$<br>.7 $V_{DD}$     |                    | V       |
| $I_{IN}$    | Input leakage current<br>ACTS/ACS                       | $V_{IN} = V_{DD}$ or $V_{SS}$              | -1                             | 1                  | $\mu A$ |
| $V_{OL}$    | Low-level output voltage <sup>3</sup><br>ACTS<br>ACS    | $I_{OL} = 12.0mA$<br>$I_{OL} = 100\mu A$   |                                | 0.40<br>0.25       | V       |
| $V_{OH}$    | High-level output voltage <sup>3</sup><br>ACTS<br>ACS   | $I_{OH} = -12.0mA$<br>$I_{OH} = -100\mu A$ | .7 $V_{DD}$<br>$V_{DD} - 0.25$ |                    | V       |
| $I_{OZ}$    | Three-state output leakage current                      | $V_O = V_{DD}$ and $V_{SS}$                | -30                            | 30                 | $\mu A$ |
| $I_{OS}$    | Short-circuit output current <sup>2,4</sup><br>ACTS/ACS | $V_O = V_{DD}$ and $V_{SS}$                | -300                           | 300                | mA      |
| $P_{total}$ | Power dissipation <sup>8,9</sup>                        | $C_L = 50pF$                               |                                | 2.0                | mW/MHz  |
| $I_{DDQ}$   | Quiescent Supply Current                                | $V_{DD} = 5.5V$                            |                                | 10                 | $\mu A$ |
| $C_{IN}$    | Input capacitance <sup>5</sup>                          | $f = 1MHz @ 0V$                            |                                | 15                 | pF      |
| $C_{OUT}$   | Output capacitance <sup>5</sup>                         | $f = 1MHz @ 0V$                            |                                | 15                 | pF      |

**Notes:**

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH}(min) + 20\%$ ,  $-0\%$ ;  $V_{IL} = V_{IL}(max) + 0\%$ ,  $-50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH}(min)$  and  $V_{IL}(max)$ .
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-M-38510, for current density  $\leq 5.0E5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose  $\leq 1E6$  rads(Si).
- Power does not include power contribution of any TTL output sink current.
- Power dissipation specified per switching output.

**AC ELECTRICAL CHARACTERISTICS <sup>2</sup>**

( $V_{DD} = 5.0V \pm 10\%$ ;  $V_{SS} = 0V$  <sup>1</sup>,  $-55^{\circ}C < T_C < +125^{\circ}C$ )

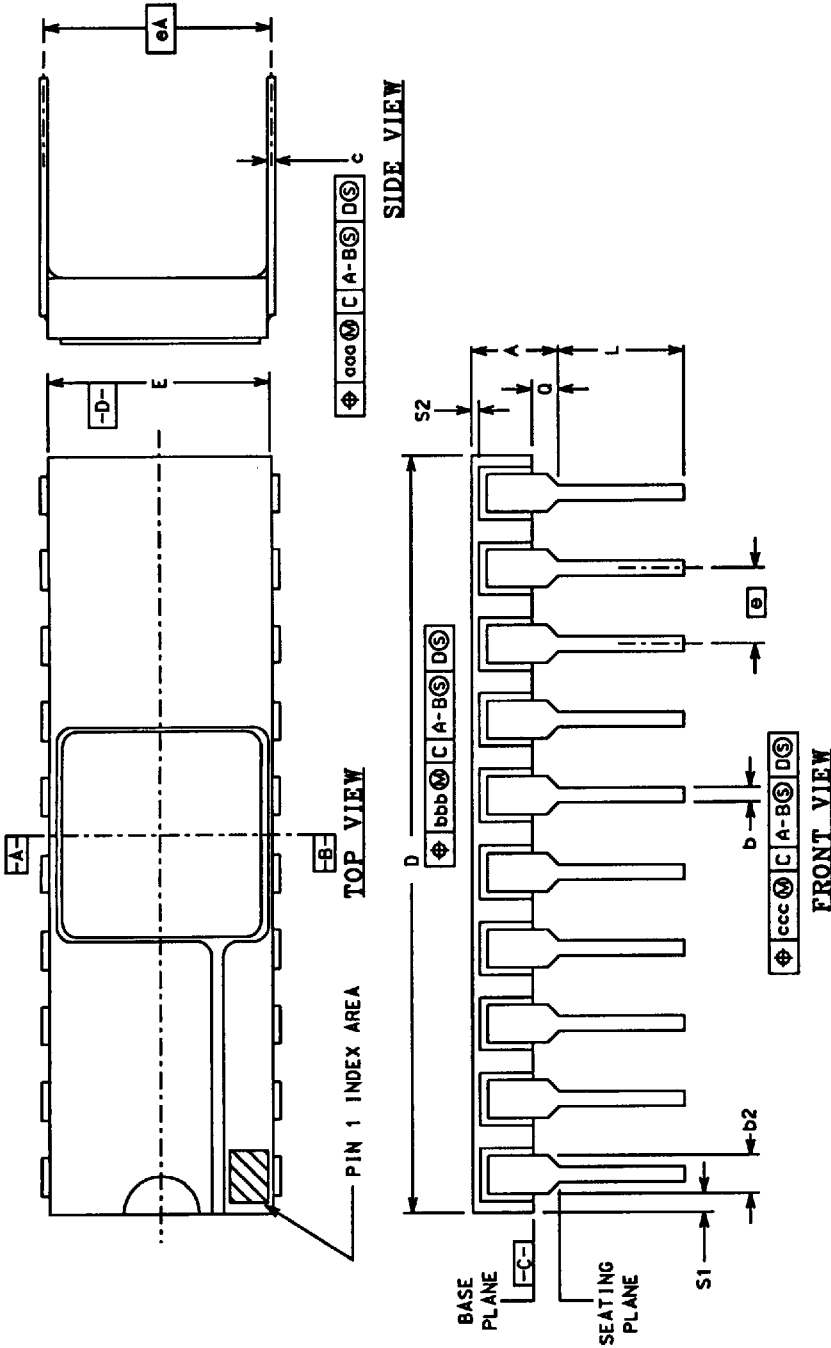
| SYMBOL    | PARAMETER                           | MINIMUM | MAXIMUM | UNIT |
|-----------|-------------------------------------|---------|---------|------|
| $t_{PLH}$ | Data to bus                         | 1       | 11      | ns   |
| $t_{PHL}$ | Data to bus                         | 1       | 15      | ns   |
| $t_{PZL}$ | $\bar{G}$ low to bus active         | 2       | 12      | ns   |
| $t_{PZH}$ | $\bar{G}$ low to bus active         | 2       | 12      | ns   |
| $t_{PLZ}$ | $\bar{G}$ high to bus three-state   | 2       | 12      | ns   |
| $t_{PHZ}$ | $\bar{G}$ high to bus three-state   | 2       | 12      | ns   |
| $t_{TLH}$ | Output transition time <sup>3</sup> | 1       | 10      | ns   |
| $t_{THL}$ | Output transition time <sup>3</sup> | 1       | 10      | ns   |

**Notes:**

1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose  $\leq 1E6$  rads(Si)
3. This is controlled via design or process parameters. These values are characterized upon initial design release and upon design changes which effect these characteristics. These are not directly tested.

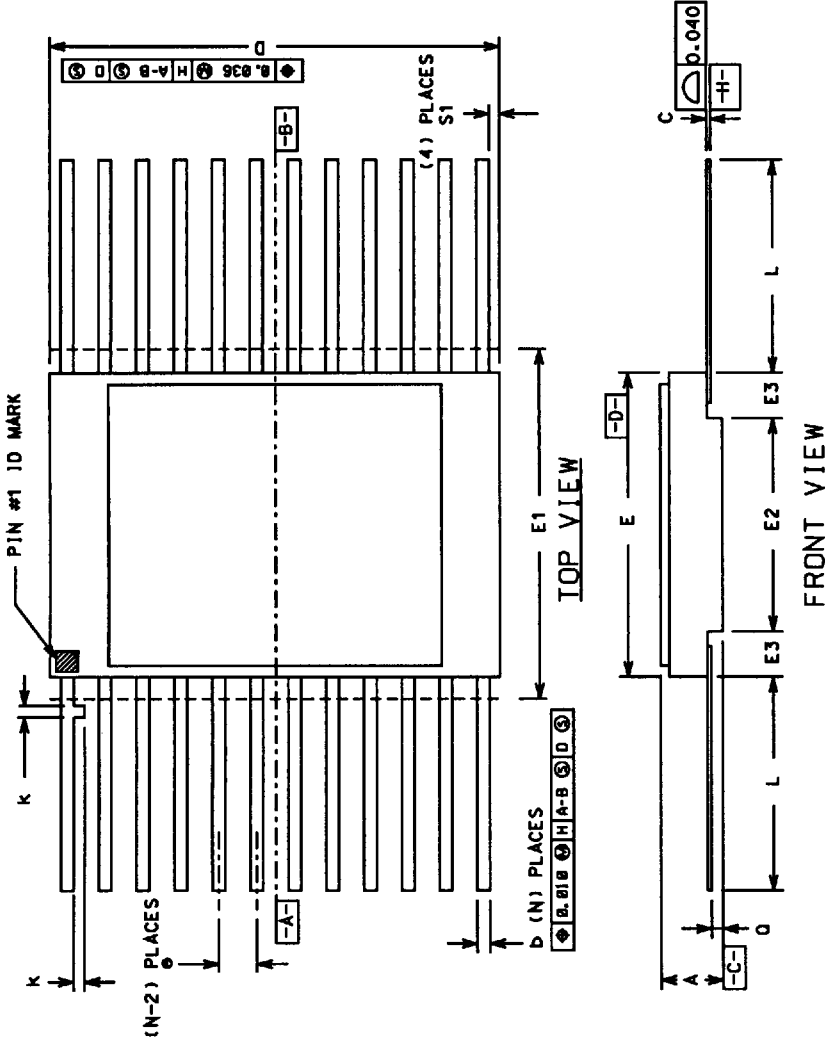
## 2.0 RAD-HARD MSI PACKAGES

### Side-Brazed Packages



| PKG<br>CONFIG | MIL-STD-<br>1835 Dwg<br>CONF C | DIMENSION SYMBOLS |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
|---------------|--------------------------------|-------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
|               |                                | A                 | b     | b2    | c     | D     | E     | e     | eA    | L     | Q     | S1    | S2    | ddd   | bbb   | ccc   |
| -01           | 14 D-1                         | 0.200             | 0.026 | 0.065 | 0.018 | 0.785 | 0.310 | 0.100 | 0.300 | 0.200 | 0.060 | 0.005 | 0.005 | 0.015 | 0.030 | 0.010 |
| -02           | 16 D-2                         | 0.200             | 0.014 | 0.065 | 0.018 | 0.840 | 0.310 | 0.100 | 0.300 | 0.200 | 0.060 | 0.005 | 0.005 | 0.015 | 0.030 | 0.010 |
| -03           | 20 D-8                         | 0.200             | 0.026 | 0.065 | 0.018 | 1.060 | 0.310 | 0.100 | 0.300 | 0.200 | 0.070 | 0.005 | 0.005 | 0.015 | 0.030 | 0.010 |
|               |                                |                   | 0.014 | 0.045 | 0.008 |       | 0.220 | 0.100 | 0.300 | 0.125 | 0.015 | 0.005 | 0.005 | 0.015 | 0.030 | 0.010 |
|               |                                |                   | 0.014 | 0.045 | 0.008 |       | 0.220 | 0.100 | 0.300 | 0.125 | 0.015 | 0.005 | 0.005 | 0.015 | 0.030 | 0.010 |

# Flatpack Packages



| PKG CONFIG | LEAD COUNT | MIL-STD 1835 DWG CONF B | DIMENSION SYMBOLS |       |       |       |       |       |     |     |       |       |       |       |       |       |       |
|------------|------------|-------------------------|-------------------|-------|-------|-------|-------|-------|-----|-----|-------|-------|-------|-------|-------|-------|-------|
|            |            |                         | A                 | b     | c     | D     | E     | E1    | E2  | E3  | e     | k     | L     | O     | S1    |       |       |
| -03        | 14         | F-2A                    | 0.115             | 0.022 | 0.009 | 0.390 | 0.260 | 0.290 | --- | --- | 0.130 | 0.030 | 0.050 | 0.015 | 0.370 | 0.045 | ---   |
|            |            |                         | 0.045             | 0.015 | 0.004 | ---   | 0.235 | ---   | --- | --- | ---   | ---   | BSC   | 0.008 | 0.270 | 0.026 | 0.005 |
| -04        | 16         | F-5A                    | 0.115             | 0.022 | 0.009 | 0.440 | 0.285 | 0.315 | --- | --- | 0.130 | 0.030 | 0.050 | 0.015 | 0.370 | 0.045 | ---   |
|            |            |                         | 0.045             | 0.015 | 0.004 | ---   | 0.245 | ---   | --- | --- | ---   | ---   | BSC   | 0.008 | 0.250 | 0.026 | 0.005 |
| -05        | 20         | F-9A                    | 0.115             | 0.022 | 0.009 | 0.540 | 0.300 | 0.330 | --- | --- | 0.130 | 0.030 | 0.050 | 0.015 | 0.370 | 0.045 | ---   |
|            |            |                         | 0.045             | 0.015 | 0.004 | ---   | 0.245 | ---   | --- | --- | ---   | ---   | BSC   | 0.008 | 0.250 | 0.026 | 0.000 |