CHIPS

5331 Dup

PRELIMINARY

82C202A ADVANCED MEMORY CONTROLLER FOR THE CS8220A-10/12 PC/AT COMPATIBLE CHIPSet™

- **Superset of 82C202 Memory Controller for CS8220 based PC/AT compatibles**
- **Synchronous switching between two user defined clock inputs**
- **Supports 256K and 1 Megabit DRAMs**
- **CMOS, 68 pin PLCC packaging**
- **Options for dividing the I/O Channel Clock and DMA Clock by 2 for high speed 10 and 12.5 MHz systems**
- **Supports very large Memory Configurations, from 1 MB to 4 MB.**
- **Memory Translation Logic to map 384KB to the top of Memory in systems with more than 1 MB**

The 82C202A is a superset of the 82C202 Memory Controller used with the CS8220 PC/AT Compatible CHIPSet. The 82C202A can replace the 82C202 in the CS8220 chipset to implement high performance PC/ATs that run at high clock rates—10 and 12.5 MHz—but are still compatible with add-on cards on the AT Bus, which were designed for slower (6-8 MHz) AT implementations.

The 82C202A functional block diagram is illustrated in Figure 1. The device consists of the following functional blocks:

Clock Selection Logic
Clock Switching Logic
ROM/RAM Decode and Memory Control Signals
Memory Translation Logic
1 MB DRAM Refresh Support
I/O Decode Logic
AT Buffer Control Logic

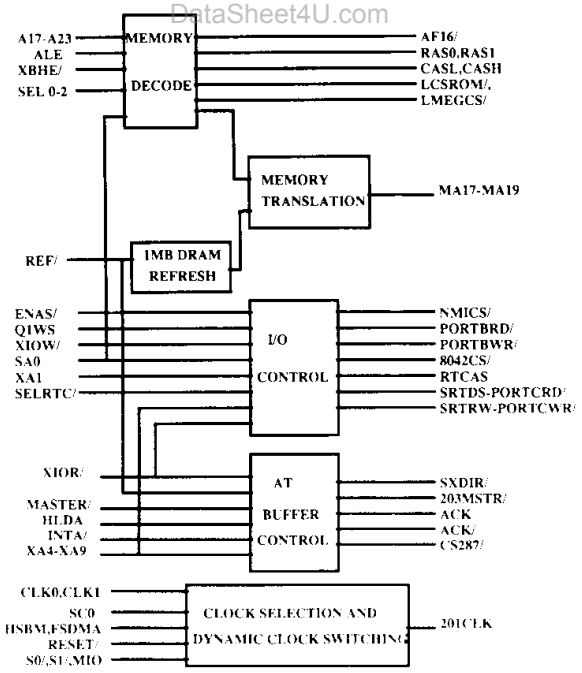


Figure 1. 82C202A Functional Block Diagram

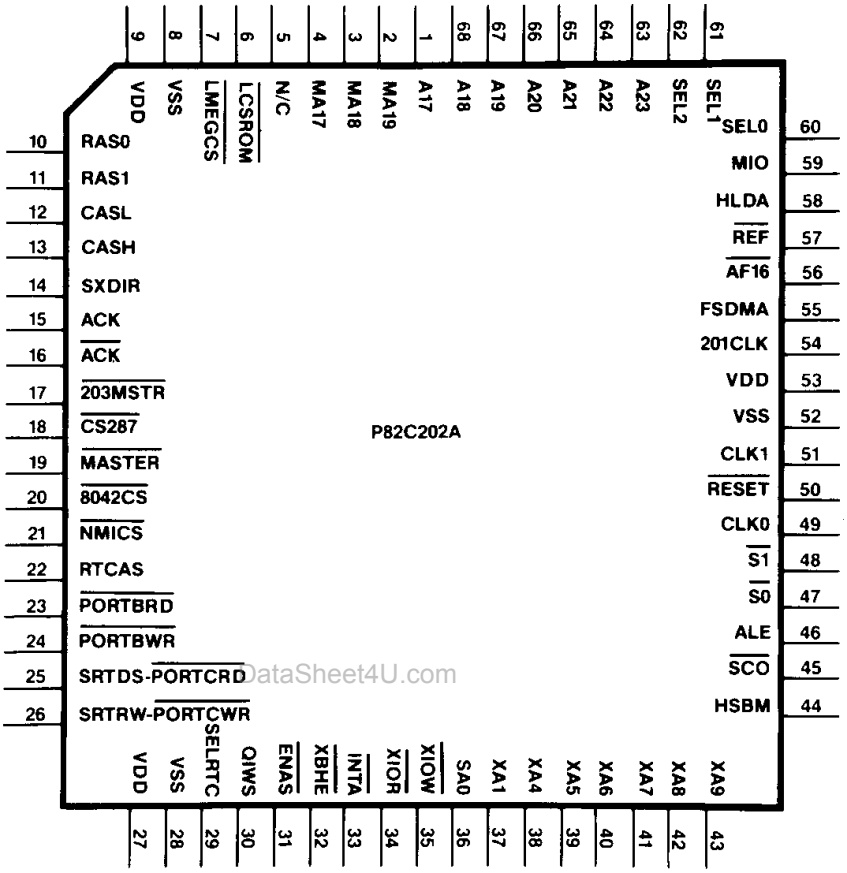


Figure 2. P82C202A Advanced Memory Controller Pinout Diagram

82C202A Pin Description

Pin No.	Pin Type	Symbol	Pin Description
1	I	A17	ADDRESS 17 input from the processor address bus.
2-4	O	MA17-MA19	MEMORY ADDRESS bits which implement the DRAM address translation for address locations from 640KB - 1024KB.
5	—	—	Leave unconnected.
6	O	$\overline{\text{LCSROM}}$	ROM CHIP SELECT is an active LOW output which is active when the ROM/PROM/EPROM space is accessed. It can be used to generate the chip select inputs for the non-volatile devices in the system.
7	O	$\overline{\text{LMEGCS}}$	LOW MEG CHIP SELECT is an active LOW output which is active when low memory address space, 0-1024 Megabyte, is accessed. It can be used to disable certain read or write signals on the I/O connector if accesses are made beyond one megabyte address space.
10,11	O	RAS0, RAS1	ROW ADDRESS SELECT 0 and 1 are used for selecting RAM banks. RAS0 selects the lower memory bank, and RAS1 selects the high memory bank.
12,13	O	CASL, CASH	COLUMN ADDRESS SELECT L and H are used to select the low and high byte respectively, during RAM access.
14	O	$\overline{\text{SXDIR}}$	SYSTEM BUS TO X BUS direction control.
15	O	ACK	This signal tri-states the SYSTEM BUS TO X BUS driver.
16	O	$\overline{\text{ACK}}$	This signal disables the module select function in the 82C206.
17	O	$\overline{\text{203MSTR}}$	This signal corresponds to $\overline{\text{MASTER}}$ qualified with REFRESH.
18	O	$\overline{\text{CS287}}$	A low signal selects the 287 Numerics processor, at addresses 0E0-0FFh.
19	I	$\overline{\text{MASTER}}$	This enables a master on the AT Bus to access the motherboard.
20	O	$\overline{\text{8042CS}}$	8042 CHIP SELECT is an active LOW signal for the 8042 device, at address 60h or 64h.
21	O	$\overline{\text{NMICS}}$	NMI CHIP SELECT is an active LOW output. It may be used to enable the Non-Maskable Interrupt to the processor.
22	O	RTCAS	REAL TIME CLOCK ADDRESS STROBE for the real time clock MC146818.
23,24	O	$\overline{\text{PORTBRD}}$ $\overline{\text{PORTBWR}}$	READ and WRITE signals for the I/O PORT B are active LOW outputs. They are generated when PORT B is either read or written to.

82C202A Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
25	O	SRTDS-/PORTCRD	Muliplexed data strobe output for the real time clock MC146818 or PORT C read strobe, at address 62h.
26	O	SRTRW-/PORTCWR	Multiplexed REAL TIME CLOCK READ/WRITE output for the real time clock device MC146818. A HIGH state indicates a read operation and a LOW state means a write operation. As the PORTCWR signal, it is the PORT C write strobe, at address 62h.
29	I	SELRTC	SELECT REAL-TIME CLOCK signal for multiplexed signals on pins 25 and 26. A LOW state selects RTC signals and a HIGH state selects PORT C signals.
30	I	Q1WS	Q1 WAIT STATE is an active HIGH input and is used to extend the Real Time Clock Address strobe by one wait state.
31	I	ENAS	ENABLE ADDRESS STROBE is an active LOW input and is used to generate the address strobe signal for the real time clock device MC146818.
32	I	XBHE	BUS HIGH ENABLE signal is used in the same way as XA0 to generate the parity error for the low or high memory data byte.
33	I	INTA	INTERRUPT ACKNOWLEDGE is generated by the 80286.
34,35	I	XIOR/XIOW	I/O READ AND WRITE are active LOW inputs and are active whenever a read or write cycle is performed with an I/O device. They are used to generate the read and write signals for the peripherals or other I/O ports on the system.
36	I	SA0	ADDRESS 0 on the S bus.
37	I	XA1	ADDRESS 1 on the X bus.
38-43	I	XA4-XA9	ADDRESS 4 through 9 on the X Bus. It is used to generate the chip selects and data strobes for other peripherals in the system.
44	I	HSBM	HALF SPEED BUS MODE controls the Dynamic Bus Clock Switching. A high state enables the 82C202A to divide by 2 the CPU Clock, whenever an off-board, memory or I/O, cycle occurs. A low state forces all cycles to have the same frequency.
45	I	SC0	SELECT CLOCK 0 selects which clock is to be used by the CPU. A low state selects CLOCK 0 and a high state selects CLOCK 1.
46	I	ALE	ADDRESS LATCH ENABLE signal to the 82C202A.
47,48	I	S0, S1	SELECT 0 and 1 status signals from the 80286.

82C202A Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
49	I	CLK0	CLOCK 0 source from an oscillator. This clock is used to provide compatibility mode to the AT. The oscillator frequency should be 32 MHz for a 8 MHz AT.
50	I	$\overline{\text{RESET}}$	This signal resets the 82C202A internal logic.
51	I	CLK1	CLOCK 1 source from an oscillator. This clock provides the high performance clock to the AT, and the oscillator frequency should be 40 MHz for a 10 MHz AT and 50 MHz for a 12.5 MHz AT.
54	O	CLK	CLOCK is the switched clock signal generated by the 82C202A, depending on the CPU cycle. It should be connected to the 82C201 X1 input.
55	O	FSDMA	FULL SPEED DMA selects the clock speed for DMA cycles. A high state selects the full speed and low state selects half the full speed.
56	O	$\overline{\text{AF16}}$	$\overline{\text{AF16}}$ is an active LOW output indicating a word memory access. It is used to generate the Command Delay control signal for delaying READ or WRITE commands for slower peripherals or I/O devices.
57	I	$\overline{\text{REF}}$	REFRESH is an active LOW input and initiates a refresh cycle for the dynamic RAMs.
58	I	HLDA	HOLD ACKNOWLEDGE is an active HIGH input from the processor. When active it indicates that the processor has relinquished the system bus in favor of another bus master in the systems.
59	I	MIO	MEMORY I/O status input from the 80286.
60,61,62	I	SEL0, SEL1, SEL2	SELECT 0, 1 and 2 select the 512K, 640K, 1M, 2M and 4M RAM option. The select logic works as follows:
63-68	I	A23-A18	ADDRESS 18-23 inputs from the processor address bus.
9,27,53	—	VDD	Power Supply.
8,28,52	—	VSS	Ground.

SEL2	SEL1	SEL0	BNK1	BNK2	TOTAL
1	1	X	512K	O	512K
1	0	1	512K	128K	640K
1	0	0	512K	512K	1M
0	1	X	2M	0	2M
0	0	X	2M	2M	4M

Clock Selection Logic

The 82C202A SC0 Select Clock signal allows the user to synchronously switch the AT from CLK0 to CLK1. In a typical AT, CLK0 would be connected to a 32 MHz Oscillator input, while CLK1 would be connected to the high speed—40 MHz or 50 MHz—Oscillator input. This would enable the AT to run at 8 MHz for compatibility reasons, and at 10 MHz or 12.5 MHz to meet performance goals.

Clock Switching Logic

In high speed, 10/12.5 MHz AT designs, add-on cards on the AT System Bus, which were designed for 6 and 8 MHz ATs, may not be able to respond to a 10/12.5 MHz data rate. The 82C202A Half Speed Bus Mode (HSBM) signal automatically divides the AT clock by 50% during Memory and I/O cycles on the AT System Bus. Consequently, the AT would run at full speed (10/12.5 MHz) for on-board cycles, but slow down to half-speed (5/6.25 MHz) for System Bus accesses. This enables high performance systems to be completely compatible to the AT architecture.

For DMA cycles, the 82C202A provides the Full Speed DMA (FSDMA) select signal. PROCCLK will be divided by 2, if FSDMA is low. By using the FSDMA and the divide by 2 option in the Integrated Peripherals Controller, 82C206, (IPC), the AT DMA cycle can be tuned to match various compatibility and performance goals for the AT.

ROM/RAM Decode and Memory Control Signals

The 82C202A contains the circuitry to decode the CPU's Address bus and provide the necessary signals for controlling both ROM and RAM on the AT system board. In order to make the 82C202A more flexible, a user configurable decode is incorporated in the device. Decode configuration is accomplished by strapping SEL0, SEL1 and SEL2 input pins. Table 1 shows the different strapping options available. This will allow the user to configure his system for 64K RAMs, 256K RAMs and 1MB DRAMs. Memory configurations ranging from 512K bytes to 4M bytes are now possible using the decode selects.

Additional support for Memory Refresh is also provided in the 82C202A. During a Refresh Cycle, the assertion of the $\overline{REF}$ input will cause the 82C202A to ignore the current Address inputs. It will instead, activate both RAS0 and RAS1 outputs while inhibiting CASL, CASH and $\overline{LCSROM}$.

$\overline{LCSROM}$ is the decoded ROM chip select output from the 82C202A. This output is asserted whenever either of the two address ranges is detected and $\overline{REF}$ is inactive. The address ranges for $\overline{LCSROM}$ are listed in Table 1.

$\overline{LMEGCS}$ is active whenever any memory access is made to an address below 100000H, or when $\overline{REF}$ is active.

RAS0 and RAS1 select the DRAM bank and CASL and CASH select the low and high byte respectively. Note, CAS is gated with SA0 and $\overline{XBHE}$ in order to implement the byte selection.

The 82C202A requires an external latch for RAS0, RAS1, CASL, CASH, $\overline{LMEGCS}$ and $\overline{LCSROM}$. ALE is generated from $\overline{S1}$ and $\overline{S0}$, in order to latch the memory control signals. See the SYS 8220A/206 schematic for an example of this circuit.

The 82C202A $\overline{AF16}$ signal indicates that a 16 bit memory transfer is taking place. This signal may be used, if required, to generate wait states.

The Parity Check Cycle can be identified by gating $\overline{AF16}$ with $\overline{LCSROM}$ and $\overline{REF}$, and then latching the output with ALE. This Parity Enable signal should be sent to the 82A205 Parity Check Logic. See the SYS 8220A/206 schematic for an example of the circuit.

Memory Translation Logic

In the IBM PC architecture, address locations from 640 KB to 1024 KB are reserved for BIOS and Device Driver functions by IBM. Consequently, Memory Systems with more than 640 KB memory cannot use this 384 KB Memory space. The 82C202A translates this 384 KB block to the top of Memory. This results in the AT having 384 KB of additional RAM memory on its system. Table 1 shows the valid address ranges for the various memory configurations.

1 MB DRAM Refresh Support

For memory systems that use 1 MB DRAMS, the high order address bits (MA8 and MA9) for the refresh cycle are available on MA17 and MA19 respectively. The low order address bits (MA0-MA7) for the refresh cycle are provided by the 82A204.

I/O Decode Logic

The I/O Decode Logic portion of the 82C202A provides signals necessary for controlling the Clock/Calendar and the Status/Control Port. IBM PC-AT compatibility is maintained for all of the decoded control signals in this section. A decoded listing of the outputs is provided in Table 2.

$\overline{\text{NMICS}}$ controls enabling and disabling of the NMI Enable Latch, and $\overline{\text{8042CS}}$ selects the Keyboard Controller.

The $\overline{\text{SELRTC}}$ signal is used for generating Real-Time Clock control signals or PORTC control signals. When $\overline{\text{SELRTC}}$ is low, it selects Real-Time Clock control signals, and when $\overline{\text{SELRTC}}$ is high, it generates PORTC control signals.

For systems that do not use the Real-Time Clock in the 82C206 Integrated Peripherals Controller, the 82C202A generates RTCAS, SRTDS and SRTRW. These signals are used for latching the address (RTCAS), latching the data (SRTDS), and determining the direction of a data transfer (SRTRW). RTCAS decode is gated with Q1WS and $\overline{\text{ENAS}}$ (which originate from the 82C201) to ensure proper latching of the register address by the Real-Time Clock.

For systems, which use the 82C206 (which internally generates SRTDS and SRTRW), $\overline{\text{PORTCRD}}$ and $\overline{\text{PORTCWR}}$ signals are provided to either latch the contents of the data bus into a latch, in the case of $\overline{\text{PORTCWR}}$, or enable status information on to the data bus using $\overline{\text{PORTCRD}}$. PORTC resides at address I/O address 62H, and can be used to provided software configurability to 82C202A options, rather than hard-wired straps.

$\overline{\text{PORTBRD}}$ and $\overline{\text{PORTBWR}}$ are provided in the 82C202A to either latch the contents of the data bus into a latch, in the case of $\overline{\text{PORTBWR}}$, or enable status information on to the data bus using $\overline{\text{PORTBRD}}$.

AT Buffer Control Logic

The 82C202A integrates additional glue logic from standard AT designs. For AT compatibles, that have used the DK8220 design, the 82C202A eliminates the use of the AT buffer control PAL as shown in the SYS 8220A/206 schematic. Table 3 shows the logic equations implemented in the 82C202A.

Select (Total RAM)			RAM Address Range		RAM Type		ROM Address Range	
S2	S1	S0	RAS0/CAS0	RAS1/CAS1	BNK0	BNK1	LOW ADDR	HIGH ADDR
0 (4MB)	0	X	000000h -09FFFFh 100000h -1FFFFFh 400000h -42FFFFh	200000h -3FFFFFh	1MB	1MB	0E0000h -0FFFFFh	FE0000h -FFFFFFh
0 (2MB)	1	X	000000h -09FFFFh 100000h -1FFFFFh 200000h -22FFFFh		1MB	NONE	0E0000h -0FFFFFh	FE0000h -FFFFFFh
1 (1MB)	0	0	000000h -07FFFFh	080000h -09FFFFFh 100000h -12FFFFh	256K	256K	0E0000h -0FFFFFh	FE0000h -FFFFFFh
1 (640KB)	0	1	000000h -07FFFFh	080000h -9FFFFFh	256K	64K	0E0000h -0FFFFFh	FE0000h -FFFFFFh
1 (512KB)	1	X	000000h -07FFFFh		256K	NONE	0E0000h -0FFFFFh	FE0000h -FFFFFFh

Table 1. Memory Configuration Selection

$\overline{PPICS}$	$\overline{SELRTC}$	SA0	XA1	XA4	$\overline{XIOR}$	$\overline{XIOW}$	$\overline{NMICS}$	$\overline{PORTBRD}$	$\overline{PORTBWR}$	$\overline{8042CS}$	SRTDS-$\overline{PORTCRD}$	RTCAS	SRTRW-$\overline{PORTCWR}$
1	X	X	X	X	X	X	1	1	1	1	1	0	1
0	0	0	0	0	X	X	1	1	1	0	1	0	1
0	0	1	0	0	0	1	1	0	1	1	1	0	1
0	0	1	0	0	1	0	1	1	0	1	1	0	1
0	0	0	0	1	1	0	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	0	0
0	0	1	0	1	0	1	1	1	1	1	0	0	1
0	1	0	1	0	0	1	1	1	1	1	0	0	1
0	1	0	1	0	1	0	1	1	1	1	1	0	0

NOTES: PPICS = $\overline{X9} \cdot \overline{X8} \cdot \overline{X7} \cdot \overline{X6} \cdot \overline{X5} \cdot (\overline{MASTER} \cdot \overline{HLDA})$

Table 2: I/O Decode Table

INPUTS	OUTPUTS
$\overline{\text{MASTER}}$	$\overline{\text{SXDIR}}$
HLDA	203MSTR
$\overline{\text{INTA}}$	ACK
$\overline{\text{XIOR}}$	$\overline{\text{ACK}}$
XA5	$\overline{\text{CS287}}$
XA6	
XA7	
XA8	
XA9	
$\overline{\text{REF}}$	

Logic Equations

SXDIR = XIOR * $\overline{\text{XA9}}$ * $\overline{\text{XA8}}$ * $\overline{\text{XA7}}$ +
XIOR * $\overline{\text{XA9}}$ * $\overline{\text{XA8}}$ * $\overline{\text{XA6}}$ +
XIOR * $\overline{\text{XA9}}$ * $\overline{\text{XA8}}$ * $\overline{\text{XA5}}$ +
INTA

DMA = $\overline{\text{MASTER}}$ * HLDA

ACK = DMA

$\overline{\text{ACK}}$ = $\overline{\text{DMA}}$

CS287 = $\overline{\text{DMA}}$ * $\overline{\text{XA9}}$ * $\overline{\text{XA8}}$ * XA7 * XA6 * XA5

203MSTR = MASTER * $\overline{\text{REF}}$

Table 3: AT Buffer Control Logic

82C202A Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C202A Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

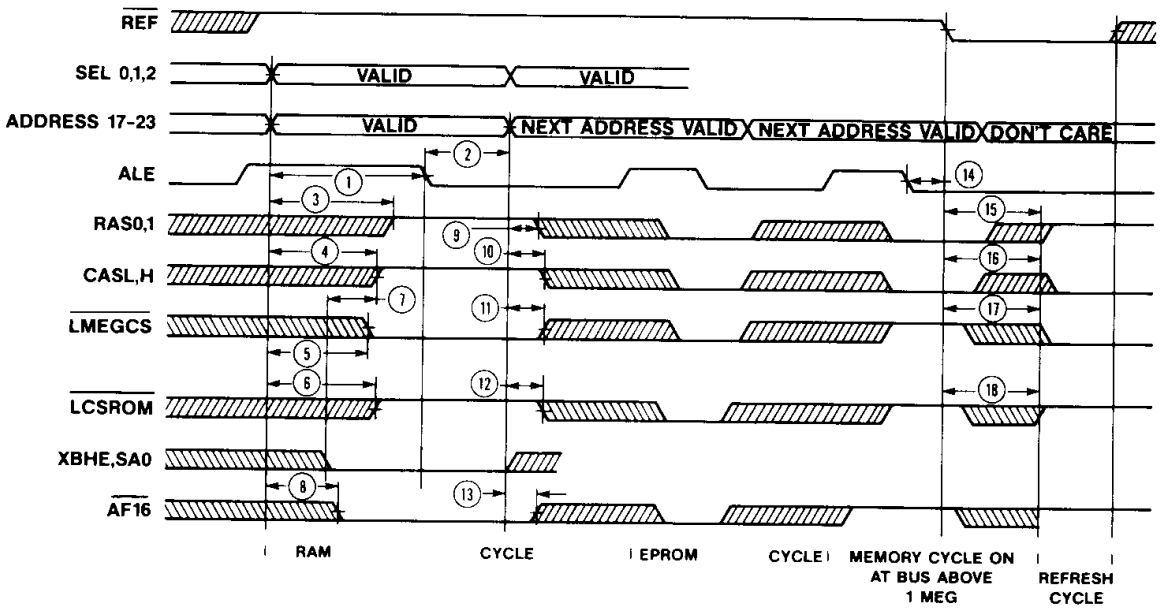
82C202A DC Characteristics

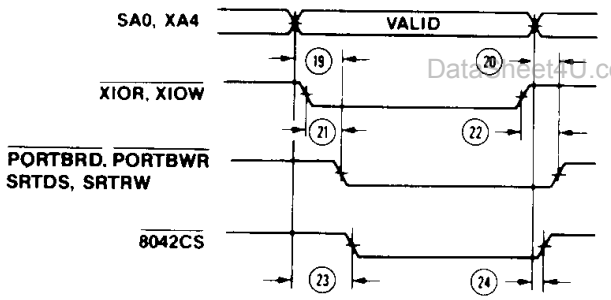
Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL} (Note 1)	V_{OL}		0.45	V
Output High Voltage I_{OH} (Note 1)	V_{OH}	2.4		V
Input Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}	TBD	TBD	mA
Input Clamp Voltage	V_{IC}		TBD	V
Power Supply Current @ 12.5 MHz Clock	I_{CC}		20	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA

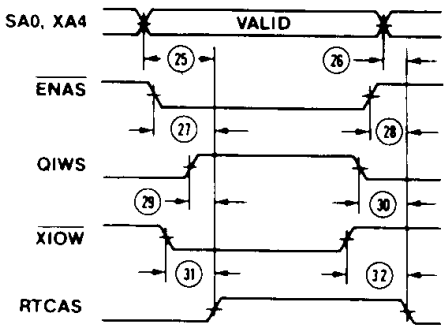
82C202A AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Max.	Units
t1	Address & Sel setup to ALE going inactive	60		ns
t2	Address & Sel hold time from ALE inactive	0		ns
t3	RAS0, 1 valid from Address valid		40	ns
t4	CASL, H valid from Address valid		40	ns
t5	$\overline{\text{LMEGCS}}$ valid from Address valid		45	ns
t6	$\overline{\text{LCSROM}}$ valid from Address valid		45	ns
t7	$\overline{\text{LMEGCS}}$ valid from XBHE, SA0 valid		15	ns
t8	$\overline{\text{AF16}}$ valid from Address valid		40	ns
t9	RAS0, 1 hold time from Address valid	0		ns
t10	CASL, H hold time from Address invalid	0		ns
t11	$\overline{\text{LMEGCS}}$ hold time from Address valid	0		ns
t12	$\overline{\text{LCSROM}}$ hold time from Address valid	0		ns
t13	$\overline{\text{AF16}}$ hold time from Address invalid	0		ns
t14	REF hold time from ALE inactive	0		ns
t15	RAS0, 1 active from REF active		30	ns
t16	CASL, H inactive from REF active		30	ns
t17	$\overline{\text{LMEGCS}}$ active from REF active		30	ns
t18	$\overline{\text{LCSROM}}$ inactive from REF active		30	ns
t19	$\overline{\text{PORTBRD}}$, $\overline{\text{PORTBWR}}$, SRTDS or SRTRW active (low) from SA0 and XA4 valid		35	ns
t20	$\overline{\text{PORTBRD}}$, $\overline{\text{PORTBWR}}$, SRTDS or SRTRW inactive (high) from SA0 and XA4 invalid	5		ns
t21	$\overline{\text{PORTBRD}}$, $\overline{\text{PORTBWR}}$, SRTDS or SRTRW active (low) from $\overline{\text{XIOR}}$ or $\overline{\text{XIOW}}$ active		35	ns
t22	$\overline{\text{PORTBRD}}$, $\overline{\text{PORTBWR}}$, SRTDS or SRTRW inactive (high) from $\overline{\text{XIOR}}$ or $\overline{\text{XIOW}}$ inactive		5	ns
t23	$\overline{\text{8042CS}}$ active from SA0 & XA4 valid		35	ns
t24	$\overline{\text{8042CS}}$ inactive from SA0 & XA4 invalid	5		ns
t25	RTCAS active from SA0 & XA4 valid		35	ns
t26	RTCAS inactive from SA0 & XA4 invalid	5	35	ns
t27	RTCAS active from $\overline{\text{ENAS}}$ active		35	ns
t28	RTCAS inactive from $\overline{\text{ENAS}}$ inactive	5	35	ns
t29	RTCAS active from Q1WS active		35	ns
t30	RTCAS inactive from Q1WS inactive	5	35	ns
t31	RTCAS active from $\overline{\text{XIOW}}$ active		35	ns
t32	RTCAS inactive from $\overline{\text{XIOW}}$ inactive	5	35	ns







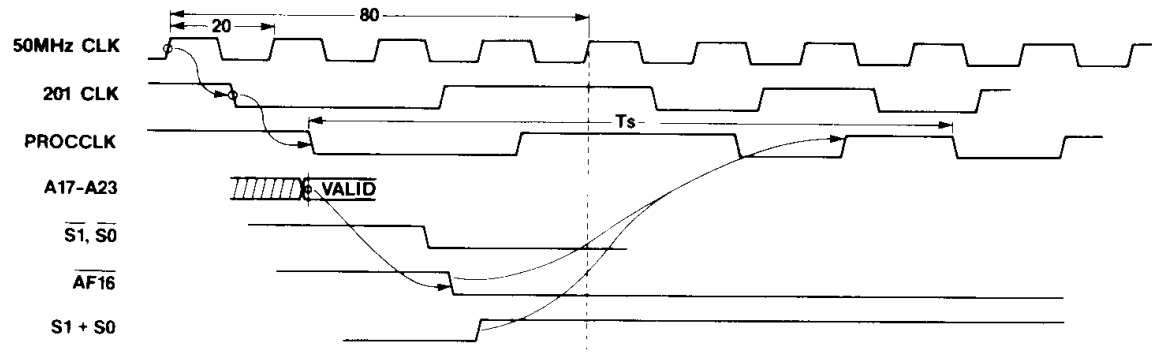
Output test conditions:

RAS0,1
CASL,H
AF16
LCSROM
LMEGCS

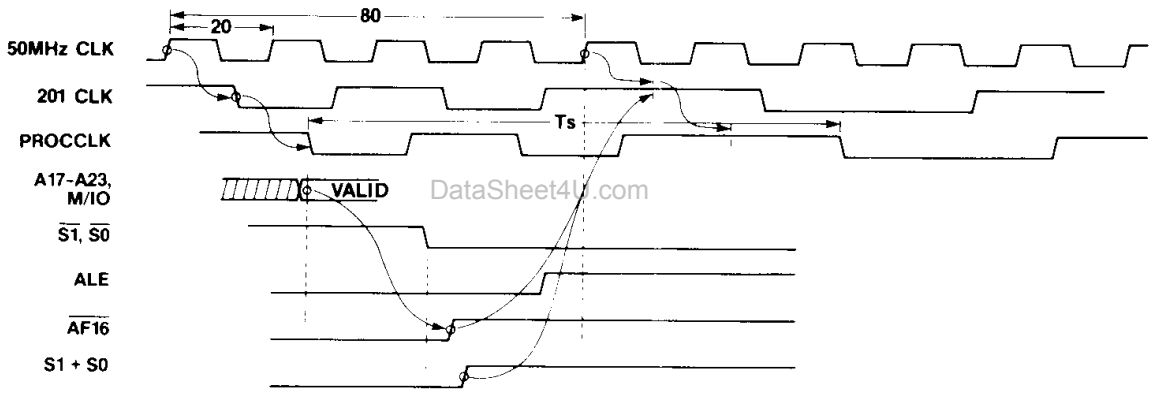
CL = 85pF
I_{ol} = 4ma
I_{oh} = 4ma

PORTBRD
PORTBWR
SRTDS
SRTRW
8042CS
RTCAS

CL = 50pF
I_{ol} = 2ma
I_{oh} = 2ma

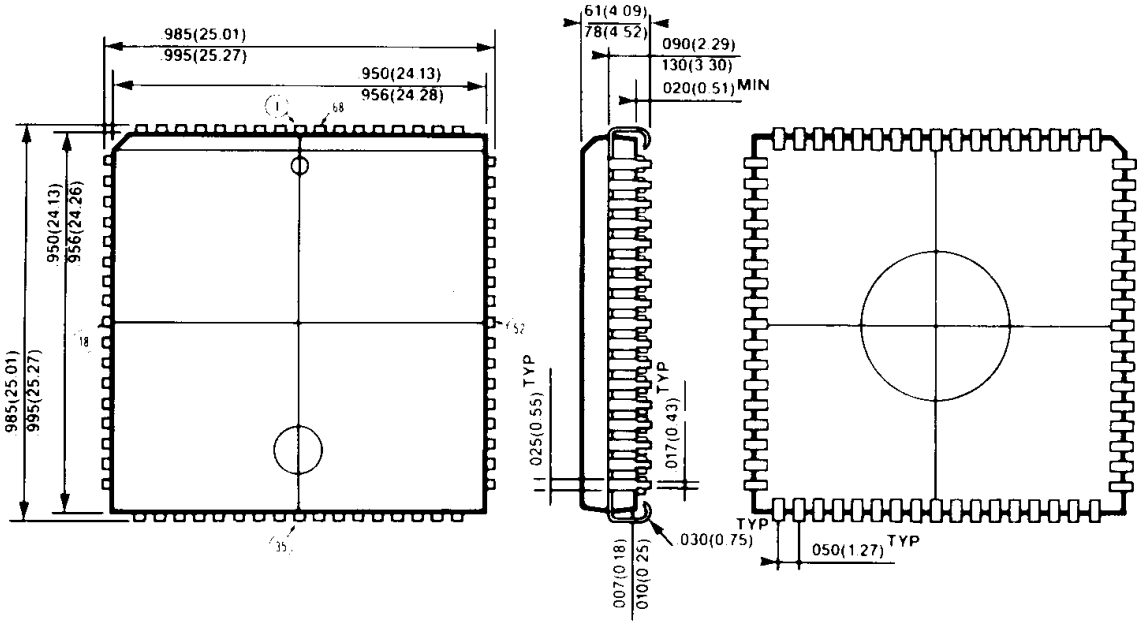


Full Speed to Half Speed Transition



Half Speed to Full Speed Transition

68-PIN PLASTIC LEADED CHIP CARRIER



Ordering Information

Order Number	Package Type
P82C202A	PLCC-68 pins

Note:
1. PLCC = Plastic Leaded Chip Carrier

68-PIN PLCC SOCKET