MAY 29 1992

Ultra-Low Noise, High-Speed Precision Op Amp

General Description

Maxim's LT1028 precision op amp is ideal for applications requiring a combination of ultra-low noise and high speed. The LT1028 features noise voltage of 0.85nV/√Hz at 1kHz and 1.0nV/√Hz at 10Hz, which is only 1/10th the noise of industry-standard precision op amps. Other precision characteristics include 10µV typ offset voltage, 0.1µV/°C drift and an open-loop gain of 30V/µV. High-speed characteristics include a 75MHz gain-bandwidth product and a 15V/µs slew rate.

With an equivalent noise resistance of 50Ω, the LT1028 is ideal for very low source-impedance transducer or audio-amplifier applications because its contribution to total system noise is negligible.

Applications

Low-Noise Frequency Synthesizers
High-Quality Audio Amplifiers
Infrared Detectors
Accelerometer and Gyro Amplifiers
350Ω Bridge Signal Conditioning
Magnetic Search-Coil Amplifiers
Ultra-Low Noise Instrumentation Amplifiers

Features

- **Ultra-Low Voltage Noise:**
  1.1nV/√Hz Max at 1kHz
  0.85nV/√Hz Typ at 1kHz
  1.0nV/√Hz Typ at 10Hz
  35nVp-p Typ, 0.1Hz to 10Hz
- **Voltage and Current Noise 100% Tested**
- **50MHz Min Gain-Bandwidth Product**
- **11V/µs Min Slew Rate**
- **40µV Max Offset Voltage**
- **0.8µV/°C Max Offset Drift**
- **7 Million Min Voltage Gain**

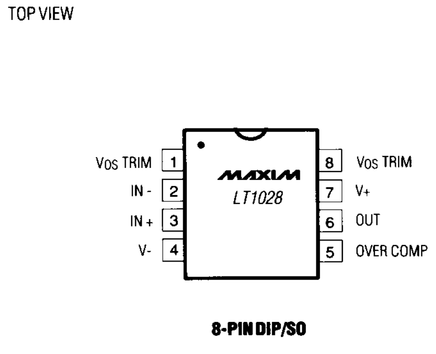
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
LT1028ACN8	0°C to +70°C	8 Plastic DIP
LT1028CN8	0°C to +70°C	8 Plastic DIP
LT1028ACSA	0°C to +70°C	8 SO
LT1028CSA	0°C to +70°C	8 SO
LT1028ACS	0°C to +70°C	16 Wide SO
LT1028CS	0°C to +70°C	16 Wide SO
LT1028ACJ8	0°C to +70°C	8 CERDIP
LT1028CJ8	0°C to +70°C	8 CERDIP
LT1028ACH	0°C to +70°C	8 TO-99 Can
LT1028CH	0°C to +70°C	8 TO-99 Can
LT1028C/D	0°C to +70°C	Dice*

*Consult factory for dice specifications.

Ordering Information continued on last page.

Pin Configurations

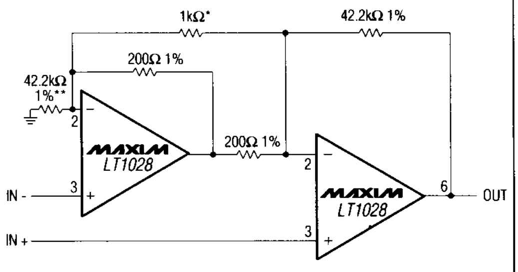


8-PIN DIP/SO

Pin Configurations continued on last page.

Typical Operating Circuit

LOW-NOISE, TWO OP-AMP INSTRUMENTATION AMPLIFIER



NOTES: AC COMMON-MODE CORNER FREQUENCY = 100Hz
* TRIM FOR GAIN
** TRIM FOR COMMON-MODE REJECTION

Ultra-Low Noise, High-Speed Precision Op Amp

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-)
-55°C to +105°C . . . . ±22V
+105°C to +125°C . . . . ±16V
Differential Input Current (Note 1) . . . . ±25mA
Differential Input Voltage . . . . V+ to V-
Common-Mode Input Voltage . . . . V+ to V-
Output Short-Circuit Duration . . . . Indefinite
Continuous Total Power Dissipation (T_A = +70°C)
8-pin Plastic DIP (derate 6.9mW/°C above +70°C) 552mW
8-pin SO (derate 5.88mW/°C above +70°C) 471mW
16-pin Wide SO (derate 9.52mW/°C above +70°C) . . .762mW
8-pin CERDIP (derate 8.0mW/°C above +70°C) 640mW
8-pin TO-99 Can (derate 6.67mW/°C above +70°C) . .533mW

Operating Temperature Ranges:
LT1028AC/C . . . . 0°C to +70°C
LT1028AE/E . . . . -40°C to +85°C
LT1028AM/M . . . . -55°C to +125°C
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . +300°C

Note 1: The amplifier inputs are protected by internal back-to-back clamp diodes. In order to achieve low noise, current-limiting resistors are not used. If differential input voltages exceeding ±1.8V are applied, input current should be limited to 25mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1028AC/AE/AM			LT1028C/E/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 2)		10	40		20	80	µV
Long-Term Input Offset Voltage Stability	$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	(Note 3)		0.3			0.3		µV/Mo
Input Offset Current	I_{OS}	V_{CM} = 0V		12	50		18	100	nA
Input Bias Current	I_B	V_{CM} = 0V		±25	±90		±30	±180	nA
Input Noise Voltage	e_n	0.1Hz to 10Hz (Note 4)		35	75		35	90	nVp-p
Input Noise Voltage Density		f_O = 10Hz (Note 5)		1.0	1.7		1.0	1.9	nV/√Hz
		f_O = 1000Hz, 100% tested		0.85	1.1		0.9	1.2	
Input Noise Current Density	i_n	f_O = 10Hz (Notes 4 & 6)		4.7	10.0		4.7	12.0	pA/√Hz
		f_O = 1000Hz, 100% tested		1.0	1.6		1.0	1.8	
Input Resistance		Common Mode		300			300		MΩ
		Differential Mode		20			20		kΩ
Input Capacitance				5			5		pF
Input Voltage Range			±11.0	±12.2		±11.0	±12.2		V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±11V	114	126		110	126		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4V to ±18V	117	133		110	132		dB
Large-Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, V_O = ±12V	7.0	30.0		5.0	30.0		V/µV
		$R_L \geq 1k\Omega$, V_O = ±10V	5.0	20.0		3.5	20.0		
		$R_L \geq 600\Omega$, V_O = ±10V	3.0	15.0		2.0	15.0		
Maximum Output Voltage Swing	V_{OUT}	$R_L \geq 2k\Omega$	±12.3	±13.0		±12.0	±13.0		V
		$R_L \geq 600\Omega$	±11.0	±12.2		±10.5	±12.2		
Slew Rate	SR	A_{VCL} = -1	11	15		11	15		V/µS
Gain-Bandwith Product	GBW	f_O = 20kHz (Note 7)	50	75		50	75		MHz
Open-Loop Output Impedance	Z_O	V_O = 0, I_O = 0		80			80		Ω
Supply Current	I_S			7.4	9.5		7.6	10.5	mA

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1028AE/AM MIN	LT1028AE/AM TYP	LT1028AE/AM MAX	LT1028E/M MIN	LT1028E/M TYP	LT1028E/M MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 2)		30	120		45	180	μV
Average Input Offset Drift	$\frac{\Delta V_{OS}}{\Delta Temp}$	(Note 8)		0.2	0.8		0.25	1.0	μV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V		25	90		30	180	nA
Input Bias Current	I_B	V_{CM} = 0V		±40	±150		±50	±300	nA
Input Voltage Range			±10.3	±11.7		±10.3	±11.7		V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±10.3V	106	122		100	120		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±16V	110	130		104	130		dB
Large-Signal Voltage Gain	A_{VOL}	$R_L \ge 2k\Omega$, V_O = ±10V	3.0	14.0		2.0	14.0		V/μV
		$R_L \ge 1k\Omega$, V_O = ±10V	2.0	10.0		1.5	10.0		
Maximum Output Voltage Swing	V_{OUT}	$R_L \ge 2k\Omega$	±10.3	±11.6		±10.3	±11.6		V
Supply Current	I_S			8.7	11.5		9.0	13.0	mA

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1028AC MIN	LT1028AC TYP	LT1028AC MAX	LT1028C MIN	LT1028C TYP	LT1028C MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 2)		15	80		30	125	μV
Average InputOffset Drift	$\frac{\Delta V_{OS}}{\Delta Temp}$	(Note 8)		0.1	0.8		0.2	1.0	μV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V		15	65		22	130	nA
Input Bias Current	I_B	V_{CM} = 0V		±30	±120		±40	±240	nA
Input Voltage Range			±10.5	±12.0		±10.5	±12.0		V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±10.5V	110	124		106	124		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	114	132		107	132		dB
Large-Signal Voltage Gain	A_{VOL}	$R_L \ge 2k\Omega$, V_O = ±10V	5.0	25.0		3.0	25.0		V/μV
		$R_L \ge 1k\Omega$, V_O = ±10V	4.0	18.0		2.5	18.0		
Maximum Output Voltage Swing	V_{OUT}	$R_L \ge 2k\Omega$	±11.5	±12.7		±11.5	±12.7		V
		$R_L \ge 600\Omega$ (Note 9)	± 9.5	±11.0		± 9.0	±10.5		
Supply Current	I_S			8.0	10.5		8.2	11.5	mA

Note 2: V_{OS} measurements are performed by automatic test equipment approximately 0.25 sec. after application of power. At T_A=25°C, offset voltage is measured with the chip heated to approximately 55°C to account for chip temperature rise when the device is fully warmed up.

Note 3: Long-Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV.

Note 4: Tested on a sample basis only.

Note 5: 10Hz noise-voltage density sample tested on every lot. 100% testing at 10Hz is available on request.

Note 6: Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from 100% testing at 1kHz.

Note 7: Gain-bandwidth product is not tested. Guaranteed by design and by inference from the slew-rate measurement.

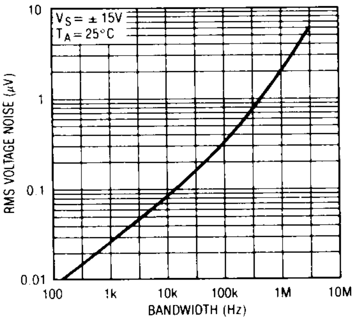
Note 8: Subject to 0.1% AQL sample test.

Note 9: Guaranteed by design, fully warmed up at T_A = 70°C. Includes chip temperature increase due to supply and load currents.

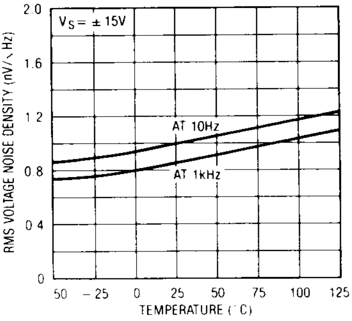
Ultra-Low Noise, High-Speed Precision Op Amp

Typical Operating Characteristics

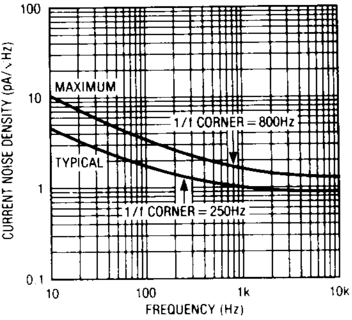
Wideband Voltage Noise (0.1Hz to Frequency Indicated)



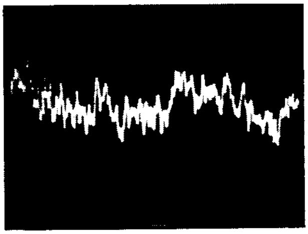
Voltage Noise vs Temperature



Current Noise Spectrum

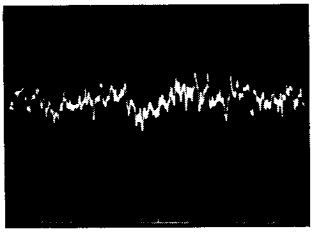


0.01 Hz to 1 Hz Voltage Noise



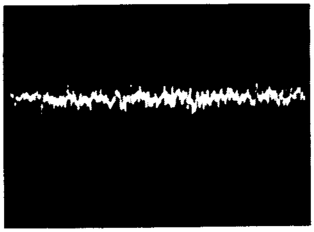
VERTICAL SCALE = 10 nV/DIV
HORIZONTAL SCALE = 10 s/DIV

0.1 Hz to 10 Hz Voltage Noise



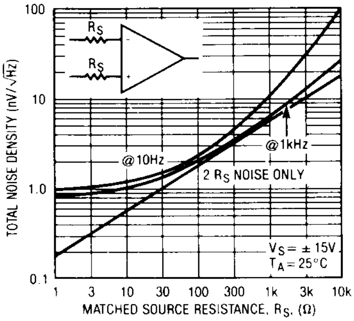
VERTICAL SCALE = 10 nV/DIV
HORIZONTAL SCALE = 1 s/DIV

Wideband Noise, DC to 20 KHz

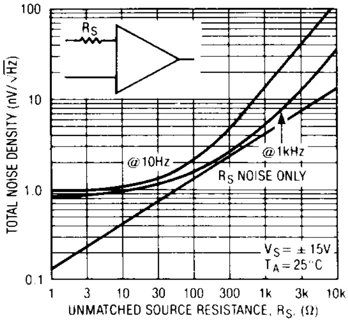


VERTICAL SCALE = 0.5µV/DIV
HORIZONTAL SCALE = 0.5ms/DIV

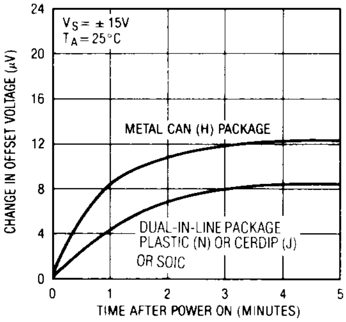
Total Noise vs Matched Source Resistance



Total Noise vs Unmatched Source Resistance

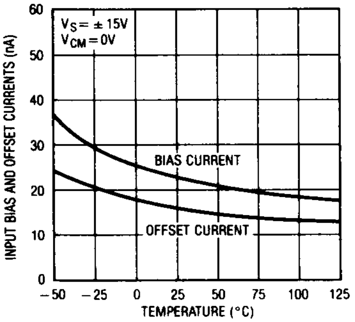


Warm-Up Drift

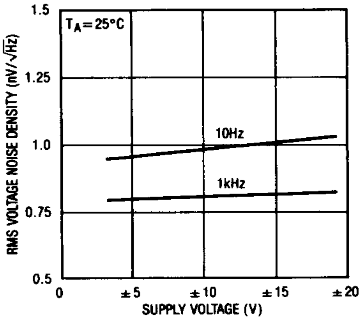


Typical Operating Characteristics (continued)

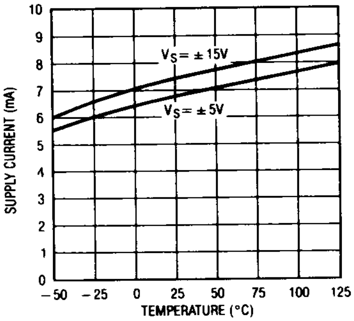
Input Bias and Offset Currents Over Temperature



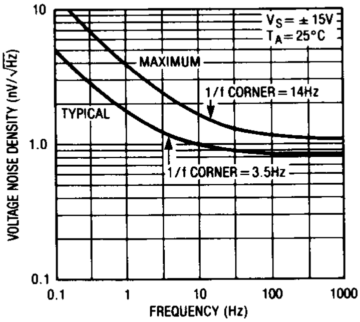
Voltage Noise vs Supply Voltage



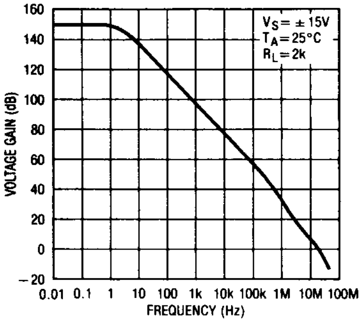
Supply Current vs Temperature



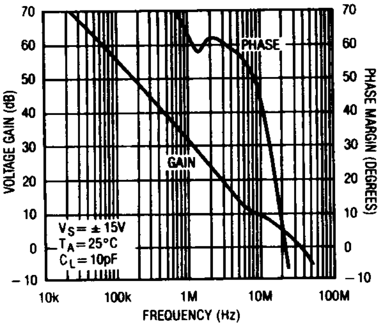
Voltage Noise vs Frequency



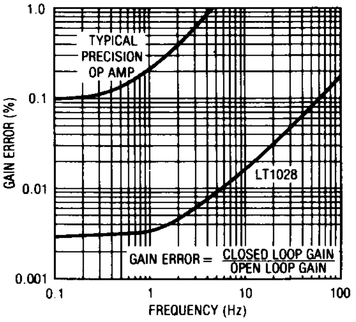
Voltage Gain vs Frequency



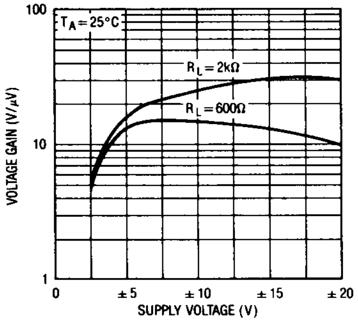
Gain, Phase vs Frequency



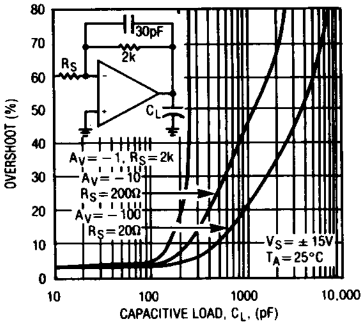
Gain Error vs Frequency Closed Loop Gain = 1000



Voltage Gain vs Supply Voltage



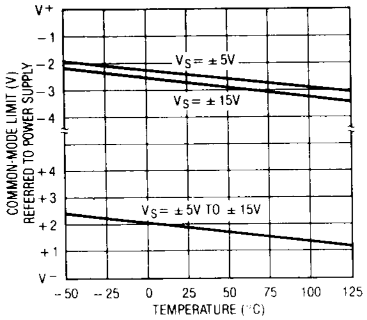
Capacitance Load Handling



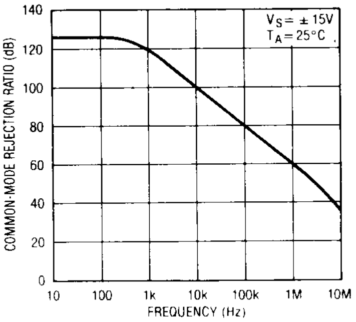
Ultra-Low Noise, High-Speed Precision Op Amp

Typical Operating Characteristics (continued)

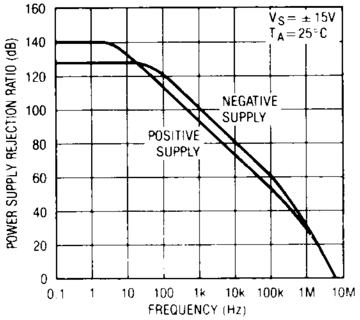
Common-Mode Limit Over Temperature



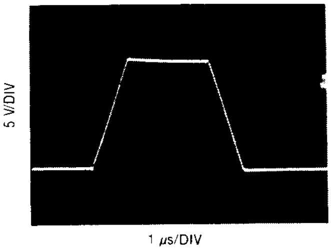
Common-Mode Rejection Ratio vs Frequency



Power Supply Rejection Ratio vs Frequency

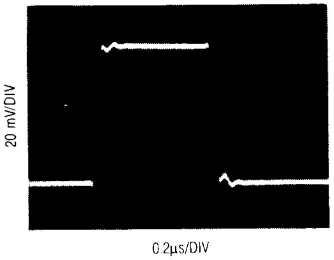


Large-Signal Transient Response



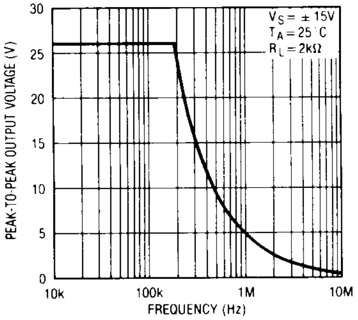
$R_S = R_F = 2$ K, $C_F = 30$ pF
$A_V = -1$

Small-Signal Transient Response

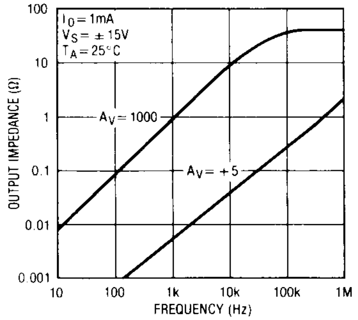


$R_S = R_F = 2K$, $O_F = 30pF$
$C_L = 80pF$, $A_V = -1$

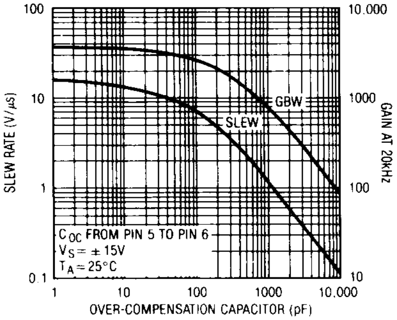
Maximum Undistorted Output vs Frequency



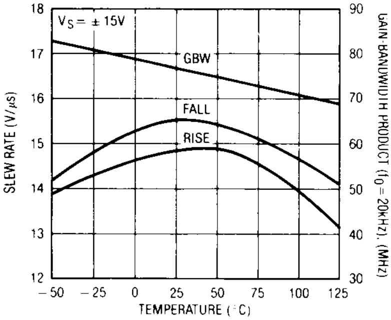
Closed Loop Output Impedance



Slew Rate, Gain-Bandwidth-Product vs Over-Compensation Capacitor



Slew Rate, Gain-Bandwidth Product Over Temperature



Pin Description

PIN # 8-Pin Pkg	PIN # 16-Pin Pkg	NAME	FUNCTION
1	3	V_{OS} TRIM	Offset Null. Connect to one end of a 1kΩ pot for voltage offset nulling.
2	4	IN-	Inverting Input
3	5	IN+	Noninverting Input
4	6	V-	Negative Supply Pin. Connect to -15V supply.
5	11	OVERCOMP	Reduction of Noise and Signal Bandwidth. Connect a capacitor from OUT to OVERCOMP (see Applications section for details).
6	12	OUT	Output
7	13	V+	Positive Supply Pin. Connect to +15V supply.
8	14	V_{OS} TRIM	Offset Null. Connect to other end of 1kΩ Pot with wiper to V+.
	1,2,7-10, 15,&16	N.C.	No Connect

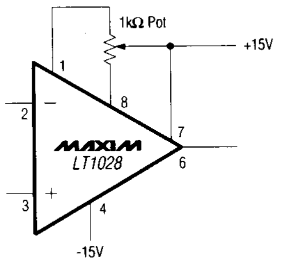
Applications

Maxim's LT1028 is both electrically and pin compatible with Linear Technology's LT1028. It can be used as a high-speed, low-noise, plug-in replacement for the OP-27, OP-37 or similar op amps without removing external trim circuitry.

Offset-Voltage Adjustment

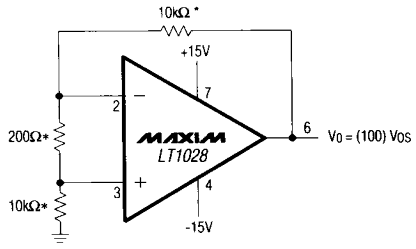
The input offset voltage, temperature drift, and input offset current of the LT1028 are minimized by laser trimming. If additional offset-voltage adjustment is necessary, connect a 1kΩ trim pot as shown in Figure 1.

The offset adjustment range with a 1kΩ pot is about ±1mV. This trim pot has a minimal affect on the total output noise of typical amplifier circuits. Figure 2 shows a simple test circuit for input offset voltage.



Pin Configuration for 8-Pin Package.

Figure 1. V_{OS} Adjustment



* MUST HAVE LOW THERMO-ELECTRIC POTENTIAL

Pin Configuration for 8-Pin Package.

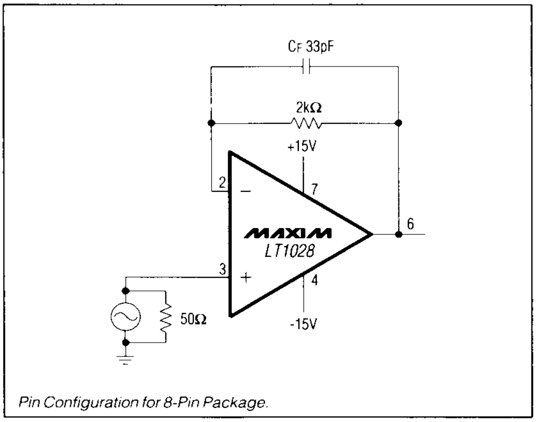
Figure 2. Test Circuit for Voltage Offset and Drift with Temperature

Voltage-Offset Drift

The thermocouple effect of temperature gradients on dissimilar metals at the contacts of the input terminals is an important factor in voltage-offset drift. This thermal effect could exceed the inherent drift characteristics of the amplifier. The induced voltage can be minimized by keeping input leads short, close together, and at the same temperature (in part by minimizing air currents around the part).

Frequency Response

As indicated by the Gain, Phase vs. Frequency graph, the phase margin of the voltage-follower configuration is inadequate for stable operation. This is especially true when driving the noninverting input from a source impedance of 50Ω, or less, while the output is shorted to the inverting input. Figure 3 shows a unity-gain circuit employing a parallel RC feedback network which is stable for values of $C_F < 68pF$. Another method to achieve unity-gain stability is to increase the source resistance at the noninverting input (Figure 4).



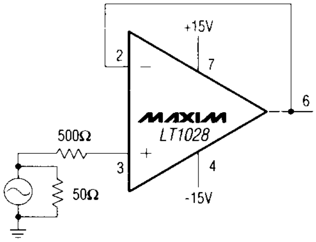
Pin Configuration for 8-Pin Package.

Figure 3. Source-Resistance Compensation

Stray input capacitance is another stability issue. All op amps have a certain amount of stray capacitance between inputs and each input and ground. Capacitance between the inverting input and ground is a frequent cause of instability. The stray capacitance and feedback network combine to create a pole that causes additional phase shift, but this shift can be canceled by connecting a capacitor in parallel with the feedback resistor (Figure 5).

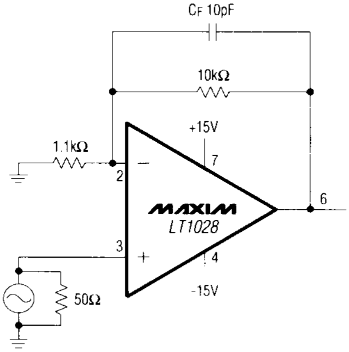
Over-Compensation

Some applications, like thermocouple amps, require low peak-to-peak voltage noise and minimum bandwidth. In these applications, use the over-compensation function to limit the noise bandwidth by connecting a capacitor between OUT and OVERCOMP. The over-compensation function enables operation under heavy capacitive load conditions. The details of gain-bandwidth product and slew rate versus the over-compensation capacitor are illustrated in the Typical Operating Characteristics section.



Pin Configuration for 8-Pin Package.

Figure 4. Unity-Gain Stability Through Increased Source Resistance



Pin Configuration for 8-Pin Package.

Figure 5. Compensation for Input Capacitance

Total Noise vs. Source Resistance

The industry-standard expression for the total input referred noise of a practical op amp is:

$e_t = \sqrt{e_n^2 + (R_p + R_n)^2 i_n^2 + 4kT(R_p + R_n)}$
R_n = Inverting input effective series resistance
R_p = Noninverting input effective series resistance
e_n = Input-noise voltage density
i_n = Input-noise current density
T = Ambient temperature in Kelvin (K)
$k = 1.38 \times 10^{-23}$j/K (Boltzman's constant)

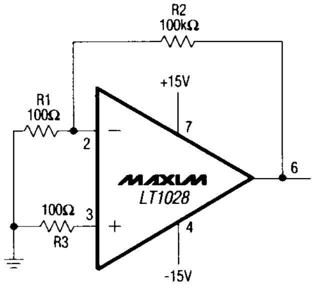
In Figure 6, R_p = R3 and R_n = R1//R2. Also, R_p and R_n must include the resistances of the input driving source(s), if any. The following example demonstrates how to calculate the LT1028's total noise at 1kHz from the circuit in Figure 6.

Gain = 1000
4kT at 25°C = $1.68 \times 10^{-20}V^2/\Omega Hz$
$R_p = 100\Omega$
$R_n = 100\Omega // 100k\Omega = 99.9\Omega$
$e_n = 0.85nV/\sqrt{Hz}$
$i_n = 1.0pA/\sqrt{Hz}$
$$e_t = [(0.85 \times 10^{-9})^2 + (100 + 99.9)^2 (1 \times 10^{-12})^2 + (1.68 \times 10^{-20})(100 + 99.9)]^{1/2} = 2.03\ nV/\sqrt{Hz}$$
Output noise = $(1000)e_n = 2.03\mu V/\sqrt{Hz}$

In general, the amplifier's voltage noise dominates with equivalent source resistances less than 40Ω. As the equivalent source resistance increases, resistor noise becomes the larger term, eventually making the voltage noise contribution from the LT1028 negligible. As the source resistance is further increased, current noise becomes dominant. For example, when the equivalent source resistance is greater than 20kΩ at 1kHz, the current-noise component is larger than the resistor noise. The graph of Total Noise vs. Matched-Source Resistance shows this phenomenon. Optimal LT1028 low-noise performance and minimum total noise is achieved with a source resistance < 400Ω.

Voltage-Noise Testing

The RMS noise density of the LT1028 is measured with the QuanTech Model 5173 Noise Analyzer, or equivalent. When analyzing op amp noise, subtract the noise contribution from the source resistor. The 0.1Hz to 10Hz peak-to-peak noise of the LT1028 is measured in the test circuit of Figure 7. Limit the test time for the 0.1Hz to 10Hz noise measurement to 10 sec., which eliminates noise contributions from frequencies less than 0.1Hz.



Pin Configuration for 8-Pin Package.

Figure 6. Total Noise vs. Source Resistance Example

When measuring the 35nVp-p noise (typical) of the LT1028 op amp, observe the following:
(1) 5 min. warmup
(2) Shield the device from air currents
(3) Avoid sudden movements in the vicinity of the device

Testing Current Noise

The current-noise density of the LT1028 for a 1Hz bandwidth is calculated using the industry-standard formula below. It is measured using the circuit in Figure 8 with the QuanTech Model 5173, or equivalent:

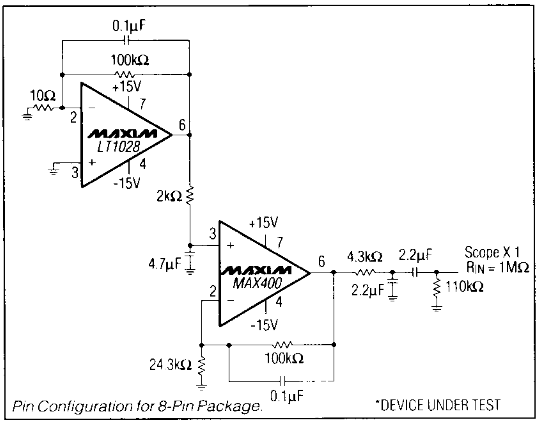
$$i_n = \frac{\sqrt{e_{no}^2 - [(A_{VCL})(4kT)(R_n + R_p)]^2}}{(R_n + R_p)A_{VCL}}$$

R_n = Inverting input effective series resistance
R_p = Noninverting input effective series resistance
e_{no} = Output-voltage noise
i_n = Input-current noise
A_{VCL} = Closed-loop gain
T = Ambient temperature in Kelvin (K)
$k = 1.38 \times 10^{-23}$j/K (Boltzman's constant)

R_p and R_n must include the resistances of the input driving source(s), if any. For the circuit in Figure 8, assuming R_p is approximately equal to R_n, the equation simplifies to:

$$i_n = \frac{\sqrt{e_{no}^2 - [(10\cdot1)(16\cdot6 \times 10^{-21})(20 \times 10^3)]^2}}{(20 \times 10^3)(10\cdot1)}$$

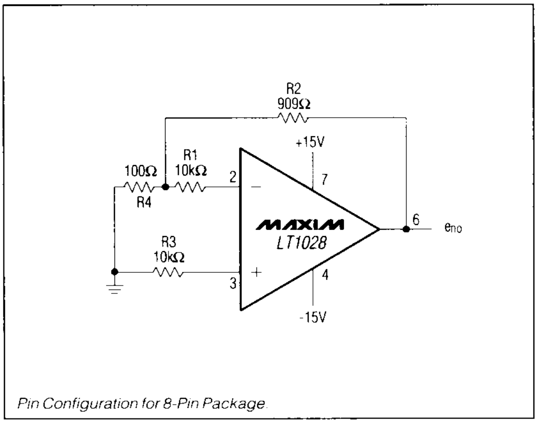
Ultra-Low Noise, High-Speed Precision Op Amp



Pin Configuration for 8-Pin Package.

*DEVICE UNDER TEST

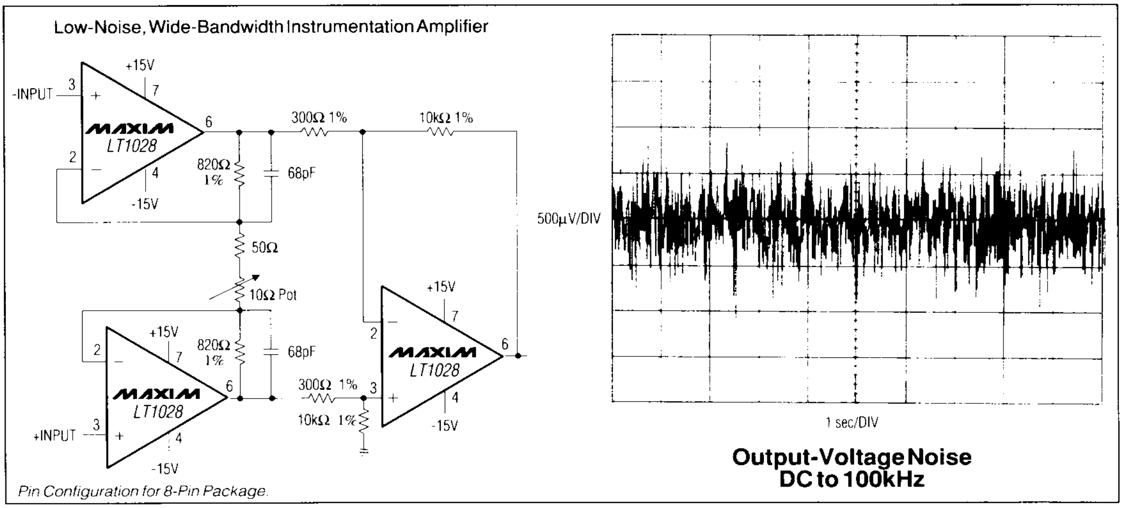
Figure 7. LT1028 0.1Hz to 10Hz Voltage-Noise Test Circuit



Pin Configuration for 8-Pin Package.

Figure 8. Current-Noise Test Circuit

Typical Applications

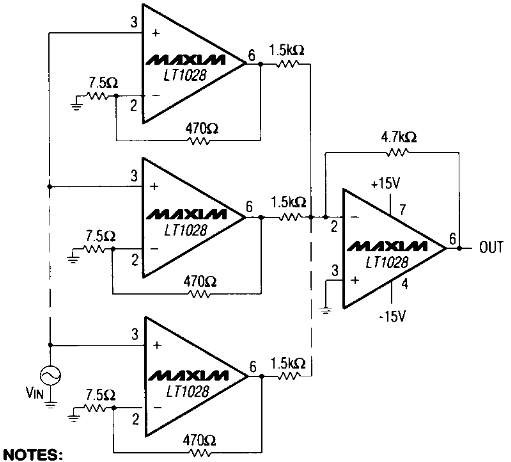

Low-Noise, Wide-Bandwidth Instrumentation Amplifier

Pin Configuration for 8-Pin Package.

**Output-Voltage Noise
DC to 100kHz**

Typical Applications (continued)

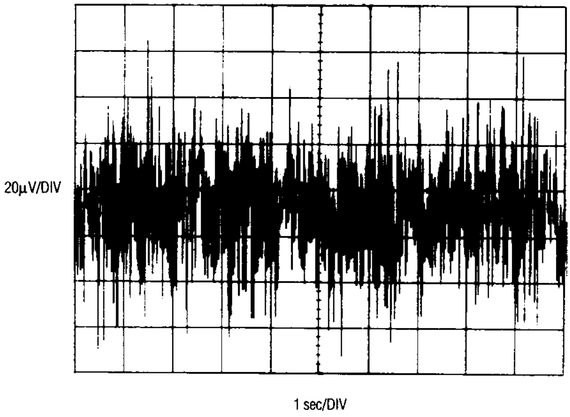
Reduced Voltage Noise by Paralleling Amplifiers



NOTES:

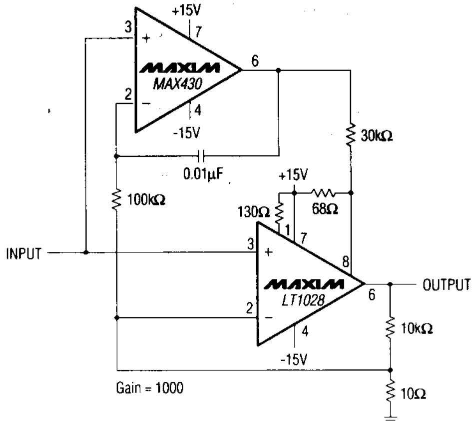
1. ASSUME VOLTAGE NOISE OF LT1028 AND 7.5Ω SOURCE RESISTOR = $0.9\text{nV}/\sqrt{\text{Hz}}$.
2. GAIN WITH n LT1028'S IN PARALLEL = n x 200.
3. OUTPUT NOISE = $\sqrt{n} \times 200 \times 0.9\text{nV}/\sqrt{\text{Hz}}$.
4. INPUT REFERRED NOISE = $\dfrac{\text{OUTPUT NOISE}}{n200} = \dfrac{0.9}{\sqrt{n}}\text{nV}/\sqrt{\text{Hz}}$
5. IF n = 3, GAIN = 600, BANDWIDTH = 1MHz,
   TOTAL INPUT REFERRED RMS NOISE = $\dfrac{0.9\text{nV}/\sqrt{\text{Hz}}}{\sqrt{3}}(1 \times 10^6\text{Hz})^{1/2} = 0.5\mu\text{V}$.

Pin Configuration for 8-Pin Package.

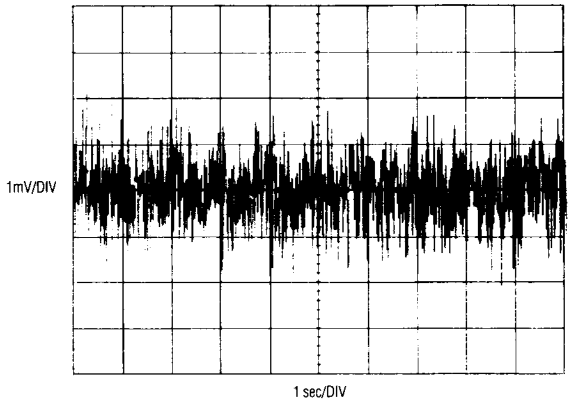


Output-Voltage Noise for Three Op Amps in Parallel DC to 100kHz

Low-Noise, Chopper-Stabilized Amplifier



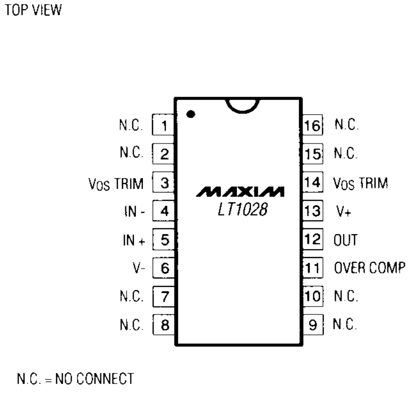
Pin Configuration for 8-Pin Package.



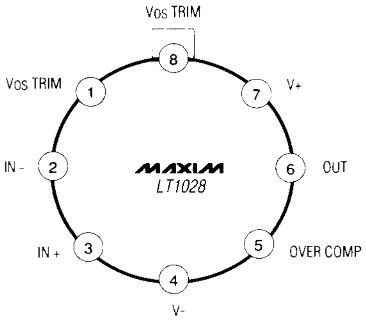
Output-Voltage Noise DC to 100kHz

Ultra-Low Noise, High-Speed Precision Op Amp

Pin Configurations (continued)



16-PIN WIDE SO



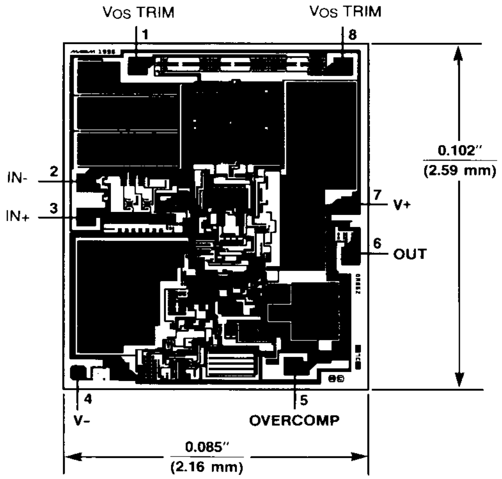
8-PIN TO-99 CAN

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
LT1028AEN8	-40°C to +85°C	8 Plastic DIP
LT1028EN8	-40°C to +85°C	8 Plastic DIP
LT1028AESA	-40°C to +85°C	8 SO
LT1028ESA	-40°C to +85°C	8 SO
LT1028AECS	-40°C to +85°C	16 Wide SO
LT1028ECS	-40°C to +85°C	16 Wide SO
LT1028AEH	-40°C to +85°C	8 TO-99 Can
LT1028EH	-40°C to +85°C	8 TO-99 Can
LT1028AMJ8	-55°C to +125°C	8 CERDIP**
LT1028MJ8	-55°C to +125°C	8 CERDIP**
LT1028AMH	-55°C to +125°C	8 TO-99 Can**
LT1028MH	-55°C to +125°C	8 TO-99 Can**

**Consult factory for processing to MIL-STD-883.

Chip Topography



NOTE: CONNECT SUBSTRATE TO V-.

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