8K x 8 CMOS SRAM

Features

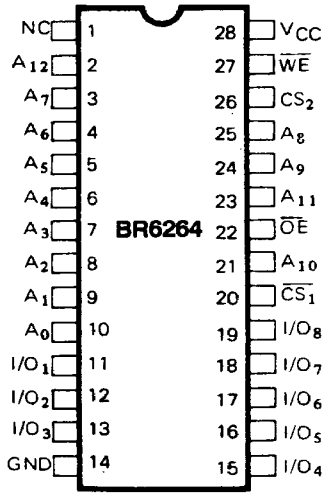
- High-speed 100/120 ns (Max.)
- Low power dissipation
  - Standard version: Operating 90mA Max. Standby 2mA Max.
  - Low power version: Operating 85mA Max. Standby 100µA Max.
- Single 5V power supply
- Fully static operation-no clock or refreshing required
- TTL compatible-all inputs and outputs
- Common I/O using three-state outputs
- Output enable and two chip enable inputs for easy application
- Data retention supply voltage: 2V Min. (BR6264-10L/12L)
- Standard 28-pin plastic DIP and SOP packages

General Description

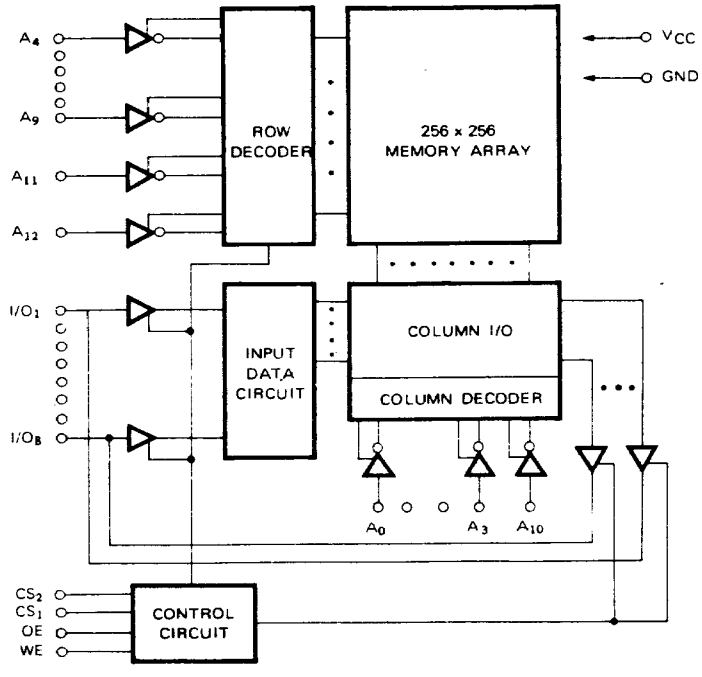
The BR6264 is a high-speed, low-power 65,536-bit static random access memory organized as 8,192 words by 8 bits and operates from a single 5 volt supply. It is built with ROHM's high performance twin tub CMOS process.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Two chip select inputs are provided for battery back-up application, and an OUTPUT ENABLE input is included for easy interface.
Data retention is guaranteed at a power supply voltage as low as 2V (BR6264-10L/12L)
The BR6264 is packaged in a standard 28-pin plastic dual-in-line package.
The BR6264F is packaged in a standard 28-pin plastic small outline IC package.

Pin Configurations



Block Diagram



Absolute Maximum Ratings*

Terminal Voltage with Respect to GND
. . . . . −0.5V to +7.0V
Temperature Under Bias . . . . . −10°C to +125°C
Storage Temperature . . . . . −40°C to +150°C
Power Dissipation 1.0W/SOP 0.7W
DC Output Current 20mA

Comments*

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Pin Name

No.	Symbol	Function
1	NC	No connection
2-10, 21, 23-25	A_0-A_{12}	Address input
11-13, 15-19	I/O_1-I/O_8	Data input/output
14	GND	Ground
20	$\overline{CS_1}$	Chip select input, active low
22	$\overline{OE}$	Output enable input
26	CS_2	Chip select input, active high
27	$\overline{WE}$	Write enable input
28	V_{CC}	+5V Power supply

Recommended DC Operating Conditions

(T_A=0 to +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5	0	0.8	V

DC Electrical Characteristics (V_{CC} = 5V ± 10%, GND = 0V, T_A = 0 to +70°C)

Symbol	Parameter	Test Conditions	BR6264-10 Min.	BR6264-10 Typ.*	BR6264-10 Max.
$\|I_{LI}\|$	Input Leakage Current	V_{IN} = GND to V_{CC}	–	–	2
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	–	–	2
I_{CC}	Operating Power Supply Current	$\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, $I_{I/O}$ = 0mA	–	50	90
I_{CC1}	Average Operating Current	Min. Duty Cycle = 100%, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}	–	50	90
I_{SB}	Standby Power Supply Current	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL}, $I_{I/O}$ = 0mA	–	–	15
I_{SB1}**		$\overline{CS_1}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V	–	–	2
I_{SB2}**		CS_2 ≤ 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V	–	–	2
V_{OL}	Output Voltage	I_{OL} = 4mA	–	–	0.4
V_{OH}		I_{OH} = −1.0mA	2.4	–	–

Symbol	BR6264-10L Min.	BR6264-10L Typ.*	BR6264-10L Max.	BR6264-12 Min.	BR6264-12 Typ.*	BR6264-12 Max.	BR6264-12L Min.	BR6264-12L Typ.*	BR6264-12L Max.	Unit
$\|I_{LI}\|$	–	–	2	–	–	2	–	–	2	μA
$\|I_{LO}\|$	–	–	2	–	–	2	–	–	2	μA
I_{CC}	–	45	85	–	50	90	–	45	85	mA
I_{CC1}	–	45	85	–	50	90	–	45	85	mA
I_{SB}	–	–	15	–	–	15	–	–	15	mA
I_{SB1}**	–	0.01	0.1	–	–	2	–	0.01	0.1	mA
I_{SB2}**	–	0.01	0.1	–	–	2	–	0.01	0.1	mA
V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	V
V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	V

* Typical limits are at V_{CC} = 5.0V, T_A = 25°C and specified loading.
** V_{IL} min = −0.3V

Truth Table

Mode	$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	I/O Operation	V_{CC} Current
Not Selected	X	H	X	X	High Z	I_{SB}, I_{SB1}
(Power Down)	X	X	L	X	High Z	I_{SB}, I_{SB2}
Output Disabled	H	L	H	H	High Z	I_{CC}, I_{CC1}
Read	H	L	H	L	D_{OUT}	I_{CC}, I_{CC1}
Write	L	L	H	X	D_{IN}	I_{CC}, I_{CC1}

Capacitance* (T_A = 25°C, f = 1.0MHZ)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

* This parameter is sampled and not 100% tested.

AC Test Conditions

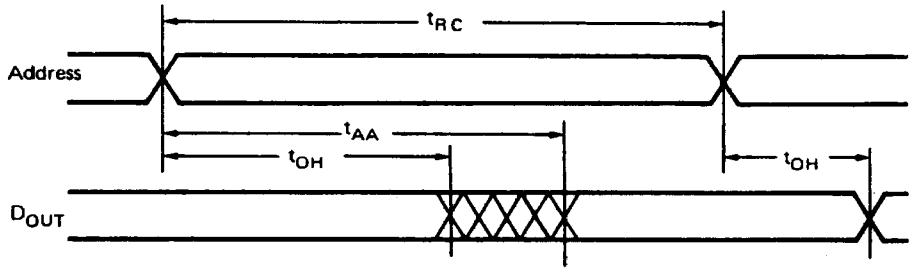
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Ouput Timing Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 30pF (including scope and jig)

AC Electrical Characteristics

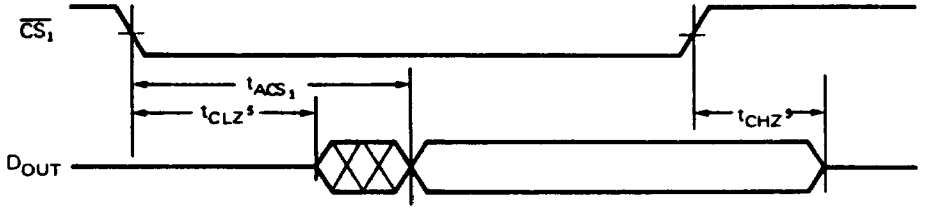
Symbol	Parameter		BR6264-10/10L Min.	BR6264-10/10L Max.	BR6264-12/12L Min.	BR6264-12/12L Max.	Unit
Read Cycle							
t_{RC}	Read Cycle Time		100	–	120	–	ns
t_{AA}	Address Access Time		–	100	–	120	ns
t_{ACS1}	Chip Select Access Time	$\overline{CS_1}$	–	100	–	120	ns
t_{ACS2}		CS_2	–	100	–	120	ns
t_{OE}	Output Enable to Output Valid		–	50	–	60	ns
t_{CLZ1}	Chip Selection to Output in Low Z	$\overline{CS_1}$	5	–	5	–	ns
t_{CLZ2}		CS_2	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z		5	–	5	–	ns
t_{CHZ1}	Chip Deselection to Output in High Z	$\overline{CS_1}$	0	35	0	40	ns
t_{CHZ2}		CS_2	0	35	0	40	ns
t_{OHZ}	Output Disable to Output in High Z		0	35	0	35	ns
t_{OH}	Output Hold from Address Change		5	–	5	–	ns
Write Cycle							
t_{WC}	Write Cycle Time		100	–	120	–	ns
t_{CW}	Chip Selection to End of Write		80	–	85	–	ns
t_{AS}	Address Setup Time		0	–	0	–	ns
t_{AW}	Address Valid to End of Write		80	–	85	–	ns
t_{WP}	Write Pulse Width		60	–	70	–	ns
t_{WR1}	Write Recovery Time	$\overline{CS_1}$, $\overline{WE}$	5	–	5	–	ns
t_{WR2}		CS_2	5	–	5	–	ns
t_{WHZ}	Write to Output in High Z		0	35	0	40	ns
t_{DW}	Data to Write Time Overlap		40	–	45	–	ns
t_{DH}	Data Hold from Write Time		5	–	5	–	ns
t_{OHZ}	Output Disable to Output in High Z		0	35	0	35	ns
t_{OW}	Output Active from End of Write		5	–	5	–	ns

NOTES: t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

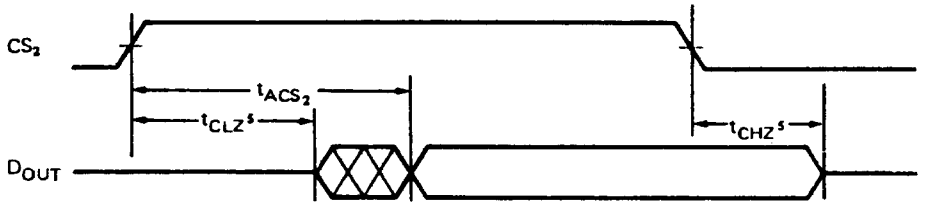
Timing Waveform of Read Cycle No. 1(1,2,4)



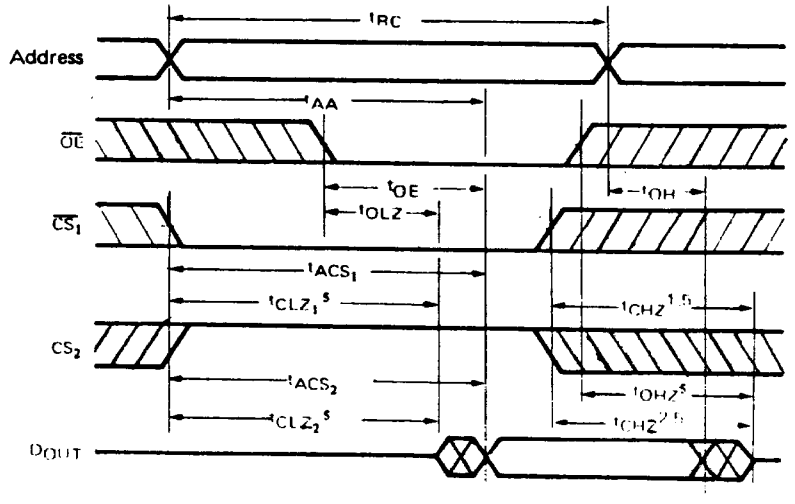
Read Cycle 2(1,3,4,6)



Read Cycle 3(1,4,7)

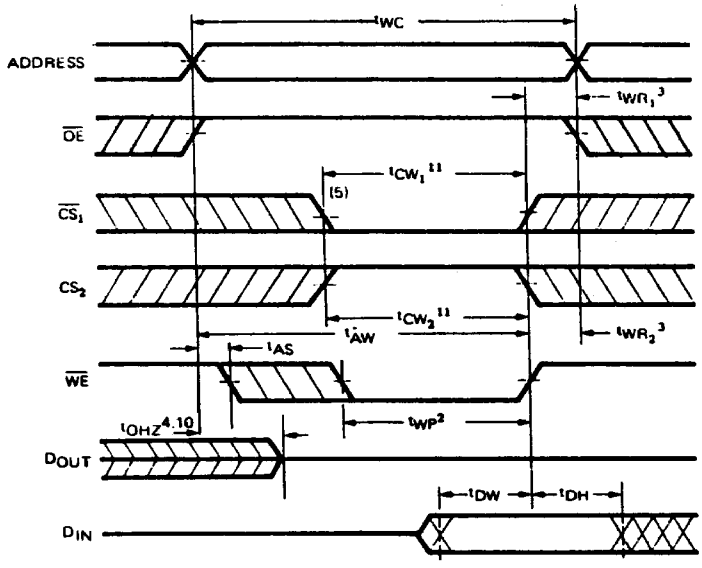


Read Cycle 4(1)

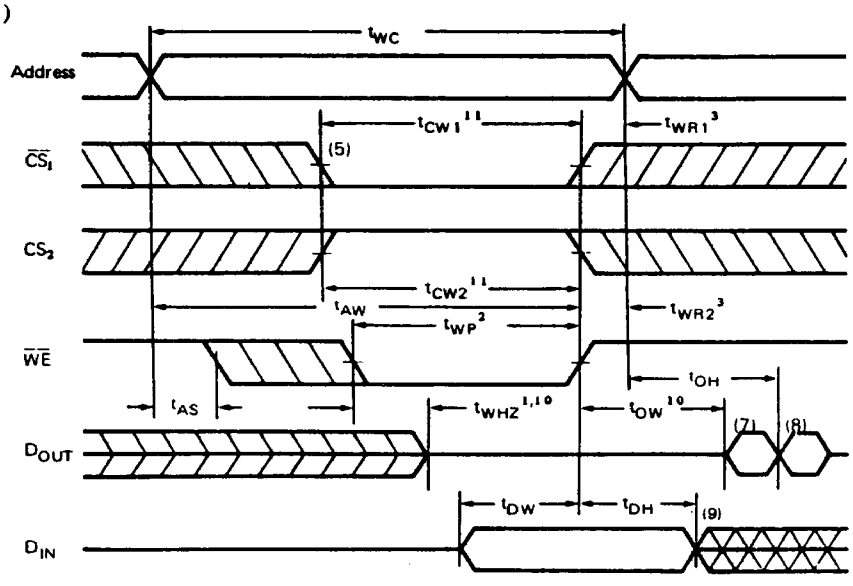


Notes: 1. $\overline{WE}$ is high for READ cycle.
2. Device is continuously selected $\overline{CS_1} = V_{IL}$ and $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS_1}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
6. CS_2 is high.
7. $\overline{CS_1}$ is low.

Timing Waveforms of Write Cycle 1(1)



Write Cycle 2(1,6)



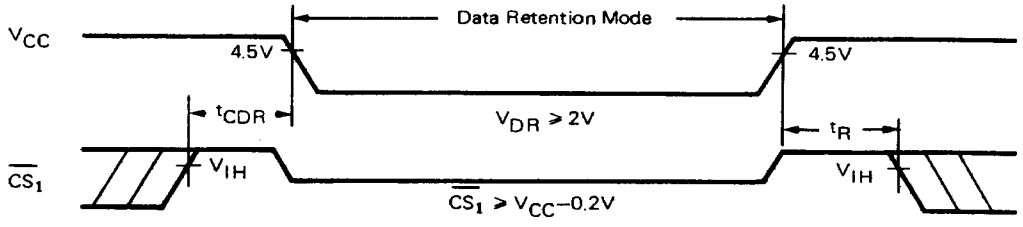
Notes:
1. $\overline{WE}$ must be high during address transitions.
2. A write occurs during the overlap (t_{wp}) of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS_1}$ low transition or the CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. if $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
11. t_{cw} is measured from the later of $\overline{CS_1}$ going low or CS_2 going high to the end of write.

Data Retention Characteristics (T_A = 0 to +70°C; L version only)

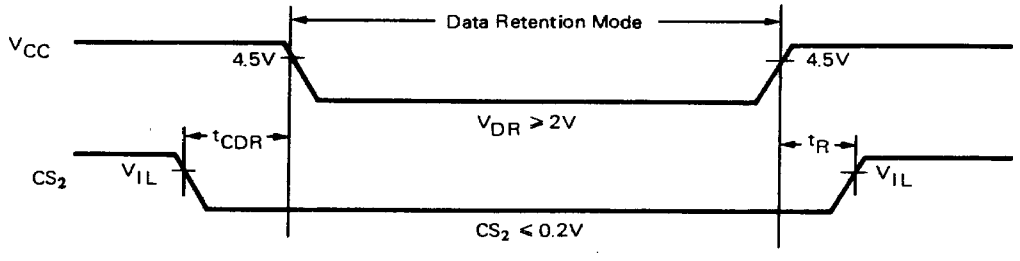
Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
V_{DR_1}	V_{CC} for Data Retention	$\overline{CS_1} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	–	–	V
V_{DR_2}		$CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	–	–	V
I_{CCDR_1}	Data Retention Current	$\overline{CS_1} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	–	2	50	μA
I_{CCDR_2}		$CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	–	2	50	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	–	–	ns
t_R	Operation Recovery Time		t_{RC}**	–	–	ns

* V_{CC} = 2V, T_A = +25°C
** t_{RC} = Read Cycle Time

Low V_{CC} Data Retention Waveform (1) ($\overline{CS_1}$ Controlled)



Low V_{CC} Data Retention Waveform (2) (CS_2 Controlled)

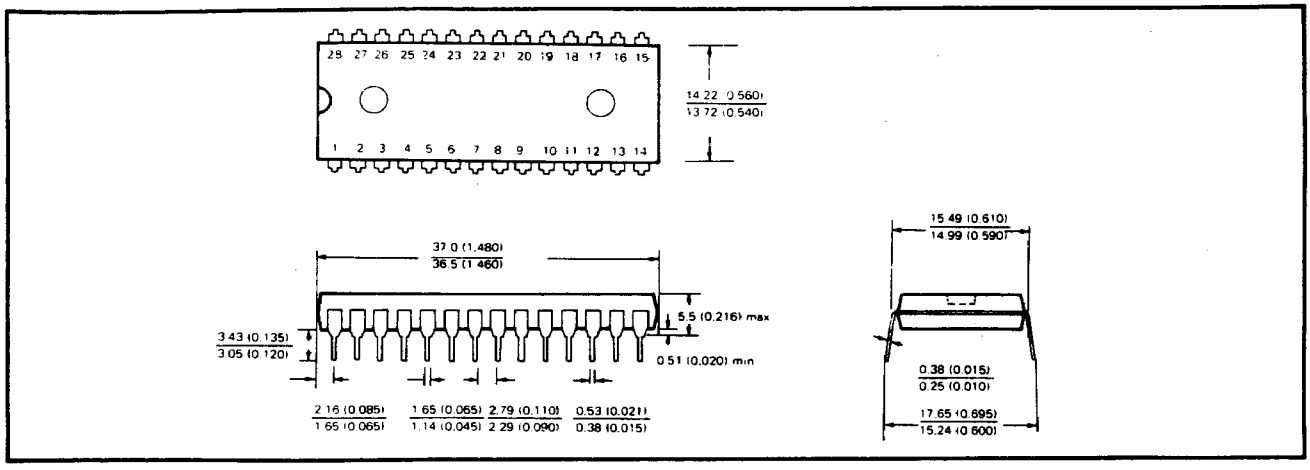


Ordering Information

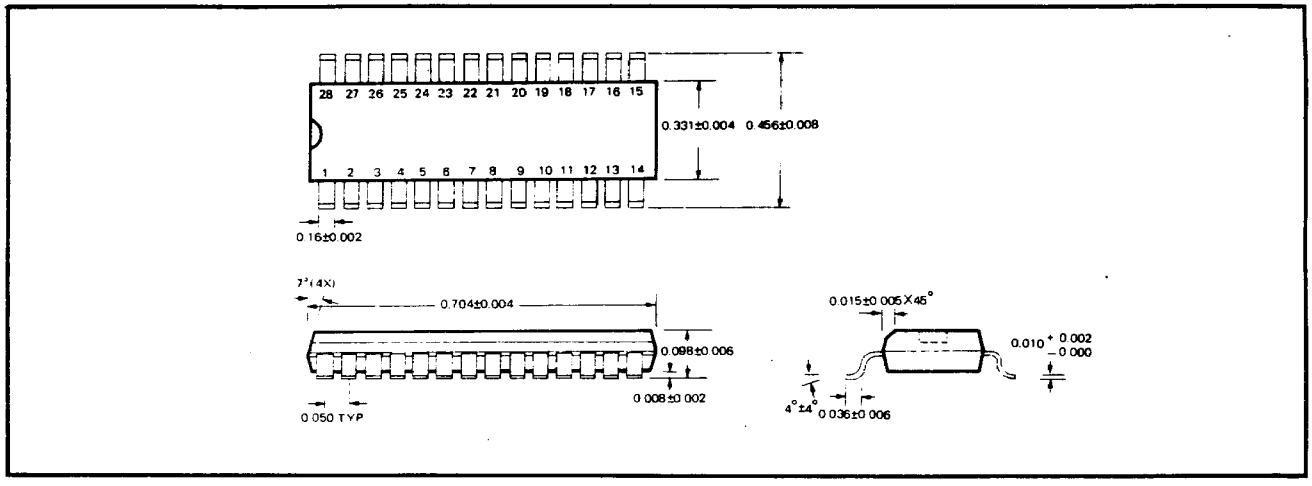
Access Time (ns)	Ordering Code	Operating Current Max. (mA)	Standby Current Max. (mA)	Package Type
100	BR6264-10	90	2	DIP-28
	BR6264-10L	85	0.1	DIP-28
	BR6264F-10L	85	0.1	SO-28
120	BR6264-12	90	2	DIP-28
	BR6264-12L	85	0.1	DIP-28
	BR6264F-12L	85	0.1	SO-28

Package Information — mm (inch)

28 LEAD DUAL IN-LINE; PLASTIC



28 Pin Small Outline Unit: mm (inch)



ROHM MEMORY PRODUCTS

Static RAM's

BR6116	2K x 8	CMOS SRAM
BR6116-100	2K x 8	CMOS SRAM (30 nsec typ.)
BR6264	8K x 8	CMOS SRAM
BR62256T	32K x 8	CMOS SRAM ON TAB

EEPROMs

BR2804A	512 x 8	4K	NMOS
BR2816A	2K x 8	16K	NMOS
BR2864A	8K x 8	64K	NMOS
BR93C46	64 x 16	1K	CMOS (Serial I/0, 5V only)
BR93CS46	64 x 16	1K	CMOS (Serial I/0, 3-5V)
BR46C15/16	2K x 8	16K	CMOS

Single In-Line DRAM Modules

BPD1000J-P9	1M x 9
BPD1000J-P8	1M x 8
BPD0256J-P9	256K x 9
BPD0256J-P8	256K x 8

Dual In-Line SRAM Modules

BPS41288P	128K x 8	CMOS

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