

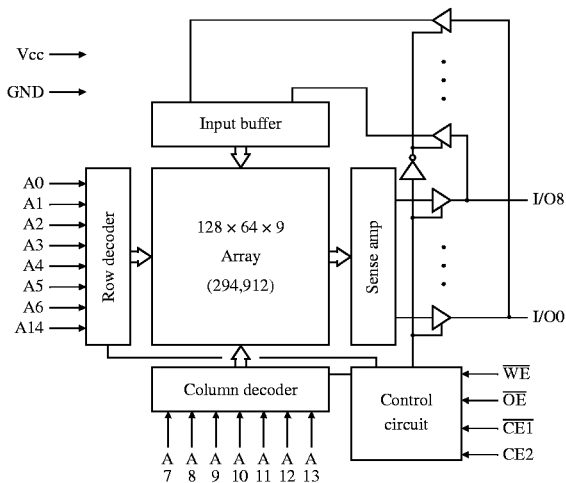
# 5V 32K×9 CMOS SRAM

## Features

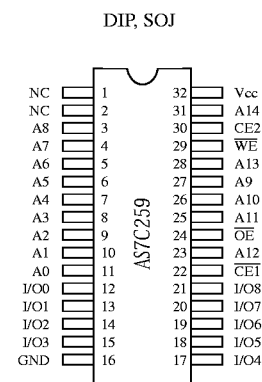
- Organization: 32,768 words × 9 bits
- High speed
  - 15/20/25 ns address access time
  - 4/5/6 ns output enable access time
- Low power consumption
  - Active: 633 mW max (10 ns cycle)
  - Standby: 11 mW max, CMOS I/O
  - Very low DC component in active power
- 2.0V data retention
- Equal access and cycle times
- Easy memory expansion with  $\overline{\text{CE1}}$ , CE2, and  $\overline{\text{OE}}$  inputs
- TTL-compatible, three-state I/O
- 32-pin JEDEC standard packages
  - 300 mil PDIP and SOJ
- ESD protection  $\geq 2000$  volts
- Latch-up current  $\geq 200$  mA

SRAM

## Logic block diagram

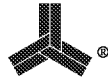


## Pin arrangement



## Selection guide

|                                   | 7C259-15 | 7C259-20 | 7C259-25 | Unit |
|-----------------------------------|----------|----------|----------|------|
| Maximum address access time       | 15       | 20       | 25       | ns   |
| Maximum output enable access time | 4        | 5        | 6        | ns   |
| Maximum operating current         | 110      | 100      | 90       | mA   |
| Maximum CMOS standby current      | 2.0      | 2.0      | 2.0      | mA   |



## Functional description

The AS7C259 is a high performance CMOS 294,912-bit Static Random Access Memory (SRAM) organized as 32,768 words × 9 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times ( $t_{AA}$ ,  $t_{RC}$ ,  $t_{WC}$ ) of 15/20/25 ns with output enable access times ( $t_{OE}$ ) of 4/5/6 ns are ideal for high performance applications. Active high and low chip enables ( $\overline{CE1}$ ,  $CE2$ ) permit easy memory expansion with multiple-bank memory systems.

When  $\overline{CE1}$  is High or  $CE2$  is Low the device enters standby mode. The standard AS7C259 is guaranteed not to exceed 11 mW power consumption in standby mode.

A write cycle is accomplished by asserting write enable ( $\overline{WE}$ ) and both chip enables ( $\overline{CE1}$ ,  $CE2$ ). Data on the input pins I/O0-I/O7 is written on the rising edge of  $\overline{WE}$  (write cycle 1) or the active-to-inactive edge of  $\overline{CE1}$  or  $CE2$  (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ( $\overline{OE}$ ) or write enable ( $\overline{WE}$ ).

A read cycle is accomplished by asserting output enable ( $\overline{OE}$ ) and both chip enables ( $\overline{CE1}$ ,  $CE2$ ), with write enable ( $\overline{WE}$ ) High. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply. The AS7C259 is packaged in common industry standard packages.

## Absolute maximum ratings

| Parameter                          | Symbol     | Min  | Max  | Unit |
|------------------------------------|------------|------|------|------|
| Voltage on any pin relative to GND | $V_t$      | -0.5 | +7.0 | V    |
| Power dissipation                  | $P_D$      | –    | 1.0  | W    |
| Storage temperature (plastic)      | $T_{stg}$  | -55  | +150 | °C   |
| Temperature under bias             | $T_{bias}$ | -10  | +85  | °C   |
| DC output current                  | $I_{out}$  | –    | 20   | mA   |

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Truth table

| $\overline{CE1}$ | $CE2$ | $\overline{WE}$ | $\overline{OE}$ | Data      | Mode                             |
|------------------|-------|-----------------|-----------------|-----------|----------------------------------|
| H                | X     | X               | X               | High Z    | Standby ( $I_{SB}$ , $I_{SB1}$ ) |
| X                | L     | X               | X               | High Z    | Standby ( $I_{SB}$ , $I_{SB1}$ ) |
| L                | H     | H               | H               | High Z    | Output disable                   |
| L                | H     | H               | L               | $D_{out}$ | Read                             |
| L                | H     | L               | X               | $D_{in}$  | Write                            |

Key: X = Don't Care, L = Low, H = High

## Recommended operating conditions

( $T_a = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

| Parameter      | Symbol   | Min               | Typ | Max          | Unit |
|----------------|----------|-------------------|-----|--------------|------|
| Supply voltage | $V_{CC}$ | 4.5               | 5.0 | 5.5          | V    |
|                | GND      | 0.0               | 0.0 | 0.0          | V    |
| Input voltage  | $V_{IH}$ | 2.2               | –   | $V_{CC}+1.0$ | V    |
|                | $V_{IL}$ | -0.5 <sup>†</sup> | –   | 0.8          | V    |

<sup>†</sup> $V_{IL}$  min = -3.0V for pulse width less than  $t_{RC}/2$ .

DC operating characteristics <sup>1</sup>(V<sub>CC</sub> = 5V±10%, GND = 0V, T<sub>a</sub> = 0°C to +70°C)

| Parameter                      | Symbol           | Test conditions                                                                                                           | -15 |     | -20 |     | -25 |     | Unit |
|--------------------------------|------------------|---------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|------|
|                                |                  |                                                                                                                           | Min | Max | Min | Max | Min | Max |      |
| Input leakage current          | I <sub>LI</sub>  | V <sub>CC</sub> = Max, V <sub>in</sub> = GND to V <sub>CC</sub>                                                           | –   | 1   | –   | 1   | –   | 1   | μA   |
| Output leakage current         | I <sub>LO</sub>  | $\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub> , V <sub>CC</sub> = Max, V <sub>out</sub> = GND to V <sub>CC</sub>     | –   | 1   | –   | 1   | –   | 1   | μA   |
| Operating power supply current | I <sub>CC</sub>  | $\overline{CE1} = V_{IL}$ , CE2 = V <sub>IH</sub> , f = f <sub>max</sub> , I <sub>out</sub> = 0 mA                        | –   | 110 | –   | 100 | –   | 90  | mA   |
| Standby power supply current   | I <sub>SB</sub>  | $\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub> , f = f <sub>max</sub>                                                 | –   | 30  | –   | 30  | –   | 25  | mA   |
|                                | I <sub>SB1</sub> | $\overline{CE1} \geq V_{CC}-0.2V$ or CE2 ≤ 0.2V, V <sub>in</sub> ≤ 0.2V or V <sub>in</sub> ≥ V <sub>CC</sub> -0.2V, f = 0 | –   | 2.0 | –   | 2.0 | –   | 2.0 | mA   |
| Output voltage                 | V <sub>OL</sub>  | I <sub>OL</sub> = 8 mA, V <sub>CC</sub> = Min                                                                             | –   | 0.4 | –   | 0.4 | –   | 0.4 | V    |
|                                | V <sub>OH</sub>  | I <sub>OH</sub> = -4 mA, V <sub>CC</sub> = Min                                                                            | 2.4 | –   | 2.4 | –   | 2.4 | –   | V    |

Capacitance <sup>2</sup>(f = 1 MHz, T<sub>a</sub> = room temperature, V<sub>CC</sub> = 5V)

| Parameter         | Symbol           | Signals                                                      | Test conditions                         | Max | Unit |
|-------------------|------------------|--------------------------------------------------------------|-----------------------------------------|-----|------|
| Input capacitance | C <sub>IN</sub>  | A, $\overline{CE1}$ , CE2, $\overline{WE}$ , $\overline{OE}$ | V <sub>in</sub> = 0V                    | 5   | pF   |
| I/O capacitance   | C <sub>I/O</sub> | I/O                                                          | V <sub>in</sub> = V <sub>out</sub> = 0V | 7   | pF   |

Read cycle <sup>3,9,12</sup>(V<sub>CC</sub> = 5V±10%, GND = 0V, T<sub>a</sub> = 0°C to +70°C)

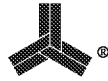
| Parameter                                     | Symbol            | -15 |     | -20 |     | -25 |     | Unit | Notes    |
|-----------------------------------------------|-------------------|-----|-----|-----|-----|-----|-----|------|----------|
|                                               |                   | Min | Max | Min | Max | Min | Max |      |          |
| Read cycle time                               | t <sub>RC</sub>   | 15  | –   | 20  | –   | 25  | –   | ns   |          |
| Address access time                           | t <sub>AA</sub>   | –   | 15  | –   | 20  | –   | 25  | ns   | 3        |
| Chip enable ( $\overline{CE1}$ ) access time  | t <sub>ACE1</sub> | –   | 15  | –   | 20  | –   | 25  | ns   | 3, 12    |
| Chip enable (CE2) access time                 | t <sub>ACE2</sub> | –   | 15  | –   | 20  | –   | 25  | ns   | 3, 12    |
| Output enable ( $\overline{OE}$ ) access time | t <sub>OE</sub>   | –   | 4   | –   | 5   | –   | 6   | ns   |          |
| Output Hold from address change               | t <sub>OH</sub>   | 3   | –   | 3   | –   | 3   | –   | ns   | 5        |
| $\overline{CE1}$ Low to Output in Low Z       | t <sub>CLZ1</sub> | 3   | –   | 3   | –   | 3   | –   | ns   | 4, 5, 12 |
| CE2 High to Output in Low Z                   | t <sub>CLZ2</sub> | 3   | –   | 3   | –   | 3   | –   | ns   | 4, 5, 12 |
| $\overline{CE1}$ High to Output in High Z     | t <sub>CHZ1</sub> | –   | 4   | –   | 5   | –   | 6   | ns   | 4, 5, 12 |
| CE2 Low to Output in High Z                   | t <sub>CHZ2</sub> | –   | 4   | –   | 5   | –   | 6   | ns   | 4, 5, 12 |
| $\overline{OE}$ Low to Output in Low Z        | t <sub>OLZ</sub>  | 0   | –   | 0   | –   | 0   | –   | ns   | 4, 5     |
| $\overline{OE}$ High to Output in High Z      | t <sub>OHZ</sub>  | –   | 4   | –   | 5   | –   | 6   | ns   | 4, 5     |
| Power up time                                 | t <sub>PU</sub>   | 0   | –   | 0   | –   | 0   | –   | ns   | 4, 5, 12 |
| Power down time                               | t <sub>PD</sub>   | –   | 15  | –   | 20  | –   | 25  | ns   | 4, 5, 12 |

## Key to switching waveforms

Rising input

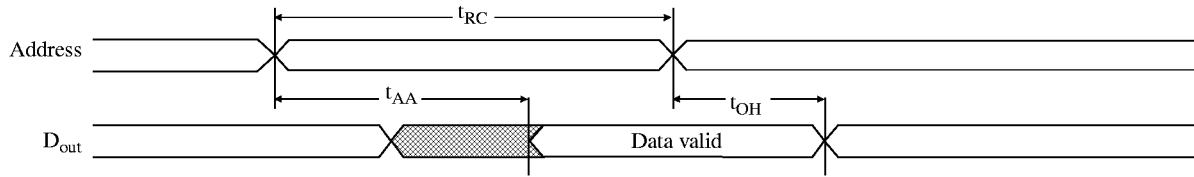
Falling input

Undefined output/don't care

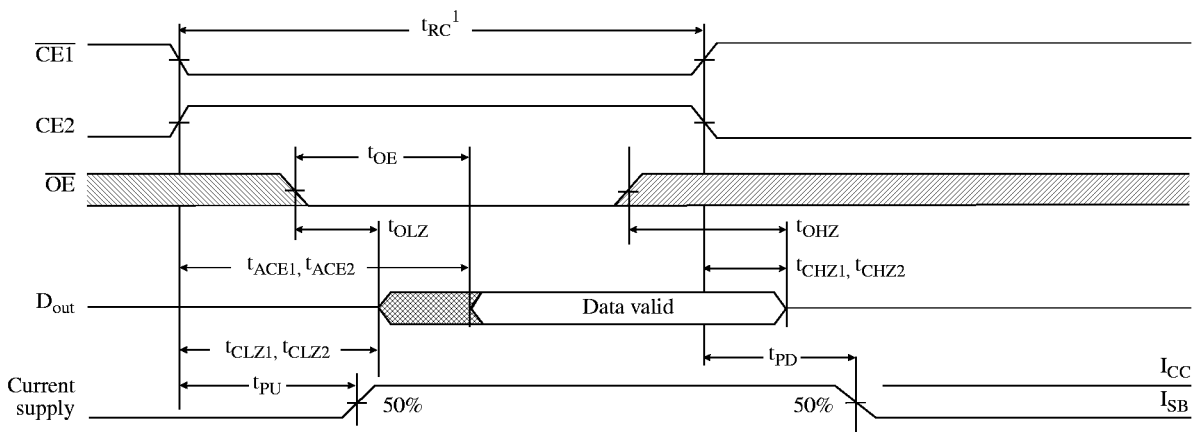


Read waveform 1 3,6,7,9,12

Address controlled



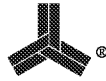
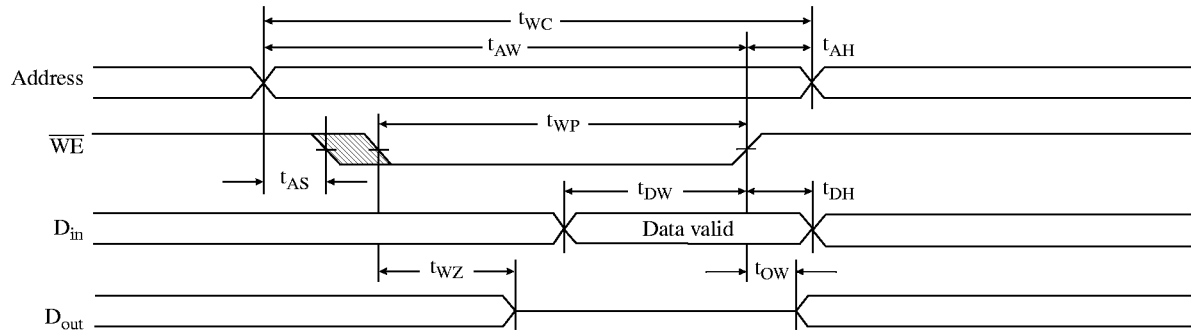
Read waveform 2 3,6,8,9,12

 $\overline{CE1}$  and CE2 controlled

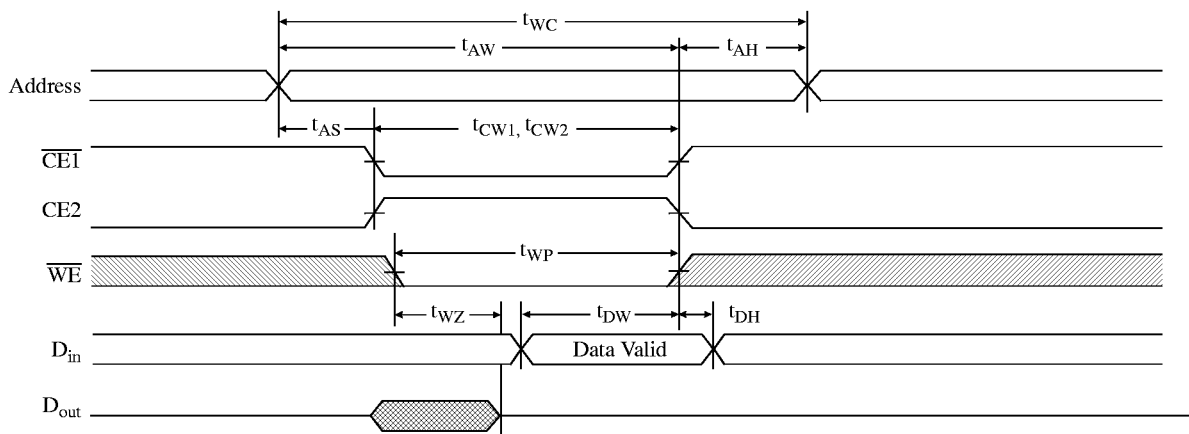
Write cycle 11,12

 $(V_{CC} = 5V \pm 10\%, GND = 0V, T_a = 0^\circ C \text{ to } +70^\circ C)$ 

| Parameter                                     | Symbol    | -15 |     | -20 |     | -25 |     | Unit | Notes |
|-----------------------------------------------|-----------|-----|-----|-----|-----|-----|-----|------|-------|
|                                               |           | Min | Max | Min | Max | Min | Max |      |       |
| Write cycle time                              | $t_{WC}$  | 15  | –   | 20  | –   | 20  | –   | ns   |       |
| Chip enable ( $\overline{CE1}$ ) to write end | $t_{CW1}$ | 12  | –   | 12  | –   | 15  | –   | ns   | 12    |
| Chip enable (CE2) to write end                | $t_{CW2}$ | 12  | –   | 12  | –   | 15  | –   | ns   | 12    |
| Address setup to write end                    | $t_{AW}$  | 12  | –   | 12  | –   | 15  | –   | ns   |       |
| Address setup time                            | $t_{AS}$  | 0   | –   | 0   | –   | 0   | –   | ns   | 12    |
| Write pulse width                             | $t_{WP}$  | 9   | –   | 12  | –   | 15  | –   | ns   |       |
| Address hold from end of write                | $t_{AH}$  | 0   | –   | 0   | –   | 0   | –   | ns   |       |
| Data valid to write end                       | $t_{DW}$  | 8   | –   | 10  | –   | 10  | –   | ns   |       |
| Data hold time                                | $t_{DH}$  | 0   | –   | 0   | –   | 0   | –   | ns   | 4, 5  |
| Write enable to output in High Z              | $t_{WZ}$  | –   | 5   | –   | 5   | –   | 5   | ns   | 4, 5  |
| Output active from write end                  | $t_{OW}$  | 3   | –   | 3   | –   | 3   | –   | ns   | 4, 5  |

Write waveform 1 *10,11,12* $\overline{WE}$  controlled

SRAM

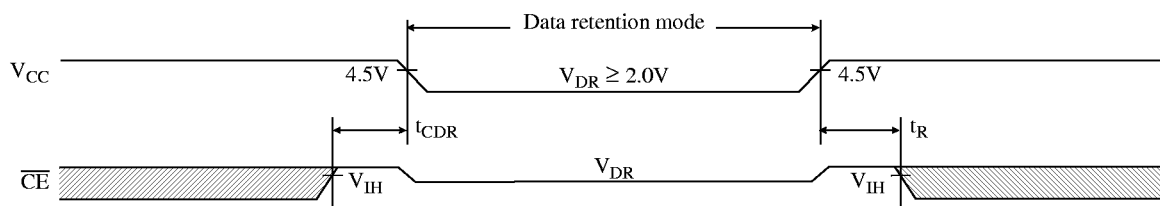
Write waveform 2 *10,11,12* $\overline{CE1}$  and CE2 controlled



## Data retention characteristics

| Parameter                            | Symbol     | Test conditions                                         | Min      | Max | Unit    |
|--------------------------------------|------------|---------------------------------------------------------|----------|-----|---------|
| $V_{CC}$ for data retention          | $V_{DR}$   | $V_{CC} = 2.0V$                                         | 2.0      | –   | V       |
| Data retention current               | $I_{CCDR}$ | $\overline{CE1} \geq V_{CC}-0.2V$ or<br>$CE2 \leq 0.2V$ | –        | 150 | $\mu A$ |
| Chip deselect to data retention time | $t_{CDR}$  |                                                         | 0        | –   | ns      |
| Operation recovery time              | $t_R$      | $V_{in} \geq V_{CC}-0.2V$ or<br>$V_{in} \leq 0.2V$      | $t_{RC}$ | –   | ns      |
| Input leakage current                | $ I_{II} $ |                                                         | –        | 1   | $\mu A$ |

## Data retention waveform



## AC test conditions

- Output load: see Figure B, except for  $t_{CLZ}$  and  $t_{CHZ}$  see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

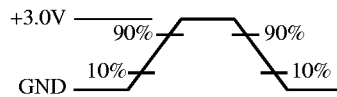


Figure A: Input waveform

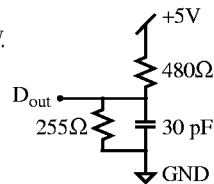
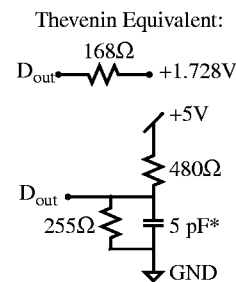


Figure B: Output load

Figure C: Output load for  $t_{CLZ}$ ,  $t_{CHZ}$ 

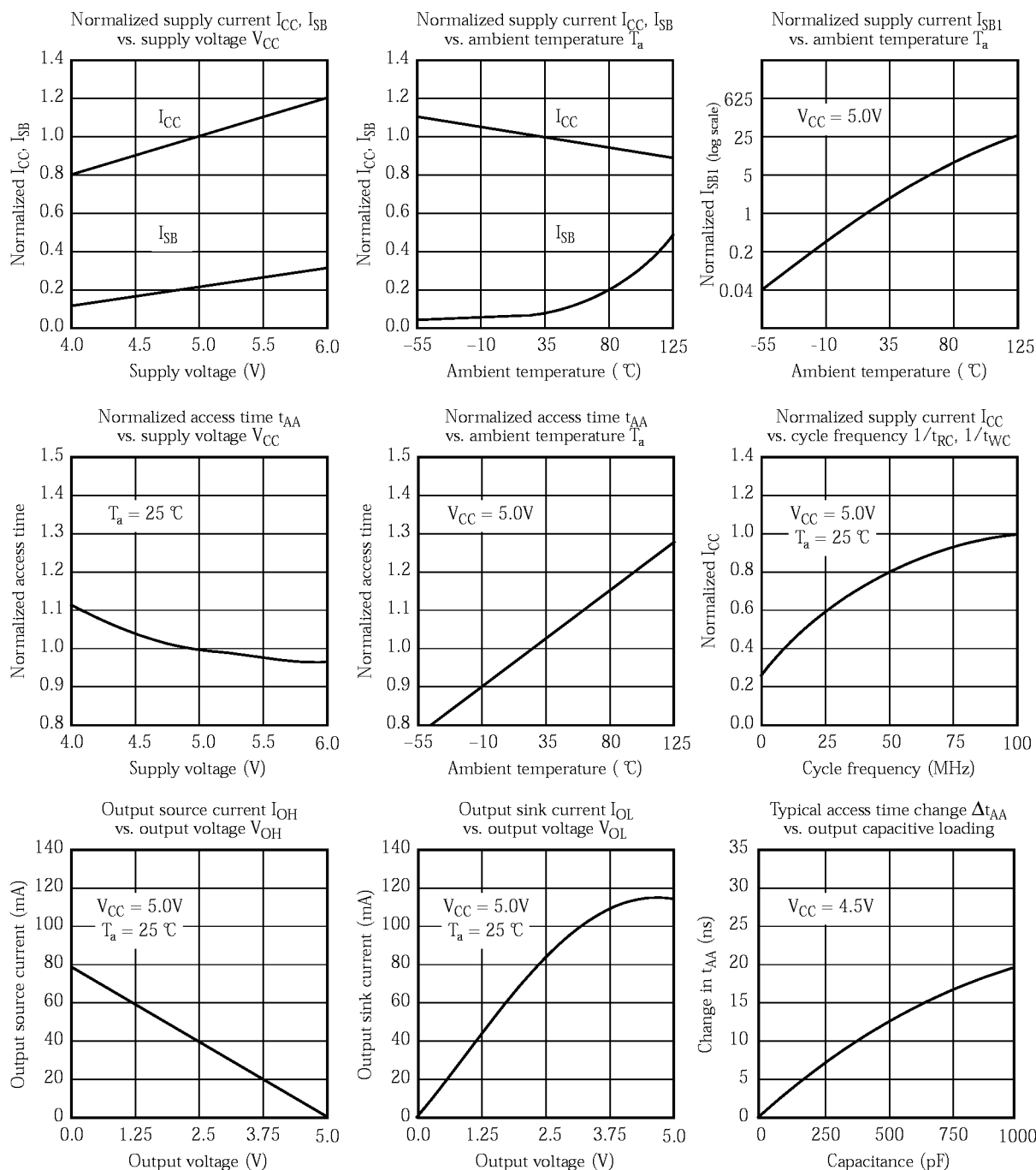
\*including scope and jig capacitance

## Notes

- 1 During  $V_{CC}$  power-up, a pull-up resistor to  $V_{CC}$  on  $\overline{CE1}$  is required to meet  $I_{SS}$  specification.
- 2 This parameter is sampled and not 100% tested.
- 3 For test conditions, see AC Test Conditions, Figures A, B, C.
- 4  $t_{CLZ}$  and  $t_{CHZ}$  are specified with  $CL = 5pF$  as in Figure C. Transition is measured  $\pm 500mV$  from steady-state voltage.
- 5 This parameter is guaranteed but not tested.
- 6  $\overline{WE}$  is High for read cycle.
- 7  $\overline{CE1}$  and  $\overline{OE}$  are Low and  $CE2$  is High for read cycle.
- 8 Address valid prior to or coincident with  $\overline{CE}$  transition Low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10  $\overline{CE1}$  or  $\overline{WE}$  must be High or  $CE2$  Low during address transitions.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12  $\overline{CE1}$  and  $CE2$  have identical timing.



# Typical AC and DC characteristics



SRAM

AS7C259



AS7C259 ordering codes

| Package / Access Time | 15 ns        | 20 ns        | 25 ns        |
|-----------------------|--------------|--------------|--------------|
| Plastic DIP, 300 mil  | AS7C259-15PC | AS7C259-20PC | AS7C259-25PC |
| Plastic SOJ, 300 mil  | AS7C259-15JC | AS7C259-20JC | AS7C259-25JC |

Shaded areas contain advance information.

AS7C259 part numbering system

|             |               |             |                                                              |                                             |
|-------------|---------------|-------------|--------------------------------------------------------------|---------------------------------------------|
| AS7C        | 256           | -XX         | X                                                            | C                                           |
| SRAM prefix | Device number | Access time | Package:P = PDIP 300 mil<br>J = SOJ 300 mil<br>T = TSOP 8x14 | Commercial temperature range, 0 °C to 70 °C |

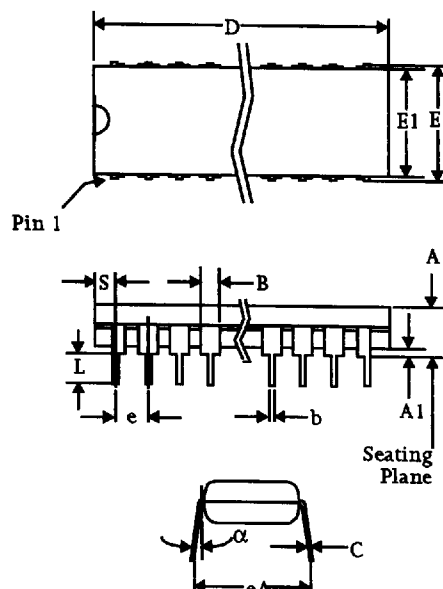




## Plastic dual in-line package (PDIP)

|          | 20-pin<br>300 mil |       | 28-pin<br>300 mil |       | 32-pin<br>300 mil |       | 32-pin<br>400 mil |       |
|----------|-------------------|-------|-------------------|-------|-------------------|-------|-------------------|-------|
|          | Min               | Max   | Min               | Max   | Min               | Max   | Min               | Max   |
| A        | -                 | 0.175 | -                 | 0.175 | -                 | 0.180 | -                 | 0.200 |
| A1       | 0.010             | -     | 0.010             | -     | 0.015             | -     | 0.015             | -     |
| B        | 0.046             | 0.054 | 0.058             | 0.064 | 0.045             | 0.055 | 0.045             | 0.065 |
| b        | 0.018             | 0.024 | 0.016             | 0.022 | 0.015             | 0.021 | 0.014             | 0.022 |
| C        | 0.008             | 0.014 | 0.008             | 0.014 | 0.008             | 0.012 | 0.009             | 0.015 |
| D        | -                 | 0.980 | -                 | 1.400 | -                 | 1.571 | -                 | 1.620 |
| E        | 0.290             | 0.310 | 0.295             | 0.320 | 0.300             | 0.325 | 0.390             | 0.425 |
| E1       | 0.263             | 0.293 | 0.278             | 0.298 | 0.280             | 0.295 | 0.340             | 0.390 |
| e        | 0.100 BSC         |       | 0.100 BSC         |       | 0.100 BSC         |       | 0.100 BSC         |       |
| eA       | 0.310             | 0.350 | 0.330             | 0.370 | 0.330             | 0.370 | 0.430             | 0.470 |
| L        | 0.110             | 0.130 | 0.120             | 0.140 | 0.110             | 0.142 | 0.118             | 0.162 |
| $\alpha$ | 0°                | 15°   | 0°                | 15°   | 0°                | 15°   | 0°                | 15°   |
| S        | -                 | 0.040 | -                 | 0.055 | -                 | 0.043 | -                 | 0.065 |

Dimensions in inches



## Plastic small outline J-bend (SOJ)

|    | 20/26-pin<br>300 mil |       | 28-pin<br>300 mil |       | 32-pin<br>300 mil |       | 28-pin<br>400 mil |       | 32-pin<br>400 mil |       | 36-pin<br>400 mil |       | 40-pin<br>400 mil |       | 42-pin<br>400 mil |           | 44-pin<br>400 mil |           |
|----|----------------------|-------|-------------------|-------|-------------------|-------|-------------------|-------|-------------------|-------|-------------------|-------|-------------------|-------|-------------------|-----------|-------------------|-----------|
|    | Min                  | Max   | Min               | Max   | Min               | Max   | Min               | Max   | Min               | Max   | Min               | Max   | Min               | Max   | Min               | Max       | Min               | Max       |
| A  | -                    | 0.140 | -                 | 0.140 | -                 | 0.145 | 0.132             | 0.146 | -                 | 0.145 | -                 | -     | -                 | 0.145 | 0.128             | 0.148     | 0.128             | 0.148     |
| A1 | 0.020                | -     | 0.025             | -     | 0.025             | -     | 0.062             | -     | 0.025             | -     | -                 | -     | 0.025             | -     | 0.025             | -         | 0.025             | -         |
| A2 | 0.095                | 0.105 | 0.095             | 0.105 | 0.086             | 0.105 | 0.105             | 115   | 0.086             | 0.115 | 0.102 NOM         |       | 0.086             | 0.115 | 1.105             | 1.115     | 1.105             | 1.115     |
| B  | 0.025                | 0.032 | 0.028 TYP         | 0.026 | 0.032             | 0.024 | 0.032             | 0.026 | 0.032             | -     | 0.032             | 0.026 | 0.032             | 0.026 | 0.032             | 0.026     | 0.032             | 0.026     |
| b  | 0.016                | 0.022 | 0.018 TYP         | 0.014 | 0.020             | 0.013 | 0.021             | 0.015 | 0.020             | 0.013 | 0.021             | 0.015 | 0.022             | 0.015 | 0.020             | 0.015     | 0.020             | 0.015     |
| c  | 0.008                | 0.014 | 0.010 TYP         | 0.006 | 0.013             | 0.005 | 0.012             | 0.007 | 0.013             | -     | -                 | 0.007 | 0.014             | 0.007 | 0.013             | 0.007     | 0.013             | 0.007     |
| D  | -                    | 0.686 | -                 | 0.730 | 0.820             | 0.830 | 0.720             | 0.729 | 0.820             | 0.830 | 0.920             | 0.930 | 1.015             | 1.035 | 1.070             | 1.080     | 1.120             | 1.130     |
| E  | 0.327                | 0.347 | 0.327             | 0.347 | 0.330             | 0.340 | 0.430             | 0.440 | 0.435             | 0.445 | 0.350             | 0.390 | 0.435             | 0.445 | 0.370 NOM         | 0.370 NOM | 0.370 NOM         | 0.370 NOM |
| E1 | 0.295                | 0.305 | 0.295             | 0.305 | 0.292             | 0.305 | 0.395             | 0.405 | 0.395             | 0.405 | 0.400 NOM         |       | 0.395             | 0.405 | 0.395             | 0.405     | 0.395             | 0.405     |
| E2 | 0.245                | 0.285 | 0.245             | 0.285 | 0.250             | 0.275 | 0.354             | 0.378 | 0.360             | 0.380 | 0.435             | 0.445 | 0.348             | 0.390 | 0.435             | 0.445     | 0.435             | 0.445     |
| e  | 0.050 BSC            |       | 0.050 BSC         |       | 0.050 BSC         |       | 0.050 BSC         |       | 0.050 BSC         |       | 0.045             | 0.055 | 0.050 BSC         |       | 0.050 NOM         |           | 0.050 NOM         |           |

Dimensions in inches

