PM7324

S/UNI-ATLAS

SATURN USER NETWORK INTERFACE ATM LAYER SOLUTION

DATASHEET

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PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	Sep., 1997	Initial release
2	Nov., 1997	Revised F4toF5 AIS processing and numerous other clarifications and expanded descriptions.
3	Feb., 1998	Updated the Ingress and Egress VC Tables to include room for Segment Defect Location and Defect Type fields. Also included GFR policing. Modified PM internal RAM to 80-bits wide to include support for I.356 measurement requirements.
4	Oct., 1998	Updated VC Table and Register Addresses. Included 432SBGA package drawing. Enhanced description of OAM processing, GFR policing, per-PHY policing, etc.
5	Jan., 1999	Removed “Proprietary and Confidential”. No content change.
6	Sep., 1999	Aligns with Revision C
7	Jan., 2000	Corrected Reliability Calculations. Corrected Block Diagram to reflect correct ingress/egress backward cell interface block positions. Modified RPOLL, IPOLL and TPOLL pin descriptions. Table 37 – Added V_{OH} specification. Table 38 – Changed the timing specification to become “Typical” for tSALR, tHALR, tSLR, tHLR. Table 40 – Changed IAVALID setup and hold times (t_{setup} and t_{hold}) to become “Typical”. Table 40-45 – Changed Min CLK Frequency for RFCLK, TFCLK, IFCLK, OFCLK, ISYSCLK, ESYSCLK. Table 40-43 – Changed Utopia input hold times for IWRENB[4:1], IAVALID, IADDR[4:0], IDAT[15:0], IPRTY, ISOC, ORDENB, RPRTY, RDAT[15:0], RCA[4:1], RSOC and TCA[4:1]. Table 40, 44, 45 – Changed prop delay times for ICA[4:1], ISD[63:0], ISP[7:0], ESD[31:0] and ESP[3:0].

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1 FEATURES

Point form summary of features.

- Monolithic single chip device which handles bi-directional ATM Layer functions including VPI/VCI address translation, cell appending (ingress only), cell rate policing (ingress only), per-connection counting and I.610 compliant OAM requirements for 65536 VCs (virtual connections).

- Instantaneous bi-directional transfer rate of 800 Mbit/s supports a bi-directional cell transfer rate of $1.42x10^6$ cells/s (one STS-12c or four STS-3c).

- The Ingress input interface supports an 8 or 16 bit SCI-PHY interface using direct addressing for up to 4 PHY devices (compatible with Utopia Level 1 cell-level handshaking) and Multi-PHY addressing for up to 32 PHY devices (Utopia Level 2 compatible).

- The Ingress output interface supports an 8 or 16 bit SCI-PHY (52 – 64 byte extended ATM cell with prepend/postpend) interface (compatible with Utopia Level 1 cell-level handshaking) to a switch fabric.

- The Egress input interface supports an 8 or 16 bit extended cell format SCI-PHY interface using direct addressing for up to 4 PHY devices (compatible with Utopia Level 1 cell-level handshaking) and Multi-PHY addressing for up to 32 PHY devices (Utopia Level 2 compatible).

- The Egress output interface supports an 8 or 16 bit extended cell format SCI-PHY interface using direct addressing for up to 4 PHY devices (compatible with Utopia Level 1 cell-level handshaking) and Multi-PHY addressing for up to 32 PHY devices (Utopia Level 2 compatible).

- Compatible with a wide range of switching fabrics and traffic management architectures including per-VC or per-PHY queuing.

- Highly flexible OAM-type cell and connection identification which can use arbitrary PHYID/VPI/VCI values and/or cell appended bytes for connection identification (N.B. this is an ingress function only). A direct lookup function is provided in the egress direction. The direct lookup can use an arbitrary header or prepend/postpend location.

- Ingress functionality includes a highly flexible search engine that covers the entire PHYID/VPI/VCI address range, programmable dual leaky bucket UPC/NPC, per-connection CLP0 and CLP1 cell counts (programmable), OAM-PM termination, generation and monitoring, and OAM-FM termination, generation and alarm generation (monitoring).

- Egress functionality includes programmable direct lookup function, OAM-PM termination, generation and monitoring, per-connection CLP0 and CLP1 cell counts (programmable) and OAM-FM termination, generation and alarm generation (monitoring). An egress per-PHY output buffering scheme resolves the head-of-line blocking issue.

- UPC/NPC function is a programmable dual leaky bucket policing device with a programmable action (tag, discard, or count only) for each bucket. A total of 3 programmable 16 bit non-compliant cell counts are provided. The non-compliant cell counts may be programmed to count, for example, dropped CLP0 cells, dropped CLP1 cells, and tagged CLP0 cells. The UPC/NPC function also has a *continuously violating* mode, where a programmable action is taken on all cells regardless of their compliance. AAL5 partial packet discard is also provided so that the remainder of an AAL5 packet can be tagged or discarded if a single cell in the packet is tagged or discarded as a result of violating policing.

- In addition to the per-connection dual leaky bucket, a single leaky bucket UPC/NPC function is provided on a per-PHY basis. A programmable action (tag, discard or count only) may be configured for each PHY policing device. Three programmable non-compliant cell counts are provided for each PHY. The non-compliant cell counts may be programmed to count, for example, dropped CLP0 cells, dropped CLP1 cells and tagged CLP0 cells. The per-PHY policing parameters and non-compliant cell counts are maintained in an on-chip RAM that can be programmed and read via the 16-bit general purpose microprocessor interface.

- Guaranteed Frame Rate frame-based policing selectable on a per-connection basis.

- OAM-Performance monitoring is provided in the ingress and egress direction for bi-directional PM sessions. A maximum of 512 (256 bi-directional sessions) PM sessions may be simultaneously active. PM is supported on the F4 and F5 levels. The S/UNI-ATLAS provides for the generation of Forward Monitoring and Backward Reporting PM cells (both segment and end-to-end), the termination of Forward Monitoring and Backward Reporting cells, and for non-intrusive monitoring of Forward Monitoring and Backward Reporting cells. The following statistics are collected when terminating or monitoring PM flows:

1. Forward Impaired Block.
2. Forward Lost/Misinserted Impaired Block
3. Forward Severely Errored Cell Block (Lost).
4. Forward Severely Errored Cell Block (Misinserted).
5. Forward Severely Errored Cell Block (BIP-16 violations).
6. Forward Severely Errored Cell Block Combined (non-saturating)
7. Forward Lost CLP0+1 cell count.
8. Forward Lost CLP0 cell count.

9. Forward Tagged CLP0 cell count
10. Forward Misinserted CLP0+1 cell count.
11. Forward Errored cell count.
12. Forward Total Lost CLP0+1 cell count.
13. Forward Total Lost CLP0 cell count.
14. Forward Lost Forward Monitoring cell count.
15. Backward Impaired Block.
16. Backward Lost/Misinserted Impaired Block.
17. Backward Severely Errored Cell Block (Lost).
18. Backward Severely Errored Cell Block (Misinserted).
19. Backward Severely Errored Cell Block (BIP-16 violations).
20. Backward Severely Errored Cell Block Combined (non-saturating)
21. Backward Severely Errored Cell Block Combined (saturating)
22. Backward Lost CLP0+1 cell count.
23. Backward Lost CLP0 cell count.
24. Backward Tagged CLP0 cell count.
25. Backward Misinserted CLP0+1 cell count.
26. Backward Errored cell count.
27. Backward Total Lost CLP0+1 cell count.
28. Backward Total Lost CLP0 cell count.
29. Backward Lost Fwd Monitoring PM cell count.
30. Backward Lost Backward Reporting PM cell count.
31. Total Transmitted CLP0+1 cell count.
32. Total Transmitted CLP0 cell count.

Statistics for PM sessions are held in on-chip RAM that can be read at any time through the 16-bit general-purpose microprocessor port.

Paced insertion of PM cells is provided.

PM block size generation and termination is per-session programmable ranging from 128 – 32768 cells.

Each of the 512 PM sessions can be configured to be a source, sink or non-intrusive monitoring point of PM cells.

- OAM-Fault Management is provided on a per-connection basis in the ingress and egress directions. Simultaneous segment and end-to-end F4 and F5 AIS, RDI and CC cell generation, termination and monitoring is supported. Alarm bits and interrupt masks are provided on a per-connection basis. F4 to F5 AIS alarm splitting is provided in the Ingress direction. Paced insertion of FM cells is provided.

- OAM-Loopback extraction (to a Microprocessor Cell Interface) is per-connection configurable in both the ingress and egress directions.

- Includes a FIFO buffered microprocessor bus interface for cell insertion and extraction (in both the ingress and egress directions), Ingress and Egress VC Table access, control and status monitoring and configuration of the device.

- Supports DMA access for cell extraction.

- Uses common external Synchronous Flow-Through SRAM (with or without parity) for maintaining per-connection information. Separate SRAM's are used for the Ingress and Egress context tables.

- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.

- Provides a generic 16 bit microprocessor bus interface for configuration, control and status monitoring.

- Low power 0.35 micron, 3.3V CMOS technology with a 3.3V UTOPIA (SCI-PHY), 3.3/5V Microprocessor I/O interfaces and 3.3V external synchronous SRAM interfaces.

- The UTOPIA (SCI-PHY) and external Synchronous SRAM interfaces are 52 MHz max.

- 432 Super BGA package.

1.1 Policing

- Policing is performed in the ingress direction for adherence to peak cell rate (PCR), cell delay variation tolerance (CDVT), sustained cell rate (SCR) and burst tolerance (BT). Violating cells can be noted, dropped or tagged.
- Policing is performed using the virtual scheduling Generic Cell Rate Algorithm (GCRA) described in ITU-T I.371.
- Two policing instantiations available per VC. The policed cell streams can be any combination of user cells, OAM cells, Resource Management, high priority cells or low priority cells.
- Per-PHY policing may also be enabled. Each of 32 PHY devices may have a single leaky bucket enabled, in addition to the dual leaky bucket of the connection. Violating cells can be noted (counted only), dropped or tagged.

1.2 Cell Counting

- Counts maintained on a per-VC basis include total low priority cells, total high priority cells and cells violating the traffic contract. Per-VC counts are maintained for both the ingress and egress directions.
- Counts maintained on a per-PHY basis (in both the Ingress and Egress directions) include: number of CLP0 cells received, number of CLP1 cells received, number of OAM cells received, number of RM cells received, number of errored OAM cells, number of errored RM cells, number of cells with unassigned/invalid VPI/VCI/PTI and the number of cells received with a non-zero GFC (ingress UNI only).

2 APPLICATIONS

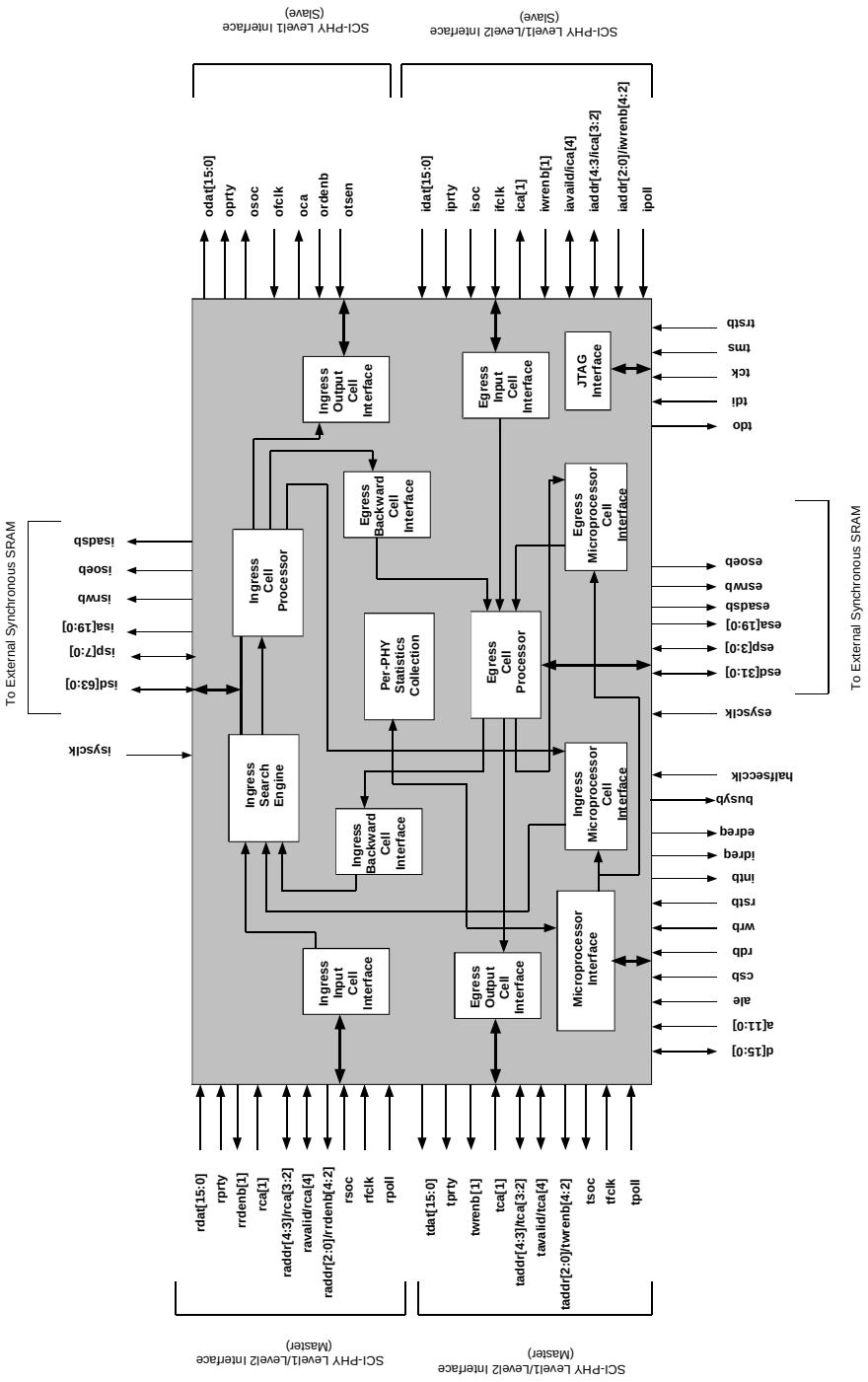
- Wide Area Network ATM Core and Edge switches.
- ATM Enterprise and Workgroup switches.
- Broadband Access multiplexers.
- XDSL Access Multiplexers (DSLAMs).

3 REFERENCES

- ATM Forum – ATM User-Network Interface Specification, V3.1 September, 1994
- ITU-T Recommendation I.361 – "B-ISDN ATM Layer Specification", November 1995
- ITU-T Recommendation I.371 – "Traffic Control and Congestion Control in B-ISDN", May, 1996
- ITU-T Recommendation I.610 – "B-ISDN Operation and Maintenance Principles and Functions", June, 1997 (Rapporteur's edition)
- Bell Communications Research – Broadband Switching System (BSS) Generic Requirements, GR-1110-CORE, Issue 1, September 1994
- Bell Communications Research – Asynchronous Transfer Mode (ATM) and ATM Adaptation Layer (AAL) Protocols, GR-1113-CORE, Issue 1, July 1994
- Bell Communications Research – Generic Requirements for Operations of Broadband Switching Systems, GR-1248-CORE, Issue 3, August, 1996.
- IEEE 1149.1 – Standard Test Access Port and Boundary Scan Architecture, May 21, 1990
- PMC-940212, ATM SCI-PHY, "SATURN Compliant Interface for ATM Devices", July 1994, Issue 2.
- ATMF TM4.0 – ATM Forum Traffic Management Specification Version 4.0, af-tm-0056.000, April, 1996.

4 APPLICATION EXAMPLES

Figure 1 S/UNI-ATLAS Block Diagram

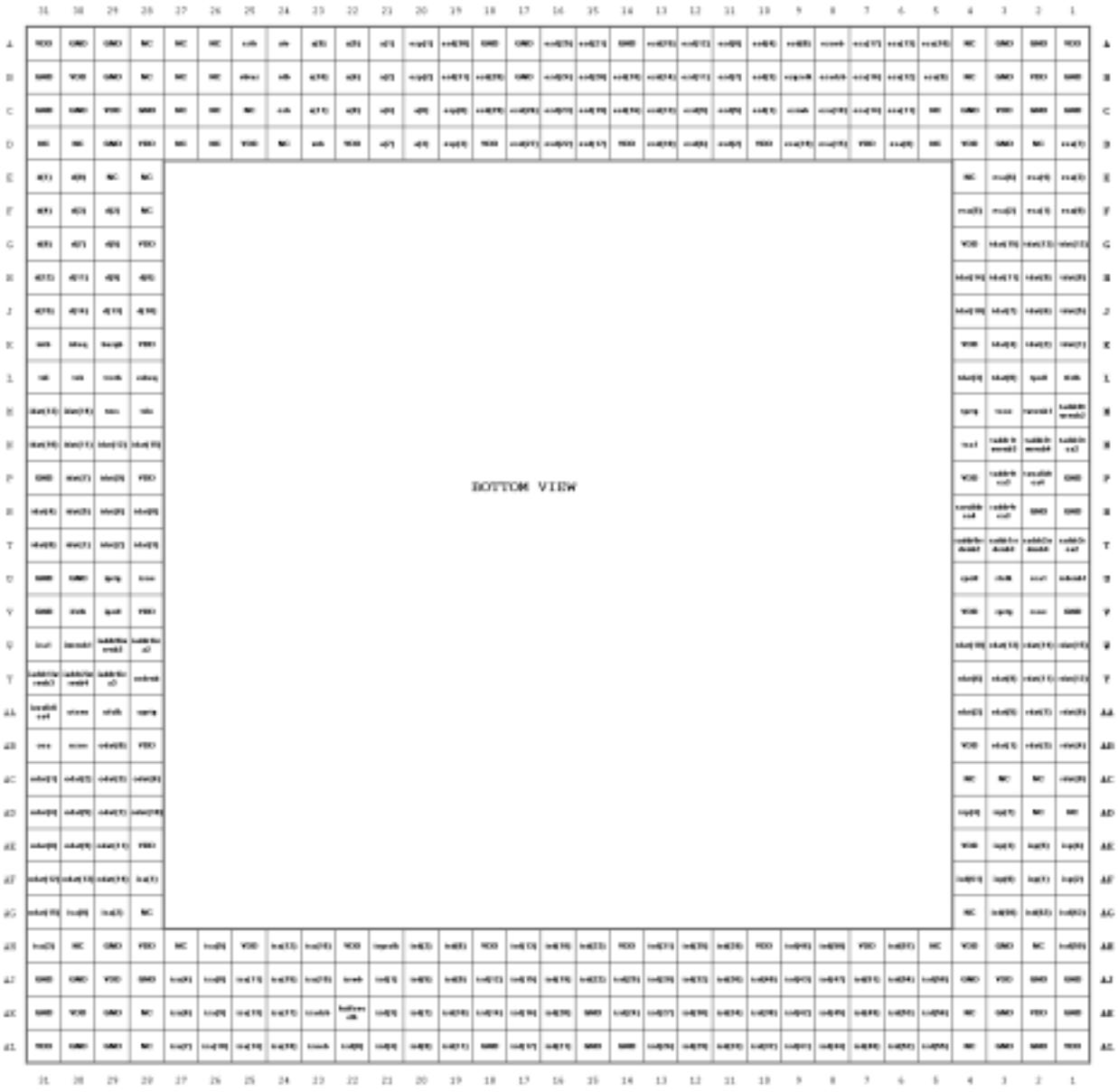


5 DESCRIPTION

The S/UNI-ATLAS is a bi-directional ATM Layer device that implements the ATM layer functions including header translation, policing, fault management, performance monitoring, per-connection and per-PHY counting. The S/UNI-ATLAS is intended to be situated between a switch core and a physical layer device. The S/UNI-ATLAS supports a sustained throughput of 1.42×10^6 cells/s in both the ingress (from the PHY into the switch core) and the egress (from the switch core to the PHY device) directions. The S/UNI-ATLAS uses external synchronous flow-through SRAM to store the per-connection data structures. The device is capable of supporting up to 65536 connections.

6 PIN DIAGRAM

The S/UNI-ATLAS is packaged in a 432 thermally enhanced BGA -SBGA package having a body size of 40 mm x 40 mm x 1.54 mm and a ball pitch of 1.27 mm. This pin diagram can be downloaded from the PMC-Sierra website (http://www.pmc-sierra.com).



7 PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
Ingress Input Cell Interface: 28 pins			
RFCLK	Input	U3	The Ingress Input Cell Interface clock (RFCLK) is used to read words from the PHY receive side into the S/UNI-ATLAS Ingress Input Cell Interface. RFCLK must cycle at a 52 MHz or lower instantaneous rate. RSOC, RCA[4:1], RPRTY and RDAT[15:0] are sampled on the rising edge of RFCLK. RRDENB[4:1], RADDR[4:0] and RAVALID are updated on the rising edge of RFCLK.
RPOLL	Input	U4	The Ingress Input Cell Interface Poll pin (RPOLL) is used to control whether the Ingress Input Cell Interface operates in SCI-PHY Level 1 mode or SCI-PHY Level 2 mode. If RPOLL is low, the Ingress Input Cell Interface operates in SCI-PHY Level 1 mode (compatible with UTOPIA Level 1 cell-level handshaking). This is a direct addressing mode using the RCA[4:1] inputs and the RRDENB[4:1] outputs. If RPOLL is high, the Ingress Input Cell Interface operates in a SCI-PHY Level 2 mode (compatible with UTOPIA Level 2). This is a polled addressing mode using the RADDR[4:0], RAVALID and RRDENB[1] outputs, and the RCA[1] input. If fewer than 32 PHY devices are used, the RAVALID pin need not be connected. Note: In direct addressing mode, the 4-PHY configuration is not recommended. Instead the 4-PHY address-polling mode should be used. This does not apply to the Single or Dual-PHY configurations. RPOLL is assumed to be a static input.
RSOC	Input	V2	The Ingress Input Cell Interface Start of Cell (RSOC) marks the start of the cell on the RDAT[15:0] bus. When RSOC is high, the first word of the cell structure is present on the RDAT[15:0] stream. It is not necessary for RSOC to be asserted for each cell. An interrupt may be generated if RSOC is high during any word other than the first word of the cell structure. RSOC is sampled on the rising edge of RFCLK and considered valid only when one of the RRDENB[4:1] signals so indicates.

Pin Name	Type	Pin No.	Function
RCA[1] RCA[2] RCA[3] RCA[4]	I/O	U2 T1 R3 R4	The active polarity of these signals is programmable and defaults to active high. If the RPOLL pin is low, the ATLAS asserts the appropriate RRDENB[4:1] signal in response to a round robin polling of the RCA[4:1] signals. Once committed, the ATLAS will transfer an entire cell from a single PHY before servicing the next. The ATLAS will complete the read of an entire cell even if the associated RCA[4:1] input is deasserted during the cell transfer. Sampling of the RCA[4:1] inputs resumes the cycle after the last octet of a cell has been transferred. Note, RCA[1] is an input only.
RCA[4:1] (continued)			If the RPOLL pin is high, the RCA[3:2] pins are redefined as RADDR[4:3] and the RCA[4] pin is redefined as RAVALID. If the RPOLL pin is high, the ATLAS polls up to 32 PHYs using the PHY address signals RADDR[4:0]. A PHY device being addressed by RADDR[4:0] is expected to indicate whether or not it has a complete cell available for transfer by driving RCA[1] during the clock cycle following that in which it is addressed. When a cell transfer is in progress, the ATLAS will not poll the PHY device which is sending the cell and so PHY devices need not support the cell availability indication during cell transfer. The selection of a particular PHY device from which to transfer a cell is indicated by the state of RADDR[4:0] and when RRDENB[1] is asserted. Note, RCA[1] is an input only. The RCA[4:1] signals are sampled on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RRDENB[1] RRDENB[2] RRDENB[3] RRDENB[4]	Output	U1 T4 T3 T2	The active low read enable (RRDENB[4:1]) outputs are used to initiate the reading of cells from a PHY device into the Ingress Input Cell Interface. If the RPOLL pin is low, the ATLAS asserts one of the RRDENB[4:1] outputs to transfer a cell from one of up to 4 PHY devices. A valid word is expected on the RDAT[15:0] bus at the second rising edge of RFCLK after one of the enables is asserted. When all of the enables are deasserted, no valid data is expected. The RRDENB[4:1] outputs are updated on the rising edge of RFCLK. If the RPOLL pin is high, the RRDENB[4:2] pins are redefined as RADDR[2:0]. The RRDENB[1] pin is used to transfer all cells. The source PHY is selected by the RADDR[4:0] signals.
RADDR[4] RADDR[3] RADDR[2] RADDR[1] RADDR[0]	Output	R3 T1 T2 T3 T4	If the RPOLL pin is high, the RADDR[4:0] pins are used for PHY addressing. If the RPOLL pin is low, the RADDR[4:0] pins are redefined as RCA[3:2] and RRDENB[4:2]. If the RPOLL pin is high, the RADDR[4:0] signals are used to address up to 32 PHY devices for the purposes of polling and selection for cell transfer. When conducting polling, in order to avoid bus contention, the ATLAS inserts gap cycles during which RADDR[4:0] is set to 0x1F and RAVALID is logic 0. When this occurs, no PHY device should drive RCA[1] during the following clock cycle. Polling is performed in incrementing sequential order. The PHY device selected for transfer is based on the RADDR[4:0] value present when RRDENB[1] is falls. The RADDR[4:0] bus is updated on the rising edge of RFCLK.
RAVALID	I/O	R4	If the RPOLL pin is high, the PHY Address Valid (RAVALID) pin is active. If the RPOLL pin is low, the RAVALID pin is redefined as RCA[4]. If the RPOLL pin is high, the RAVALID pin indicates that the RADDR[4:0] bus is asserting a valid PHY address for polling purposes. When this signal is deasserted, the RADDR[4:0] bus is set to 0x1F. RAVALID is not necessary when less than 32 PHY devices are being polled. RAVALID is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RDAT[15] RDAT[14] RDAT[13] RDAT[12] RDAT[11] RDAT[10] RDAT[9] RDAT[8] RDAT[7] RDAT[6] RDAT[5] RDAT[4] RDAT[3] RDAT[2] RDAT[1] RDAT[0]	Input	W1 W2 W3 Y1 Y2 W4 Y3 AA1 AA2 Y4 AA3 AB1 AB2 AA4 AB3 AC1	The Ingress Input Cell Interface cell data bus (RDAT[15:0]) carries the ATM cell octets that are written to the Ingress Input Cell Interface. The RDAT[15:0] bus is sampled on the rising edge of RFCLK and considered valid only when one of the RRDENB[4:1] signals so indicates. RDAT[15:8] is only valid if the RBUS8 register bit is low.
RPRTY	Input	V3	The Ingress Input Cell Interface parity (RPRTY) signal indicates the parity (programmable for odd or even parity) of the RDAT[15:0] bus. If the RBUS8 register bit is low, the RPRTY signal indicates parity over the RDAT[15:0] data bus. If RBUS8 is high, the RPRTY signal indicates parity over the RDAT[7:0] data bus. A maskable interrupt status is generated upon a parity error; no other actions are taken. The RPRTY signal is sampled on the rising edge of RFCLK and is considered valid only when one of the RRDENB[4:1] signals so indicates.
Ingress SRAM Interface: 96 pins			
ISYSCLK	Input	AH21	The Ingress System clock (ISYSCLK) is used for the Ingress portion of the ATLAS. ISYSCLK must cycle at a 52 MHz or lower instantaneous rate, but a high enough rate to maintain an 800Mbit/s throughput. ISADSB, ISOEB, ISRWB are updated on the rising edge of ISYSCLK. When ISD[63:0] and ISP[7:0] are outputs, they are updated on the rising edge of ISYSCLK. When ISD[63:0] and ISP[7:0] are inputs, they are sampled on the rising edge of ISYSCLK.

Pin Name	Type	Pin No.	Function
ISD[63]	I/O	AG1	The bi-directional Ingress VC Table SRAM data bus (ISD[63:0]) pins interface directly with the synchronous SRAM data ports. A SRAM read is performed when the ATLAS drives the address strobe (ISADSB) low and the ISRWB output high. The ATLAS tristates the ISD[63:0] pins and samples the value driven by the SRAM on the second rising edge of the ISYSCLK input after ISADSB is asserted. A SRAM write is performed when the ATLAS drives the address strobe low (ISADSB) and the ISRWB output low. The ATLAS presents valid data on the ISD[63:0] pins upon the rising edge of ISYSCLK which is written into the SRAM on the next ISYSCLK rising edge. ISD[63:0] is tristated on the rising edge of ISYSCLK. Contention is avoided by not performing a write during the cycle after a read burst.
ISD[62]		AG2	
ISD[61]		AF4	
ISD[60]		AG3	
ISD[59]		AH1	
ISD[58]		AJ5	
ISD[57]		AH6	
ISD[56]		AK5	
ISD[55]		AL5	
ISD[54]		AJ6	
ISD[53]		AK6	
ISD[52]		AL6	
ISD[51]		AJ7	
ISD[50]		AH8	

Pin Name	Type	Pin No.	Function
ISD[49]	I/O	AK7	Continued
ISD[48]		AL7	
ISD[47]		AJ8	
ISD[46]		AH9	
ISD[45]		AK8	
ISD[44]		AL8	
ISD[43]		AJ9	
ISD[42]		AK9	
ISD[41]		AL9	
ISD[40]		AJ10	
ISD[39]		AH11	
ISD[38]		AK10	
ISD[37]		AL10	
ISD[36]		AJ11	
ISD[35]		AH12	
ISD[34]		AK11	
ISD[33]		AL11	
ISD[32]		AJ12	

Pin Name	Type	Pin No.	Function
ISD[31]	I/O	AH13	Continued
ISD[30]		AK12	
ISD[29]		AL12	
ISD[28]		AJ13	
ISD[27]		AK13	
ISD[26]		AL13	
ISD[25]		AJ14	
ISD[24]		AK14	
ISD[23]		AH15	
ISD[22]		AJ15	
ISD[21]		AL16	
ISD[20]		AK16	
ISD[19]		AJ16	
ISD[18]		AH16	
ISD[17]		AL17	
ISD[16]		AK17	

Pin Name	Type	Pin No.	Function
ISD[15]	I/O	AJ17	Continued
ISD[14]		AK18	
ISD[13]		AH17	
ISD[12]		AJ18	
ISD[11]		AL19	
ISD[10]		AK19	
ISD[9]		AJ19	
ISD[8]		AL20	
ISD[7]		AK20	
ISD[6]		AH19	
ISD[5]		AJ20	
ISD[4]		AL21	
ISD[3]		AK21	
ISD[2]		AH20	
ISD[1]		AJ21	
ISD[0]		AL22	

Pin Name	Type	Pin No.	Function
ISP[7] ISP[6] ISP[5] ISP[4] ISP[3] ISP[2] ISP[1] ISP[0]	I/O	AD3 AE1 AE2 AD4 AE3 AF1 AF2 AF3	The Ingress VC Table SRAM parity (ISP[7:0]) pins provide parity protection over the ISD[63:0] data bus. ISP[0] completes odd parity for ISD[7:0] ISP[1] completes odd parity for ISD[15:8] ISP[2] completes odd parity for ISD[23:16] ISP[3] completes odd parity for ISD[31:24] ISP[4] completes odd parity for ISD[39:32] ISP[5] completes odd parity for ISD[47:40] ISP[6] completes odd parity for ISD[55:48] ISP[7] completes odd parity for ISD[63:56] ISP[7:0] has the same timing as ISD[63:0]. When data are being written into the SRAM, the ATLAS generates correct parity. When data are being read from the SRAM, the ATLAS asserts a maskable interrupt indication upon parity error detection. No other action is taken, therefore, the ISP[7:0] may be unconnected if parity protection is not required.

Pin Name	Type	Pin No.	Function
ISA[19] ISA[18] ISA[17] ISA[16] ISA[15] ISA[14] ISA[13] ISA[12] ISA[11] ISA[10] ISA[9] ISA[8] ISA[7] ISA[6] ISA[5] ISA[4] ISA[3] ISA[2] ISA[1] ISA[0]	Output	AJ23 AL24 AK24 AH23 AJ24 AL25 AK25 AH24 AJ25 AL26 AK26 AJ26 AL27 AK27 AH26 AJ27 AH31 AG29 AF28 AG30	The Ingress VC Table SRAM (ISA[19:0]) outputs identify the SRAM locations accessed. The 16 least significant bits (ISA[15:0]) locate 1 of 65536 possible Ingress VC Table entries. If 65536 connections are not required, the most significant bits of ISA[15:0] may be unconnected with no physical memory associated with the unused memory space. The four most significant bits (ISA[19:16]) identify the fields within an Ingress VC Table record. In most applications, the ISA[19:16] pins are decoded to SRAM chip selects. Physical memory need not be allocated for unused fields. The ISA[15:0] outputs are also used to access the Ingress VC Table Search Table. The ISA[19:0] bus is updated on the rising edge of ISYSCLK.
ISRWB	Output	AJ22	The Ingress VC Table SRAM Read Write Bar (ISRWB) qualifies the data and parity busses. If the ISRWB output is asserted high, a read operation is performed and the ATLAS tristates the data and parity busses so they may be driven by the SRAM. If the ISRWB output is asserted low, a write operation is performed and the ATLAS drives the data and parity busses. ISRWB is updated on the rising edge of ISYSCLK.
ISADSB	Output	AK23	The Ingress VC Table SRAM Address Strobe (ISADSB) qualifies the address bus. If the ISADSB output is asserted low, an SRAM access is initiated. ISADSB is updated on the rising edge of ISYSCLK.

Pin Name	Type	Pin No.	Function
ISOEB	Output	AL23	The Ingress VC Table asynchronous SRAM Output Enable (ISOEB) controls the SRAM tristate outputs. When ISOEB is low during a read cycle, the selected SRAM (as determined by ISA[19:0] decoding) is expected to drive the ISD[63:0] and ISP[7:0] data busses. ISOEB is updated on the rising edge of ISYSCLK.
Ingress Output Cell Interface: 22 pins			
OFCLK	Input	AA29	The Ingress Output Cell Interface clock (OFCLK) is used to read words from the Ingress Output Cell Interface. OFCLK must cycle at a 52 MHz or lower instantaneous rate, but a high enough rate to avoid a FIFO overflow. OSOC, OCA, OPRTY and ODAT[15:0] are updated on the rising edge of OFCLK. ORDENB is sampled on the rising edge of OFCLK.
ORDENB	Input	Y28	The active low read enable (ORDENB) signal is used to indicate transfers from the Ingress Output Cell Interface. When ORDENB is sampled low, using the rising edge of OFCLK, a word is read from the internal synchronous Ingress Output Cell Interface FIFO, and output on bus ODAT[15:0]. When ORDENB is sampled high, no read is performed and outputs ODAT[15:0], OPRTY and OSOC are tristated if the OTSEN input is high. ORDENB must operate in conjunction with OFCLK to access the FIFO at a high enough rate to avoid a FIFO overflow.

Pin Name	Type	Pin No.	Function
ODAT[15] ODAT[14] ODAT[13] ODAT[12] ODAT[11] ODAT[10] ODAT[9] ODAT[8] ODAT[7] ODAT[6] ODAT[5] ODAT[4] ODAT[3] ODAT[2] ODAT[1] ODAT[0]	Tristate	AG31 AF29 AF30 AF31 AE29 AD28 AE30 AE31 AD29 AC28 AD30 AD31 AC29 AC30 AC31 AB29	The Ingress Output Cell Interface data bus (ODAT[15:0]) carries the ATM cell octets that are read from the Ingress Output Cell Interface FIFO. If the OBUS8 register bit is high, only ODAT[7:0] carries cell octets, The ODAT[15:0] bus is updated on the rising edge of OFCLK. When the Ingress Output Cell Interface is configured for tristate operation using the OTSEN input, tristating of the ODAT[15:0] output bus is controlled by the ORDENB input. When OTSEN is low, the ODAT[15:0] bus is low when no cells are being transferred.
OPRTY	Tristate	AA28	The Ingress Output Cell Interface parity (OPRTY) signal indicates the parity of the ODAT[15:0] data bus. OPRTY is the parity (programmable odd or even parity) calculation over the ODAT[15:0] data bus if the OBUS8 register bit is low. If OBUS8 is high, OPRTY indicates the parity of the ODAT[7:0] data bus. OPRTY is updated on the rising edge of OFCLK. When the Ingress Output Cell Interface is configured for tristate operation using the OTSEN input, tristating of the OPRTY output signal is controlled by the ORDENB input.
OSOC	Tristate	AB30	The Ingress Output Cell Interface start of cell (OSOC) signal marks the start of cell on the ODAT[15:0] data bus. When OSOC is high, the first word of the cell structure is present on the ODAT[15:0] bus. OSOC is updated on the rising edge OFCLK. When the Ingress Output Cell Interface is configured for tristate operation using the OTSEN input, tristating of the OSOC output is controlled by the ORDENB input.

Pin Name	Type	Pin No.	Function
OCA	Output	AB31	The active polarity of this signal is programmable and defaults to active high. The OCA signal indicates when the Ingress Output Cell Interface has a cell available. When asserted, OCA indicates that at least one cell is available to be read from the Ingress Output Cell Interface FIFO. The OCA signal is deasserted when the Ingress Output Cell Interface has 0 to 4 words available for the current cell. OCA is updated on the rising edge of OFCLK.
OTSEN	Input	AA30	The tristate enable, OTSEN, signal allows control over the Ingress Output Cell Interface ODAT[15:0], OPRTY, and OSOC outputs. When OTSEN is high, the active low read enable input, ORDENB controls when the ODAT[15:0], OPRTY, and OSOC outputs are driven. When OTSEN is low, the ODAT[15:0], OPRTY and OSOC outputs are always driven.
Egress Input Cell Interface: 28 pins			
IFCLK	Input	V30	The Egress Input Cell Interface clock (IFCLK) is used to write words from the Traffic Shaper (or Switch Port) transmit port into the S/UNI-ATLAS Egress Input Cell Interface. IFCLK must cycle at a 52 MHz or lower instantaneous rate. ISOC, IPRTY, IDAT[15:0] and IWRENB[4:1] are sampled on the rising edge of IFCLK. IADDR[4:0], IAVALID and ICA[4:1] are updated on the rising edge of IFCLK.
IPOLL	Input	V29	The Egress Input Cell Interface POLL pin (IPOLL) is used to control whether the Egress Input Cell Interface operates in SCI-PHY Level 1 mode or SCI-PHY Level 2 mode. If IPOLL is low, the Egress Input Cell Interface operates in SCI-PHY Level 1 mode (compatible with UTOPIA Level 1 cell-level handshaking). This is a direct addressing mode using the ICA[4:1] outputs and the IWRENB[4:1] inputs. If IPOLL is high, the Egress Input Cell Interface operates in SCI-PHY Level 2 mode (compatible with UTOPIA Level 2). This is a polled addressing mode using the IADDR[4:0], IAVALID and IWRENB[1] inputs, and the ICA[1] output. If fewer than 32 PHY devices are used, the IAVALID pin can be tied high. Note: In direct addressing mode, the 4-PHY configuration is not recommended. Instead the 4-PHY address-polling mode should be used. This does not apply to the Single or Dual-PHY configurations. IPOLL is assumed to be a static input.

Pin Name	Type	Pin No.	Function
ISOC	Input	U28	The Egress Input Cell Interface Start of Cell (ISOC) marks the start of the cell on the IDAT[15:0] bus. When ISOC is high, the first word of the cell structure is present on the IDAT[15:0] stream. It is not necessary for ISOC to be asserted for each cell. An interrupt may be generated if ISOC is high during any word other than the first word of the cell structure. ISOC is sampled on the rising edge of IFCLK and considered valid only when one of the IWRENB[4:1] signals so indicates.
ICA[1] ICA[2] ICA[3] ICA[4]	O I/O I/O I/O	W31 W28 Y29 AA31	The active polarity of these signals is programmable and defaults to active high. If the IPOLL pin is low, the ATLAS asserts the appropriate ICA[4:1] signal indicating the availability of space in the Egress Input Cell Interface per-PHY 4 cell FIFO of the ATLAS. The Egress Input Cell Interface of the ATLAS must be programmed to emulate the number of PHY devices to which the ATLAS is connected. Note, ICA[1] is an output only.
ICA[4:1] (continued)			If the IPOLL pin is high, the ICA[3:2] pins are redefined as IADDR[4:3] and the ICA[4] pin is redefined as IAVALID. If the IPOLL pin is high, the ATLAS asserts the availability of space in the FIFO of a particular PHY device when polled using the IADDR[4:0] and IAVALID signals. The ATLAS will drive the ICA[1] signal to the appropriate value during the clock cycle following that in which a particular PHY device is addressed. When a cell transfer is in progress, the ATLAS will assert the availability of the PHY device to which the current cell is being transmitted, and the true availability of the PHY device will be asserted 4 words before the end of the cell transfer. The selection of a particular PHY device to which a cell is to be transferred is indicated by the state of the IADDR[4:0] bus when IWRENB[4:1] is asserted. Note, ICA[1] is an output only.

Pin Name	Type	Pin No.	Function
IWRENB[1] IWRENB[2] IWRENB[3] IWRENB[4]	I I I I	W30 W29 Y31 Y30	The active low write enable (IWRENB[4:1]) inputs are used to initiate the transfer of cells from the Traffic Shaper into the ATLAS Egress Input Cell Interface. If the IPOLL pin is low, the ATLAS samples the IWRENB[4:1] inputs to determine to which one of up to 4 PHY devices a cell is to be written. A valid word is expected on the IDAT[15:0] bus when one of the enables is sampled low on the rising edge of IFCLK. If a cell is written into the ATLAS while that particular PHY ICA[x] is deasserted, that cell transfer is ignored, and a maskable interrupt is asserted. If more than one enable is asserted simultaneously, a maskable interrupt is asserted, and the cell transfer is ignored. If the IPOLL pin is high, the IWRENB[4:2] pins are redefined as IADDR[2:0]. The IWRENB[1] pin is used to transfer all cells. The destination PHY is selected by the IADDR[4:0] signals.
IADDR[4] IADDR[3] IADDR[2] IADDR[1] IADDR[0]	I/O I/O I I I	Y29 W28 Y30 Y31 W29	If the IPOLL pin is high, the IADDR[4:0] pins are used for PHY addressing. If the IPOLL register bit is logic pin is low, the IADDR[4:0] pins are redefined as ICA[3:2] and IWRENB[4:2]. If the IPOLL pin is high, the IADDR[4:0] signals are used to address up to 32 PHY devices for polling and selection for cell transfer. The PHY devices selected for transfer is based on the IADDR[4:0] value present when the IWRENB[1] signal falls. The IADDR[4:0] bus is sampled on the rising edge of IFCLK.
IAVALID	I/O	AA31	If the IPOLL pin is high, the PHY address valid pin (IAVALID) is active. If the IPOLL pin is low, the IAVALID pin is redefined as ICA[4]. If the IPOLL pin is high, the IAVALID pin indicates that the IADDR[4:0] bus is asserting a valid PHY address for polling purposes. When this signal is deasserted, the IADDR[4:0] bus must be set to 0x1F. If fewer than 32 PHY devices are being polled and the IAVALID pin is not functionally used, then IAVALID must be tied high. IAVALID is sampled on the rising edge of IFCLK.

Pin Name	Type	Pin No.	Function
IDAT[15] IDAT[14] IDAT[13] IDAT[12] IDAT[11] IDAT[10] IDAT[9] IDAT[8] IDAT[7] IDAT[6] IDAT[5] IDAT[4] IDAT[3] IDAT[2] IDAT[1] IDAT[0]	Input	N28 M30 M31 N29 N30 N31 P29 R28 P30 R29 R30 R31 T28 T29 T30 T31	The Egress Input Cell Interface cell data bus (IDAT[15:0]) carries the ATM cell octets that are written to the Egress Input Cell Interface. The IDAT[15:0] bus is sampled on the rising edge of IFCLK and considered valid only when one of the IWRENB[4:1] signals so indicates. IDAT[15:8] is only valid if the IBUS8 register bit is low.
IPRTY	Input	U29	The Egress Input Cell Interface parity (IPRTY) signal indicates the parity (programmable for odd or even parity) of the IDAT[15:0] bus. If the IBUS8 register bit is low, the IPRTY signal indicates parity over the IDAT[15:0] data bus. If IBUS8 is high, the IPRTY signal indicates parity over the IDAT[7:0] data bus. A maskable interrupt status is generated upon a parity error; no other actions are taken. The IPRTY signal is sampled on the rising edge of IFCLK and is considered valid only when one of the IWRENB[4:1] signals so indicates.
Egress Output Cell Interface: 28 pins			
TFCLK	Input	L1	The Egress Output Cell Interface clock (TFCLK) is used to write words from the Egress Output Cell Interface. TFCLK must cycle at a 52 MHz or lower instantaneous rate, but a high enough rate to avoid a FIFO overflow. TSOC, TWRENB[4:1], TADDR[4:0], TAVALID, TPRTY and TDAT[15:0] are updated on the rising edge of TFCLK. TCA[4:1] is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TPOLL	Input	L2	The Egress Output Cell Interface POLL pin (TPOLL) is used to control whether the Egress Output Cell Interface operates in SCI-PHY Level 1 mode or SCI-PHY Level 2 mode. If TPOLL is low, the Egress Output Cell Interface operates in SCI-PHY Level 1 mode (compatible with UTOPIA Level 1 cell-level handshaking). This is a direct addressing mode using the TCA[4:1] inputs and the TWRENB[4:1] outputs. If TPOLL is high, the Egress Output Cell Interface operates in SCI-PHY Level 2 mode (compatible with UTOPIA Level 2). This is a polled addressing mode using the TADDR[4:0], TAVALID and TWRENB[1] outputs, and the TCA[1] input. If fewer than 32 PHY devices are used, the TAVALID pin can be left unconnected. Note: In direct addressing mode, the 4-PHY configuration is not recommended. Instead the 4-PHY address-polling mode should be used. This does not apply to the Single or Dual-PHY configurations. TPOLL is assumed to be a static input.
TSOC	Output	M3	The Egress Output Cell Interface start of cell (TSOC) indication signal marks the start of cell on the TDAT[15:0] data bus. When TSOC is high, the first word of the cell structure is present on the TDAT[15:0] bus. TSOC is updated on the rising edge of TFCLK.
TCA[4] TCA[3] TCA[2] TCA[1]	I/O	P2 P3 N1 N4	The active polarity of these signals is programmable and defaults to active high. If the TPOLL pin is low, the ATLAS samples the state of the cell available signals of the PHY devices to examine whether or not cells can be transferred to the PHY devices. The ATLAS will complete the writing of an entire cell into the PHY device even if the associated TCA[4:1] input is deasserted during the cell transfer. Sampling of the TCA[4:1] signals resumes the cycle after the last octet of a cell has been transferred. If the TPOLL pin is high, the TCA[3:2] pins are redefined as TADDR[4:3] and the TCA[4] pin is redefined as TAVALID. Note, TCA[1] is an input only.

Pin Name	Type	Pin No.	Function
TCA[4:1] (continued)			If the TPOLL pin is high, the ATLAS polls up to 32 PHYs using the PHY address signals TADDR[4:0]. A PHY device being addressed by TADDR[4:0] is expected to indicate whether or not it has a complete cell available for transfer by driving the TCA[1] during the clock cycle following that in which it is addressed. When a cell transfer is in progress, the ATLAS will not poll the PHY device which is sending the cell and so PHY devices need not support the cell availability indication during cell transfer. The selection of a particular PHY device to which a cell will be written is indicated by the state of TADDR[4:0] and when TWRENB[1] is asserted. Note, TCA[1] is an input only.
TWRENB[4] TWRENB[3] TWRENB[2] TWRENB[1]	Output	N2 N3 M1 M2	The active low write enable (TWRENB[4:1]) signals are used to indicate transfers from the Egress Output Cell Interface to the PHY devices. If the TPOLL pin is low, the ATLAS asserts one of the TWRENB[4:1] outputs to transfer a cell to one of up to 4 PHY devices. A valid word is output on the TDAT[15:0] bus at the same time one of the write enables is asserted. When all of the enables are deasserted, no valid data is output. The TWRENB[4:1] outputs are updated on the rising edge of TFCLK. If the TPOLL pin is high, the TWRENB[4:2] pins are redefined as TADDR[2:0]. Note, TWRENB[1] is an output only.
TADDR[4] TADDR[3] TADDR[2] TADDR[1] TADDR[0]	I/O	P3 N1 N2 N3 M1	If the TPOLL pin is high, the TADDR[4:0] pins are used for PHY addressing. If the TPOLL pin is low, the TADDR[4:0] pins are redefined as TCA[3:2] and TWRENB[4:2]. If the TPOLL pin is high, the TADDR[4:0] signals are used to address up to 32 PHY devices for the purposes of polling and selection for cell transfer. When conducting polling, in order to avoid bus contention, the ATLAS inserts gap cycles during which the TADDR[4:0] bus is set to 0x1F and TAVALID is logic 0. When this occurs, no PHY device should drive TCA[1] during the following clock cycle. Polling is performed in incrementing sequential order. The PHY device selected for transfer is based on the TADDR[4:0] value present when TWRENB[1] falls. The TADDR[4:0] bus is updated on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TAVALID	I/O	P2	If the TPOLL pin is high, the PHY Address Valid (TAVALID) pin is active. If the TPOLL pin is low, the TAVALID pin is redefined as TCA[4]. If the TPOLL pin is high, the TAVALID pin indicates that the TADDR[4:0] bus is asserting a valid PHY address for polling purposes. When this signal is deasserted, the TADDR[4:0] bus is set to 0x1F. TAVALID is not necessary when less than 32 PHY devices are being polled. TAVALID is updated on the rising edge of TFCLK.
TDAT[15] TDAT[14] TDAT[13] TDAT[12] TDAT[11] TDAT[10] TDAT[9] TDAT[8] TDAT[7] TDAT[6] TDAT[5] TDAT[4] TDAT[3] TDAT[2] TDAT[1] TDAT[0]	Output	G3 H4 G2 G1 H3 J4 H2 H1 J3 J2 J1 K3 L4 K2 K1 L3	The Egress Output Cell Interface cell data bus (TDAT[15:0]) carries the ATM cell octets that are written to the PHY devices. The TDAT[15:0] bus is updated on the rising edge of TFCLK and considered valid only when one of the TWRENB[4:1] signals so indicates. TDAT[15:8] is only valid if the TBUS8 register bit is low.
TPRTY	Output	M4	The Egress Output Cell Interface parity (TPRTY) signal indicates the parity (programmable for odd or even parity) of the TDAT[15:0] bus. If the TBUS8 register bit is low, the TPRTY signal indicates parity over the TDAT[15:0] data bus. If TBUS8 is high, the TPRTY signal indicates parity over the TDAT[7:0] data bus. The TPRTY signal is updated on the rising edge of TFCLK and is considered valid only when one of the TWRENB[4:1] signals so indicates.
Egress SRAM Interface: 60 pins			

Pin Name	Type	Pin No.	Function
ESYSCLK	Input	B9	The Egress System clock (ESYSCLK) is used for the Egress portion of the ATLAS. ESYSCLK must cycle at a 52 MHz or lower instantaneous rate, but a high enough rate to maintain an 800Mbit/s throughput. ESADSB, ESOEB and ESRWB are updated on the rising edge of ESYSCLK. When ESD[31:0] and ESP[3:0] are outputs, they are updated on the rising edge of ESYSCLK. When ESD[31:0] and ESP[3:0] are inputs, they are sampled on the rising edge of ESYSCLK.
ESD[31] ESD[30] ESD[29] ESD[28] ESD[27] ESD[26] ESD[25] ESD[24] ESD[23] ESD[22] ESD[21] ESD[20] ESD[19] ESD[18] ESD[17] ESD[16]	I/O	B19 A19 C18 B18 D17 C17 A16 B16 C16 D16 A15 B15 C15 B14 D15 C14	The bi-directional Egress VC Table SRAM data bus (ESD[31:0]) pins interface directly with the synchronous SRAM data ports. A SRAM read is performed when the ATLAS drives the address strobe (ESADSB) low and the ESRWB output high. The ATLAS tristates the ESD[31:0] pins and samples the value driven by the SRAM on the second rising edge of the ESYSCLK input after ESADSB is asserted. A SRAM write is performed when the ATLAS drives the address strobe low (ESADSB) and the ESRWB output low. The ATLAS presents valid data on the ESD[31:0] pins upon the rising edge of ESYSCLK which is written into the SRAM on the next ESYSCLK rising edge. ESD[31:0] is tristated on the rising edge of ESYSCLK. Contention is avoided by not performing a write during the cycle after a read burst.

Pin Name	Type	Pin No.	Function
ESD[15] ESD[14] ESD[13] ESD[12] ESD[11] ESD[10] ESD[9] ESD[8] ESD[7] ESD[6] ESD[5] ESD[4] ESD[3] ESD[2] ESD[1] ESD[0]	I/O	A13 B13 C13 A12 B12 D13 C12 A11 B11 D12 C11 A10 B10 D11 C10 A9	Continued
ESP[3] ESP[2] ESP[1] ESP[0]	I/O	D19 B20 A20 C19	The Egress VC Table SRAM parity (ESP[3:0]) pins provide parity protection over the ESD[31:0] data bus. ESP[0] completes the odd parity for ESD[7:0] ESP[1] completes the odd parity for ESD[15:8] ESP[2] completes the odd parity for ESD[23:16] ESP[3] completes the odd parity for ESD[31:24] ESP[3:0] has the same timing as ESD[31:0]. When data are being written into the SRAM, the ATLAS generates correct parity. When data are being read from the SRAM, the ATLAS asserts a maskable interrupt indication upon parity error detection. No other action is taken, therefore, the ESP[3:0] may be unconnected if parity protection is not required.

Pin Name	Type	Pin No.	Function
ESA[19] ESA[18] ESA[17] ESA[16] ESA[15] ESA[14] ESA[13] ESA[12] ESA[11] ESA[10] ESA[9] ESA[8] ESA[7] ESA[6] ESA[5] ESA[4] ESA[3] ESA[2] ESA[1] ESA[0]	Output	D9 C8 A7 B7 D8 C7 A6 B6 C6 A5 B5 D6 D1 E3 F4 E2 E1 F3 F2 F1	The Egress VC Table SRAM (ESA[19:0]) outputs identify the SRAM locations accessed. The 16 least significant bits (ESA[15:0]) locate 1 of 65536 possible Egress VC Table entries. If 65536 connections are not required, the most significant bits of ESA[15:0] may be unconnected with no physical memory associated with the unused memory space. The four most significant bits (ESA[19:16]) identify the fields within an Egress VC Table record. In most applications, the ESA[19:16] pins are decoded to SRAM chip selects. Physical memory need not be allocated for unused fields. The ESA[15:0] outputs are also used to access the Egress VC Table Search Table. The ESA[19:0] bus is updated on the rising edge of ESYSCLK.
ESRWB	Output	C9	The Egress VC Table SRAM Read Write Bar (ESRWB) qualifies the data bus. If the ESRWB output is asserted high, the external SRAM samples this signal and performs a read operation and the ATLAS tristates the ESD[31:0] and ESP[3:0] pins so they may be driven by the external SRAM). If the ESRWB output is asserted low, a write operation is performed, and the ATLAS drives the ESD[31:0] and ESP[3:0] pins. ESRWB is updated on the rising edge of ESYSCLK.
ESADSB	Output	B8	The Egress VC Table SRAM Address Strobe (ESADSB) qualifies the address bus. If the ESADSB output is asserted low, the external SRAM samples the address asserted by the ATLAS. ESADSB is updated on the rising edge of ESYSCLK

Pin Name	Type	Pin No.	Function
ESOEB	Output	A8	The Egress VC Table asynchronous SRAM Output Enable (ESOEB) controls the SRAM tristate outputs. When ESOEB is low during a read cycle, the selected SRAM (as determined by the decoding of the ESD[31:0] multiplexed address bus) is expected to drive the ESD[31:0] and ESP[3:0] data busses. ESOEB is updated on the rising edge of ESYSCLK.
Microprocessor Interface: 38 pins			
CSB	Input	C24	CSB is low during ATLAS Microprocessor Interface Port register accesses. If CSB is not required (i.e. register accesses controlled using RDB and WRB signals only), CSB should be connected to an inverted version of the RSTB input. CSB is a 5V tolerant input.
RDB	Input	B24	RDB is low during ATLAS Microprocessor Interface Port register read accesses. The ATLAS drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low. RDB is a 5V tolerant input.
WRB	Input	D23	WRB is low during ATLAS Microprocessor Interface Port register write accesses. The D[15:0] bus contents are clocked into the addressed register on the rising edge of WRB while CSB is low. WRB is a 5V tolerant input.
IDREQ	Output	K30	The Ingress Microprocessor Cell Interface DMA request (IDREQ) is asserted when the Ingress Microprocessor Cell Interface contains a cell to be read, and the DMAEN register bit in the Ingress MCIF Configuration register is a logic 1. The first read of the Ingress MCIF Data register will return the first word of the cell. IDREQ is deasserted after the last word of the cell has been read or an abort has been signaled.
EDREQ	Output	L28	The Egress Microprocessor Cell Interface DMA request (EDREQ) is asserted when the Egress Microprocessor Cell Interface contains a cell to be read, and the DMAEN register in the Egress MCIF configuration register is a logic 1. The first read of the Egress MCIF Data register will return the first word of the cell. EDREQ is deasserted after the last word of the cell has been read or an abort has been signaled.

Pin Name	Type	Pin No.	Function
BUSYB	Output	K29	The BUSYB output is asserted while a microprocessor initiated access to external RAM data is pending (for internal RAM accesses, a microprocessor must poll the appropriate BUSY register bit). The BUSYB output is deasserted after the access has been completed. A microprocessor access to external SRAM is typically completed within 37 ISYSCLK or ESYSCLK cycles. If the ISTANDBY and ESTANDBY bits in the Master Configuration are set to logic 1, the access time is reduced to less than 5 ISYSCLK or ESYSCLK cycles. The polarity of the BUSYB output is programmable and defaults to active low. The BUSYB signal should be treated as a glitch-free asynchronous output.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	J31 J30 J29 H31 H30 J28 H29 G31 G30 H28 G29 F31 F30 F29 E31 E30	The bi-directional data bus, D[15:0] is used during ATLAS Microprocessor Interface Port register reads and write accesses. D[15:8] should contain the most significant 8-bits and D[7:0] should contain the least significant 8-bits of a word. The bi-directional data bus, D[15:0], is a 5V tolerant bus.

Pin Name	Type	Pin No.	Function
A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	C23 B23 A23 C22 D21 B22 A22 C21 D20 B21 A21 C20	A[11:0] selects specific Microprocessor Interface Port registers during ATLAS register accesses. A[11] is the Test Register Select (TRS) address pin. TRS selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses. A[11:0] is a 5V tolerant input bus.
ALE	Input Input Internal Pull-Up	A24	ALE is active high and latches the address bus, A[11:0], when low. When ALE is high, the internal address latches are transparent. It allows the ATLAS to interface to a multiplexed address/data bus. ALE is a 5V tolerant input.
HALFSECCLK	Input	AK22	The 0.5 second clock (HALFSECCLK) input provides precise timing for events such as the generation of CC, RDI and AIS cells and the declaration and clearing of the AIS, RDI and CC alarms. By default, the initiation of 0.5 second events is based on the ISYSCLK period; therefore, the HALFSECCLK input is ignored. If the SEL1SEC register bit is logic 1, the HALFSECCLK input becomes the source of the half second clock. HALFSECCLK must be glitch free and may be treated as an asynchronous input. HALFSECCLK is a 5V tolerant input.
INTB	Open Drain Output	K31	The Interrupt Request (INTB) output goes low when an ATLAS interrupt source is active and that source is unmasked. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.

Pin Name	Type	Pin No.	Function
RSTB	Schmitt Trigger Input Internal Pull-Up	A25	The active low reset (RSTB) signal provides an asynchronous ATLAS reset. RSTB is a Schmitt trigger input with an integral pull up resistor. When RSTB is forced low, all ATLAS registers are forced to their default states. RSTB is a 5V tolerant input.
IEEE P1149.1 (JTAG) Interface: 5 pins			
TCK	Input Internal Pull-up	L30	The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port. TCK is a 5V tolerant input.
TMS	Input Internal Pull-Up	M29	The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull up resistor. TMS is a 5V tolerant input.
TDI	Input Internal Pull-Up	L31	The test data input (TDI) signal carries test data into the ATLAS via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull-up resistor. TDI is a 5V tolerant input.
TDO	Tristate	M28	The test data output (TDO) signal carries test data out of the ATLAS via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is tri-stated except when the scanning of data is in progress
TRSTB	Schmitt Trigger Input Internal Pull-Up	L29	The active low test reset (TRSTB) signal provides an asynchronous ATLAS test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. The JTAG TAP controller must be initialized when the ATLAS is powered up. If the JTAG port is not used, TRSTB must be connected to the RSTB input or GND. TRSTB is a 5V tolerant input.
VBIAS	Input	B25	+5V Bias (VBIAS). The VBIAS input is used to implement the 5V tolerance on the inputs of the Microprocessor and JTAG interfaces Interface. If 5 volt tolerance is not required, VBIAS should be connected to the 3.3 volt power supply (i.e. the same as VDD).

Pin Name	Type	Pin No.	Function
VDD	Power	A1 A31 B2 B30 C3 C29 D4 D7 D10 D14 D18 D22 D25 D28 G4 G28 K4 K28	The VDD power pins should be connected to a well-decoupled +3.3V DC supply.

Pin Name	Type	Pin No.	Function
VDD	Power	P4 P28 V4 V28 AB4 AE4 AB28 AE28 AH4 AH7 AH10 AH14 AH18 AH22 AH25 AH28 AJ3 AJ29 AK2 AK30 AL1 AL31	Continued

Pin Name	Type	Pin No.	Function
GND	Ground	A2 A3 A14 A17 A18 A29 A30 B1 B3 B17 B29 B31 C1 C2 C4 C28 C30 C31 D3 D29 P1 P31 R1	The ground pins should be connected to GND.

Pin Name	Type	Pin No.	Function
GND	Ground	R2 U30 U31 V1 V31 AH3 AH29 AJ1 AJ2 AJ4 AJ30 AJ28 AJ31 AK1 AK3 AK15 AK29 AK31 AL2 AL3 AL14 AL15 AL18 AL29 AL30	Continued.

Notes on Pin Description:

1. All S/UNI-ATLAS inputs and bi-directional pads present minimum capacitive loading and operate at TTL logic levels.

2. Inputs RSTB, ALE, TCK, TMS, TDI and TRSTB have internal pull-up resistors.

3. The recommended power supply sequencing is as follows:

   3.1 During power-up, the voltage on the VBIAS pin must be kept equal to or greater than the voltage on the VDD pins to avoid damage to the device.

   3.2 The VDD power must be applied before input pins are driven or the input current per pin be limited to less than the maximum DC input current specification. (20 mA)

   3.3 Power down the device in the reverse sequence.

8 FUNCTIONAL DESCRIPTION

The PM7324 S/UNI-ATM Layer Solution (S/UNI-ATLAS or abbreviated as ATLAS) is a monolithic integrated circuit that implements the ATM Layer functions that include fault and performance monitoring, header translation and cell rate policing. The S/UNI-ATLAS is a bi-directional part which is intended to be situated between the physical layer (PHY) devices and a switch core in the ingress side, and a traffic shaper and the PHY devices in the egress side. The S/UNI-ATLAS supports a sustained aggregate throughput of $1.42x10^6$ cells/s in both the ingress and egress directions. The S/UNI-ATLAS uses external SRAM to store per-VPI/VCI data structures. The device is capable of supporting up to 65536 connections.

The Ingress Input Cell Interface can be connected to up to 32 PHY devices through a SCI-PHY compatible bus. The 53-byte ATM cell is encapsulated in a data structure that can contain prepended or postpended routing information. Received cells are buffered in a four cell deep FIFO. All idle cells, physical layer and unassigned cells are discarded. For the remaining cells, a subset of ATM header and appended bits is used as a search key to find the VC Table record for the virtual connection. If a connection is not provisioned and the search terminates unsuccessfully as a result, the cell is discarded and the VPI/VCI value of the cell is captured. If the search is successful, subsequent processing of the cell is dependent on the contents of the cell and configuration fields in the VC Table Record.

The S/UNI-ATLAS performs header translation, if so configured. The ATM header is replaced by the contents of fields in the VC Table Record for that connection. The VCI contents are passed through transparently for VPC connections. In the Ingress direction appended bytes can be replaced, added or removed. The egress direction only supports translation of the VCI, VPI or both.

If the S/UNI-ATLAS is the end point for a F4 or F5 OAM flow, the OAM cells are terminated and processed. If the S/UNI-ATLAS is not the end point, the OAM cells are passed to the Ingress/Egress Output Cell Interface with an optional copy passed to the Microprocessor Cell Interface FIFO. The reception of AIS or RDI cells results in the appropriate alarms (segment or end-to-end alarm). The interrupts corresponding to the alarm bits can be masked on a per-connection basis. When configured as a sink of PM cells, upon the arrival of a Forward Monitoring cell, error counts are updated and a Backward Reporting cell is optionally generated and routed to the Output Cell Interface in the opposite direction. When configured as a source of PM cells, the S/UNI-ATLAS generates a Forward Monitoring cell when the user cell block size (programmable on a per-connection basis) is reached. Note, the insertion of PM cells is paced so that bursts of generated cells will not cause a backup in the Ingress or Egress directions. Both the Egress and Ingress interfaces allow for the generation and monitoring of PM flows. All generated Backward Reporting cells are output to the Backward OAM Cell Interfaces so they may be inserted in the opposite flow direction (e.g. if a Forward Monitoring cell is terminated in the Ingress direction, a Backward Reporting PM cell will be generated by the Ingress Cell Processor into the Ingress Backward OAM Cell Interface so that it may be inserted in the Egress path), while generated Forward Monitoring cells are output to the Output Cell Interface of the normal flow direction.

Cell rate policing is supported in the Ingress direction through a dual leaky bucket policer which conforms to the ITU-T I.371 Generic Cell Rate Algorithm for each connection. Each cell that violates the traffic contract can be noted, tagged or discarded. To allow full flexibility, each GCRA instance can be programmed to police any combination of user cells, OAM cells, Resource Management cells, high priority cells or low priority cells. On a per-connection basis, one of eight policing configurations may be chosen. Three 16-bit non-compliant cell counts are provided on a per-connection basis. These counters are programmable and allow for the counting of, for example, dropped CLP0 cells, dropped CLP1 cells and tagged CLP0 cells.

The S/UNI-ATLAS also supports a single leaky bucket policer on a per-PHY basis (up to 32 instances can be programmed). The PHY GCRA can police any or all connections on a particular PHY. Each PHY GCRA has a programmable action field that allows violating cells to be noted, tagged or discarded. Three configurable non-compliant cell counts (on each PHY GCRA) are also provided. Each PHY GCRA can be programmed to police any combination of user cells, OAM cells, Resource Management cells, high priority cells or low priority cells. Any one of four PHY policing configurations may be chosen.

The Ingress Output Cell Interface can be connected to the switch core through a single PHY extended cell format SCI-PHY compatible bus interface. Cells are stored in a four cell deep FIFO until the downstream devices are ready to accept them.

The 16-bit Microprocessor Interface is provided for device configuration, control and monitoring by an external microprocessor. This interface provides access to the external SRAM to allow creation of the data structure, configuration of individual connections, and monitoring of the connections. The Microprocessor Cell FIFO gives access to the cell stream in both the ingress and egress directions. Programmed cell types can be routed to the Microprocessor Cell FIFO (and subsequently read through the Microprocessor cell interface). The microprocessor can send cells to the Ingress Output Cell Interface and the Egress Output Cell Interface.

The Egress Input Cell Interface can emulate up to 32 PHY devices through an 8 or 16 bit SCI-PHY compatible bus (compatible with UTOPIA Level1 and UTOPIA Level 2). This interface can be configured for up to 4 PHY direct addressing, or 32 PHY polled addressing. Received cells are buffered in a per-PHY four cell deep FIFO (i.e. a 4 cell FIFO is provided for each of the 32-PHY devices). All Physical Layer and unassigned cells are discarded. For all other cells, a programmable 16-bit location in the header, prepend words or postpend words is used to provide a direct lookup into the VC Table Record for the virtual connection. The apparent FIFO depth control can be configured to control the early deassertion of the Egress Input Cell Interface cell available signal. The apparent FIFO depth can be configured from 1 to 4 (default) cells.

Egress cell processing includes F4 and F5 OAM-PM monitoring and generation, and F4 and F5 OAM-FM monitoring and generation. The performance monitoring statistics are held in an on-chip RAM that can be accessed through the Microprocessor port. Two programmable 32-bit cell counts are also maintained on a per-connection basis. The Egress Cell Processor requires a 50 MHz ESYSCLK frequency to sustain a 622 Mbit/s throughput.

The Egress Output Cell Interface is a 8 or 16 bit SCI-PHY compatible interface which can address up to four PHY devices using direct addressing or up to 32 PHY devices using polled addressing. Cells are stored in a per-PHY four cell deep FIFO and subsequently transferred to a PHY device. The per-PHY cell buffering eliminates head-of-line blocking. The Egress Output Cell Interface can also be configured to provide the early deassertion of its internal cell available signal (to the Egress Cell Processor). The apparent FIFO depth can be configured from 1 to 4 (default) cells.

The S/UNI-ATLAS is implemented in low power 0.35 micron 3.3 Volt CMOS technology. All SCI-PHY interfaces are 3.3 Volt only, the SRAM interfaces are 3.3 Volt only, and the Microprocessor Interface and JTAG pins are 3.3V/5V tolerant. The S/UNI-ATLAS is packaged in a 432-pin Super BGA package.

8.1 Ingress VC Table

The Ingress VC Table is a 15-row 64-bit data structure that contains context information for up to 65536 connections. The Ingress VC Table is used for connection identification, connection configuration and connection processing functions. The connection identification fields of the VC Table are located in the first two rows of the structure, and the remaining rows are used for connection configuration and cell processing.

The Ingress VC Table is a total of 960 bits per connection, however, not all rows need be used if features are disabled. Unused bits should be set to zero for backward compatibility with future devices within the ATLAS family.

Table 1 Ingress VC Table

ISA [19:16]	63															0
0000	Unused (8)			Selector (6)			Left Leaf (1)		Left Branch (16)				Right Leaf (1)		Right Branch (16)				Primary Table Record (16)	
0001	CLPcc_en (1)	F4toF5AIS (1)		PHYID (5)		Unused (1)		PM Active2 (1)		PM Addr2 (7)		PM Active1 (1)		PM Addr1 (7)		NNI (1)	Field B (11)		VPI (12)	VCI (16)
0010	Status (8)			Configuration (14)				Internal Status (17)				OAM Configuration (9)				VPC Pointer (16)				
0011	COCUP (1)		Reserved (3)				TAT2 (30)								TAT1 (30)					
0100	GFR (1)		Police Configuration (3)			Action2 (2)		Action1 (2)		I2 (14)			L2 (14)			I1 (14)			L1 (14)	
0101	PHY Police (1)		Remaining Frame Count (11)				Violate (1)		GFR State (3)		Non-Compliant3 (16)				Non-Compliant2 (16)				Non-Compliant1 (16)	
0110	Ingress Cell Count 2 (32)															Ingress Cell Count 1 (32)				
0111	Header (40)															UDF (8)			PrePo1 (8)	PrePo2 (8)
1000	PrePo3 (8)		PrePo4 (8)			PrePo5 (8)		PrePo6 (8)		PrePo7 (8)			PrePo8 (8)			PrePo9 (8)			PrePo10 (8)	
1001	Alternate Ingress Cell Count 2 (32)															Alternate Ingress Cell Count 1 (32)				
1010	Unused (32)												Unused (5)		Maximum Frame Length (11)		Received Segment AIS Defect Type (8)		Received End-to-End AIS Defect Type (8)	
1011	Received End-to-End AIS Defect Location [127:64] (Most significant bytes)																			
1100	Received End-to-End AIS Defect Location [63:0] (Least significant bytes)																			
1101	Received Segment AIS Defect Location [127:64] (Most significant bytes)																			
1110	Received Segment AIS Defect Location [63:0] (Least significant bytes)																			

8.2 Connection Identification

8.2.1 Ingress Connection Identification

In the ingress direction, the ATLAS makes use of a flexible approach to identify incoming cells and to determine which record in the Ingress VC Table with which they are associated. The ATLAS identifies the VC record of each connection by searching the Ingress VC Table using selected portions of the cell header, prepend, postpend and the PHY address. To do this, the ATLAS creates an internal *Routing Word*, which is the concatenation of the cell header, cell prepend and cell postpend. The ATLAS is programmed to select portions of the Routing Word plus the PHY address to create a *VC Search Key*. The VC Search Key, therefore, consists of portions of the cell's header, prepend, postpend and PHY address.

The figure below illustrates the Routing Word and VC Search Key construction. This figure is not intended to imply any restrictions on the positioning of Field A and Field B. These fields may occur anywhere within the appended octets or the ATM header. The Primary Key and Secondary Key may also intersect.

Figure 2 VC Search Key Composition

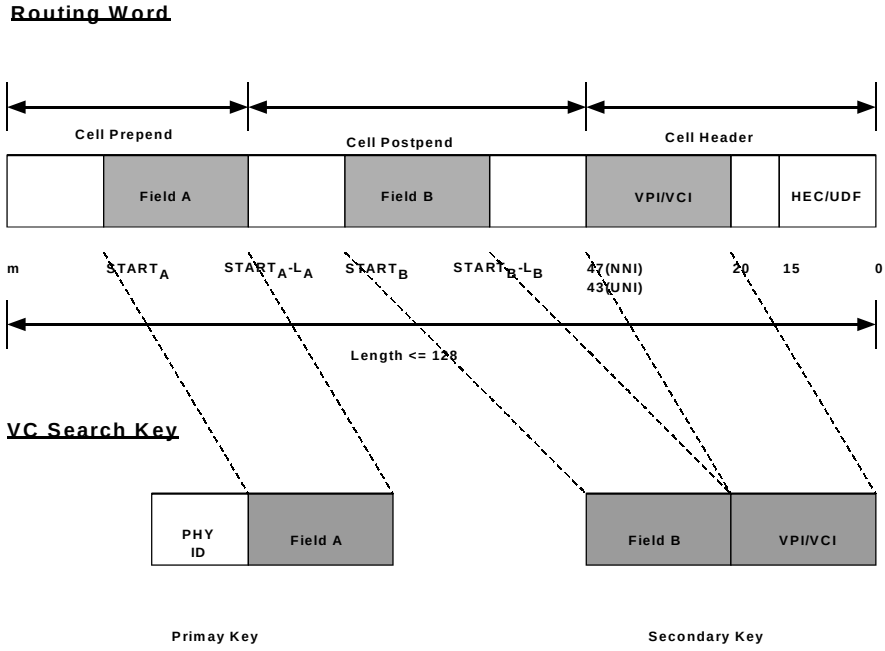


Table 2 Ingress VC Table Cell Fields

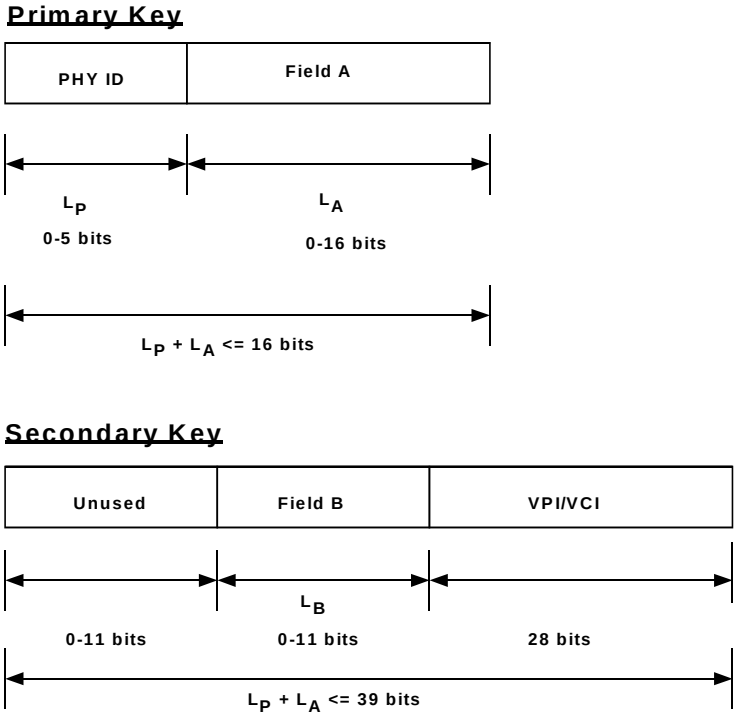
Name	Description
PHYID[4:0]	Indicates the Physical Layer device that this connection is associated with. This field is used to determine the destination of all generated RDI and Backward Reporting PM cells. This field is also used in determining the per-PHY statistics.
Field B[10:0]	Contains the value of the Secondary Search key field B from the cell header.
NNI	If this bit is a logic 1, the NNI bit identifies the connection as belonging to a Network-to-Network Interface. If this bit is a logic 0, the connection is part of a UNI.
VPI[11:0]	The VPI field identifies the Virtual Path of the connection. If the connection is a UNI connection (as defined by the NNI bit of the VC Table), the four MSBs of the VPI field are the GFC bits. The VPI field represents the VPI (and GFC, if the connection is a UNI connection) which will be inserted in all generated OAM cells.
VCI[15:0]	The VCI field identifies the Virtual Channel of the connection. If the connection is a VPC (F4) connection, then this field shall be encoded as all zeros. If the VCI field is non-zero, then the connection is a VCC (F5) connection. This VCI field represents the VCI which will be inserted in all F5 generated OAM cells If this field is encoded as all zeros, the generated OAM cells use the correct VCI to indicate whether they are segment OAM cells (VCI=3) or end-to-end OAM cells (VCI=4).

The ATLAS divides the VC Search Key into two search keys – the Primary Key and the Secondary Key. The Primary Key is 0 to 16 bits long. It is constructed from two fields – the *PHY ID* field and *Field A*. The PHY ID field and Field A can be programmed to be 0-5 bits and 0-16 bits long, respectively. The PHY ID field is the SCI-PHY address and must, therefore, include sufficient bits to encode all the PHYs at the PHY Layer interface of the ATLAS. Field A starts at location STARTA of the Routing Word, and has length L_A. The number of bits in Field A plus the number of bits in the PHY ID field must be less than or equal to 16. Field A and the PHYID are always LSB justified within the Primary Key (any unused MSBs are set to logic 0).

The Secondary Key is 39 bits long and is composed of two fields. The first field, *Field B*, is 0 to 11 bits long and may start anywhere in the Routing Word. Field B parameters include starting position, STARTB and length, L_B. The second field is the 28-bit VPI/VCI. This field is always taken from the cell header.

Field B and the VPI/VCI field are “right justified” i.e. shifted towards the LSB, within the Secondary Key.

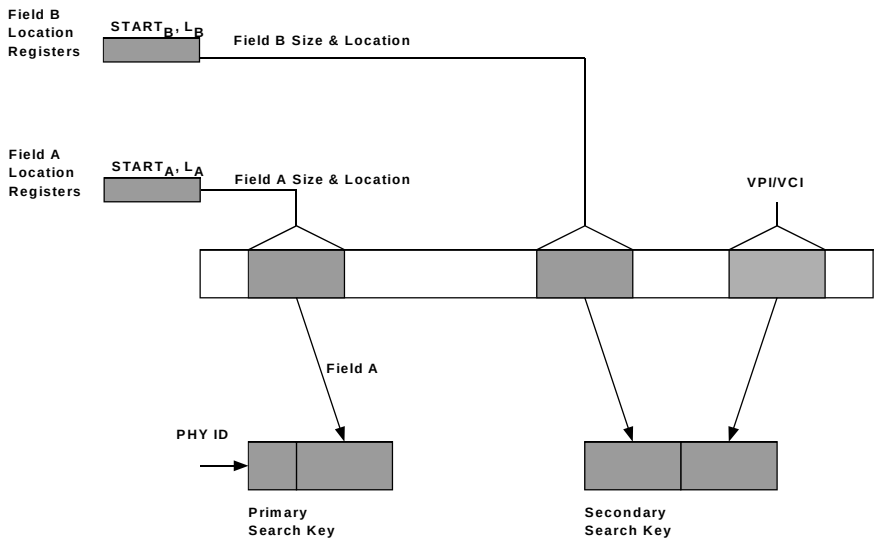
Figure 3 Parameters of the Primary Key and Secondary Key



The user can program the ATLAS with the length and position parameters of Fields A and B.

The figure below provides a representation of how the ATLAS creates the Primary and Secondary Search Keys. Field location and length registers are used to select Field A and Field B from the Routing Word. Field A and the PHY ID are concatenated to form the Primary Search Key. Field B and the VPI/VCI field are concatenated to form the Secondary Search Key.

Figure 4 Search Key locations within the Routing word



Once the search keys are assembled, the Primary Search Key is first used to address an external direct look-up table (this is the Primary Table Record of the Ingress VC Table at ISA[19:16]=0000). This table occupies 2^n memory locations, where $n = L_P + L_A$, i.e. the length of the Primary Search Key. The result of this direct lookup is the address of a root node of a search tree. From this root node, the Secondary Search Key is used by a patented search algorithm to find the Ingress VC Table record address of the connection. The ATLAS requires this table record for cell processing functions. If the search process does not lead to the successful identification of the cell concerned (i.e. the contents of the Ingress VC Table address returned do not match the Secondary Search Key contents), the cell is declared to be invalid, and will not be output. Optionally, the cell may be routed to the Ingress Microprocessor Cell Interface for error logging.

The length of time required to perform the VC Table search is variable. Since the Primary Search Key is used in a direct lookup, only one cycle is required to process the Primary Search Key. The Secondary Search Key processing time is highly dependent on the key's contents, but the maximum number of processing cycles required is equal to the number of bits in the Secondary Search Key which must be examined to make a unique identification. Some VPI and VCI bits may always be zero; therefore, they need not be used in the search. In some instances, the Primary Search Key may overlap the Secondary Search Key; therefore, the intersecting bits are only required for the confirmation of a search. If the number of bits used by the binary search is no greater than 16, a sustained rate of 1.42×10^6 cells/s is guaranteed. The general expression for guaranteed throughput is given below:

$$\text{Throughput} = \frac{1}{(17 + \text{max. binary tree depth})(\text{ISYSCLK period})} \text{ cells/s}$$

A total of 17 ISYSCLK cycles are dedicated to cell processing (this represents the worst-case number of ISYSCLK cycles required for cell processing). The total number of cycles allocated for searching is 18 (one for the Primary Search, sixteen for the binary search and one cycle for the verification process).

Note, however, if the binary tree depth is less than 10, the throughput formula becomes:

$$\text{Throughput} = \frac{1}{(\text{cell word length})(\text{ISYSCLK period})} \text{ cells/s}$$

where the cell word length is the number of 16-bit words in the cell.

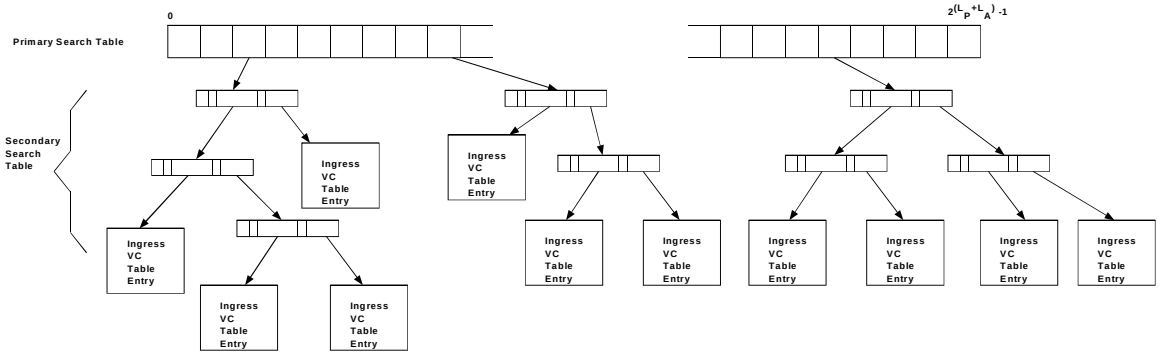
The second word of the Ingress VC Table contains the Secondary Search Key and the NNI bit. The Secondary Search Key (Field B, VPI and VCI) field is used to confirm whether or not the incoming cell belongs to a provisioned virtual connection. Any unused bits within this word must be set to zero. The NNI bit identifies if the virtual connection belongs to a Network-Network Interface. If the NNI bit is set to zero, the connection is part of a UNI, which means that the four MSBs of the VPI are excluded from the Secondary Key verification. If the VCI field in the Ingress VC Table is set to all zeros, this signifies the connection is a VPC, and the VCI field is to be ignored.

8.3 Search Table Data Structure

The Primary and Secondary Search Key table fields reside in the Ingress VC Table. The Primary Table Record entry is located in the least significant 16-bits of ingress VC Table locations with ISA[19:16]=0000, and requires $2^{(LP + LA)}$ words of memory. The Secondary Search Key entry is located at locations with ISA[19:16]=0001 and its size is bounded by the number of virtual connections supported.

The figure below illustrates the relationship between the Primary Search Table Key, Secondary Search Table Key and the Ingress VC Table.

Figure 5 Atlas Search Table Structure



The following gives the immutable coding rules for the search data structures. The coding supports numerous possible algorithms, but the Operations Section presents an algorithm that is optimized for most applications.

8.3.1 Primary Search Table

The Primary Search Table contains an array of pointers that point to the roots of binary trees. The table is directly indexed by the contents of the Primary Search Key, as defined above.

The entire Primary Search Table must be initialized to all zeros. A table value of zero represents a null pointer; therefore, the initial state means no provisioned connections are defined. If a connection is added which results in a new binary search tree (i.e. it is the only connection associated with a particular Primary Search Key), the appropriate Primary Search Table location must point to the newly created binary search tree root. If the last connection with a particular Primary Search Key is removed, the associated Primary Search Table location must be set to all zeros.

8.3.2 Secondary Search Key Table

The Secondary Search Table consists of a set of binary search trees. Each tree's root is pointed to by an entry in the Primary Search Tree. Each node in the tree is represented by a 40 bit data structure located at ISA[19:16]=0000. The fields of the Secondary Search Table are described below.

63						0
Unused (8)	Selector (6)	Left Leaf (1)	Left Branch (16)	Right Leaf (1)	Right Branch (16)	Primary Search Key (16)

Name	Description
Selector	The Selector field is a 6 bit field which is the index of the Secondary Search Key bit upon which the branching decision of the binary search is based. An index of zero represents the LSB. If the selected bit is a logic 1, the Left Leaf and Left Branch fields are subsequently used. Likewise, if the selected bit is a logic 0, the Right Leaf and Right Branch are subsequently used. Typically, the Selector value decreases monotonically with the depth of the tree, but other search sequences are supported by the flexibility of this bit.
Left Leaf	This flag indicates if this node is a leaf. If Left Leaf is a logic 1, the left branch is a leaf and the binary search terminates if the decision bit is a logic 1. If Left Leaf is a logic 0, the Left Branch value points to another node in the binary tree.
Left Branch	The pointer to the node accessed if the decision bit is a logic 1. If Left Leaf is a logic 1, Left Branch contains the 16-bit address identifying the VC Table Record for that connection. If Left Leaf is a logic 0, Left Branch contains the (up to) 16-bit address pointing to another Secondary Search Table entry.
Right Leaf	This flag indicates if this node is a leaf. If Right Leaf is a logic 1, the Right Branch is a leaf and the binary search terminates if the decision bit is a logic 0. If Right Leaf is a logic 0, the Right Branch field points to another node in the binary tree.
Right Branch	The pointer to the node accessed if the decision bit is a logic 0. If Right Leaf is a logic 1, Right Branch contains the (16-bit address identifying the VC Table Address for that connection. If Right Leaf is a logic 0, Right Branch contains the 16-bit address pointing to another Secondary Search Table entry.

The above encoding defines the binary search tree recursively.

The following special cases must be respected:

1. A binary tree with only one connection must have both the Left and Right Branches pointing to the solitary VC Table Record. Both the Left Leaf and Right Leaf flags must be a logic 1.

2. If the Primary Search Table is not used (i.e. $L_P = L_A = 0$), the root of the single resulting binary search tree must be located at the Secondary Search Table entry at ISA[15:0]=0x0000.

3. If the Primary Search Table is in use, no root node shall use location ISA[15:0]=0x0000, although this location may be used for nodes at least one level down. A value of 0x0000 in the Primary Table Record field represents a null pointer.

8.4 Ingress Cell Processing

After an ingress VPI/VCI search has been completed for a cell, the resulting actions are dependent upon the cell contents and the Ingress VC Table Record. Particular features such as policing and OAM cell processing can be disabled on a global and per-connection basis.

The Ingress VPI/VCI search results in a ISA[15:0] value which points to an Ingress VC Table record. The fields of each VC Table record are described below. If fewer than 32768 connections are supported, the most significant bits of ISA[15:0] and the associated memory may not be required. The individual fields of the Ingress VC Table record are accessed by the ISA[19:16] outputs. If particular features are disabled, the associated fields are unused and no memory need be provided for them.

When a new VC is provisioned, the management software must initialize the contents of the VC Table record. Once provisioned, the management software can retrieve the contents of the VC Table record.

Table 3 Ingress VC Table Status Field

The Status field of the Ingress VC Table is described below.

Bit	Name	Description
7	Reserved	This bit should be set to zero when the connection is setup.
6	AIS_end_to_end alarm	This bit becomes a logic 1 upon receipt of a single end-to-end AIS cell. The alarm status is cleared upon the receipt of a single user or end-to-end CC cell, or if no end-to-end AIS cell has been received within the last 2.5 +/- 0.5 sec.
5	AIS_segment alarm	This bit becomes a logic 1 upon receipt of a single segment AIS cell. The alarm status is cleared upon the receipt of a single user or segment CC or end-to-end CC cell, or if no segment AIS cell has been received within the last 2.5 +/- 0.5 sec.
4	RDI_end_to_end alarm	This bit becomes a logic 1 upon receipt of a single end-to-end RDI cell. This bit is cleared if no end-to-end RDI cell has been received within the last 2.5 +/- 0.5 sec.
3	RDI_segment alarm	This bit becomes a logic 1 upon receipt of a single segment RDI cell. This bit is cleared if no segment RDI cell has been received within the latest 2.5 +/- 0.5 sec.
2	CC_end_to_end alarm	This bit becomes a logic 1 if no user or end-to-end CC cell has been received within the last 3.5 +/- 0.5 sec. This bit is cleared upon receipt of a user cell, or end-to-end CC cell.
1	CC_segment alarm	This bit becomes a logic 1 if no user, segment CC or end-to-end CC cell has been received within the last 3.5 +/- 0.5 sec. This bit is cleared upon receipt of a user cell, segment CC cell or end-to-end CC cell.
0	XPOLICE	The Excessive Policing bit is a logic 1 if any of the per-VC non-compliant cell counts on this connection is greater than 32767 (i.e. the MSB on one or more of the non-compliant cell counts is set to logic 1). This bit indicates that the non-compliant cell counts should be read and cleared to avoid counter saturation.

Table 4 Ingress VC Table Configuration Field

The Configuration field of the Ingress VC Table is shown below.

Bit	Name	Description
13	Active	Identifies the connection as active. This bit is checked during the ATLAS background processes to determine if the connection is still active. It is the responsibility of the management software to set and clear this bit during activation and deactivation, respectively, of a connection. Cells received on a connection for which Active is a logic 0 will be dropped, with an optional copy to the Ingress Microprocessor Cell Interface if the InactiveToUP register bit is a logic 1. These cells will not be counted by the Ingress Cell Processor.
12	SegmentFlow	The SegmentFlow bit indicates whether or not an F5 (VCC) connection is part of a defined segment. This bit is only significant if the connection is an F5. When an F4 (VPC) is terminated (i.e. there is an F4 connection end-point which is associated with this F5 connection) at the Ingress of the ATLAS, the F5 connections are switched. If the SegmentFlow bit is logic 1, the F5 connection is considered to be part of a segment flow. Thus, if an F4 End-to-End or Segment AIS cell is terminated by the F4 connection associated with this F5 connection, an F5 Segment AIS cell will be generated while the F4 connection is in AIS alarm. If the SegmentFlow bit is logic 0, an F5 End-to-End AIS cell will be generated when the F4 connection is in AIS alarm. The generation of F4 to F5 AIS cell generation process can be disabled by using setting the F4toF5AIS bit at ISA[19:16]=0001 to logic 0. The SegmentFlow bit should not be set to a logic 1 at segment end-points.
11	Count_Type	This bit is used to address one of two possible combinations of programmable cell counts. If this bit is a logic 0, the Cell Count 1[31:0] and Cell Count 2[31:0] are programmed from the settings in the Ingress Cell Counting Configuration 1 register 0x236. If this bit is a logic 1, the cell counts are derived from the settings in Ingress Cell Counting Configuration 2 register 0x237.
10	FM_interrupt_enable	This bit enables the generation of segment and end-to-end AIS, RDI and Continuity Check alarm interrupts. If this bit is logic 1, the ATLAS will assert segment and end-to-end AIS,

		RDI and Continuity Check interrupts, as required, regardless of whether or not the ATLAS is a connection end-point (segment or end-to-end) for the connection. The ATLAS would normally be programmed to assert interrupts at connection end-points only. If this bit is logic 0, no alarm interrupts will be asserted, however, the Status field will reflect the connection state.
9	LB_to_UP	If this bit is a logic 1, all Loopback cells are copied to the Ingress Microprocessor Cell Interface. The Drop_LB bit determines whether or not Loopback cells are output to the Ingress Output Cell Interface.
8	Drop_LB	If this bit is a logic 1, Loopback cells are not output to the Ingress Output Cell Interface. The LB_to_UP bit determines whether or not Looopback cells are output to the Ingress Microprocessor Cell Interface.
7	FM_to_UP	If this bit is a logic 1, all Fault Management cells (AIS, RDI, CC) are copied to the Ingress Microprocessor Cell Interface. The Segment_Point and End_to_end_point bits determines whether or not FM cells are output to the Ingress Output Cell Interface.
6	Drop_UP	If this bit is a logic 1, all cells are output to the Ingress Microprocessor Cell Interface only (not to the Ingress Output Cell Interface). The setting of this bit supercedes all other routing bits. If the Drop_UP bit is set, the ATLAS will not output generated OAM cells (AIS, RDI, CC, Fwd PM and Bwd PM) cells on this connection.
5	XPOLI_interrupt_enable	The Excessive Policing Interrupt enable bit controls whether or not the ATLAS will assert the XPOLI interrupt. If this bit is a logic 1, then the ATLAS will assert the XPOLI interrupt whenever any of the per-VC non-compliant cell counts on this connection becomes greater than 32767 (i.e. the MSB of one or more of the non-compliant cell counts first set). If this bit is a logic 0, the XPOLI interrupt will not be asserted.
4:1	Defect_Type[3:0]	The Defect_Type[3:0] bits choose which one of 16 possible Defect Type settings (maintained in the Defect Type 1-16 registers 0x226 – 0x22D in the Ingress Cell Processor). For example, if Defect_Type[3:0]=0000, the Defect Type 1 setting will be used in generated AIS cells. RDI cells which are generated as a result of the CC_RDI process, the per-PHY register configurations 0x224, 0x225 (i.e. a forced generation of an RDI cell) and RDI cells which are generated as a result of the Send_RDI_Segment or Send_RDI_end_to_End bits also this setting to determine which Defect Type will be inserted.
0	COS_enable	If this bit is a logic 1, any change of alarm state on this

		connection will result in a write to the Change of State FIFO (if enabled via the COS register bit of the Ingress Cell Processor Configuration register 0x200). If this bit is a logic 0, no writes will be made to the COS FIFO.

The OAM Configuration field of the Ingress VC Table is described below.

Table 5 Ingress VC Table OAM Configuration Field

Bit	Name	Description
8	Send_AIS_segment	If this bit is a logic 1, a segment AIS cell is generated once per second (nominally).
7	Send_AIS_end_to_end	If this bit is a logic 1, an end-to-end AIS cell is generated once per second (nominally).
6	Send_RDI_segment	If this bit is a logic 1, a segment RDI cell is generated once per second (nominally).
5	Send_RDI_end_to_end	If this bit is a logic 1, an end-to-end RDI cell is generated once per second (nominally).
4	CC_RDI	If this bit is a logic 1, RDI cells are generated at one second intervals upon the declaration of a CC_alarm and the state of the AUTORDI bit in register 0x200. The type of RDI cell (segment or end-to-end) generated depends upon the alarm declaration (segment CC alarm or end-to-end CC alarm) and whether or not the ATLAS is an end point (end-to-end point, segment end point, or both). If the ATLAS is not an end point, the RDI cell will not be generated. If both the segment and end-to-end CC alarms are asserted, then both types of RDI cells will be generated if the ATLAS is configured as both a segment end point and an end-to-end point. RDI cells which are generated as a result of the CC_RDI function have the Defect Location and Defect Type values which are programmed in the ATLAS registers OAM Defect Type0 and 1, 0x226-0x22D and OAM Defect Location Octets 0 & 1, 0x22E-0x235, inserted in the Defect Location and Defect Type fields of the cells.
3	CC_Activate_Segment	Enables Continuity Checking on segment flows. If the ForceCC bit in the Cell Processor Configuration Register 0x238 is logic 0, then when no user cells are transmitted over a 1.0 second (nominal) interval, a segment CC OAM cell is generated. The segment CC cell is generated at an interval of one per second (nominally).

		If the ForceCC register bit is logic 1, then when the CC_Activate_Segment bit is logic 1, a segment CC cell will be generated at an interval of once per second (nominally), regardless of the flow of user cells. ITU-T I.610 9.2.1.1.2, 9.2.2.1.2.
2	CC_Activate_End_to_End	Enables Continuity Checking on end-to-end flows. If the ForceCC bit in the Cell Processor Configuration Register 0x238 is logic 0, then when no user cells are transmitted over a 1.0 second (nominal) interval, an end-to-end CC OAM cell is generated. The end-to-end CC cell is generated at an interval of one per second (nominally). If the ForceCC register bit is logic 1, then when the CC_Activate_End_to_End bit is logic 1, an end-to-end CC cell will be generated at an interval of once per second (nominally), regardless of the flow of user cells. ITU-T I.610 9.2.1.1.2, 9.2.2.1.2.
1	Segment_Point	Defines the ATLAS as a Segment termination point. For F4 connections (VPCs), all cells with VCI = 3 are terminated and processed. For F5 connections (VCCs), all cells with PTI = 100 are terminated and processed.
0	End_to_End_Point	Defines the ATLAS as an End-to-End termination point. For F4 connections (VPCs), all cells with VCI = 4 are terminated and processed. For F5 connections (VCCs), all cells with PTI = 101 are terminated and processed. An End-to-End termination point wil also terminate all Segment connections, since by definition the End-to-End point is the end point for all OAM traffic.

The Ingress Internal Status field contains connection state information. The count fields decrement at a rate of once per second. The Ingress Internal Status field is shown below.

Table 6 Ingress Internal Status Field

Bit	Name	Description
16:14	Reserved	These bits should be set to zero at connection setup.
13	Send_Seg_CC_Count	The Send_Seg_CC_Count is set to logic 1 (to provide a one second count) at connection setup time and each time the ATLAS sends a user cell on this connection. The count is decremented at one second intervals. If this count reaches zero (i.e. if the ATLAS writes back a zero at a one second boundary and

		subsequently reads a zero at the next one second boundary, indicating that no user cells have been sent on this connection), then a Segment CC cell is generated, if the CC_Activate_Segment bit is set.
12	Send_End_CC_Count	The Send_End_CC_Count is set to logic 1 (to provide one second count) at connection setup time and each time the ATLAS sends a user cell on this connection. The count is decremented at one second intervals. If this count reaches zero (i.e. if the ATLAS writes back a zero at a one second boundary and subsequently reads a zero at the next one second boundary, indicating that no user cells have been sent on this connection), then an End-to-End CC cell is generated, if the CC_Activate_End_to_End bit is set.
11:10	Seg_CC_Count[1:0]	The Seg_CC_Count is set to a value of 3 (to provide a 3.5 +/- 0.5 sec count) upon receipt of a user or segment CC cell, and decremented at one second intervals. If the Seg_CC_Count reaches 0, the CC_segment Alarm is raised.
9:8	End_CC_Count[1:0]	The End_CC_Count is set to a value of 3 (to provide a 3.5 +/- 0.5 sec count) upon receipt of a user or end-to-end CC cell, and decrements at one second intervals. If the End_CC_Count reaches 0, the CC_end_to_end Alarm is raised. ITU-T I.610 9.2.1.1.2, 9.2.2.1.2
7:6	Seg_RDI_Count[1:0]	The Seg_RDI_count is set to a value of 3 (to provide a 2.5 +/- 0.5 sec count) upon receipt of a segment RDI cell, and decrements at one second intervals. If the Seg_RDI_Count reaches 0, the RDI_segment Alarm is cleared.
5:4	End_RDI_Count[1:0]	The End_RDI_Count is set to a value of 3 (to provide a 2.5 +/- 0.5 sec count) upon receipt of an end-to-end RDI cell, and decrements at one second intervals. If the End_RDI_count reaches 0, the RDI_end_to_end Alarm is cleared.
3:2	Seg_AIS_Count[1:0]	The Seg_AIS_Count is set to a value of 3 (to provide a 2.5 +/- 0.5 sec count) upon receipt of a segment AIS cell, and decrements at one second intervals. If the Seg_AIS_Count reaches 0, the AIS_segment Alarm is cleared.
1:0	End_AIS_Count[1:0]	The End_AIS_Count is set to a value of 3 (to provide a 2.5 +/- 0.5 sec count) upon receipt of an end-to-end AIS cell, and decrements at one second intervals. If the End_AIS_Count reaches 0, the AIS_end_to_end Alarm is cleared.

Table 7 Ingress VC Table Miscellaneous Fields

Name	Description
F4toF5AIS	If this bit is logic 1, the F4 to F5 Fault Management scenarios listed in Table 28 F4 to F5 Fault Management Processing are enabled. If this bit is logic 0, no F5 Fault Management cells will be generated as a result of the reception of F4 Fault Management cells.
VPC Pointer[15:0]	This field is used to point to the F4-OAM connections of a terminated VPC. For a VCC connection, the VPC Pointer will contain the address of the table entry for the F4 Segment OAM VPC connection. For the segment OAM VPC connection, the VPC Pointer will contain the address of the table entry for the End-to-End OAM VPC connection. If the VPC Pointer[15:0] field points to its own address, this indicates that the current VCC is NOT part of a VPC termination. See section 8.18 for a description of the use of this field.
Ingress Cell Count 1 and 2 [31:0] Alternate Cell Count 1 and 2 [31:0]	These fields contain a configurable cell count, as described in the Count_Type table field. The Alternate count is selected via the Alternate_Count bit in the Ingress Cell Processor Configuration register 0x238. Note, these counts represent the state of the counts **before** policing. The non-compliant cell counts can be subtracted to determine the state of the counts **after** policing. Cells received on connections with the Active bit equal to logic 0 will not be counted.
Received End-to-End AIS Defect Location [127:0]	This field is used to store the Defect Location from a received end-to-end AIS cell. This field is used in end-to-end RDI cells generated via the AUTORDI function (see Ingress Cell Processor Configuration 1 register 0x200). If RDI cell generation is forced (using either the send_RDI Ingress VC table bits or the per-phy RDI register bits 0x224 and 0x225) or generated by the CC_RDI process, either the local Defect Location field programmed in the Ingress Defect Location registers, 0x22F-0x235, or an unused value (0x6A) will be used.
Received End-to-End AIS Defect Type [7:0]	This field is used to store the Defect Type from a received end-to-end AIS cell. This field is used in end-to-end RDI cells generated via the AUTORDI function (see Ingress Cell Processor Configuration 1 register 0x200). If RDI cell generation is forced (using either the send_RDI Ingress VC table bits or the per-phy RDI register bits, 0x224 and 0x225) or generated by the CC_RDI process, either the local Defect Type field programmed in the Ingress Defect Type registers, 0x226-0x22D, or an unused value (0x6A) will be used.
Received Segment AIS	This field is used to store the Defect Location from a segment AIS

Defect Location [127:0]	cell. This field is used in segment RDI cells generated via the AUTORDI function (see Ingress Cell Processor Configuration 1 register 0x200). If RDI cell generation is forced (using either the send_RDI Ingress VC table bits or the per-phy RDI register bits, 0x224 and 0x225) or generated by the CC_RDI process, either the local Defect Location field programmed in the Ingress Defect Location registers, 0x22F-0x235, or an unused value (0x6A) will be used.
Received Segment AIS Defect Type [7:0]	This field is used to store the Defect Type from a segment AIS cell. This field is used in segment RDI cells generated via the AUTORDI function (see Ingress Cell Processor Configuration 1 register 0x200). If RDI cell generation is forced (using either the send_RDI Ingress VC table bits or the per-phy RDI register bits, 0x224 and 0x225) or generated by the CC_RDI process, either the local Defect Type field programmed in the Ingress Defect Type registers, 0x226-0x22D, or an unused value (0x6A) will be used.

Table 8 Ingress VC Table Activation Fields

Name	Description
PM Active2	Indicates the PM session pointed to by PM Addr2[6:0] is active.
PM Active1	Indicates the PM session pointed to by PM Addr1[6:0] is active.
PM Addr2[6:0]	Indicates which internal PM RAM Address is to be used for a PM session.
PM Addr1[6:0]	Indicates which internal PM RAM Address is to be used for a PM session.

All fields relating to per-connection policing and per-phy policing are described in Section 8.11. This includes all fields in rows ISA[19:16] = 0011, 0100, 0101 and the Maximum Frame Length field in row ISA[19:16] = 1010.

All fields in rows ISA[19:16] = 0111 and 1000 are described in Section 8.9 Header Translation.

8.5 Egress VC Table

The Egress VC Table is a 16 row 32 bit data structure which contains context information for up to 65536 connections.

Table 9 Egress VC Table

ESA [19:16]	31						0
0000	Activation Field[2:0]			Connection Identifier Field [28:0]			
	Active (1)	PM Active2 (1)	PM Active (1)	NNI (1)	VPI (12)	VCI (16)	
0001	Reserved (1)	COS_ Enable (1)	VPC Pointer (16)		PM Addr2 (7)	PM Addr1 (7)	
0010	Status (7)		Internal Status (16)			OAM Configuration (9)	
0011	Received End-to-End AIS Defect Type (8)		Received Segment AIS Defect Type (8)		Configuration (11)	PHYID (5)	
0100	Egress Cell Count 1 (32)						
0101	Egress Cell Count 2 (32)						
0110	Alternate Egress Cell Count 1 (32)						
0111	Alternate Egress Cell Count 2 (32)						
1000	Received End-to-End AIS Defect Location [127:96] (Most Significant Bytes)						
1001	Received End-to-End AIS Defect Location [95:64]						
1010	Received End-to-End AIS Defect Location [63:32]						
1011	Received End-to-End AIS Defect Location [31:0] (Least Significant Bytes)						
1100	Received Segment AIS Defect Location [127:96] (Most Significant Bytes)						
1101	Received Segment AIS Defect Location [95:64]						
1110	Received Segment AIS Defect Location [63:32]						
1111	Received Segment AIS Defect Location [31:0] (Least Significant Bytes)						

The Egress VC Table requires 512 bits per connection, however, not all rows need be populated with RAM if not all features are used. Unused bits should be set to zero for backward compatibility with future devices within the ATLAS family.

The Egress VC Table Connection Identifier fields are described below.

Table 10 Egress VC Table Connection Identifier Fields

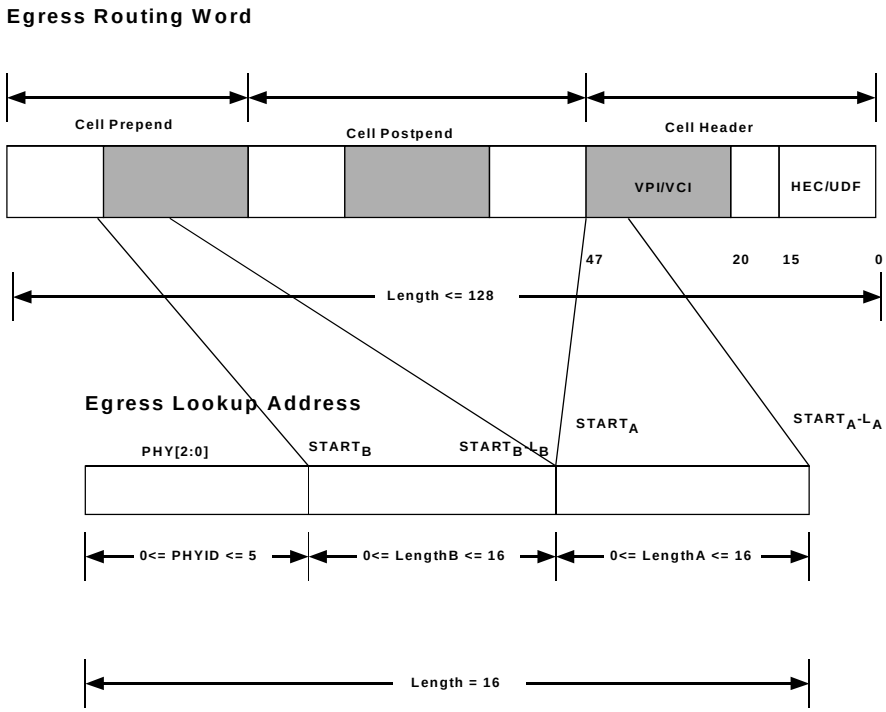
Bit	Name	Description
28	NNI	If this bit is a logic 1, the NNI bit identifies the connection as belonging to a Network-to-Network Interface. If this bit is a logic 0, the connection is part of a UNI.
27:16	VPI	The VPI field identifies the Virtual Path of the connection. If the connection is a UNI connection (as defined by the NNI bit of the VC Table), the four MSBs of the VPI field are the GFC bits. The VPI field represents the VPI (and GFC, if the connection is a UNI connection) which will be inserted in all generated OAM cells. If header translation is enabled, all cells received from the Egress Input Cell Interface, the Egress Backward OAM Cell Interface and the Egress Microprocessor Cell Interface (when the E_UPHDRX bit, register 0x061, is a logic 1) will have the VPI portion of their header replaced with the contents of this field. If the connection is a UNI connection, the GFC portion of the header will be replaced with the VPI[11:8] field if the Egress Cell Processor is so configured (GFC bit in register 0x280, set to logic 0). If the connection is an NNI connection, the GFC register bit is ignored and the VPI portion of the header will be replaced if header translation is enabled.
15:0	VCI	The VCI field identifies the Virtual Channel of the connection. If the connection is a VPC (F4) connection, then this field shall be encoded as all zeros. If the VCI field is non-zero, then the connection is a VCC (F5) connection. This VCI field represents the VCI which will be inserted in all F5 generated OAM cells. If this field is encoded as all zeros, the generated OAM cells use the correct VCI to indicate whether they are segment OAM cells (VCI=3) or end-to-end OAM cells (VCI=4). If header translation is enabled, all F5 cells received from the Egress Input Cell Interface will have the VCI portion of their header replaced with this VCI field. If the connection is an F4 connection, the VCI portion of the cell header is passed transparently.

8.5.1 Egress Connection Identification

In the Egress direction, the ATLAS uses a direct lookup for connection identification. Any combination of prepend bytes, cell header (including HEC and UDF bytes) and/or PHY ID may be used to form a direct lookup address. The Egress Cell

Processor forms an Egress Routing Word, as shown in the figure below, and the Egress Lookup Address is formed from that routing word in up to three parts.

Figure 6 Egress Routing Word and Egress Lookup Address



The Egress Lookup Address can be a maximum of 16-bits in length (allowing up to 65536 connections). If fewer than 16-bits of total length are used, the Egress Lookup Address is LSB justified, and the unused MSBs are set to zero.

8.5.1.1 Ingress Generated RDI and Backward Reporting PM Cells

RDI and Backward Reporting PM cells which are generated by the Ingress Cell Processor are routed to the Egress direction via the Egress Backward OAM Cell Interface. In order to allow these cells to be header translated, counted and be part of OAM cell flows, they must be looked up in the Egress VC Table. Thus, the Ingress and Egress VC Table connection addresses must be related in one of four ways. **It is the responsibility of the management software to ensure connections are setup in accordance with the rules and conditions described below.**

1. If the Ingress VC Table connection address is equal to the Egress VC Table connection address (i.e. the ISA[15:0] and ESA[15:0] addresses, which represent the pointer to a connection, are the same), the ATLAS-generated RDI and Backward Reporting PM cells have their HEC and UDF byte locations overwritten with the 16-bit VC Table connection address. This allows a direct lookup to be performed.

2. If the Ingress VC Table connection address is not equal to the Egress VC Table connection address, the Header[7:0] (the least significant 8-bits of the Header field at ISA[19:16]=0111 which represents the HEC field) and UDF[7:0] fields of the Ingress VC Table can be used to represent the associated Egress VC Table connection address. The ATLAS-generated RDI and Backward Reporting PM cells will contain these fields in the HEC and UDF byte locations. This allows a direct lookup to be performed.

3. If the Ingress VC Table connection address is not equal to the Egress VC Table connection address, the PrePo1[7:0] and PrePo2[7:0] fields at ISA[19:16] = 0111 can be used to represent the associated Egress VC Table connection address. The ATLAS-generated RDI and Backward Reporting PM cells will contain these fields in the HEC and UDF byte locations (the HEC field will contain the contents of the PrePo1 field, and the UDF field will contain the contents of the PrePo2 field). This allows a direct lookup to be performed.

4. Finally, if the ATLAS-generated RDI and Backward Reporting PM cells can be uniquely identified by their PHYID[4:0], VPI[11:0] and VCI[15:0], the Egress VC Table pointer can be extracted in exactly the same manner as cells received from the Egress Input Cell Interface (**this assumes that a direct lookup of the cells is normally performed by extracting a pointer from those same fields).**

8.5.1.2 Egress Generated RDI and Backward Reporting PM Cells

RDI and Backward Reporting PM cells which are generated by the Egress Cell Processor are routed to the Ingress direction via the Ingress Backward OAM Cell Interface. In order to allow these cells to be header translated, counted and be part of OAM cell flows, they must be looked up in the Ingress VC Table. Thus, the Ingress and Egress VC Table connection addresses must be related in one of two ways. **It is the responsibility of the management software to ensure connections are setup in accordance with the rules and conditions described below.**

1. If the Egress VC Table connection address is equal to the Ingress VC Table connection address (i.e. the ISA[15:0] and ESA[15:0] addresses, which represent the pointer to a connection, are the same), the ATLAS-generated RDI and Backward Reporting PM cells have their HEC and UDF byte locations overwritten with the 16-bit VC Table connection address. This allows a direct lookup to be performed. In this case, the cells are not subject to the search algorithm as cell received from the Ingress Input Cell Interface, or the Ingress Microprocessor Cell Interface (when I_UPHDRX bit in register 0x051 is set to logic 1). The decision of which field to use for the search is controlled by the BCIFHECUDF bit of the Egress Cell processor Direct Lookup Index Configuration 1 register 0x282 and the Ingress BCIFHECUDF bit in the Ingress Cell Processor Configuration 2 register 0x238.

2. If the Ingress and Egress VC Table connection addresses are not identical, then a search must be performed in the Ingress direction, and the connection must be uniquely identified by its PHYID[4:0], VPI[11:0] and VCI[15:0] fields. The HEC and UDF fields of the ATLAS-generated RDI and Backward Reporting PM cells are overwritten with the 16-bit connection address. As a programmable option, the HEC byte can be overwritten with the PHYID[4:0] field (LSB justified with the 3 MSBs set to logic 0, the UDF byte is then set to 0x6A). This is controlled by the PHYIDinHEC register bit of the Egress Cell Processor Configuration #1 register 0x280.

   If any other prepend or postpend bytes are used in the Ingress Search algorithm, this option will not work. **It is the responsibility of the management software to ensure the connection addresses and search fields are setup correctly.**

8.6 Egress Cell Processing

After a direct lookup has been completed for a cell, the resulting actions are dependent upon the cell contents and the Egress VC Table record. Particular features such as cell counting and OAM Processing can be disabled on a global and per-connection basis.

The Egress direct lookup results in a ESA[15:0] value which points to an Egress VC Table record. The fields of the Egress VC Table record are described below. If fewer than 32768 connections are supported, the most significant bits of ESA[15:0] and the associated memory may not be required.

The Egress Cell Processor uses the ESA[19:0], ESRWB, ESOEB and ESADSB pins to perform read and write accesses to the external synchronous SRAM**.**

When a new VC is provisioned, the management software must initialize the contents of the VC Table record. Once provisioned, the management software can retrieve the contents of the VC Table record.

The Egress Cell Processor performs an odd parity check of the received data. As a programmable option, the Egress Cell Processor can also perform a parity check over the extracted connection lookup address. The AddrParityEn bit in the Egress Cell processor Configuration 1 register 0x280 enables address parity. The check assumes that parity exists in the external SRAM, and is connected appropriately to the ESD[35:0] pins. The Address parity checking uses the most significant parity bit of the first row (i.e. ESA[19:16] = 0000), to perform its odd parity check. If the parity is found to be in error, the BADVCtoUP bit, in register 0x280, determines whether the cell will be output to the Egress Microprocessor Cell Interface for logging, or discarded.

The Activation field of the Egress VC Table is shown below:

Table 11 Egress VC Table Activation Field

Bit	Name	Description
2	Active	Identifies the connection as active. It is the responsibility of the management software to set and clear this bit during activation and deactivation, respectively, of a connection.
1	PM Active2	Indicates the PM session pointed to by PM Addr2[6:0] is active.
0	PM Active1	Indicates the PM session pointed to by PM Addr1[6:0] is active.

Table 12 Egress VC Table Status Field.

The Egress VC Table Status field is described below.

Bit	Name	Description
6	Reserved	This bit should be set to zero at connection setup.
5	AIS_end_to_end alarm	This bit becomes a logic 1 upon receipt of a single end-to-end AIS cell. The alarm status is cleared upon the receipt of a single user or end-to-end CC cell, or if no end-to-end AIS cell has been received within the last 2.5 +/- 0.5 sec.
4	AIS_segment alarm	This bit becomes a logic 1 upon receipt of a single segment AIS cell. The alarm status is cleared upon the receipt of a single user or segment CC or end-to-end CC cell, or if no segment AIS cell has been received within the last 2.5 +/- 0.5 sec.
3	RDI_end_to_end alarm	This bit becomes a logic 1 upon receipt of a single end-to-end RDI cell. This bit is cleared if no end-to-end RDI cell has been received within the last 2.5 +/- 0.5 sec.
2	RDI_segment alarm	This bit becomes a logic 1 upon receipt of a single segment RDI cell. This bit is cleared if no segment RDI cell has been received within the latest 2.5 +/- 0.5 sec.
1	CC_end_to_end alarm	This bit becomes a logic 1 if no user or end-to-end CC cell has been received within the last 3.5 +/- 0.5 sec. This bit is cleared upon receipt of a user cell, or end-to-end CC cell
0	CC_segment alarm	This bit becomes a logic 1 if no user or segment CC, or end-to-end CC cell has been received within the last 3.5 +/- 0.5 sec. This bit is cleared upon receipt of a user cell, segment CC cell or end-to-end CC cell

Table 13 Egress VC Table Configuration Field

The Egress VC Table Configuration field is described below.

Bit	Name	Description
10	Count_Type	This bit is used to index one of two possible register locations, which provide programmable options for cell counting on Cell Count 1[31:0] and Cell Count 2[31:0]. If this bit is a logic 0, the programmable option from the Egress VC Table Counting Configuration 1 register 0x290 is chosen. If this bit is a logic 1, the programmable option from the Egress VC Table Counting Configuration 2 register 0x291, is chosen.
9	FM_interrupt_enable	This bit enables the generation of segment and end-to-end AIS, RDI and Continuity Check alarm interrupts. If this bit is logic 1, the ATLAS will assert segment and end-to-end AIS, RDI and Continuity Check interrupts, as required, regardless of whether or not the ATLAS is a connection end-point (segment or end-to-end) for the connection. The ATLAS would normally be programmed to assert interrupts at connection end-points. If this bit is logic 0, no alarm interrupts will be asserted, however, the Status field will reflect the connection state.
8	LB_to_UP	If this bit is a logic 1, all Loopback cells are copied to the Egress Microprocessor Cell Interface. The Drop_LB bit determines whether or not Loopback cells are output to the Egress Output Cell Interface.
7	Drop_LB	If this bit is a logic 1, Loopback cells are not output to the Egress Output Cell Interface. The LB_to_UP bit determines whether or not Loopback cells are output to the Egress Microprocessor Interface.
6	FM_to_UP	If this bit is a logic 1, all Fault Management cells (AIS, RDI, CC) are copied to the Egress Microprocessor Cell Interface. The Segment_Point and End_to_End_Point bits determine whether or not FM cells are output to the Egress Output Cell Interface.
5	Drop_UP	If this bit is a logic 1, all cells are output to the Egress Microprocessor Cell Interface only (not to the Egress Output Cell Interface). The setting of this bit supercedes all other routing bits. If the Drop_UP bit is set, the ATLAS will not output generated OAM cells (Fwd PM, Bwd PM and Fault management) on this connection.
4	Reserved This bit must be set to a logic 0 during connection	

		initialization.
[3:0]	Defect_Type[3:0]	The Defect_Type[3:0] is used to select 1 of 16 Defect Type settings from the Egress OAM Defect Type registers, 0x292-0x299. For example, if Defect_Type[3:0] = 0000, the Defect Type 1 setting will be used in AIS cells which are generated as a result of the Send_AIS_Segment, Send_AIS_End_to_End bits being set, or as a result of a Per-PHY AIS Cell Generation register, 0x28A and 0x28B, being set. RDI cells which are generated as a result of the CC_RDI process, the Per-PHY RDI Cell Generation register, 0x28C and 0x28D, or the Send_RDI_Segment and Send_RDI_end_to_end bits also use this setting to determine which Defect Type will be inserted.

The Egress OAM Configuration Field is described below.

Table 14 Egress OAM Configuration Field

Bit	Name	Description
8	Send_AIS_segment	If this bit is a logic 1, a segment AIS cell is generated once per second (nominally).
7	Send_AIS_end_to_end	If this bit is a logic 1, an end-to-end AIS cell is generated once per second (nominally).
6	Send_RDI_segment	If this bit is a logic 1, a segment RDI cell is generated once per second (nominally).
5	Send_RDI_end_to_end	If this bit is a logic 1, an end-to-end RDI cell is generated once per second (nominally).
4	CC_RDI	If this bit is a logic 1, RDI cells are generated at one second intervals upon the declaration of a CC alarm. The type of RDI cell (segment or end-to-end) generated depends upon the alarm declaration (segment CC alarm or end-to-end CC alarm) and whether or not the connection is configured as a segment end point or end-to-end point, or both. If both the segment and end-to-end CC alarms are asserted, then both types of RDI cells will be generated (if the ATLAS is configured as both a segment end point and an end-to-end point). RDI cells which are generated as a result of the CC_RDI function, have the Defect Location and Defect Type values which are programmed in the ATLAS registers, inserted in the Defect Location and Defect Type fields.
3	CC_Activate_Segment	Enables Continuity Checking on segment flows. If the ForceCC bit in the Egress Cell Processor Direct Lookup Index Configuration 2 register 0x283, is logic 0, then when no user cells are transmitted over a 1.0 second (nominal) interval, a segment CC OAM cell is generated. The segment CC cell is generated at an interval of one per second (nominally). If the ForceCC register bit is logic 1, then when the CC_Activate_Segment bit is logic 1, a segment CC cell will be generated at an interval of once per second (nominally), regardless of the flow of user cells.
2	CC_Activate_End_to_End	Enables Continuity Checking on end-to-end flows. If the ForceCC bit in the Egress Cell Processor Direct Lookup Index Configuration 2 register 0x283, is logic 0, then when no user cells are transmitted over a 1.0 second (nominal) interval, an end-to-end CC OAM cell is generated. The end-to-end CC cell is generated at an interval of one per second (nominally).

		If the ForceCC register bit is logic 1, then when the CC_Activate_End_to_End bit is logic 1, an end-to-end CC cell will be generated at an interval of once per second (nominally), regardless of the flow of user cells. .
1	Segment_Point	Defines the ATLAS as a Segment termination point. For F4 connections (VPCs), all cells with VCI = 3 are terminated and processed. For F5 connections (VCCs), all cells with PTI = 100 are terminated and processed.
0	End_to_End_Point	Defines the ATLAS as an End-to-End termination point. For F4 connections (VPCs), all cells with VCI = 4 are terminated and processed. For F5 connections (VCCs), all cells with PTI = 101 are terminated and processed. An End-to-End termination point will also terminate all Segment connections, since by definition the End-to-End point is the end point for all OAM traffic.

Table 15 Egress Internal Status Field

The Egress Internal State field contains connection state information. The counts are decremented at a rate of once per second. The Egress Internal Status field is shown below.

Bit	Name	Description
15:14	Reserved	These bits should be set to zero to guarantee future backward compatibility.
13	Send_Seg_CC_Count	The Send_Seg_CC_Count is set to logic 1 (to provide a one second count) at connection setup time and each time the ATLAS sends a user cell on this connection. The count is decremented at one-second intervals. If this count reaches zero (i.e. if the ATLAS writes back a zero at a one second boundary and subsequently reads a zero at the next one second boundary, indicating that no user cells have been sent on this connection), then a Segment CC cell is generated, if the CC_Activate_Segment bit is set.
12	Send_End_CC_Count	The Send_End_CC_Count is set to logic 1 (to provide one second count) at connection setup time and each time the ATLAS sends a user cell on this connection. The count is decremented at one second intervals. If this count reaches zero (i.e. if the ATLAS writes back a zero at a one second boundary and subsequently reads a zero at the next one second boundary, indicating that no user cells have been sent on this connection), then an End-to-End CC cell is generated, if the CC_Activate_End_to_End bit is set
11:10	Seg_CC_Count[1:0]	The Seg_CC_Count is set to a value of 3 (to provide a 3.5 +/- 0.5 sec count) upon receipt of a user or segment CC cell, and decremented at one second intervals. If the Seg_CC_Count reaches 0, the CC_segment Alarm is raised.
9:8	End_CC_Count[1:0]	The End_CC_Count is set to a value of 3 (to provide a 3.5 +/- 0.5 sec count) upon receipt of a user or end-to-end CC cell, and decrements at one second intervals. If the End_CC_Count reaches 0, the CC_end_to_end Alarm is raised.
7:6	Seg_RDI_Count[1:0]	The Seg_RDI_count is set to a value of 3 (to provide a 2.5 +/- 0.5 sec count) upon receipt of a segment RDI cell, and decrements at one second intervals. If the Seg_RDI_Count reaches 0, the RDI_segment Alarm is cleared.
5:4	End_RDI_Count[1:0]	The End_RDI_Count is set to a value of 3 (to provide a 2.5 +/- 0.5 sec count) upon receipt of an end-to-end RDI cell, and

		decrements at one second intervals. If the End_RDI_count reaches 0, the RDI_end_to_end Alarm is cleared.
3:2	Seg_AIS_Count[1:0]	The Seg_AIS_Count is set to a value of 3 (to provide a 2.5 +/- 0.5 sec count) upon receipt of a segment AIS cell, and decrements at one second intervals. If the Seg_AIS_Count reaches 0, the AIS_segment Alarm is cleared.
1:0	End_AIS_Count[1:0]	The End_AIS_Count is set to a value of 3 (to provide a 2.5 +/- 0.5 sec count) upon receipt of an end-to-end AIS cell, and decrements at one second intervals. If the End_AIS_Count reaches 0, the AIS_end_to_end Alarm is cleared.

Table 16 Egress VC Table Miscellaneous Fields

Name	Description
PHYID[4:0]	Indicates the Physical Layer device that this connection is associated with. This field is used to determine the destination of all generated OAM cells. RDI and Backward Reporting Cells received from Ingress do not use this field, instead the PHYID provided from the Ingress is used to determine the destination.
VPC Pointer[15:0]	This field is used to point to the F4 OAM VPC connections of an aggregated VPC. For a VCC connection, the VPC Pointer will contain the address of the table entry for the Segment F4 OAM VPC connection. If the VPC Pointer[15:0] field points to itself, that VCC connection is not used on any VPC Continuity Check process. The VPC Pointer should point to itself for all F4 connections. See section 8.19 for a description regarding the use of this field.
COS_enable	If this bit is a logic 1, any change of alarm state on this connection will result in a write to the Change of State FIFO (if enabled via the COS register bit of the Egress Cell Processor Configuration register 0x280). If this bit is a logic 0, no writes will be made to the COS FIFO.
Egress Cell Count 1 and 2 [31:0] Alternate Cell Count 1 and 2 [31:0]	These fields contain a configurable cell count, as described in the Count_Type table bit. The Alternate count is selected via the Alternate_Count bit in the Egress Cell Processor Configuration 2 register 0x283.
Received End-to-End AIS Defect Location [127:0]	This field is used to store the Defect Location from a received end-to-end AIS cell. This field is used in end-to-end RDI cells generated via the AUTORDI function (see Egress Cell Processor Configuration 1 register 0x280). If RDI cell generation is forced (using either the send_RDI Egress VC table bits or the Per-PHY RDI Cell generation

	registers 0x28C-0x28D) or generated by the CC_RDI process, either the local Defect Location field programmed in the Egress Cell Processor OAM Defect Location registers 0x29A-0x2A1 or an unused value (0x6A) will be used.
Received End-to-End AIS Defect Type [7:0]	This field is used to store the Defect Type from a received end-to-end AIS cell. This field is used in end-to-end RDI cells generated via the AUTORDI function (see Egress Cell Processor Configuration 1 register 0x280). If RDI cell generation is forced (using either the send_RDI Egress VC table bits or the Per-PHY RDI Cell generation registers 0x28C-0x28D) or generated by the CC_RDI process, either the local Defect Type field programmed in the Egress Cell Processor OAM Defect Type registers 0x292-0x299 or an unused value (0x6A) will be used.
Received Segment AIS Defect Location [127:0]	This field is used to store the Defect Location from a segment AIS cell. This field is used in segment RDI cells generated via the AUTORDI function (see Egress Cell Processor Configuration 1 register 0x280). If RDI cell generation is forced (using either the send_RDI Egress VC table bits or the Per-PHY RDI Cell generation registers 0x28C-0x28D) or generated by the CC_RDI process, either the local Defect Location field programmed in the Egress Cell Processor OAM Defect Location registers 0x29A-0x2A1or an unused value (0x6A) will be used.
Received Segment AIS Defect Type [7:0]	This field is used to store the Defect Type from a segment AIS cell. This field is used in segment RDI cells generated via the AUTORDI function (see Egress Cell Processor Configuration 1 register 0x280). If RDI cell generation is forced (using either the send_RDI Egress VC table bits or the Per-PHY RDI Cell Generation register 0x28C-0x28D) or generated by the CC_RDI process, either the local Defect Type field programmed in the Egress Cell Processor OAM Defect Type registers 0x292-0x299 or an unused value (0x6A) will be used.

8.7 Performance Monitoring

The OAM-PM statistics are collected in an on-chip RAM accessible through the microprocessor port. The Ingress Cell Processor and Egress Cell Processor maintain separate internal PM RAMs.

Table 17 Internal PM

PM Addr [2:0]	79													0
000	PM Configuration & Status (16)		BIP-16 (16)		Current Count CLP0 (16)		Current Count CLP0+1 (16)		BLER stored (8)	Fwd BMCSN (8)				
001	Fwd TRCC0 (16)		Fwd TRCC0+1 (16)		Fwd TUC0 (16)		Fwd TUC0+1 (16)		Fwd FMCSN (8)	Unused (8)				
010	Bwd TRCC0 (16)		Bwd TRCC0+1 (16)		Bwd TUC0 (16)		Bwd TUC0+1 (16)		Bwd FMCSN (8)	Bwd BMCSN (8)				
011	Fwd Errors (8)	Fwd Impaired (8)	Fwd Lost/Mis Impaired (8)	Fwd SECB Errored (8)	Fwd SECB Lost (8)	Fwd SECB Misins (8)	Fwd SECBC (8)	Fwd Lost FM Cells (8)	Fwd Tagged CLP0 (16)					
100	Fwd Misinserted (16)		Fwd Lost CLP0 (16)		Fwd Lost CLP0+1 (16)		Fwd Total Lost CLP0 (16)		Fwd Total Lost CLP0+1 (16)					
101	Bwd Errors (8)	Bwd Impaired (8)	Bwd Lost/Mis Impaired (8)	Bwd SECB Errored (8)	Bwd SECB Lost (8)	Bwd SECB Misins (8)	Bwd SECBC (8)	Bwd SECBC Accum. (8)	Bwd Tagged CLP0 (16)					
110	Bwd Misinserted (16)		Bwd Lost CLP0 (16)		Bwd Lost CLP0+1 (16)		Bwd Total Lost CLP0 (16)		Bwd Total Lost CLP0+1 (16)					
111	Transmitted CLP0 Count (32)				Transmitted CLP0+1 Count (32)				Bwd Lost FM Cells (8)	Bwd Lost BR Cells (8)				

The Configuration Field of the internal PM Table is shown below:

Table 18 PM Table Configuration Field

Bit	Name	Description
15	Source_FwdPM	If this bit is a logic 1, the PM session is configured to source a PM flow, and a Forward Monitoring cell is output from the ATLAS once per block of user cells (nominally). Received Forward Monitoring and Backwards Reporting cells will not be processed by this PM session. If the session is an F4 session, then any generated F5 Fwd PM cells, F5-AIS or F5-CC cells will be included in the user cell flow. If the Source_FwdPM bit is a logic 0, then the PM session is configured to process received Forward Monitoring and Backwards Reporting cells. Termination of PM cells depends only on whether the ATLAS is configured as an end-to-end or segment end point. If the Source_FwdPM bit is a logic 0, and the ATLAS is not configured as a flow end point (segment or end-to-end), then the ATLAS will monitor a PM flow.
14	Generate_BwdPM	If this bit is a logic 1 and the Source_FwdPM bit is a logic 0, a Backward Reporting PM cell is generated when an appropriate Forward Monitoring PM cell is received. The F4_F5B and ETE_SegB bits determine the type of Forward Monitoring cells that are processed, and thus the type of Backward Reporting cell that is generated. If the Fwd_PM0 bit is a logic 1, then a Backward Reporting cell will not be generated (the Fwd_PM0 bit is cleared upon receipt of the first Forward Monitoring PM cell).
13	F4_F5B	If this bit is a logic 1, this PM address is for a F4 (VPC) PM flow. F5 cells, including OAM cells, are user cells as far as this flow is concerned. If this bit is a logic 0, the PM address is for a F5 (VCC) PM flow. F4 OAM cells are ignored.
12	ETE_SegB	If this bit is a logic 1, this PM address is for an end-to-end PM flow. Segment PM cells are ignored. If this bit is a logic 0, this PM address is for a segment PM flow. End-to-end PM cells are ignored. Despite the setting of this bit, F5 OAM cells are treated as user cells if the F4_F5B bit is logic 1.
11	Force_FwdPM	This bit controls the forced insertion of a Forward Monitoring PM cell when the ATLAS is configured to insert Forward Monitoring PM cells. When the Force_FwdPM bit is logic 1, the ATLAS will force the insertion of a Forward Monitoring PM cell when the current cell count of CLP0+1 cells reaches N+N/2, where N is the

		programmed block size, regardless of the state of the Forward Monitoring Pacing register. If this bit is logic 0, then the ATLAS will not insert a Forward Monitoring PM cell unless the Forward Monitoring Pacing register allows for a PM cell to be inserted. This bit has no effect when Source_FwdPM is logic 0.
[10:9]	Threshold_Select[1:0]	These bits are used to index one of four possible threshold selection register pairs (PM Threshold A1/A2 through PM Threshold D1/D2) which hold the threshold values for Errored, Misinserted and Lost Severely Errored Cell Blocks.
[8:5]	Blocksize[3:0]	The block size of PM cells selects the nominal block of user cells as follows: 0000 128 cells 0001 256 cells 0010 512 cells 0011 1024 cells 0100 2048 cells 0101 4096 cells 0110 8192 cells 0111 16384 cells 1000 32768 cells 1001-1111 Reserved.
4	Unused	
3	Reserved	This bit must be set to logic 0 at initialization time.
2	Bwd_PM_Pending	This bit is a logic 1 if a Bwd PM cell is to be generated. Normally, Bwd PM cells are generated immediately upon receipt of a Fwd PM cell (if so configured), however, in the event that the Bwd OAM cell FIFO is full, the request must be left pending until such time as it can be sent.
1	Fwd_PM0	If Source_FwdPM is a logic 0, the Fwd_PM0 bit must be set to a logic 1 initially. This bit is cleared upon receiving the first Forward Monitoring cell. This clears the current cell count and BIP-16. The Fwd_PM0 bit is used to denote the arrival of the first Forward Monitoring cell. The Fwd_PM0 bit suppresses accumulation of the Forward error counts. If this bit is not set, error counts will be accumulated. If Source_FwdPM is a logic 1, then if this bit is set to a logic 1 initially, rows 1 and 7 will be cleared at the end of the first block of user cells. Initializing Row 0 is the responsibility of the management software during setup.
0	Bwd_PM0	The Bwd_PM0 bit must be set to a logic 1 initially. This bit is cleared upon receiving the first Backward Reporting cell. This clears the TUC_0, TUC_0+1, TRCC_0 and TRCC_0+1 counts. The Bwd_PM0 bit suppresses accumulation of error counts. If this bit is not set, error counts will be accumulated.

The QOS parameters of the internal PM table are described below.

Table 19 QOS Parameters for Performance Monitoring

N.B. TUCD0 and TUCD0+1 (which are referred to in this table) are internally computed values in accordance with Bellcore GR-1248-CORE, ITU-T I.610 and ITU-T I.356.

Name	Description
BIP16	When this PM instance is the source of forward monitoring cells, the Bit-Interleaved Parity 16 is the even parity error detection code computed over the information field of the block of user data cells (CLP0+1) transmitted after the last Forward Monitoring PM cell. When this PM instance terminates or monitors Forward Monitoring cells, BIP-16 is the even parity error detection code computed over the information field of user data cells received after the last Forward Monitoring PM cell.
Current Cell Count CLP0 (16)	When this PM process is the source of Forward Monitoring cells, this count is incremented each time a CLP0 user cell is transmitted. It is used along with the Fwd TUC_0 field to determine the TUC_0 field of newly generated Forward PM cells. When this PM process terminates/monitors Forward Monitoring cells, this count is incremented each time a CLP0 user cell is received. It is used along with Fwd TRCC_0 to determine the new TRCC_0 upon reception of a Forward PM cell, and thus to calculate the Total User Cell Difference CLP0.
Current Cell Count CLP0+1 (16)	When this PM process is the source of Forward Monitoring cells, this count is incremented each time a user cell is transmitted. Whenever this count equals or exceeds the programmed PM block size, a request to generate a Forward PM cell will be made, subject to cell slot availability and pacing. It is also used along with the Fwd TUC_0+1 field to determine the TUC_0+1 field of newly generated Forward PM cells. When this PM process terminates/monitors Forward Monitoring cells, this count is incremented each time a user cell is received. It is used along with Fwd TRCC_0+1 to determine the new TRCC_0+1 upon reception of a Forward PM cell, and thus to calculate the Total User Cell Difference CLP0+1.
BLER Stored (8)	The Stored Block Error Result is the Block Error Result calculated on reception of the previous Forward PM cell. It is stored in this field until the generated Backwards Reporting cell can use it.

Fwd TRCC_0 (16)	Total Received Cell Count CLP0. This field is used when terminating/ monitoring Forward PM cells, and stores a running count modulo 65536 of the total number of received CLP0 user cells just previous to the most recent Forward Monitoring cell. Fwd TRCC_0 is inserted in the TRCC_0 field of the generated Backwards Reporting cell. It is also used along with the Current Cell Count CLP0 to determine the new TRCC_0 upon reception of a Forward PM cell.
Fwd TRCC_0+1 (16)	Total Received Cell Count CLP0+1. This field is used when terminating/ monitoring Forward PM cells, and stores a running count modulo 65536 of the total number of received user cells just previous to the most recent Forward Monitoring cell. Fwd TRCC_0+1 is inserted in the TRCC_0+1 field of the generated Backwards Reporting cell. It is also used along with the Current Cell Count CLP0+1 to determine the new TRCC_0+1 upon reception of a Forward PM cell.
Fwd TUC_0 (16)	Total CLP0 User Cells for Forward Monitoring PM Cells. TUC_0 indicates the number modulo 65536 of CLP 0 user cells transmitted just before the transmission of a Forward PM cell. If this PM process is the source of Forward PM cells then this field stores the value of TUC_0 inserted into the most recent generated Forward PM Cell, and is used together with the Current Cell Count CLP0 to determine TUC_0 of the subsequent generated PM cell. This is a running count and does not need to be initialized. If this PM process terminates/monitors Forward PM cells, then this field stores the value of TUC_0 received from the most recent Forward PM cell, and is used with the received PM cell's TUC_0 to determine the number of CLP0 user cells transmitted between successive Forward PM cells. This count will be initialized automatically on reception of the first Forward Monitoring cell. When not a monitor point, Fwd TUC_0 will be inserted in the TUC_0 field of generated Backwards Reporting cells.
Fwd TUC_0+1 (16)	Total CLP0+1 User Cells. TUC_0+1 indicates the total number modulo 65536 of CLP0 and CLP1 user cells transmitted just before the transmission of a Forward PM cell. If this PM process is the source of Forward PM cells then this field stores the value of TUC_0+1 inserted into the most recent generated Forward PM Cell, and is used together with the Current Cell Count CLP0+1 to determine TUC_0+1 of the subsequent generated PM cell. This is a running count and does not need to be initialized. If this PM process terminates/monitors Forward PM cells, then this field stores the value of TUC_0+1 received from the most recent Forward PM cell, and is used with the received PM cell's TUC_0+1 to determine the number of user cells transmitted between successive Forward PM cells. This count will be initialized automatically on reception of the first Forward Monitoring cell. When not a monitor point, Fwd TUC_0+1 will be inserted in the TUC_0+1 field of generated Backwards Reporting cells.

Fwd FMCSN	The Forward FM Cell Sequence Number. This field contains the sequence number modulo 256 of the most recent Forward Monitoring cell generated/received. The MCSN is incremented for each PM cell generated/received during the PM session. When Forward PM cells are terminated or monitored, the Fwd MCSN is used to identify lost Forward PM cells. If the Fwd FMCSN is out of sequence, then BIP-16 calculations are not done, the Bit Error Code is sent as all-ones in the Backwards Reporting cell, and the Fwd Lost FM Cells counter is incremented by the number of lost FM cells. The calculation and reporting of lost, misinserted, and tagged cells, impaired blocks, and SECBs proceeds as normal. Any inference of SECBs due to lost FM cells is left up to the management software.
Fwd BMCSN	The Forward BR Monitoring Cell Sequence Number is used to determine the MCSN for generated Backwards Reporting cells. The Fwd BMCSN value is incremented each time a Backwards Routing cell is generated. There is no need to initialize this running count.
Bwd TRCC_0 (16)	Total Received Cell Count CLP0 for Backwards Reporting cells. This field stores the TRCC_0 value received from the most recent Backwards Reporting cell, and is used along with the TRCC_0 field of newly received Backwards reporting cells to determine the number of CLP0 user cells received by the far end point between successive Forwards Monitoring cells. This count will be initialized automatically on reception of the first BR cell.
Bwd TRCC_0+1 (16)	Total Received CLP0+1 User Cell Count for Backwards Reporting cells. This field stores the TRCC_0+1 value received from the most recent Backwards Reporting cell, and is used along with the TRCC_0+1 field of newly received Backwards reporting cells to determine the number of user cells received by the far end point between successive Forwards Monitoring cells. This count will be initialized automatically on reception of the first BR cell.
Bwd TUC_0 (16)	Total CLP0 User Cell Count for Backwards Reporting PM Cells. This field stores the value of TUC_0 received from the most recent Backwards Reporting cell, and is used with a newly received BR cell's TUC_0 to determine the number of cells transmitted by the Forward Monitoring source point between successive Forward PM cells. This count will be initialized automatically on reception of the first BR cell.
Bwd TUC_0+1 (16)	Total CLP0+1 User Cell Count for Backwards Reporting PM Cells. This field stores the value of TUC_0+1 received from the most recent Backwards Reporting cell, and is used with a newly received BR cell's TUC_0+1 to determine the number of cells transmitted by the Forward Monitoring source point between successive Forward PM cells. This count will be initialized automatically on reception of the first BR cell.

Bwd FMCSN (8)	This field contains the Fwd MCSN copied from the most recently received Backwards Reporting cell. It is used to infer the loss of Forward Monitoring cells at the far end point. If the Bwd FMCSN is out of sequence, then the Bwd Lost FM Cells count is incremented by the number of lost FM cells, which is presumed to be equal to the change in FMCSN less the change in BMCSN. Any inference of SECBs due to lost FM cells is left up to the management software.
Bwd BMCSN (8)	This field contains the MCSN copied from the most recently received Backwards Reporting cell. It is used to infer the loss of Backwards Reporting cells. If the received Backwards Reporting MCSN is out of sequence, then the Bwd Lost BR Cells Count will be incremented by the number of missed MCSNs. All other processing will proceed as normal.
Fwd Errored Cell Count (8) Bwd Errored Cell Count (8)	The Errored Cell Count represents the number of BIP-16 violations (BIPV) during a PM session (on CLP0+1 cells). The Errored Cell counter is incremented whenever the number of BIPV is greater than 0 and less than MERROR in the selected threshold register, so long as there are no lost or misinserted cells, and the Forward MCSN is in sequence.
Fwd Impaired Blocks (8) Bwd Impaired Blocks (8)	The Impaired Block count represents the sum of PM cell blocks containing at least one BIP error, lost cell or misinserted cell (CLP0+1).
Fwd Lost/ Misinserted Impaired Blocks (8) Bwd Lost/ Misinserted Impaired Blocks (8)	The Lost/Misinserted Impaired Block count represents the sum of the PM cell blocks for which there was at least one lost or misinserted cell (CLP0+1). The Lost/Misinserted Block Impaired Block count is incremented whenever there is a non-zero TUCD_0+1.
Fwd SECB Errored (8) Bwd SECB Errored (8)	Severely Errored Cell Block Errored Cells (CLP0+1). The SECB Errored is incremented whenever the number of BIPV errors exceeds MERROR in the selected threshold register, and there are no lost/misinserted cells, and the Forward MCSN is in sequence. The accumulation of SECB Errored inhibits the accumulation of the count of BIP Errors.
Fwd SECB Lost (8) Bwd SECB Lost (8)	Severely Errored Cell Block Lost Cells. The SECB Lost is incremented whenever the number of Lost CLP0+1 cells exceeds MLOST in the selected threshold register. The accumulation of SECB Lost inhibits the accumulation of the count of Lost CLP0+1 cells.
Fwd SECB Misinserted (8) Bwd SECB Misinserted(8)	Severely Errored Cell Block Misinserted Cells (CLP0+1). The SECB Misinserted is incremented whenever the number of Misinserted cells exceeds MMISINS in the selected threshold register. The accumulation of SECB Misinserted inhibits the accumulation of the count of Misinserted Cells.
Fwd SECBC (8)	Forward Severely Errored Cell Blocks Combined. This running counter increments each time a SECB is declared. This value is inserted into the SECBC field of generated Backwards Reporting cells.

Bwd SECBC (8)	Backward Severely Errored Cell Blocks Combined. This value is copied from the SECBC field of received Backwards Reporting cells, and represents a rolling modulo-256 count of all Severely Errored Cell Blocks. There is no need to initialize this running counter.
Bwd SECBC Accum. (8)	Backward Accumulating SECBC Count. Whenever a received BR cell has a SECBC field different from the stored Bwd SECBC, this field is incremented by the modulo-256 difference. This is a saturating counter that initializes itself when the first BR cell is received.
Fwd Lost FM Cells (8)	The Fwd Lost FM Cells count uses the MCSN of received Forward Monitoring cells to determine the number of lost FM cells. Whenever the MCSN of a received FM cell is out of sequence, this count is incremented by the difference between the expected and received MCSN, and BIP-16 calculations are suppressed.
Fwd Tagged CLP0 Cells (16) Bwd Tagged CLP0 Cells (16)	Whenever there are less CLP0 cells received than were transmitted (TUCD is negative) then those cells have either been lost or tagged. The inference is made that if CLP0 cells were lost, then they should be lost from the CLP0+1 stream as well. Thus when TUCD0 < 0, the Lost CLP0 cells count is incremented by the lesser of -TUCD0 and -TUCD0+1, and the Tagged CLP0 Cell Count is incremented by (-TUCD0) – (-TUCD0+1), so long as the result is positive. This count is not incremented if the SECB Lost count is incremented.
Fwd Lost CLP0 (16) Bwd Lost CLP0 (16)	The Lost CLP0 Cell Count represents the total number of Lost CLP0 user cells during a PM session. The Lost CLP0 cell count is incremented by the lesser of -TUCD_0 and -TUCD_0+1, whenever that number is greater than zero. This count is not incremented if the SECB Lost count is incremented.
Fwd Lost CLP0+1 (16) Bwd Lost CLP0+1 (16)	The Lost CLP0+1 Cell Count represents the total number of Lost CLP0+1 user cells during a PM session. The Lost CLP0+1 cell count is incremented by the number of Lost CLP0+1 cells, whenever TUCD_0+1 < 0 and the number of Lost CLP0+1 cells is less than or equal to MLOST in the selected threshold register. If the count is greater than the MLOST register value than the SECB lost count will be incremented instead.
Fwd Misinserted Cells (16) Bwd Misinserted Cells (16)	The Misinserted Cell Count represents the total number of Misinserted CLP0+1 user cells during a PM session. The Misinserted Cell Count is incremented by the number of misinserted CLP0+1 cells, whenever MMISINS >= TUCD_0+1 > 0.
Fwd Total Lost CLP0+1 (16) Bwd Total Lost CLP0+1 (16)	The Total Lost CLP0+1 cell count represents the total number of lost CLP0+1 user data cells during a PM session. This count is not dependent on a threshold. That is, the Total Lost CLP0+1 cell count is always incremented by the number of lost CLP0+1 user cells.
Fwd Total Lost CLP0 (16) Bwd Total Lost CLP0 (16)	The Total Lost CLP0 cell count represents the total number of lost CLP0 user data cells during a PM session. This count is not dependent on a threshold. That is, the Total Lost CLP0 cell count is always incremented by the number of lost CLP0 user cells.

Transmitted CLP0+1 User Cells	The Transmitted CLP0+1 User Cell count represents the number of cells that are originated on a monitored connection by the transmitting end point. If the PM session is configured as a monitoring point (intermediate point), this count is derived from the difference of the TUC 0+1 fields of two successive Backward Reporting cells. If the PM session is configured as an end point sink, this count is derived from the difference of the TUC 0+1 fields of two successive Forward Monitoring cells. If the PM session is configured as an end point source, this count is derived from the actual number of CLP0+1 cells transmitted.
Transmitted CLP0 User Cells	The Transmitted CLP0 User Cell count represents the number of cells that are originated on a monitored connection by the transmitting end point. If the PM session is configured as a monitoring point (intermediate point), this count is derived from the difference of the TUC 0 fields of two successive Backward Reporting cells. If the PM session is configured as an end point sink, this count is derived from the difference of the TUC 0 fields of two successive Forward Monitoring cells. If the PM session is configured as an end point source, this count is derived from the actual number of CLP0 cells transmitted.
Bwd Lost BR Cells (8)	If the MCSN of a received BR cell is out of sequence, then this count will be incremented by the difference between the expected MCSN and the received MCSN.
Bwd Lost FM Cells (8)	The Bwd Lost FM Cells count represents the number of forward monitoring cells lost in transit to the far end point. This calculation is performed based on the Fwd MCSN field of arriving Backwards Reporting fields. Whenever the FMCSN field of the BR cell is out of sequence, this count is incremented by the difference between the received and expected MCSN. However, if the BR cell's own MCSN is also out of sequence, this count will increment by the number of apparently lost FM cells minus the number of lost BR cells.

All error (Lost, Misinserted and Errored) counts and the Total Transmitted CLP0 and Total Transmitted CLP0+1 saturate at all ones and will not rollover.

PM Cell Format as defined by ITU-T I.610

Header Fields 5x8	OAM Cell Type (= 0010) 4	OAM Function Type 4	Performance Management Function Specific Fields 45x8	Reserved 6	EDC (CRC-10) 10

The Performance Management Function Specific Fields are listed below:

FM = Forward Monitoring PM cell field

BR = Backward Reporting PM cell field

FM + BR	FM + BR	FM	FM + BR	FM		BR	BR	BR	BR	BR
MCSN 1x8	TUC_0+1 2x8	BEDC_0+1 2x8	TUC_0 2x8	Time Stamp 4x8	Unused 6AH 27x8	Fwd MCSN 1x8	SECBC 1x8	TRCC_0 2x8	Block Error Result 1x8	TRCC_0+1 2x8

The ATLAS does not support the Time Stamp field option in PM cells. The default value of all ones is inserted in the Time Stamp field for all generated PM cells.

8.7.1 Performance Monitoring Flows

The ATLAS supports a highly configurable internal PM statistics RAM. The Ingress and Egress VC Tables are used to index internal PM RAM locations. In each of the VC tables, two pointers are provided. Each pointer can access up to 128 unique PM RAM locations. These two pointers can be used to perform simultaneous sinking and sourcing of a PM flow, simultaneous F4 and F5 PM flows, etc. In the Ingress VC Table, the PM pointers are located at ISA[19:16]=0001, and the fields are as follows:

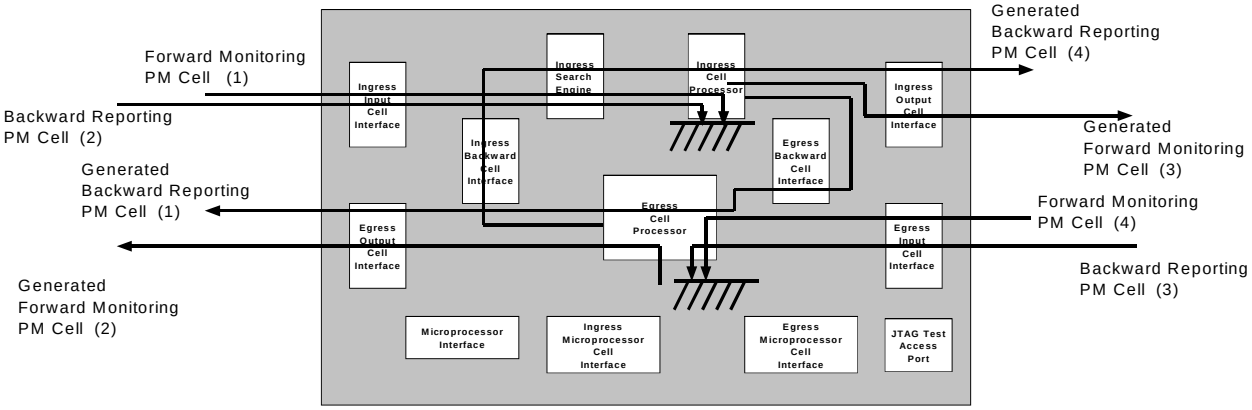
PM Active2	PM Addr2[6:0]	PM Active1	PM Addr1[6:0]

The PM Addr1[6:0] is a pointer to an internal PM RAM location. This PM connection may be configured to be a sink or source or monitoring point of F4 or F5 segment or end-to-end PM flow.

In the Egress VC Table, the PM pointers are located at ESA[19:16] = 0000 (PM Active2 and PM Active1) and 0001 (PM Addr2[6:0] and PM Addr1[6:0]).

The figure below illustrates the PM flow capability of the ATLAS.

Figure 7 ATLAS PM Flows



The figure above illustrates two unique bi-directional PM flows. In the first PM flow, indicated by (1), the ATLAS is terminating a Forward Monitoring PM cell at the Ingress Cell Processor, and the Ingress Cell Processor generates a Backward Reporting PM cell through the Egress Backward Cell Interface and the Egress Cell Processor. This is one half of the bi-directional PM flow. The second half of the bi-directional flow is indicated by (2). Here, the ATLAS is generating a Forward Monitoring PM cell in the Egress Cell Processor. Another downstream entity (e.g. another ATLAS device) would terminate that Forward Monitoring cell and transmit a Backward Reporting PM cell. This Backward Reporting PM cell is received at the Ingress of the ATLAS and terminated in the Ingress Cell Processor. To enable this PM session, the termination of the Forward Monitoring PM cell (1) and the statistics collected from the termination of the Backward Monitoring PM cell (2) would be maintained by the Ingress Cell Processor in one RAM location. The generation of the Forward Monitoring PM cell (2) would be maintained by the Egress Cell Processor in one RAM location.

The tags (3) and (4) indicate the second bi-directional PM flow. At the Ingress side of the ATLAS, the Ingress Cell Processor generates a Forward Monitoring Cell that is transmitted to the Ingress Output Cell Interface (and into the Switch Fabric). A downstream device (e.g. another ATLAS device) would terminate the Forward Monitoring PM cell and generate a Backward Reporting PM cell. This Backward Reporting PM cell is received at the Egress of the ATLAS and terminated in the Egress Cell Processor. This is the first half of the bi-directional flow, indicated by (3). The second half of the bi-directional flow is indicated by (4). Here, the ATLAS terminates a Forward Monitoring PM cell in the Egress Cell Processor. The ATLAS then generates a corresponding Backward Reporting PM cell which is transmitted from the Egress Cell Processor to the Ingress Backward Cell Interface and back into the switch core. The generation of the Forward Monitoring PM cell (4) would be maintained by the Ingress Cell Processor in one RAM location. The termination of the Forward Monitoring PM cell (4) and the statistics collected from the termination of the Backward Monitoring PM cell (3) would be maintained by the Egress Cell Processor in one RAM location.

The above discussion is just one example of the PM Flow capability of the ATLAS. Each of the PM flows can be configured as a monitoring point in which PM cells are neither generated nor terminated (note, however, PM cells will be terminated OAM flow end points), but merely monitored and their statistics maintained. The ATLAS can also be configured to monitor/sink/source an F4 PM flow. Each F5 connection that is a member of an F4 VPC flow must have one common PM Address for the F4 flow. All user cells (at the F4 level) will be considered to be part of the F4 PM flow, and thus counted as such.

The ATLAS can also be configured to perform bi-directional PM on a segment connection and an end-to-end connection (simultaneously) for up to 128 connections simultaneously. For each location (in the Ingress and Egress directions), one pointer would be used to point to the PM RAM location for the end-to-end PM flow, and the other pointer would be used to point to the PM RAM location for the segment PM flow.

In order to guard against possible changes in ATM Specifications, the ATLAS provides a configurable register set to determine whether or not to include certain VCI values in F4-PM flows, and whether or not to include certain PTI values in F5-PM flows. Changes in ITU-T I.610 and Bellcore GR-1248-CORE should be monitored closely to ensure compliance.

The insertion of Forward Monitoring PM Cells is controlled in both the Ingress and Egress directions by the Paced Forward PM Cell Generation registers. These registers provide a counter to set the number of cell intervals (defined as 32 ISYSCLK or ESYSCLK clock cycles) between successive Forward Monitoring PM cells. This prevents the ATLAS from generating Forward Monitoring PM cells back-to-back. Each time a Forward Monitoring PM cell is generated, a counter is loaded with the value set in the Paced Fwd PM Cell Generation register, and the register then decrements at intervals of 32 clock cycles. Another Forward Monitoring cell will not be generated until the counter reaches 0.

Since policing is performed in the Ingress direction, the position of the UPC/NPC needs to be clearly defined. If the ATLAS is a sink of Forward Monitoring PM cells, or a monitoring point, the counts maintained in the PM RAM represent the state of the device **before** the UPC/NPC function. If the ATLAS is a source of Forward Monitoring PM cells, the counts maintained in the PM RAM represent the state of the device **after** the UPC/NPC function.

8.8 Change of Connection State

As a configurable option, the ATLAS maintains two FIFOs that monitor all ingress and egress connections for changes of state (i.e. Continuity Check Alarm, AIS Alarm and RDI Alarm (and XPOLICE in the Ingress)). If a connection has a change of state at some time (e.g. due to the receipt of an AIS cell, or due to loss of continuity), a copy of the ingress or egress Status field and the 16-bit connection address will be written into the FIFO.

A maskable interrupt for each FIFO is provided to notify when valid data are in the FIFO. A maskable interrupt for each FIFO is provided to notify when the FIFO is at least half full.

If the FIFO becomes full, the background process that checks for changes of state will be suspended. The process will remain suspended until such time as data have been read out of the FIFO**. It is the responsibility of the management software to ensure the FIFO is polled often enough to ensure the monitoring of changes of state remain compliant to the GR-1248-CORE Bellcore and ITU-T I.610 standards.**

As result of the internal operation of the Ingress cell processor and the maximum number of the data enteries the processor can write in one process, there can be three or four items less than the maximum in the FIFO when the COSFULLI interrupt is asserted. When reading out from the FIFO the COSVALID (Ingress register 0x23B and Egress register 0x2D7) signal should always be used to ensure that valid data is read.

Table 20 Ingress and Egress Change of State FIFO

Each FIFO is 256 entries deep, and the contents of the FIFO are shown below:

Bit	Name	Description
25	Segment End Point	If this bit is logic 1, the connection is a segment end-point.
24	End-to-End Point	If this bit is logic 1, the connection is an end-to-end point.
[23:16]	Status Field	The Status field contains a copy of the Status field contained in the Ingress or Egress VC Table.
[15:0]	Connection Address	This field contains the 16-bit connection address with which the change of state is associated.

The FIFO contents may be read through the microprocessor port. The microprocessor may read the COS FIFO, and when the COSVALID bit in the Egress VC Table Change of Connection Status Data register 0x2D7 is asserted, the contents of the COS FIFO are valid. The FIFO read-pointer is incremented when the COSDATA[15:0] register is read (assuming the FIFO is not empty). When the COSDATA[15:0] is read, the COS FIFO BUSY bit is asserted. At this time, the state of the COSVALID bit is undefined. The BUSY bit will be deasserted 3-5 ISYSCLK/ESYSCLK cycles after the COSDATA[15:0] register is read. At this time, the COSVALID bit will be defined and will indicate whether subsequent reads are appropriate.

8.9 Header Translation

Any appended octets (used by non-standard PHY devices or in special applications) can be removed after they have been used for VC identification. In the Ingress direction, once VC identification has been made, new octets (PrePo1 – PrePo10) contained in the VC table can be prepended or postpended to each cell. The Egress Cell Processor does not support this option.

The new octets are contained in locations identified by ISA[19:16] = 0111 and 1000 in the Ingress VC Table. Substitution of appended octets can be disabled by clearing the GPREPO bit in register 0x200. If the 16-bit bus format is configured, the eight bit UDF field in the ISA[19:16] = 0111 word is placed in the user defined octet following the HEC octet location. All other appended octets are sequenced in the extended cell format SCI-PHY data structure, starting with the PrePo1 octet of ISA[19:16] = 0111. Physical memory need not be provided for all octets if the SCI-PHY cell is less than 63 octets.

Note that if the ATLAS is placed in 8-bit output mode, with the Ingress Output Cell Interface configured for an even length output cell (i.e. an odd number of appended octets), the ATLAS will sequence the appended octets starting with the second most significant byte.

The header contents of each cell can be altered. The Header word at ISA[19:16] = 0111 contains the new header. This 40-bit field contains the entire header, although not all bits are required for all connections. The VPI portion, the VCI portion, or both can be replaced with new values recovered from the VC table once VC identification has been made. Substitution of the VPI/VCI contents can be disabled by clearing the GVPIVCI bit in register 0x200. The PTI field is not modified by the header translation process. If the connection is a Virtual Path (i.e. the VCI value in the search key is coded as all zeros), the VCI field is passed through transparently. As a globally configured option, the GFC field in UNI cells can be left unmodified; otherwise, it is replaced by the four most significant bits of the output header word. The HEC and UDF bytes can be passed through transparently, or replaced by the output header word and the UDF field of the Ingress VC Table. This is controlled by the GHEC and GUDF bits in register 0x200.

In the Egress direction, header translation is also supported. The VPI portion, the VCI portion, or both can be replaced with new values from the Egress VC Table once VC identification has been made. The ATLAS does not support the replacement of prepend or postpend bytes, however, those bytes can be passed transparently. If a cell length mismatch between the Egress Input Cell Interface and the Egress Output Cell Interface exists, appended bytes will be removed or added until the cell lengths are equal, however, any added bytes will have 0x6A. Any RDI or Backward Monitoring PM cells which are generated in the Ingress direction and routed to the Egress direction will have 0x6A in appended bytes. The HEC and UDF bytes are passed through transparently, or the HEC byte may be overwritten with the PHYID[4:0] field (LSB justified with the 3 MSBs set to logic 0). This is controlled by the PHYIDinHEC register bit of the Egress Cell Processor Configuration 1 register 0x280.

8.10 Cell Routing

Generated reverse flow cells (Backward Reporting PM cells and RDI cells) are routed through the Backward OAM Cell Interfaces of the ATLAS. The Ingress and Egress Backward OAM Cell interfaces maintain separate FIFO's for RDI and Backward Reporting cells. RDI cells are held in a 4-cell FIFO until they are inserted in the cell flow stream, and the Backward Reporting cells are held in a 16-cell FIFO.The destination of each OAM cell depends on the type of OAM cell and whether or not the ATLAS is the end-point for that particular OAM flow. If the ATLAS is not an end-point, the OAM cells are routed to the same destination as user cells. If the ATLAS is an end point, the default configuration terminates and processes all OAM cells except Activate/Deactivate and Loopback cells, which are routed to either the Output Cell Interfaces (ingress or egress), or the Microprocessor Cell Interfaces (ingress or egress).

When the ATLAS receives a segment OAM cell on a connection marked as an end-to-end point only, i.e. not as a segment end point, the cell will be terminated. They will also be dropped to the Microprocessor interface if the BRMtoUP, FRMtoUP, PMtoUP global control bits are enabled in the Ingress Cell Processor Routing Configuration register 0x220 or the Egress Cell Processor Routing Configuration register 0x287. OAM cells can also be dropped to the Microprocessor interface on a Per-VC basis by setting the LB_to_UP or FM_to _UP in the Ingress VC Table Configuration Register or the Egress VC Table Status Field.

8.11 Cell Rate Policing

The ATLAS supports two instances of the Generic Cell Rate Algorithm (GCRA) for each connection. The policing operation is performed according to the Virtual Scheduling Algorithm outlined in ITU-T I.371.

To allow full flexibility, the ATLAS supports 8 possible configurations which allow each GCRA to police any combination of user cells, OAM cells, RM Cells, high priority cells or low priority cells.

The Theoretical Arrival Time fields (TAT1 and TAT2), Increment fields (I1 and I2), and Limit fields (L1 and L2) must be initialized before policing is enabled. When the connection is setup, the TAT fields must be set to all zeros, and they should not be modified by the management software after the connection has been initialized. The Atlas uses these fields for policing the connection and is responsible for updating them. The Increment and Limit fields must be programmed to the desired traffic rate. These fields relate to the traffic contract parameters as follows:

$$I = \frac{1}{PCR(\Delta t)}$$

$I = \text{Increment Field}$

$PCR = \text{Peak Cell Rate (cells/s)}$

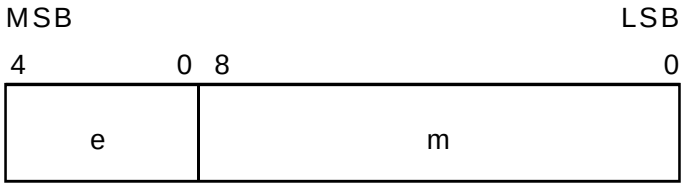
$\Delta t = \text{time quantum (s)}$

In order to obtain the granularity required in ITU-T I.371, the Increment fields are encoded as floating-point fields as follows:

$$I = 2^e\left(1 + \frac{m}{512}\right) \quad \text{where} \quad 0 \le e \le 31$$

$$0 \le m \le 511$$

The exponent, *e*, is a 5-bit field and the mantissa, *m*, is a 9-bit field. The Increment field is formatted as follows:



The floating-point encoding format of the Increment field ensures the granularity of the ATLAS is 0.19% in accordance with ITU-T I.371 5.4.1.2.

The Limit field is defined as:

$$L = \frac{\tau}{\Delta t}$$

where $\tau = \text{Cell Delay Variation Tolerance (s)}$

For a Sustained Cell Rate (SCR) conformance definition, the parameters relate as follows:

$$I = \frac{1}{SCR(\Delta t)}$$

$$L = \frac{BT}{\Delta t} = \frac{(MBS - 1)\left(\frac{1}{SCR} - \frac{1}{PCR}\right)}{\Delta t}$$

where

$SCR = \text{Sustaned Cell Rate (cells/s)}$

$MBS = \text{Maximum Burst Size at the Peak Cell Rate (cells)}$

$BT = \text{Burst Tolerance (s)}$

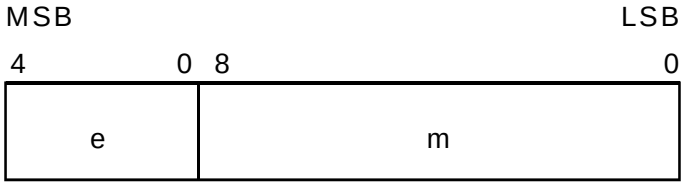
The time quantum, Δt, can be programmed to be a 1, 2, 4 or 8 multiple of the ISYSCLK period. With a 50 MHz clock, Δt is 20, 40, 80 or 160 ns.

In order to compensate for the potentially large CDVT and Burst Tolerance limits anticipated in ATM networks, the Limit fields, L1 and L2 are encoded as floating-point values, in the same manner as the Increment fields:

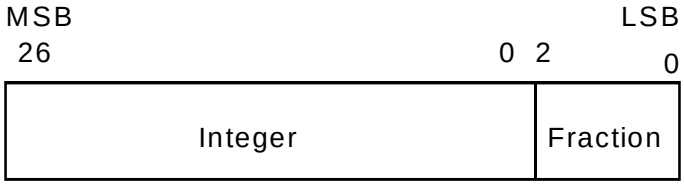
$$L = 2^e\left(1 + \frac{m}{512}\right) \quad \text{where} \quad 0 \le e \le 31$$

$$0 \le m \le 511$$

where *e* is the 5-bit exponent and *m* is the 9-bit mantissa. The Limit fields are formatted as follows:



The Theoretical Arrival Times (TAT1 and TAT2) are encoded as fixed-point values with an integer and fraction portion. The integer portion of the TAT field is a 27-bit value, and the fractional portion is a 3-bit value. The TAT fields are formatted as follows:



The fractional portion of the TAT field is measured in fractions of the time quantum, Δt. For a 20ns time quantum, the accuracy of the policing algorithm can be measured as follows:

$$PCR\max = 1412832 \text{ cells/s} \qquad \text{(this is the maximum cell rate at 622Mbps)}$$

$$T\min = \frac{1}{PCR\max} = 707.798 \text{ ns}$$

$$\text{Accuracy} = \frac{TAT\min}{T\min} = \frac{(0.125)(20\text{ns})}{707.798 \text{ ns}} = 0.0035 = 0.35\%$$

Thus, the accuracy of the ATLAS policing algorithm satisfies the ITU-T I.371 recommendation of 1%.

It is important to note that since the Limit field is a floating-point number, its maximum value exceeds the maximum TAT (132217727) value; therefore, L should not exceed this value. If the encoded value of L is greater than TAT_{max}, then L shall be taken to be TAT_{max}. Thus,

$$L \le TAT_{\max}$$

The value of Δt and the range of I and L determine the lowest PCR that can be policed, the PCR granularity supported at the highest expected PCR and the largest CDVT expected.

$$PCR_{\min} = \frac{1}{I_{\max}(\Delta t)}$$

$$\text{granularity as a fraction of PCR} = PCR(\Delta t)$$

$$\tau_{\max} = L_{\max}(\Delta t)$$

The maximum value for increment field supported in the ATLAS is 2^{24} –1 = 16777215, therefore, the smallest peak (or sustainable) cell rate supported is:

$$PCR_{\min} = \begin{cases} 2.98 \text{ cells/s} : \Delta t = 20ns \\ 1.49 \text{ cells/s} : \Delta t = 40ns \\ 0.75 \text{ cells/s} : \Delta t = 80ns \\ 0.37 \text{ cells/s} : \Delta t = 160ns \end{cases}$$

As described previously, the Limit field, L is a 14-bit floating point field, with L_{max} = 134217727 (which is equal to TAT_{max}). Therefore

$$CDVT_{\max} = \begin{cases} 2.68s : \Delta t = 20ns \\ 5.36s : \Delta t = 40ns \\ 10.73s : \Delta t = 80ns \\ 21.47s : \Delta t = 160ns \end{cases}$$

Note, the PCR (or SCR) and CDVT (or BT) can be changed while the connection is provisioned without disrupting the policing algorithm. That is, the Increment and Limit fields may be changed at any point, and the policing algorithm will begin policing to the new settings.

The action taken on a non-conforming cell is programmed on a per-connection basis by the Action1[1:0] and Action2[1:0] fields at ISA[19:16] = 0100 (Action1 controls the action taken when a cell is non-conforming with GCRA1, and Action2 controls the action taken when a cell is non-conforming with GCRA2).

Action1[1:0] and Action2[1:0]	Definition
00	Set the Police status bit, but take no other action than to increment the appropriate non-compliant cell count.
01	Reduce the priority of high priority cells (i.e. tag CLP=0 cells. Increment the appropriate non-compliant cell count.
10	Reduce the priority of high priority cells and discard the low priority cells. Increment the appropriate non-compliant cell count.
11	Discard all non-conforming cells. Increment the appropriate non-compliant cell count.

Policing can be effectively disabled for a connection if the increment fields (I1 and I2) are set to all zeros.

The Conditional Conformance Update (COCUP) bit is used to introduce a coupling between the two GCRAs.

1. If COCUP=0, then GCRA1 and GCRA2 are completely independent of each other and the updating of the TAT1 and TAT2 fields are independent. If the cell is conforming to a GCRA, the TAT field for that GCRA will be updated. If COCUP = 0 and Policing Action = No Action for a GCRA instance, then the TAT's will be updated even if the cells are non-compliant. Cell flow will not be affected, but the non-compliant cell counts can be incorrect. The table below describes the behavior of the ATLAS:

Table 21 ATLAS Actions on Policing with COCUP=0

GCRA1		GCRA2			
		Pass	Fail		
			No Action	Tag	Discard
Pass		Update TAT1 Update TAT2	Update TAT1 Update TAT2	Update TAT1	Update TAT1
Fail	No Action	Update TAT2	Update TAT1, TAT2	Update TAT1, TAT2	Update TAT1, TAT2
	Tag	Update TAT2	Update TAT1, TAT2	No Update	No Update
	Discard	Update TAT2	Update TAT1, TAT2	No Update	No Update

2. If COCUP=1, then GCRA1 and GCRA2 are coupled and the updating of the TAT1 and TAT2 fields are conditional. The ATLAS reacts as described in the table below.

Table 22 ATLAS Actions on Policing with COCUP=1

GCRA1		GCRA2			
		Pass	Fail		
			No Action	Tag	Discard
Pass		Update TAT1 Update TAT2	Update TAT1	Update TAT1	No Update
Fail	No Action	Update TAT2	No Update	No Update	No Update
	Tag	Update TAT2	No Update	No Update	No Update
	Discard	No Update	No Update	No Update	No Update

In both cases (COCUP=1 and COCUP=0), if a cell fails both GCRA1 and GCRA2, the most severe action is taken on the cell. GCRA1 is evaluated before GCRA2 is evaluated.

Three programmable 16 bit non-compliant cell counts are maintained in the Ingress VC Table. These cell counts can be programmed as follows:

Each non-compliant cell count can be programmed as follows:

1. Non-compliant CLP0 cells.
2. Non-compliant CLP0+1 cells.
3. Tagged CLP0 cells.
4. Discarded CLP0 cells.
5. Discarded CLP0+1 cells.

The non-compliant cell counts are programmed in the Ingress Policing Configuration and Non-Compliant Cell Counting register. Both non-compliant cell count 1 and non-compliant cell count 2 have the following programming options:

NCOUNT1[1:0] or NCOUNT2[1:0]	Definition
00	Non-compliant CLP=0 cells.
01	Non-compliant CLP=0+1 cells.
10	Discarded CLP=0 cells.
11	Discarded CLP=0+1 cells.

Non-compliant cell count 3 may be programmed as follows:

NCOUNT3[1:0]	Definition
00	Non-compliant CLP=0 cells.
01	Non-compliant CLP=0+1 cells.
10	Tagged CLP=0 cells which are not discarded.
11	Discarded CLP=0+1 cells.

These non-compliant cell counts may be programmed to satisfy the following requirements:

1. Non-Compliant Cell Count1[15:0]: the number of CLP0+1 cells discarded by the UPC/NPC function. GR-1248-CORE R9-6.

2. Non-Compliant Cell Count2[15:0]: the number of CLP0 cells discarded by the UPC/NPC function. GR-1248-CORE R9-7.

3. Non-Compliant Cell Count3[15:0]: the number of CLP0 cells tagged as CLP1 cells by the UPC/NPC function. GR-1248-CORE CO9-8.

8.11.1 Per-PHY Policing

The Ingress Cell Processor also maintains a single GCRA instance per-PHY (32 in total) in an internal RAM. The per-PHY policing may be selectively enabled for any number of connections for a PHY. The PHY Police bit of the Ingress VC Table at ISA[19:16] = 0101 determines whether or not the PHY policing is active on that connection. The PHYID[4:0] field at ISA[19:16]=0001 determines which of the 32 internal policing instances is addressed if per-PHY policing is active.

The per-PHY policing is always evaluated after the per-connection policing is performed. If a cell is discarded as a result of per-PHY policing, the per-connection policing parameters are not updated. Similarly, if a cell is discarded as a result of per-connection policing, the per-PHY policing parameters are not updated. The COCUP bit for the connection should be set to logic 1, when per-PHY policing is enabled.

The table below describes the ATLAS actions when per-PHY policing is enabled.

Table 23 ATLAS Actions with per-PHY Policing

Per-VC GCRA (Note, the per-VC GCRAs are evaluated as described in Table 19)		Per-PHY GCRA			
		Pass	Fail		
			No Action	Tag	Discard
Pass		Update VC TAT Update PHY TAT	Update VC TAT	Update VC TAT	No Update
Fail	No Action	Update PHY TAT	No Update	No Update	No Update
	Tag	Update PHY TAT	No Update	No Update	No Update
	Discard	No Update	No Update	No Update	No Update

The per-PHY policing has a programmable action field and configurable register bits to police any combination of user cells, OAM cells, RM cells, high priority cells and low priority cells.

Non-compliant cell counts are also maintained on a per-PHY basis.

Please note that it is not recommended that per-PHY tagging of cells be enabled when there are Guaranteed Frame Rate (GFR) connections in the PHY. The GFR standard does not permit tagging of partial frames. As a result, if per-PHY policing is enabled to tag cells any GFR connections on that PHY would violate the GFR requirements. See the GFR section below for a description of the ATLAS GFR configuration settings.

It is the responsibility of the management entity to ensure the per-PHY policing parameters are programmed correctly. All RAM addresses can be written to and read by an external microprocessor.

The internal per-PHY policing RAM is shown below

Table 24 Internal Per-PHY Policing RAM

Address [1:0]	31					0
00	Reserved (2)	PHYTAT (30)				
01	Unused (4)	PHY I (14)	PHY L (14)			
10	PHY Non-Compliant2 (16)		PHY Non-Compliant1 (16)			
11	Unused (11)	PHYVCCount (1)	PHY Police Config. (2)	PHY Action (2)	PHY Non-Compliant3 (16)	

The PHY Policing Configuration[1:0] field (of the Internal PHY Policing RAM at Addr[1:0] = 11) selects 1 of 4 settings (in the Ingress PHY Policing 1 Register 0x201 and Ingress PHY Policing 2 register 0x202) in the Ingress Cell Processor which allows any combination of user cells, OAM cells, RM cells, high priority cells or low priority cells to be policed by the PHY GCRA.

The PHY Action[1:0] field controls the programmable action to be taken on cells which are non-conforming to the PHY GCRA. The PHY Action field is programmed as follows:

PHY Action[1:0]	Description
00	Set the Police status bit, but take no other action than to increment the appropriate non-compliant cell count.
01	Reduce the priority of high priority cells (i.e. tag CLP=0 cells. Increment the appropriate non-compliant cell count.
10	Reduce the priority of high priority cells and discard the low priority cells. Increment the appropriate non-compliant cell count.
11	Discard all non-conforming cells. Increment the appropriate non-compliant cell count.

The PHY Non-Compliant cell counts are programmable as follows:

1. Non-compliant CLP0 cells.
2. Non-compliant CLP0+1 cells.
3. Tagged CLP0 cells.
4. Discarded CLP0 cells.
5. Discarded CLP0+1 cells.

The PHY non-compliant cell counts are programmed in the Ingress Policing Configuration and Non-Compliant Cell Counting register 0x210. Both non-compliant cell count 1 and non-compliant cell count 2 have the following programming options:

PHYNCOUNT1[1:0] or PHYNCOUNT2[1:0]	Definition
00	Non-compliant CLP=0 cells.
01	Non-compliant CLP=0+1 cells.
10	Discarded CLP=0 cells.
11	Discarded CLP=0+1 cells.

And PHY non-compliant cell count 3 can be programmed as follows:

PHYNCOUNT3[1:0]	Definition
00	Non-compliant CLP=0 cells.
01	Non-compliant CLP=0+1 cells.
10	Tagged CLP=0 cells which are not discarded.
11	Discarded CLP=0+1 cells.

The PHYVCCount bit determines whether cells which are non-compliant with the per-VC policer are counted in the per-PHY non-compliant cell counts and vice versa (i.e. cells which are non-compliant with the per-PHY policer are counted in the per-VC non-compliant cell counts). The table below describes the programming options.

Table 25 Per-PHY and per-VC Non-Compliant Cell Counting PHYVCCount=0

PHYVCCount=0		Per-VC Policing	
		Compliant	Non-Compliant
Per-PHY Policing	Compliant	No update.	Update per-VC non-compliant counts Don't update per-PHY non-compliant counts.
	Non-Compliant	Don't update per-VC non-compliant counts. Update per-PHY non-compliant counts	Update per-VC non-compliant counts. Update per-PHY non-compliant counts.

Table 26 Per-PHY and per-VC Non-Compliant Cell Counting PHYVCCount=1

PHYVCCount=1		Per-VC Policing	
		Compliant	Non-Compliant
Per-PHY Policing	Compliant	No update.	Update per-VC non-compliant counts Update per-PHY non-compliant counts.
	Non-Compliant	Update per-VC non-compliant counts. Update per-PHY non-compliant counts	Update per-VC non-compliant counts. Update per-PHY non-compliant counts.

8.11.2 Guaranteed Frame Rate

The ATLAS supports Guaranteed Frame Rate (GFR) policing. A total of four policing actions are observed for the GFR policing. They are: Maximum Frame Length (MFL) conformance test, Peak Cell Rate (PCR) test, Minimum Cell Rate (MCR) conformance test, and the CLP Conformance test. When GFR policing is enabled, the GFR policing algorithm is enabled. The conformance tests are evaluated sequentially, in the following order:

1. MFL conformance test. When an End Of Message cell in a packet is received, the Remaining Frame Count field of the Ingress VC Table (at ISA[19:16]=0101) is loaded with the value programmed in the Maximum Frame Length field of the Ingress VC Table (at ISA[19:16]=0101) after testing for MFL conformance with the current value. The Remaining Frame Count then decrements with each cell received in the new frame. If this value reaches zero before an End-Of-Message cell is received, the remainder of the frame is discarded (the EOM cell is identified by having an SDUTYP equal to logic 1 (i.e. PTI = 001 or 011). The MFL conformance test can be disabled with the MFL register bit in the Ingress Cell Processor Configuration 2 register 0x238. If the MFL bit is logic 0, the MFL conformance test is evaluated using the Maximum Frame Length Counter (MFLC[11:0]) or the Maximum Frame Length Counter register 0x239 (no physical memory need be provided for the Maximum Frame Length field of the Ingress VC Table in this case).

   If the MFL register bit is set to logic 1, the MFL conformance test can be disabled on a per-connection basis by setting the Maximum Frame Length field to all ones. If the MFL register bit is set to logic 0, the MFL conformance test can be disabled on a global basis by setting the Maximum Frame Length Counter register to all ones.

2. PCR conformance test. This test is performed using GCRA1 in exactly the same manner as normal cell policing. For this test the ACTION1[1:0] should be set to discard, i.e. '11'. If the PCR conformance test is deemed to be non-compliant, the action will be to discard the remainder of the cells in the current frame. In other words, a "partial packet action" can be taken when cells in the current frame fail this conformance test.

   The PCR conformance test implements a partial packet discard (PPD). The ATLAS will do a complete Frame discard, if the first cell of the packet was discarded as a result of PCR or SCR failure (and the buckets are configured to discard)

3. MCR conformance test. This test is performed using GCRA2, however, it differs slightly from the normal cell policing. The MCR conformance test is only performed at the start of a frame. If the first cell of a frame is a conforming CLP=0 cell, then all remaining cells in that frame will be processed as if they are conforming to the MCR conformance test. The MCR conformance test should be programmed to tag non-conforming CLP=0 cells, ACTION2[1:0]='01'. If the first cell of a frame is a non-conforming CLP=0 cell, then that cell and all other cells in that frame (including the EOM) will be tagged. In other words, the tagging action taken by this conformance test is determined at frame boundaries only. If the MCR conformance test is programmed to discard, the Atlas can discard at any point in the frame and is not restricted by frame boundaries.

4. CLP conformance test: This test is performed on every cell in a frame, including the EOM. The CLP conformance test can be enabled on a per-connection basis; this is controlled by the CLPCC_EN bit of the Ingress VC Table ISA[19:16]=0001. If the first cell of the frame is a CLP=0 cell, and the cell is otherwise conforming, then any CLP=1 cell received in the frame will be discarded (if the CLPCC_EN bit of the VC table is set to logic 1), and the GFR state will enter the Partial Packet Discard state. Irrespective of the setting of the CLPCC_EN bit, if the first cell of the frame is a CLP = 1 cell, then any otherwise conforming CLP = 0 cells in the frame will be tagged.

The relevant GFR fields in the Ingress VC Table are the GFR, bit location 63 at ISA[19:16]=0101,the GFR State, bit location 48 at ISA[19:16]=0100, the CLPCC_EN, bit 63 at ISA[19:16]=0001, the Remaining Frame Count at ISA[19:16]=0101 and the Maximum Frame Count at ISA[19:16]=1110. They are described below:

Name	Description
CLPCC_EN	Indicates that the CLP Conformance Check is enabled on a connection which is subject to GFR policing. If the start of message cell was a CLP=0 cell, then the reception of any CLP=1 cell shall cause that cell to be discarded and the packet to be partially-packet-discarded.
GFR	If this bit is a logic 1, the will utilize the GFR policing as described above. If this bit is logic 0, the connection will not use the GFR policing, rather it will use the normal cell-based policing described previously.
GFR State[2:0]	The GFR State is an internally maintained state variable that identifies the state of the connection during GFR policing. This field is cleared each time an EOM is received. The state encoding is as follows: 000: Start of packet. 001: Tag Entire Packet. 010: Partial Packet Discard. 011: Disable tagging for current packet (set if the first CLP0 cell of a frame is compliant to the MCR policing instance). 100: Complete Packet Discard 101: Partial Packet Discard with Tagging (packet was initially being tagged, then entered PPD discard). 110-111: Reserved
Remaining Frame Count[10:0]	The Remaining Frame Count holds the number of cells received for the current frame. This value is only used when the MFL conformance test is enabled. The count is loaded with the Maximum Frame Length Field at the End of Message cell. The value then decrements with each cell received in the new frame.
Maximum Frame Length[10:0]	The Maximum Frame Length field is a user programmable field to hold the maximum permissible frame length. Maximum Frame Length field is used when performing the MFL Conformance Test of the Generic Frame Rate policing. Setting the MFL bit in the Ingress Cell Processor Configuration 2 register 0x238 to logic 1 enables the field. Setting this field to all zeros disables the MFL conformance test when the MFL bit, is set to logic 1.

When GFR policing is enabled, the Ingress VC Table must be configured such that the PCR conformance test is performed by GCRA1 (I1, L1, Action1) and the MCR/SCR conformance test is performed by GCRA2 (I2, L2, Action2).

The GFR standard does not permit tagging of partial frames. As a result, if per-PHY policing is enabled to tag cells any GFR connections on that PHY would violate the GFR requirements. Therefore, it is not recommended to perform per-PHY tagging when there are GFR connections in the PHY.

8.11.3 Continuously Violating Mode

Independent of the outcome of policing, the ATLAS may be configured to tag or discard all cells. If the Violate field of the Ingress VC Table is set to logic 1, a forced action, independent of the outcome of policing is taken on each cell. The forced action that is taken is dependent on the state of the Action2[1:0] field of the Ingress VC Table at ISA[19:16]=0100. The Violate field may be encoded as follows:

Violate=1 Action2[1:0]:	Description
00	Take no forced action
01	Tag all CLP=0 cells. Take no action on CLP=1 cells.
10	Tag all CLP=0 cells. Discard all CLP=1 cells
11	Discard all CLP=0+1 cells.

If a cell is discarded as a result of the forced discarding, the connection and PHY policing parameters are not updated. Otherwise, the connection and PHY policing parameters are updated contingent on the outcome of their respective GCRAs.

The connection and PHY non-compliant cell counts are not updated as a result of forced tagging or forced discarding.

The VIOLATE mode should not be enabled together with the GFR policing function.

8.11.4 ATLAS Policing Configuration

The ATLAS may be programmed to police any combination of user cells, OAM cells, RM cells, high priority cells or low priority cells. The Police Configuration Field of the Ingress VC Table at ISA[19:16]=0100 addresses up to 8 different policing configuration registers in the Ingress Cell Processor (Ingress Connection Policing Configuration Registers 1-8, 0x208-0x20F). Each of these registers may be programmed separately for GCRA1 and GCRA2.

When PHY-policing is enabled, the PHY-Police Configuration [1:0] field in the Internal PHY Policing RAM is used to addresses 1 of 4 possible combinations of policed cell types in the Ingress Cell Processor (Ingress PHY Policing Configuration Registers 1-4).

In the case of errored cells the ATLAS will behave in manner which is not consistent with the configuration register settings. The Policer will treat both RM cells with bad CRC and cells with invalid PTI/VCI as end-to-end OAM cells.

8.12 Cell Counting

The ATLAS maintains counts on a per-connection basis, per-PHY basis and over the aggregate cell stream.

The following parameters are stored on a per-connection basis in both the Ingress and Egress VC Tables:

Two 32-bit cell counts that may be programmed to count any combination of the following:

A. CLP0 user cells.
B. CLP1 user cells.
C. CLP0 OAM cells.
D. CLP1 OAM cells.
E. CLP0 RM cells.
F. CLP1 RM cells.
G. CLP0 cells with Invalid VCI/PTI
H. CLP1 cells with Invalid VCI/PTI.

Three Non-compliant cell counts (Discarded CLP0 cells, Discarded CLP0+1 cells and Tagged CLP0)

In order to maintain accurate non-compliant cell counts in the Ingress VC Table, the ATLAS asserts a maskable interrupt (I_XPOLI and I_PHYXPOLI) whenever the most significant bit is set for any of the three non-compliant cell counts. This allows an external microprocessor to read the counts to prevent saturation or rollover.

The two programmable 32-bit cell counts represent the state of the cells before policing. The non-compliant cell counts can be used to derive the cell counts after policing.

The programmability of the two 32-bit cell counts allows the ability to provision scheduled measurements and special studies on each connection.

If performance monitoring is activated, the following forward monitoring and backward reporting statistics are stored:

Number of lost CLP0 cells not in SECB (lost). An inference is used as per GR-1248-CORE to separate lost CLP0 cells (which are counted) from tagged CLP0 cells (which are counted separately).

Number of tagged CLP0 cells.

Number of lost CLP0+1 cells not in SECB (lost)

Number of misinserted CLP0+1 cells not in SECB (misinserted)

Number of BIP-16 errors. BIP-16 errors are not counted if there are lost cells, misinserted cells, or if the MCSN is out of sequence.

Number of Impaired Blocks (blocks with BIP-16 errors, lost cells, or misinserted cells, including SECBs).

Number of Severely Errored Cell Blocks for Lost CLP0+1 cells

Number of Severely Errored Cell Blocks for Misinserted cells

Number of Severely Errored Cell Blocks for BIP-16 violations

Total Lost CLP0 cells, including those in SECB (lost). An inference is made as per GR-1248-CORE to separate lost CLP0 cells (which are counted) from tagged CLP0 cells (which are counted separately).

Total Lost CLP0+1 cells including those in SECB (lost)

Number of Lost/Misinserted Impaired Blocks (including SECBs)

Total transmitted CLP0 user cells

Total transmitted CLP0+1 user cells

Number of lost Forward Monitoring PM and Backward Reporting PM cells.

The PM counts can be cleared upon a microprocessor read access to their locations in the internal PM RAM table.

The following parameters are maintained on a per-PHY basis (up to 32 PHYs are supported):

Number of CLP0 cells received at the Ingress/Egress Input Cell Interface.

Number of CLP1 cells received at the Ingress/Egress Input Cell Interface.

Number of CLP0 cells output through the Ingress/Egress Output Cell Interface.

Number of CLP1 cells output through the Ingress/Egress Output Cell Interface.

Number of valid OAM cells received.

Number of valid RM cells received.

(Ingress only) Number of (UNI-only) cells with a non-zero GFC field.

Number of OAM cells with an incorrect CRC-10, undefined OAM Type of undefined Function Type, or RM cells with an incorrect CRC-10.

(Ingress only) Number of cells with errored headers. These include cells with unassigned/invalid VPI/VCIs or invalid PTI values.

(Ingress only) Last Unknown VPI.VCI value.

On an aggregate basis, the ATLAS maintains the following counts:

Number of cells received.

Number of cells transmitted

Number of Physical Layer Idle cells received.

Events are accumulated over consecutive intervals as defined by the period of the microprocessor initiated data latching. The ATLAS maintains current counts and holding registers. A latching event transfers the counter values into holding registers and resets the counters (if the Clear_On_Read register bit is set to logic 1) to begin accumulating events for the next interval. The counters are reset in such a manner that events occurring during the reset are not missed. The holding registers can be read via the microprocessor interface.

The ATLAS can be configured to have some of its counters roll over or saturate at all ones. All per-PHY counts and the per-connection cell counts and non-compliant cell counts are configurable in this manner. The CounterWrap register bit in the Egress Cell Processor Configuration 1 register 0x280 controls whether the per-VC counts maintained in the Egress VC Table rollover or saturate. The CounterWrap register bit in the Ingress Cell Processor Configuration 2 register 0x238 controls whether the per-VC counts maintained in the Ingress VC Table rollover or saturate. The CounterWrap register bit in the Ingress per-PHY Counter Configuration register 0x400 controls whether the Ingress per-PHY counts rollover or saturate. The CounterWrap register bit in the Egress per-PHY Counter Configuration register 0x600 controls whether the Egress per-PHY counts rollover or saturate.

All per-PHY and per-VC counts have a Clear On Read option. If this bit is logic 1, then when a counter value is immediately set to zero as soon as its value is read by a microprocessor initiated read. If the per-PHY or per-VC Clear On Read register bit is logic 0, the counter value is not cleared when it is read, and the value must be cleared by explicitly writing all zeros to that counter location. Note, the per-PHY counts are read only values and therefore cannot be cleared by writing all zeros.

The Performance Monitoring counts always saturate and non-compliant per-VC cell counts always saturate.

In order to allow for a time-of-day billing mechanism, the ATLAS may be configured to perform its general 32-bit cell counting at alternative locations. The Ingress and Egress VC Tables maintain additional storage for both cell counts. For each VC Table, the Alternate_Count register bits (in the Ingress Cell Processor Configuration 2 register 0x238 and the Egress Cell Processor Direct Lookup Index Configuration 1 register 0x282) determine whether the counting is maintained at the default location (ISA[19:16]=0110 and ESA[19:16]= 0100 and 0101) or at the alternative location of (ISA[19:16]=1001 and ESA[19:16]=0110 and 0111). Note this is a configurable option, and RAM need not be populated if this feature is not supported.

When the global register bits are set to begin accumulating counts at the alternate locations, the ATLAS will begin incrementing the cell counts at the above addresses. It is the responsibility of the management software to ensure these locations are cleared before the ATLAS begins accumulating.

8.13 Operations, Administration and Maintenance (OAM) Cell Servicing

The ATLAS is capable of terminating and monitoring F4 and F5 OAM flows. Complete processing of Fault Management cells is provided on all connections. Performance Monitoring is provided on a limited number of connections (256 simultaneous sessions are supported). Activate/Deactivate and Loopback cells are passed to the Ingress/Egress Microprocessor Cell Interface or to the Ingress/Egress Output Cell Interface for external processing. The ATLAS supports both segment and end-to-end OAM flows.

The programming of the OAM Configuration field in the Ingress and Egress VC Tables determines how the ATLAS will behave with respect to a particular connection.

Table 27 Ingress/Egress OAM Configuration Field

The OAM functionality of the ATLAS is symmetric in the Ingress and Egress directions. The OAM Configuration field for both the Ingress and Egress VC Tables is shown below:

Bit	Name	Description
8	Send_AIS_segment	If this bit is a logic 1, a segment AIS cell is generated once per second (nominally).
7	Send_AIS_end_to_end	If this bit is a logic 1, an end-to-end AIS cell is generated once per second (nominally).
6	Send_RDI_segment	If this bit is a logic 1, a segment RDI cell is generated once per second (nominally).
5	Send_RDI_end_to_end	If this bit is a logic 1, an end-to-end RDI cell is generated once per second (nominally).
4	CC_RDI	If this bit is a logic 1, RDI cells are generated at one second intervals upon the declaration of a CC alarm. The type of RDI cell (segment or end-to-end) generated depends upon the alarm declaration (segment CC alarm or end-to-end CC alarm) and whether or not the ATLAS is an end point (end-to-end point, segment end point, or both). If the ATLAS is not an end point, the RDI cell will not be generated. If both the segment and end-to-end CC alarms are asserted, then both types of RDI cells will be generated if the ATLAS is configured as both a segment end point and an end-to-end point. RDI cells which are generated as a result of the CC_RDI function have the Defect Location and Defect Type values which are programmed in the ATLAS registers, inserted in the Defect Location and Defect Type fields of the cells.
3	CC_Activate_Segment	Enables Continuity Checking on segment flows. If the ForceCC register bit is logic 0, then when no user cells are transmitted over a 1.0 second (nominal) interval, a segment CC OAM cell is generated. The segment CC cell is generated at an interval of one per second (nominally). If the ForceCC register bit is logic 1, then when the CC_Activate_Segment bit is logic 1, a segment CC cell will be generated at an interval of once per second (nominally), regardless of the flow of user cells. .
2	CC_Activate_End_to_End	Enables Continuity Checking on end-to-end flows. If the ForceCC register bit is logic 0, then when no user cells are transmitted over a 1.0 second (nominal) interval, an end-to-end CC OAM cell is generated. The end-to-end CC cell is generated at an interval of one per second (nominally). If the ForceCC register bit is logic 1, then when the CC_Activate_End_to_End bit is logic 1, an end-to-end CC cell will be generated at an interval of once per second (nominally), regardless of the flow of user cells.

1	Segment_Point	Defines the ATLAS as a Segment termination point. For F4 connections (VPCs), all cells with VCI = 3 are terminated and processed. For F5 connections (VCCs), all cells with PTI = 100 are terminated and processed.
0	End_to_End_Point	Defines the ATLAS as an End-to-End termination point. For F4 connections (VPCs), all cells with VCI = 4 are terminated and processed. For F5 connections (VCCs), all cells with PTI = 101 are terminated and processed. The End-to-End point, by definition, is also the end point for segment cells. Therefore, at End-to-End points all segment cells, as defined above, are also terminated.

Upon receipt of an OAM cell, the CRC-10 is checked. If the check sum is incorrect, the OAM cell is not processed (i.e. alarms and counts are not updated) and the per-PHY errored OAM cell count is incremented. Otherwise, further processing is dependent upon the contents of the OAM Type field and the programming of the ATLAS for that connection.

If a connection is not provisioned as an end point (segment end-point or end-to-end point), all incoming OAM cells are passed to the Ingress/Egress Output Cell Interface (subject to policing in the Ingress direction), regardless of whether or not the OAM Type or Function Type fields have defined values. As an option, OAM cells may be discarded at non-flow end points if the CRC-10 is incorrect. At flow end points, all OAM cells are terminated, except Activate/Deactivate and Loopback cells. Loopback cells may, on a per-connection basis, be routed to the Ingress/Egress Microprocessor Cell Interface for further processing. If the UNDEFtoUP register bit is a logic 1, all undefined OAM cells are routed to the Ingress/Egress Microprocessor Cell Interface for further processing or error logging. If the UNDEFtoOCIF register bit, 0x200 and 0x285, is a logic 1, all undefined OAM cells are routed to the Ingress/Egress Output Cell Interface, independent of the UNDEFtoUP register bit, 0x220 and 0x281, setting. If both register bits are logic 0 than all undefined OAM cells are discarded.

8.14 Fault Management Cells

Fault Management cells are identified with an OAM Cell Type field of 0001. The ATLAS supports segment and end-to-end AIS, RDI Continuity Check (CC) and Loopback cells.

Segment and End-to-End AIS alarm status bits in the Ingress and Egress Status fields are set upon receipt of a single AIS (function type = 0000) cell (segment or end-to-end). If the connection FM_Interrupt_Enable bit is set, a globally maskable interrupt will be asserted at the change of state of the (segment or end-to-end) AIS alarm. The alarm status is cleared upon receipt of a single user or CC cell, or if no AIS cell has been received within the last 2.5 +/- 0.5 sec. If the AUTORDI register bit is set, an RDI cell (segment or end-to-end) is generated immediately upon receipt of the first AIS cell at a flow end point and once a second thereafter until the AIS state is exited. The ATLAS inserts RDI cells in the reverse flow. That is, if an AIS cell were received in the Ingress direction, an RDI cell would be generated and sent to the Egress Output Cell Interface via the Egress Backward OAM Cell Interface and the Egress Cell Processor.

AIS cells that are generated by the ATLAS use the programmed values of Defect Location and Defect Type which are maintained in the Ingress and Egress Cell Processor register spaces. The Defect_Type[3:0] field of the Ingress and Egress Configuration Fields of the respective VC Tables are used to identify which programmed register value to use when inserting the Defect Type fields of a generated AIS cell. The Defect Location field programmed in the Ingress and Egress Defect Location registers is inserted in all generated AIS cells. The only exception to this case is the generation of an F4 End-to-End AIS cell as a result of the reception of an F4 Segment AIS cell (controlled by the APSx register bits). In this case, the default (0x6A) value is inserted in the Defect Type field of the F4 End-to-End AIS cell.

When the ATLAS receives a segment or end-to-end AIS cell, the Defect Location and Defect Type fields of the AIS cell are copied in the Ingress and Egress VC Tables. These fields are used when RDI cells are generated at segment or end-to-end points as a result of the AUTORDI process. The use of these RAM locations is controlled by the IAISCOPY and EAISCOPY register bits. If these register bits are not set, then the ATLAS does not use these RAM locations to store the received segment and end-to-end AIS Defect Location and Defect Type fields, and these RAM locations need not be populated. If these rows are not provisioned (EAISCOPY=0 register 0x283), then the RDI cells will contain the local defect type selected by the Defect_Type field in the configuration field of the Egress VC Table, and will contain the default 0x6A6A pattern in the defect location field.

Segment and End-to-End RDI alarm status bits are set upon receipt of a single RDI (function type = 0001) cell (segment or end-to-end). If the connection FM_Interrupt_Enable bit is set, a globally maskable interrupt will be asserted at the change of state of the (segment or end-to-end) RDI alarm. The alarm status is cleared if no RDI cell has been received within the last 2.5 +/- 0.5 sec.

If the CC_Activate_Segment bit is a logic 1, and no user cells have been transmitted within a 1.0 second (nominal) window, a segment CC cell is generated and sent to the Ingress/Egress Output Cell Interface. The forced generation of CC cells (independent of the flow of user cells) at one second (nominal) intervals is enabled when the CC_Activate_Segment bit is logic 1 and the ForceCC register bit is logic 1. If the ForceCC register bit is logic 0, then the generation of CC cells is dependent on the flow of user cells. Regardless of the state of the CC_Activate_Segment bit, if no user cells or segment CC cells have been received within a 3.5 +/- 0.5 sec window, the CC_Alarm_Segment status bit is set. If the connection FM_Interrupt_Enable bit is set, a globally maskable interrupt will be asserted at the change of state of the segment CC alarm. If the AUTORDI register bit is set and the CC_RDI bit of the Ingress/Egress OAM Configuration field is set, a segment RDI cell is generated once per second while the segment CC alarm is declared (if and only if the ATLAS is configured as a segment end point). Note the ATLAS inserts RDI cells in the reverse flow.

Note, RDI cells that are generated as a result of the CC_RDI process use the Defect_Type[3:0] field of the Ingress and Egress Configuration Fields of the respective VC Tables to identify which programmed register values to use when inserting the Defect Location and Defect Type fields in the generated cell. The Defect Location field of the Defect Location register (both Ingress and Egress) is also used when generating RDI cells as a result of the CC_RDI process.

The same capability exists for the End-to-End Continuity Check process and cell generation.

The Ingress of the ATLAS also supports the generation of F5 AIS and RDI cells when associated F4 connections, which are terminated, enter the AIS alarm state. This is described in detail in section 8.18.

The ATLAS may also be configured on a per-PHY basis to output AIS or RDI cells (or both) on all connections whose PHYID matches those set in a programmable register. The Ingress RDI PHY register, Ingress AIS PHY register, Egress RDI PHY register and Egress AIS PHY register control the generation of end-to-end RDI and end-to-end AIS cells generated in the Ingress and Egress directions. When set to a logic 1, these registers control the generation of AIS cells on a per-PHY basis. Each connection belonging to a PHY device for which the defect condition is set will generate a Fault Management cell of the appropriate type. For RDI cells, only those connections that are end-to-end points will have RDI cells generated.

8.15 Loopback Cells

The ATLAS provides support for processing of Loopback cells by an external processor. Loopback cells can, on a per-connection basis, be filtered to the Ingress/Egress Microprocessor Cell Interface. If the Loopback Indication is non-zero, and the Loopback Location ID matches this node (coded as all ones for flow end-points), the microprocessor should insert into the reverse flow direction, a copy of the Loopback cell with the Loopback Indication set to 0. Otherwise, the microprocessor should discard the cell.

8.16 Activation/Deactivation Cells

Activation/Deactivation cells are identified with an OAM Cell Type of 1000. They are used by the management entity to implement the handshaking required to initiate or cease the Performance Monitoring or Continuity Check processes.

The ATLAS does not process these cells. If this ATLAS is not an end-point for an OAM flow, all Activate/Deactivate cells are passed to the Ingress/Egress Output Cell Interface. If the ATLAS is an OAM flow end-point, the Activate/Deactivate cells are optionally passed to the Ingress/Egress Microprocessor Cell Interface or to the Ingress/Egress Output Cell Interface. The flow of Activate/Deactivate cells is controlled by the ACTDEtoUP and ACTDEtoOCIF register bits.

8.17 System Management Cells

System Management cells are identified with an OAM Cell Type of 1111. Their use is for further study by the ITU. The ATLAS does not process these cells. If the ATLAS is not a flow end-point for an OAM flow, all System Management cells are passed to the Ingress/Egress Output Cell Interface. If the ATLAS is an OAM flow end-point, the System Management cells are optionally passed to the Ingress/Egress Microprocessor Cell Interface.

8.18 F4 to F5 OAM Processing

The Ingress portion of the ATLAS supports the termination of F4 (VPCs) to F5 (VCCs) while maintaining the F4 to F5 transmission of OAM cells. Each VCC of a VPC must be setup as a separate connection in the Ingress VC Table. An additional connection must be setup for F4 OAM flow: the search table must be setup such that both Segment OAM cells (VCI=3) and End-to-End OAM cells (VCI=4) of the VPC resolve to this F4 OAM connection. The F4 OAM connection maybe setup as both a segment and end-to-end point, or as an end-to-end point only. The VCC connections have a VPC Pointer [15:0] at location ISA[19:16] = 0010. This pointer must be configured to point to the F4 OAM connection.

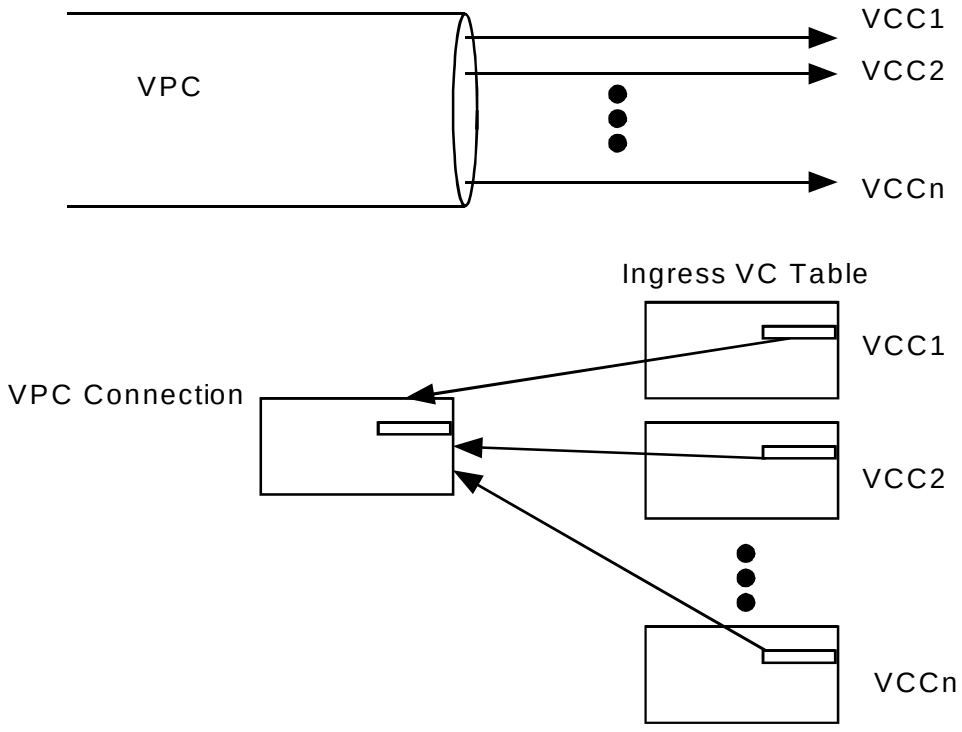
The F4 to F5 process (described above) can be disabled by setting the VPC Pointer [15:0] field equal to the connection address (i.e. a connection points to itself).

If a segment or end-to-end AIS alarm condition is indicated on the VPC connections, a background process ensures that VCC AIS cells will be transmitted on all VCCs associated with that VPC, while the VPC is in AIS alarm condition.

The Continuity Check process is also active at the F4 and F5 levels. When a user cell or CC cell is received on a VCC, both VPC connections are updated to ensure they do not enter the CC Alarm state.

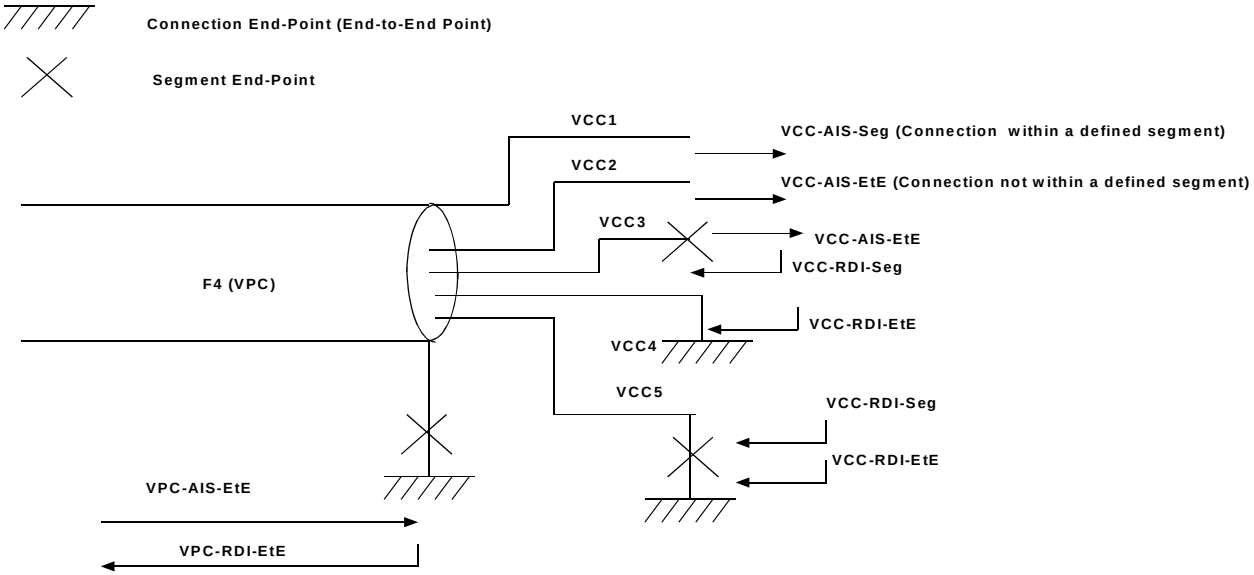
The figure below illustrates how ATLAS supports OAM flows when terminating VPC connections at the Ingress. Note that each VCC connection has its VPC pointer pointing to the Segment F4 OAM connection, and the Segment F4 connection points to the End-to-End F4 OAM connection.

Figure 8 F4 to F5 OAM Flows



The following F4 to F5 Fault Management scenarios are supported by the ATLAS at the Ingress direction.

Figure 9 Ingress Termination of F4 Segment and End-to-End-Point Connections.



In Figure 9 above, a VPC flow is being terminated. The VPC flow is both a segment end-point, and a connection (end-to-end) point. Five VCCs are being switched out from the VPC connection (all five VCCs would be setup as separate connections). In the event that an end-to-end VPC-AIS cell is received on end-to-end VPC connection, an end-to-end VPC-RDI cell would be generated (if the AUTORDI register bit is enabled). The end-to-end VPC-RDI cell would carry the end-to-end AIS Defect Location and Defect Type fields. The response of the switched VCCs is as follows:

VCC1 belongs to a segment flow, therefore, a segment VCC-AIS cell is generated within 0.5 seconds of noticing that the end-to-end VPC connection is in AIS alarm. VCC1 will continue to generate segment VCC-AIS cells at a rate of one per second (nominally) while the VPC connection is in AIS alarm (i.e. the AIS_end_to_end alarm bit is asserted for the end-to-end VPC connection).

VCC2 does not belong to a segment flow, therefore, an end-to-end VCC-AIS cell is generated within 0.5 seconds of noticing that the end-to-end VPC connection is in AIS alarm. VCC2 will continue to generate end-to-end VCC-AIS cells at a rate of one per second (nominally) while the VPC connection is in AIS alarm (i.e. the AIS_end_to_end alarm bit is asserted for the end-to-end VPC connection).

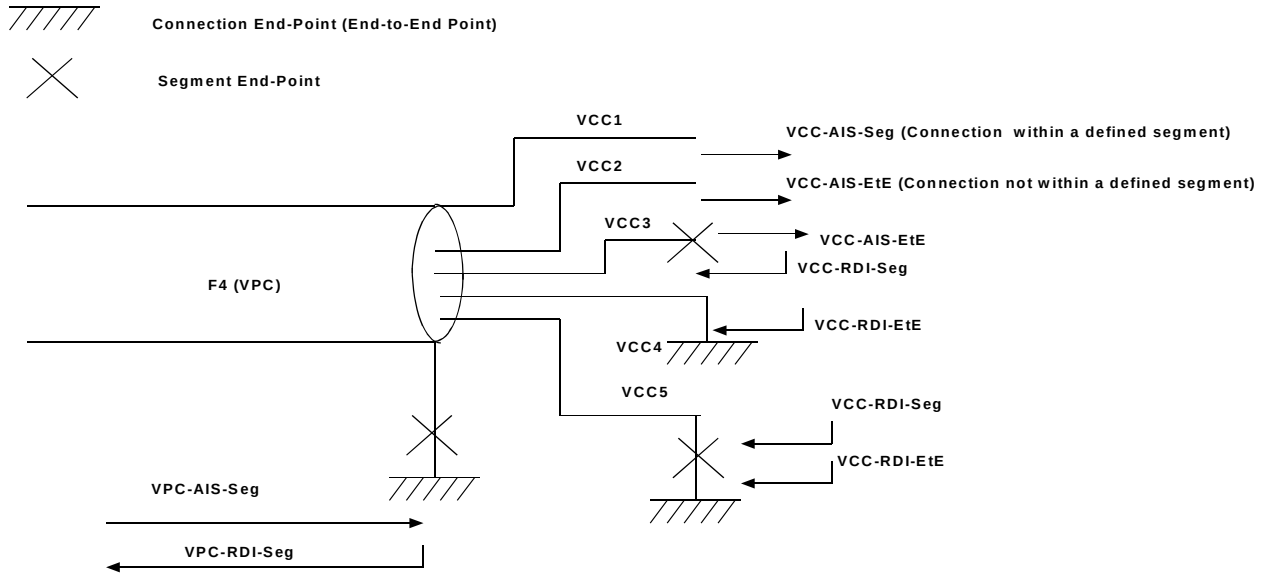
VCC3 is a segment end-point, therefore a segment VCC-RDI cell (assuming the AUTORDI register bit is set) and an end-to-end VCC-AIS cell are generated for this connection within 0.5 seconds of noticing that the end-to-end VPC connection is in AIS alarm. VCC3 will continue to generate segment VCC-RDI and end-to-end VCC AIS cells at a rate of one per second (nominally) while the end-to-end VPC connection is in AIS alarm (i.e. the AIS_end_to_end alarm bit is asserted for the VPC connection).

VCC4 is a connection end-point, therefore an end-to-end VCC-RDI cell is generated (assuming the AUTORDI register bit is set) within 0.5 seconds of noticing that the end-to-end VPC connection is in AIS alarm. VCC4 will continue to generate end-to-end VCC-RDI cells at a rate of one per second (nominally) while the end-to-end VPC connection is in AIS alarm (i.e. the AIS_end_to_end alarm bit is asserted for the VPC connection).

VCC5 is a segment end-point and a connection end-point, therefore a segment VCC-RDI cell and an end-to-end VCC-RDI cell are generated (assuming the AUTORDI register bit is set) within 0.5 seconds of noticing that the end-to-end VPC connection is in AIS alarm. VCC5 will continue to generated segment VCC-RDI and end-to-end VCC-RDI cells at a rate of one per second (nominally) while the end-to-end VPC connection is in AIS alarm (i.e. the AIS_end_to_end alarm bit is set).

The next scenario has the same connection configurations, however, a VPC-Segment AIS cell is received.

Figure 10 Ingress Termination of F4 Segment and End-to-End Point Connection



In Figure 10 above, a VPC flow is being terminated. The VPC flow is both a segment end-point, and a connection (end-to-end) point. Five VCCs are being switched out from the VPC connection (all five VCCs would be setup as separate connections). In this scenario, a segment VPC-AIS cell is received on the segment VPC connection. A segment VPC-RDI cell would be generated (if the AUTORDI register bit is enabled). The segment VPC-RDI cell would carry the segment Defect Location and segment Defect Type information. The response of the switched VCCs is as follows:

VCC1 belongs to a segment flow, therefore, a segment VCC-AIS cell is generated within 0.5 seconds of noticing that the segment VPC connection is in AIS alarm. VCC1 will continue to generate segment VCC-AIS cells at a rate of one per second (nominally) while the VPC connection is in AIS alarm (i.e. the AIS_segment alarm bit is asserted for the segment VPC connection).

VCC2 does not belong to a segment flow, therefore, an end-to-end VCC-AIS cell is generated within 0.5 seconds of noticing that the segment VPC connection is in AIS alarm. VCC2 will continue to generate end-to-end VCC-AIS cells at a rate of one per second (nominally) while the VPC connection is in AIS alarm (i.e. the AIS_segment alarm bit is asserted for the end-to-end VPC connection).

VCC3 is a segment end-point, therefore a segment VCC-RDI cell (assuming the AUTORDI register bit is set) and an end-to-end VCC-AIS cell are generated for this connection within 0.5 seconds of noticing that the segment VPC connection is in AIS alarm. VCC3 will continue to generate segment VCC-RDI and end-to-end VCC AIS cells at a rate of one per second (nominally) while the segment VPC connection is in AIS alarm (i.e. the AISsegment alarm bit is asserted for the VPC connection).

VCC4 is a connection end-point, therefore an end-to-end VCC-RDI cell is generated (assuming the AUTORDI register bit is set) within 0.5 seconds of noticing that the segment VPC connection is in AIS alarm. VCC4 will continue to generate end-to-end VCC-RDI cells at a rate of one per second (nominally) while the segment VPC connection is in AIS alarm (i.e. the AIS_segment alarm bit is asserted for the VPC connection).

VCC5 is a segment end-point and a connection end-point, therefore a segment VCC-RDI cell and an end-to-end VCC-RDI cell are generated (assuming the AUTORDI register bit is set) within 0.5 seconds of noticing that the segment VPC connection is in AIS alarm. VCC5 will continue to generated segment VCC-RDI and end-to-end VCC-RDI cells at a rate of one per second (nominally) while the segment VPC connection is in AIS alarm (i.e. the AIS_end_to_end alarm bit is set).

Figure 11 Ingress Termination of F4 Segment End-Point Connection.

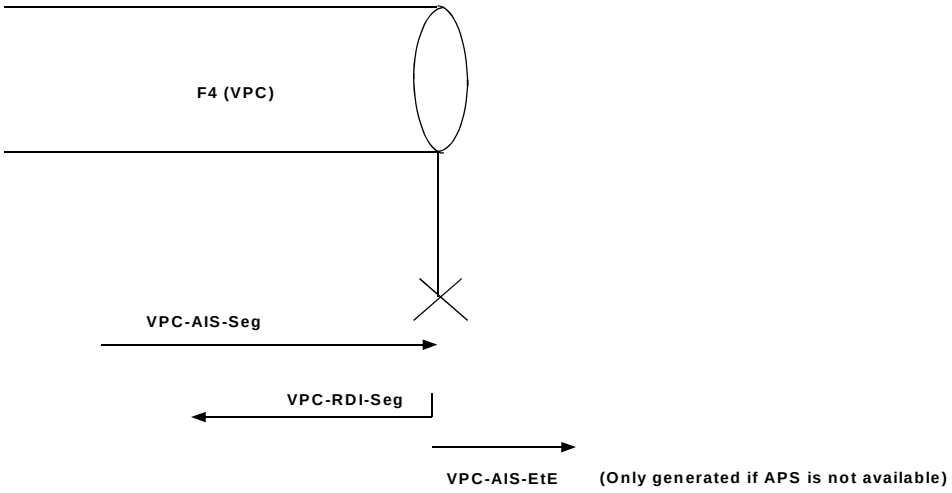


Figure 11 above illustrates the scenario where a VPC segment is being terminated at the Ingress of the ATLAS. In this case, because only a segment end-point is defined, it is assumed that only the VCCs are not switched out of the VPC (because the VPC end-to-end point is not provisioned). To enable this scenario, the VPC Pointer [15:0] field is set to the VPC segment connection address (i.e. the connection points to itself), and the connection would be configured as a segment end-point. A segment VPC-AIS cell is received and terminated. Within 0.5 seconds of receiving the segment VPC-AIS cell, a segment VPC-RDI cell is generated (assuming the AUTORDI register bit is set). As a programmable option, an end-to-end VPC-AIS cell can be generated (if end-to-end VPC-AIS cells are not being received). This per-PHY configurable option would normally only be enabled if APS is not available. The APSx register bit (where x is 0-31) determines whether or not PHYx has protection switching available. If the APSx register bit is logic 0, an end-to-end VPC-AIS cell will be generated within 0.5 seconds of entering the VPC Segment AIS alarm condition and once per second (nominally) thereafter until the VPC Segment AIS alarm condition is exited.

Figure 12 Ingress Termination of F4 End-to-End Point Connection.

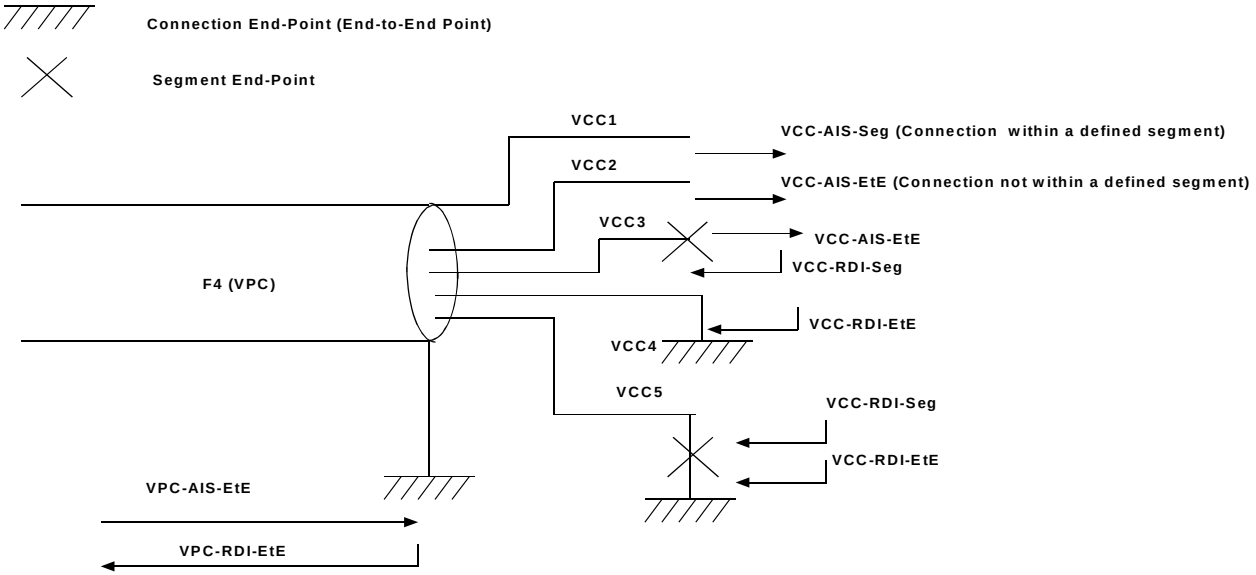


Figure 12 above illustrates the scenario where a VPC is being terminated at an end-to-end point at the Ingress of the ATLAS. In this scenario, no VPC segment exists, so all VCCs point to the associated end-to-end VPC connection, and the end-to-end VPC connection is configured as an end-to-end point and has its VPC Pointer[15:0] field set to its connection address (i.e. the connection points to itself). If an end-to-end VPC-AIS cell is received, it is terminated and an end-to-end VPC RDI cell is generated within 0.5 seconds (assuming the AUTORDI register bit is set). The response of the switched VCCs is as follows:

VCC1 is belongs to a segment flow, therefore a segment VCC-AIS cell is generated within 0.5 seconds of noticing that the VPC connection is in AIS alarm, and once per second (nominally) thereafter until the VPC connection exits the AIS alarm state.

VCC2 belongs to an end-to-end flow, therefore an end-to-end VCC-AIS cell is generated within 0.5 seconds of noticing that the VPC connection is in AIS alarm, and once per second (nominally) thereafter until the VPC connection exits the AIS alarm state.

VCC3 is a segment end-point, therefore a segment VCC-RDI cell and an end-to-end VCC-AIS cell are generated within 0.5 seconds of noticing that the VPC connection is in AIS alarm (assuming the AUTORDI register bit is set), and once per second (nominally) thereafter until the VPC connection exits the AIS alarm state.

VCC4 is an end-to-end point, therefore an end-to-end VCC-RDI cell is generated within 0.5 seconds of noticing that the VPC connection is in AIS alarm (assuming the AUTORDI register bit is set), and once per second (nominally) thereafter until the VPC connection exits the AIS alarm state.

VCC5 is a segment end-point and an end-to-end point, therefore, a segment VCC-RDI and an end-to-end VCC-RDI cell are generated within 0.5 seconds of noticing that the VPC connection is in AIS alarm (assuming the AUTORDI register bit is set), and once per second (nominally) thereafter until the VPC connection exits the AIS alarm state.

Note, in the unlikely event that a segment VPC-AIS cell is received on the end-to-end VPC connection, no action would be taken at the F5 level. This is because the VPC connection is only configured as an end-to-end point and no segment OAM cells should be received. The end-to-end VPC connection would only terminate the segment VPC-AIS cell and no further action would be taken at the F4 level.

The table below summarizes the behavior of the ATLAS for F4 to F5 Fault Management:

Table 28 F4 to F5 Fault Management Processing

Actions taken by ATLAS upon receipt of F4 AIS cells		VC Connection End-Point	VC Segment End-Point	VC Connection End-Point and Segment End-Point	VC Non End-Point	
VP Termination Type	Received Cell at F4 level				Within a VC Segment	Not within a VC Segment
VP Connection End-Point and Segment End-Point	VP End-to-End AIS	Generate VC End-to-End RDI **(4)**	Generate VC Segment RDI **(1), (4)** Generate VC End-to-End AIS **(2), (4)**	Generate VC End-to-End RDI **(4)** Generate VC Segment RDI **(1), (4)**	Generate VC Segment AIS **(3), (4)**	Generate VC End-to-End AIS **(4)**
		Generate VP End-to-End RDI cell on the End-to-End F4 connection.				
	VP Segment AIS	Generate VC End-to-End RDI **(5), (4)**	Generate VC Segment RDI **(4)** Generate VC End-to-End AIS **(4), (6)**	Generate VC End-to-End RDI **(4) (5)** Generate VC Segment RDI **(4)**	Generate VC Segment AIS **(3), (4)**	Generate VC End-to-End AIS **(4)**
		Generate VP Segment RDI cell on the Segment F4 connection.				
VP Connection End-Point Only	VP End-to-End AIS	Generate VC End-to-End RDI **(4)**	Generate VC Segment RDI **(1), (4)** Generate VC End-to-End AIS **(2), (4)**	Generate VC End-to-End RDI **(4)** Generate VC Segment RDI **(1), (4)**	Generate VC Segment AIS **(3), (4)**	Generate VC End-to-End AIS **(4)**
		Generate VP End-to-End RDI cell on the End-to-End F4 connection.				
	VP Segment AIS	Generate VC End-to-End RDI **(5), (4)**	Generate VC Segment RDI **(4)** Generate VC End-to-End AIS **(4), (6)**	Generate VC End-to-End RDI **(4) (5)** Generate VC Segment RDI **(4)**	Generate VC Segment AIS **(3), (4)**	Generate VC End-to-End AIS **(4)**
VP Segment End-Point only	VP End-to-End AIS	No cells are generated. The VP End-to-End AIS cell is passed through. We are assuming that VCs are not switched if the F4 is a Segment End-Point only.				
	VP Segment AIS	Generate VC End-to-End RDI **(5), (4)**	Generate VC Segment RDI **(4)** Generate VC End-to-End AIS **(4), (6)**	Generate VC End-to-End RDI **(4) (5)** Generate VC Segment RDI **(4)**	Generate VC Segment AIS **(3), (4)**	Generate VC End-to-End AIS **(4)**
VP non-end point	VP End-to-End AIS	No cells are generated. The received cells are passed through transparently.				
	VP Segment AIS	Generate VC End-to-End RDI **(5), (4)**	Generate VC Segment RDI **(4)** Generate VC End-to-End AIS **(4), (6)**	Generate VC End-to-End RDI **(4) (5)** Generate VC Segment RDI **(4)**	Generate VC Segment AIS **(3), (4)**	Generate VC End-to-End AIS **(4)**

1. **(1)** This feature is controlled by the F4EAISF5SRDI register bit. When this bit is logic 1, a segment VC-RDI cell will be generated when an end-to-end VPC-AIS cell is terminated at a VPC end-to-end point, and an associated VCC segment end-point is switched from that VPC. If this bit is logic 0, a segment VC-RDI cell will not be generated in this circumstance.

2. **(2)** This feature is controlled by the F4EAISF5EAIS register bit. When this bit is logic 1, an end-to-end VC-AIS cell will be generated when an end-to-end VPC-AIS cell is terminated at a VPC end-to-end point, and an associated VCC segment end-point is switched from that VPC. If this bit is logic 0, an end-to-end VC-AIS cell will not be generated in this circumstance.

3. **(3)** This feature is controlled by the SegmentFlow bit in the Ingress VC Table Configuration field at ISA[19:16]=0010. If this bit is logic 1, the VCC is considered to be part of a segment flow, and a segment VC-AIS cell will be generated when an end-to-end VP-AIS cell is terminated at a VPC end-to-end point.

4. **(4)** This feature is controlled by the F4toF5AIS bit in the Ingress VC Table at ISA[19:16]=0001. If this bit is logic 1, the F4 to F5 Fault Management scenarios are enabled. If this bit is logic 0, no F5 Fault Management cells will be generated as a result of the reception of F4 Fault Management cells. However, the Continuity Check process will still be active on the F4 and F5 levels if the VPC Pointer[15:0] fields do not point to their own connection addresses (i.e. the VCCs do not point to themselves) and the VPC Pointer fields are correctly setup.

5. **(5)** This feature is controlled by the F4SAISF5ERDI register bit. When this bit is 1, an end-to-end VC-RDI cell will be generated when a segment VPC-AIS cell is terminated at a VPC segment end-point. If this bit is logic 0, an end-to-end VC-RDI cell will not be generated in this circumstance.

6. **(6)** This feature is controlled by the F4SAISF5EAIS register bit. When this bit is logic 1, an end-to-end VC-AIS cell will be generated when a segment VPC-AIS cell is terminated at a VPC segment end-point. Note, the VCC connection is not part of a segment flow (SegmentFlow=0). If this bit is logic 0, and end-to-end VC-AIS cell will not be generated in this circumstance.

7. **(7)** This feature is controlled on a per-PHY basis by the APSx register bit (where x is from 0-31). When the APSx register bit is logic 0, it indicates there is no automatic protection switching on PHY x . When a VPC connection is configured as a segment end-point only and a segment VPC-AIS cell is received, an end-to-end VPC-AIS cell is generated (assuming that end-to-end VPC-AIS cells are not being received). When the APSx register bit is logic 1, an end-to-end VPC-AIS cell is not generated in this circumstance.

When an RDI cell is generated due to the CC_RDI, per-PHY RDI, Send_RDI_End_to_End or Send_RDI_Segment, the RDI will contain the defect type selected by the Defect_Type[3:0] field in the Configuration field of the Ingress VC Table, and the local Defect Location programmed in the Ingress Defect Location register. When an RDI cell is generated due to the reception of an AIS cell, the RDI cell will contain the AIS Defect Location and AIS Defect Type fields which are stored in the Ingress VC Table at ISA[19:16] = 1010, 1011 and 1100 of the connection which received the AIS. For example, an F5-RDI cell generated as the result of receiving and F4 Segment AIS would use the segment defect location and type stored for the F4 segment connection. If these rows are not provisioned (IAISCOPY=0), then the RDI cells will contain the local defect type selected by the Defect_Type field in the configuration field of the Ingress VC Table, and will contain the default 0x6A6A pattern in the defect location field.

If an F4 connection enters the AIS alarm condition (segment or end-to-end), the associated F5 connections will not enter the AIS alarm condition (i.e. the AIS_end_to_end alarm and/or the

AIS_segment alarm bit will not be asserted on the F5 connection). The F5 connections will, however, most likely be in the CC_alarm (segment and end-to-end) condition.

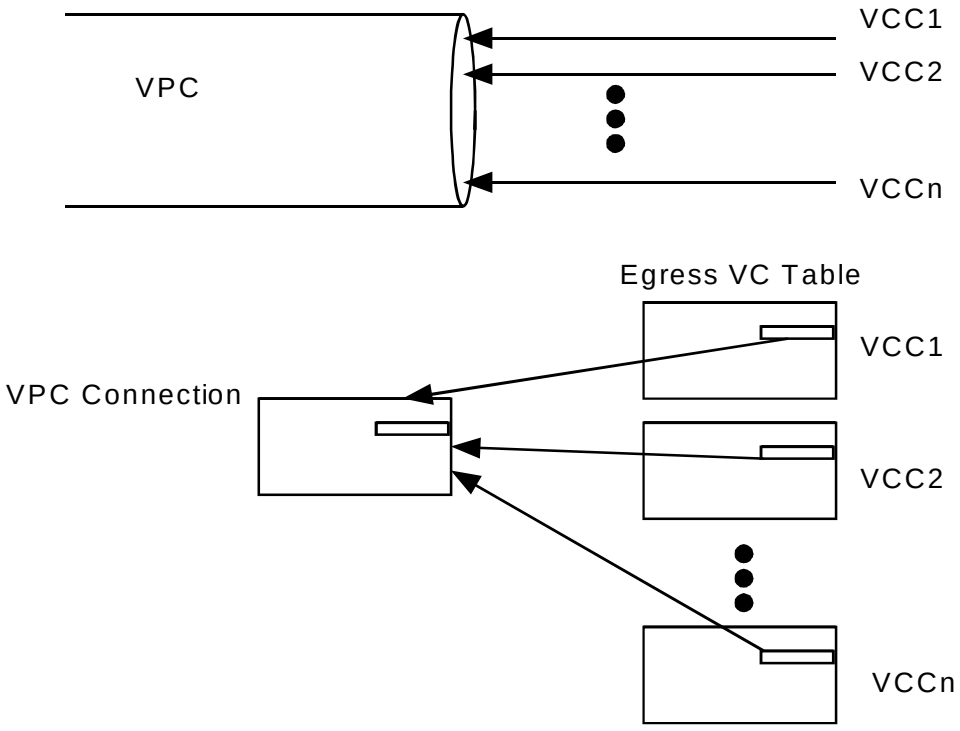
8.19 F5 to F4 OAM Processing

The Egress portion of the ATLAS supports the aggregation of F4 connections (VPCs) from F5 connections (VCCs). Each VCC of a VPC must be setup as a separate connection in the Egress VC Table (this provides the ability of performing both F4 and F5 performance monitoring simultaneously). Two additional connections must also be setup: the Segment OAM connection (VCI=3) and the End-to-End OAM connection (VCI=4) of the VPC. The VCC connections have a VPC Pointer[15:0] field at location ESA[19:16]=0011. Each VCC must have their VPC Pointer[15:0] field configured to point at the Segment OAM connection. The Segment OAM connection uses its VPC pointer to point to the End-to-End OAM connection. The F5 to F4 process can be deactivated by setting the VPC Pointer[15:0] field equal to the connection address (i.e. the connection points to itself).

The Continuity Check process is active at both the F4 and F5 levels. When a user cell or CC cell is transmitted on a VCC, both the segment and end-to-end VPC connections are updated to ensure they do not enter the CC Alarm state. If user or CC cells are not transmitted, the VPC and VCC connections will enter the CC Alarm state, and CC cells can be optionally transmitted to ensure the downstream entities do not enter the CC Alarm state.

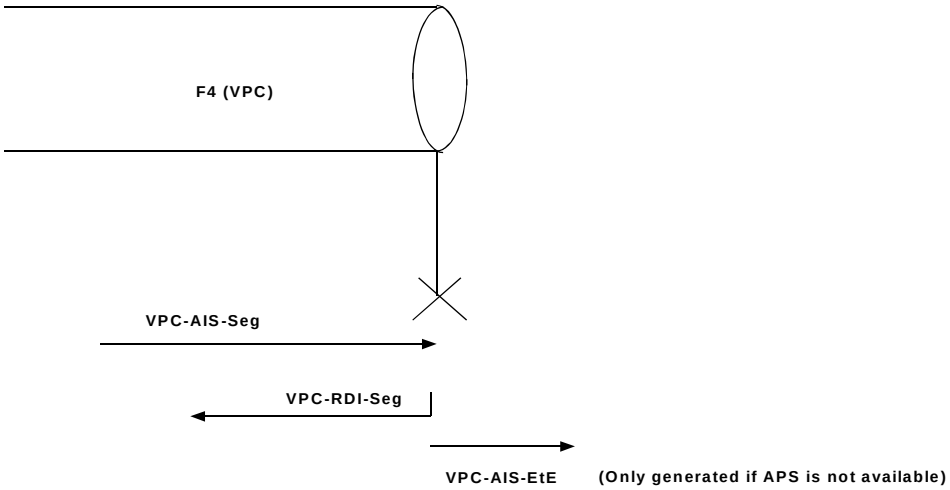
The figure below illustrates how the ATLAS supports the aggregation of the VCCs into a VPC at the Egress. Note that each VCC connection has its VPC pointer pointing to the Segment F4 OAM connection, and the Segment F4 connection points to the End-to-End F4 OAM connection.

Figure 13 F5 to F4 OAM Flows



The Egress path of the ATLAS also supports termination of segment VPC connections (where VCCs are **not** switched). This case is shown below in figure 14 below.

Figure 14 Egress Termination of a VPC Segment End-point



In this case, because only a VPC segment end-point is defined VCCs are not switched out (recall that the Egress of the ATLAS does not support F4 to F5 switching because this should be done at the Ingress of the ATLAS). To enable this scenario, the VPC Pointer[15:0] field is set to point to itself, and the connection would be configured as a segment end-point. A segment VPC-AIS cell is received and terminated. Within 0.5 seconds of receiving the segment VPC-AIS cell, a segment VPC-RDI cell is generated (assuming the AUTORDI register bit is set). As a programmable option, an end-to-end VPC-AIS cell can be generated (assuming that end-to-end VPC-AIS cells are not being received). This per-PHY configurable option would normally only be enabled if APS is not available. The APSx register bit (where x is 0-31) determines whether or not PHYx has protection switching available. If automatic protection switching is not available, the VPC segment end-point will generate an end-to-end VPC AIS cell within 0.5 seconds and once per second (nominally) thereafter until the VPC Segment AIS alarm condition has exited.

S/UNI-ATLAS OAM Functionality

The following figures illustrate the OAM capability of the ATLAS. The following definitions are applicable:

- Obs: Observation (non-intrusive monitoring point) point.
- Gen: Generation.
- Del: Termination point.
- F41: F4 (VPC) End-to-End flow.
- F42: F4 (VPC) Segment flow.

- F51: F5 (VCC) End-to-End flow.
- F52: F5 (VCC) Segment flow.

Figure 15 VPC Intermediate Point

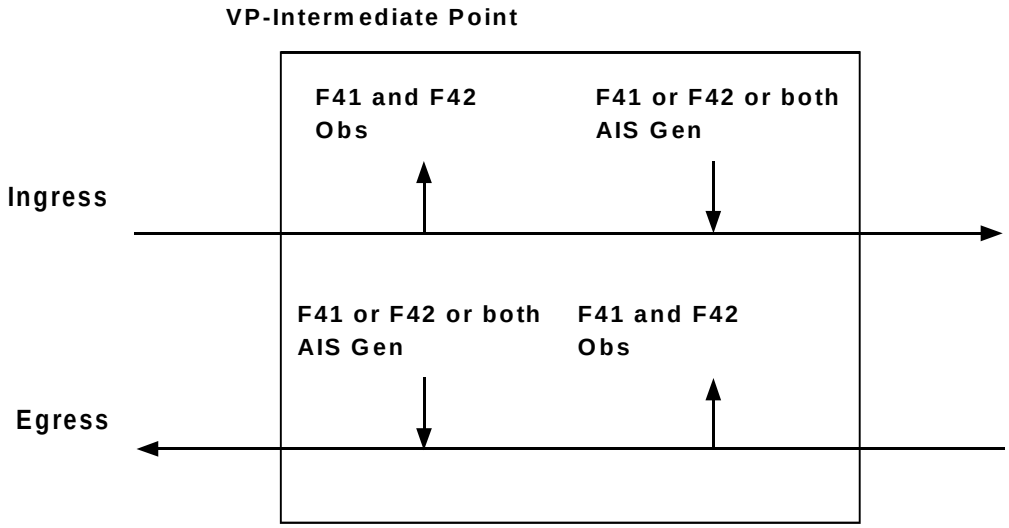


Figure 16 VCC Intermediate Point

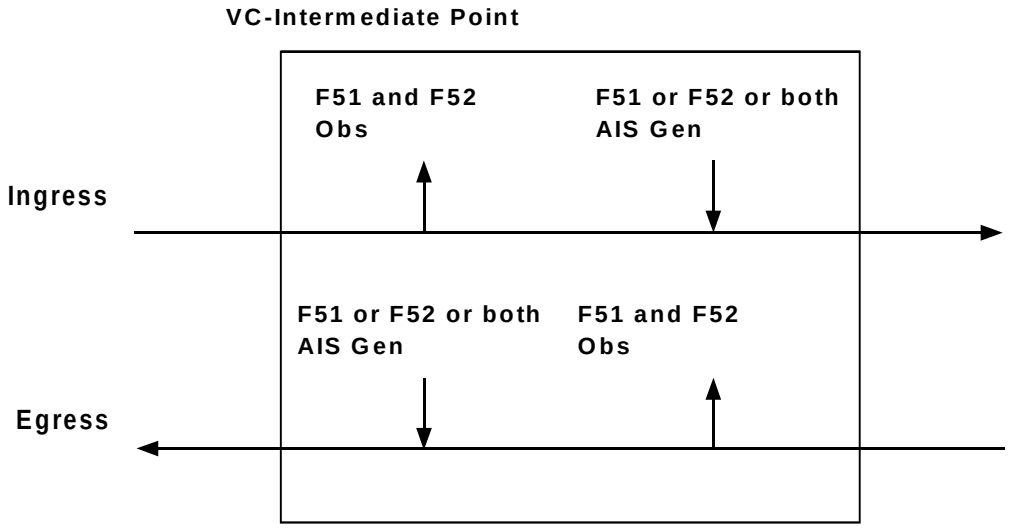


Figure 17 VPC Segment End-Point

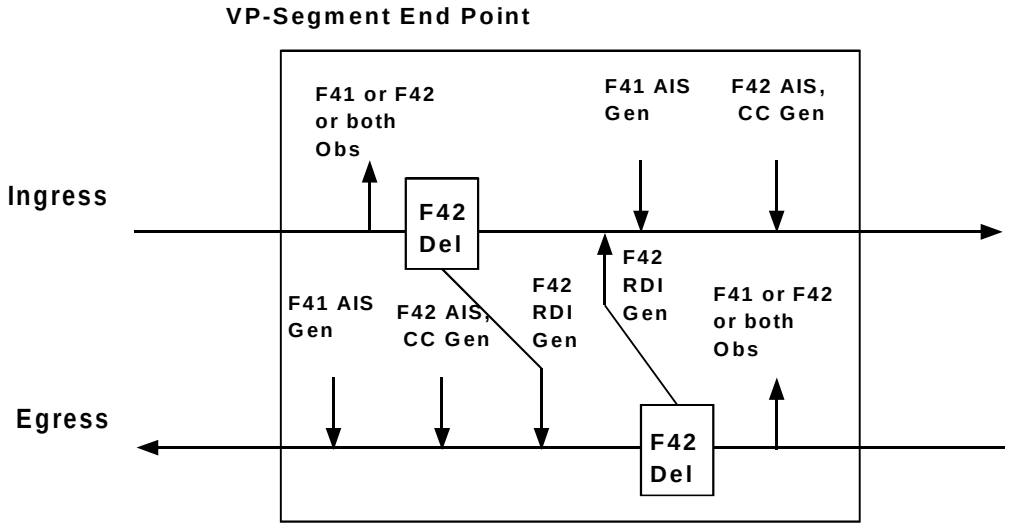


Figure 18 VCC Segment End Point

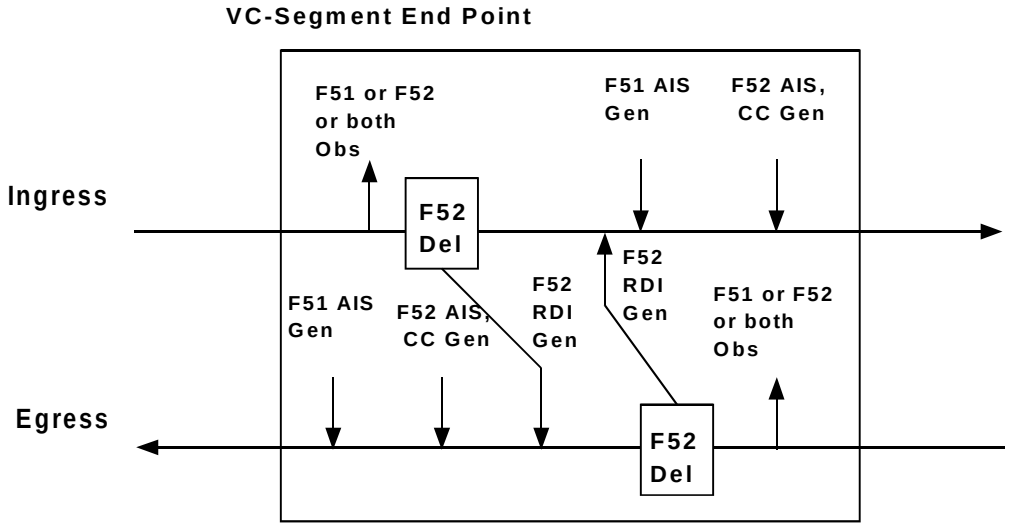


Figure 19 VPC Segment End-Point and End-to-End Point

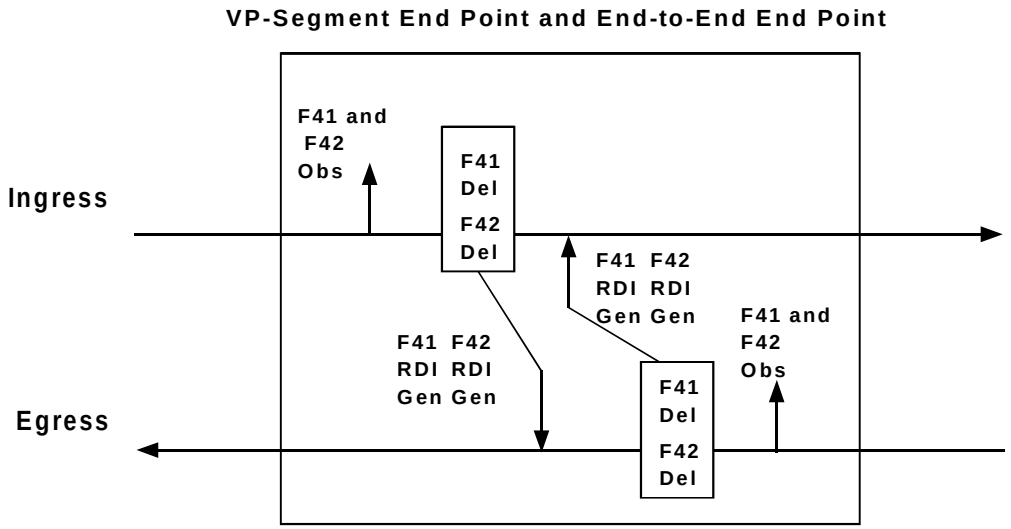
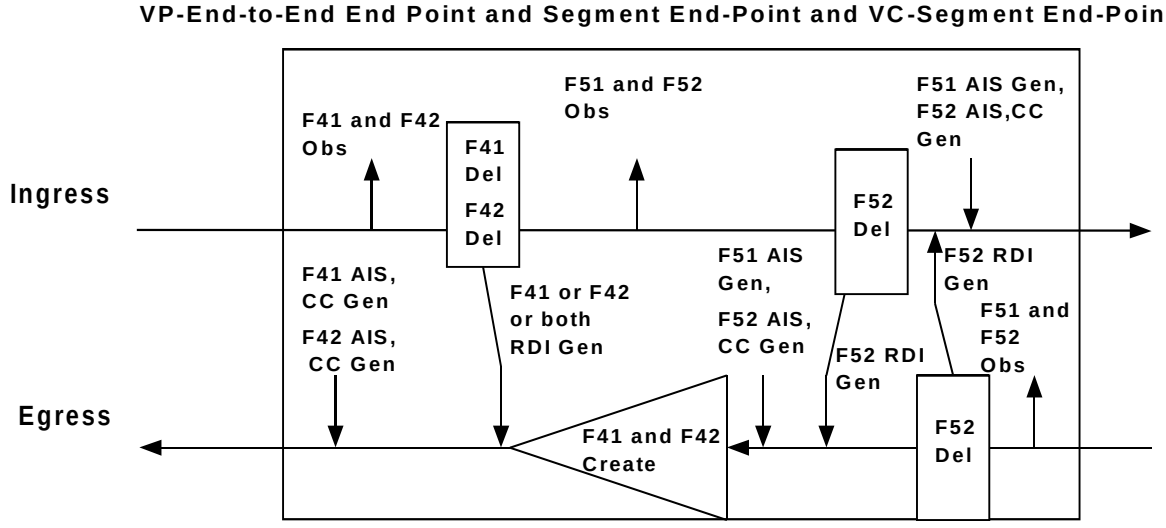
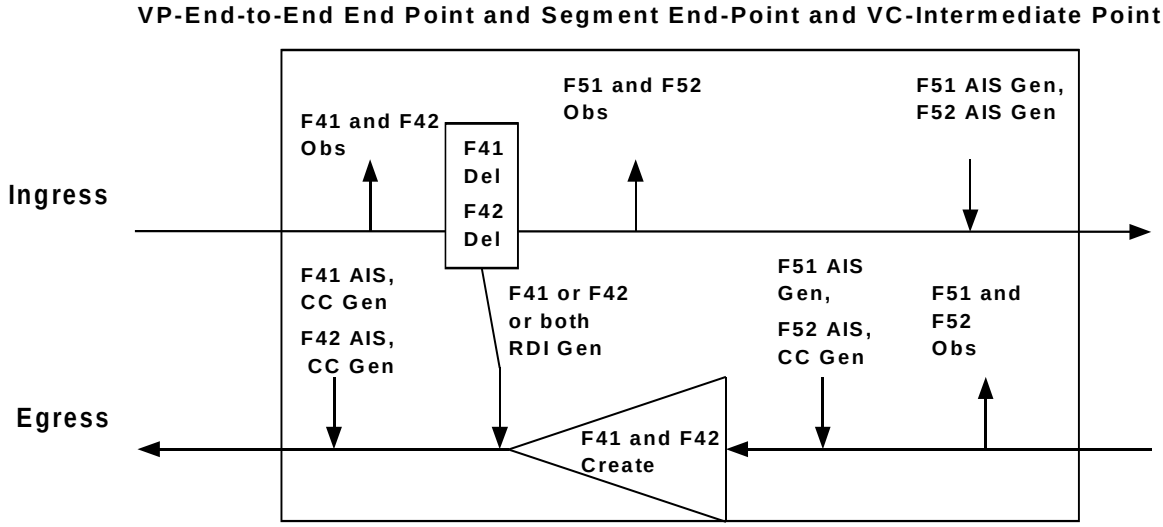


Figure 20 Ingress VPC End-to-End Point and Segment End-Point, VC Segment End-Point and Segment Source Point. Egress VPC End-to-End and Segment Source Point with VCC Segment End-Point and VCC Segment Source Point



In the figure above, an F4 is created (aggregated) at the Egress of the ATLAS.

Figure 21 Ingress VPC End-to-End and Segment End Point with VC Intermediate Point. Egress VPC End-to-End and Segment Source Point with VC Intermediate Point and VC Segment Source Point.



In the figure above, an F4 is created (aggregated) at the Egress of the ATLAS.

8.20 Resource Management Cells

Resource Management (RM) cells are identified by a PTI=110 for VC-RM cells and by VCI=6 for VP-RM cells. As a programmable option, VP-RM cells can be further qualified by PTI=110.

The ATLAS does not process the RM cell payload, but simply passes these cells to the Ingress/Egress Output Cell Interface with a translated header (optional). As a programmable option, the ATLAS can copy RM cells to the Ingress/Egress Microprocessor Cell Interface.

8.21 S/UNI-ATLAS Background Processes

The ATLAS performs numerous background processes to perform correct and compliant OAM-Fault Management cell generation, and alarm monitoring as well as maintaining the per-connection and per-PHY TAT policing parameters. The background processes are triggered either by the internally generated 0.5 second clock event, or by the external 0.5 second clock input pin.

The Ingress Cell Processor maintains 4 background processes. They are:

1. RDI cell generation.

2. AIS/CC cell generation.

3. TAT updating.

4. CC, RDI and AIS Change of State and alarm monitoring.

The Ingress VC Table Maximum Index register controls the maximum 16-bit Ingress VC Table address which must be monitored by the various background processes.

The RDI cell generation process is controlled by the status of the Egress Backward Cell Interface. If this FIFO is filled, no RDI cells will be generated. This ensures that no RDI cells will be lost due to overflow of the Egress Backward Cell Interface. If the FIFO is filled, this background process will be suspended.

The AIS/CC cell generation process is controlled by the status of the Ingress Output Cell Interface, and by a programmable threshold that determines the maximum rate at which AIS/CC cells can be generated. If the Ingress Output Cell Interface is full, this process will be suspended. If an AIS or CC cell is generated, the process will be suspended until the expiry of a user programmable counter threshold.

The TAT updating process ensures the theoretical-arrival-times track the free running time-of-arrival counter of the ATLAS. This ensures that connections which have a long gap between inter-cell arrivals are never mistakenly policed due to a roll over of the free running time-of-arrival counter.

The CC, RDI and AIS change of state and alarm monitoring process is controlled by the fill status of the Change of State FIFO. If the change of state FIFO is not used, then this process is not throttled by the FIFO fill status. If the FIFO is used, then notification of changes of state in CC, RDI and AIS alarms will be suspended until the FIFO is not full. This ensures the management software never misses any change of connection status. The Excessive Policing Status bit is also part of the Ingress Change of State FIFO. If the XPOLICE status bit changes state, the Change of State FIFO will be updated. **It is the responsibility of the management software to ensure the FIFO is read often enough so that the alarm declarations remain compliant with Bellcore GR-1248-CORE and ITU-T I.610.**

All background processes have the lowest priority over cells which are received at the Ingress Input Cell Interface.

The Egress Cell Processor maintains 3 background processes. They are:

1. RDI cell generation.

2. AIS/CC cell generation.

3. CC, RDI and AIS Change of State and alarm monitoring.

The Egress VC Table Maximum Index register controls the maximum 16-bit Egress VC Table address which must be monitored by the various background processes.

The RDI cell generation is controlled by the status of the Ingress Backward Cell Interface. If this FIFO is filled, no RDI cells will be generated. This ensures that no RDI cells will be lost due to overflow of the Ingress Backward Cell Interface. If the FIFO is filled, this background process will be suspended.

The status of the Egress Output Cell Interface and the state of the PHY TCA signals control the AIS/CC cell generation process. The AIS/CC cell generation process is also controlled by a programmable threshold that determines the maximum rate at which AIS/CC cells can be generated. If the Egress Output Cell Interface is full, or if the PHY TCA signal is deasserted, the process will be suspended. Also, if an AIS or CC cell is generated, the process will be suspended until the expiry of a user programmable counter threshold.

Policing is not performed in the Egress path of the ATLAS, therefore, no TAT updating process needs to be performed.

The CC, RDI and AIS change of state and alarm monitoring process is controlled by the fill status of the Change of State FIFO. If the change of state FIFO is not used, then this process is not throttled by the FIFO fill status. If the FIFO is used, then notifications of changes of state in CC, RDI and AIS alarms will be suspended until the FIFO is not full. This ensures the management software never misses any change of connection status**. It is the responsibility of the management software to ensure the FIFO is read often enough so that the alarm declarations remain compliant with Bellcore GR-1248-CORE and ITU-T I.610**.

All background processes have the lowest priority over cells which are received at the Egress Input Cell Interface.

8.22 Ingress Backward OAM Cell Interface

The Ingress Backward OAM Cell Interface (Ingress BCIF) uses a common memory to store all Egress-generated RDI and Backward Reporting PM cells until such time as they are transmitted by the Ingress Cell Processor. The Ingress Backward OAM Cell Interface maintains a 4-cell FIFO for Egress-generated RDI cells, and a 16-cell FIFO for Egress-generated Backward Reporting PM cells. The ATLAS will insert cells from the Ingress Backward OAM Cell Interface at the specified insertion rate. The BCIF insertion rate is the minimum rate at which cells will be inserted from the Ingress BCIF.

8.23 Egress Backward OAM Cell Interface

The Egress Backward OAM Cell Interface uses a common memory to store all Ingress-generated RDI and Backward Reporting PM cells until such time as they are transmitted by the Egress Cell Processor. Under normal operating conditions, the ATLAS will insert cells from the Egress Backward OAM Cell Interface into the Egress cell stream at the specified insertion rate. In the event the PHY device, for which the cell at the head of the FIFO is destined, becomes inoperative (i.e. the PHY's TCA signal is never asserted), that cell must be dealt with so that it does not prevent other PHY devices from having cells inserted in the Egress stream. The Egress Cell Processor can be programmed with a Head-of-Line Time Out function to deal with this problem. If a PHY does not respond with the re-assertion of its TCA signal after a specified time, the ECP can take a programmable action on that cell. The time out counter is defined in terms of cell periods at the ESYSCLK rate, where one cell period is equal to 32 clock cycles. The Head-of-Line Time Out can be programmed to take into account the worst case time for TCA assertion (e.g. 4 cell periods at a T1-PHY rate). The ECP may be programmed to discard the cell, or to route the cell to the Egress Microprocessor Interface, where it may be stored and re-inserted at a later time when the PHY problem has been resolved. This function is provided solely to retain a quality of service for other PHY devices in case a catastrophic event occurs on a particular PHY device. In normal operating mode, this situation will never be encountered. The Head-of-Line Time Out can be disabled.

8.24 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST are supported. The ATLAS identification code is 073240CD hexadecimal.

8.25 Microprocessor Interface

The microprocessor interface is provided for device configuration, control and monitoring by an external microprocessor. Normal mode registers, test mode registers, the external Ingress and Egress VC Tables (external SRAM) and the internal PM and per-PHY policing RAM can be accessed through this port. Test mode registers are used to enhance the testability of the ATLAS.

The interface has a 16-bit wide data bus. Multiplexed address and data operation is supported.

8.26 External SRAM Access

Microprocessor access to the external SRAM is provided to allow configuration of individual connections. The Ingress Search Engine and Egress Cell Processor allocate a single cycle at the beginning of each search/processing cycle for microprocessor accesses. The maximum time to complete a external SRAM access is 1200 ns with a I/E SYSCLK frequency of 50 MHz. The average completion time is less than 700ns. Upon placing the ISE in standby mode (default upon power up), all SRAM cycles become available to the microprocessor. This allows for rapid configuration of the device at startup. The Egress Cell Processor may also be placed in standby mode (default upon power up) to allow all SRAM cycles for the microprocessor.

For externally requested write cycles, the ATLAS can cache all data rows for a single VC Table connection in internal memory. The Ingress Search Engine maintains the data cache for externally requested write cycles, and it can cache all rows of the Ingress VC Table. Similarly, the Egress Cell Processor maintains the data cache for externally requested write cycles and it can cache all rows of the Egress VC Table. The BUSYB signal is asserted when an Ingress or Egress external SRAM access is pending. The signal is then deasserted when the external SRAM access is completed. The IBUSY and EBUSY register status bits are also asserted until the external SRAM access is completed.

For externally requested read cycles, the ATLAS may cache an entire VC Table worth of data in internal memory. The Ingress Search Engine can be configured to read all rows of the Ingress VC Table. Similarly, the Egress Cell Processor can be configured to read all rows of the Egress VC Table for any connection. The BUSYB signal are asserted when an Ingress or Egress external access is pending. The signals are then deasserted when the external SRAM access is completed. The IBUSY and EBUSY register status bits are also asserted until the external SRAM access is completed. If the ClearOnRead register bit is set, then a clearing write-back is made whenever a read of the Non-Compliant Cell counts, CLP0 or CLP1 cell counts is made.

The BUSYB output can be connected to a DMA request input of a DMA controller. The rising edge of BUSYB would initiate the next external SRAM access upon completion of the current access.

8.27 Writing Cells

The ATLAS contains a one cell buffer for the assembly of a cell by the microprocessor for presentation on the Ingress or Egress Output Cell Interface. Optional header translation and CRC-10 protection provides full support of diagnostic and OAM requirements.

In the Ingress direction, cells inserted via the Ingress Microprocessor Cell Interface are inserted into the Ingress cell stream by the Ingress Search Engine. The Ingress Search Engine gives an equal priority between cells received from the Ingress Input Cell Interface and cells received from the Ingress Microprocessor Cell Interface. Therefore, it is the responsibility of the management software to ensure that cells are not inserted via the Ingress Microprocessor Cell Interface too frequently (i.e. the management software must ensure these inserted cells are paced).

Similarly, in the Egress direction, cells inserted via the Egress Microprocessor Cell Interface are inserted into the Egress cell stream by the Egress Cell Processor. The Egress Cell Processor gives an equal priority between cells received from the Egress Input Cell Interface and cells received from the Egress Microprocessor Cell Interface. Therefore, it is the responsibility of the management software to ensure that cells are not inserted via the Egress Microprocessor Cell Interface too frequently.

Writes are performed through the Ingress and Egress Microprocessor Cell Interface Control and Status and Microprocessor Cell Interface Data registers. The steps below outline how to insert a cell in the Ingress/Egress Microprocessor Cell Interface:

Poll the INSRDY register bit of the Ingress/Egress Microprocessor Cell Interface Insert Control and Status register until it is a logic 1. Alternatively, service the interrupts that result from setting the Ingress/Egress INSRDYE bit in the Master Interrupt Enable register. The Ingress/Egress INSRDYI bit in the Master Interrupt Status register is set whenever the Ingress/Egress INSRDY bit is set.

Write the WRSOC bit in the Ingress/Egress Microprocessor Cell Interface Insert Control and Status register. At the same time, ensure that the OLEN[2:0], CRC10, UPHDRX and PHY[4:0] register bits are set to their correct values, depending on what operation is required.

If the UPHDRX register bit is a logic 1, PHY[4:0] represents the PHY address that the cell is associated with and will be included in the search key used for VC identification in the ingress direction, and to determine which PHY device to transmit the cell will be transferred to in the egress direction.

Write the cell contents to the Ingress/Egress Microprocessor Cell Interface Data register. Each subsequent write enters the next word in the cell. The words shall be written in the following order:

Word #	Contents
1	1st prepended word (optional)
…	…
M	Last prepended word (optional)
M+1	1st postpended word (optional)
N	Last postpended word, N<6 (optional)
N+1	ATM Header: GFC, VPI, VCI[15:12]
N+2	ATM Header: VCI[11:0], PTI, CLP
N+3	HEC and UDF fields
N+4	1st ATM payload word
N+5	2nd ATM payload word
…	…
N+27	27th ATM payload word

In the ingress direction, if the cell's header is to be translated (UPHDRX logic 1), the number of appended words shall match that programmed in the Ingress Input Cell Interface Configuration register. If the cells' header is not to be translated (UPHDRX logic 0), the number of appended bytes shall match that programmed in the Ingress Output Cell Interface Configuration register. The ATLAS automatically handles cell length mismatches. Extra words shall be stripped off with no consequences, but words that must be added will have arbitrary contents; therefore, the resulting cell processing may be unpredictable. The Ingress Search Engine does not perform a search of inserted cells when UPHDRX=0, therefore the per-connection counts will not increment and the cell need not belong to a provisioned connection.

In the egress direction, if the cell's header is to be translated (UPHDRX logic 1), the number of appended words shall match that programmed in the Egress Input Cell Interface Configuration register. The Egress Cell Processor performs a direct lookup on the prepended/postpended, header or HEC/UDF bytes, therefore it is the responsibility of the microprocessor to ensure that the field used for direct lookup is correct. If the cell's header is not to be translated (UPHDRX logic 0), the number of appended words shall match that programmed in the Egress Output Cell Interface Configuration register. The Egress Cell Processor does not perform a direct lookup of cells inserted when UPHDRX=0, therefore the cell need not belong to a provisioned connection. The per-connection cell counts will not increment as a result of an inserted cell with UPHDRX=0.

8.28 Reading Cells

Cells received on the Ingress or Egress Input Cell Interface can be routed to the Ingress/Egress Microprocessor Cell Interface based on the type of cell.

The Ingress and Egress MCIF buffers have a capacity of 15 to 18 cells depending on the length of the extracted cells:

Words in cell	LEN[2:0]	Buffer Capacity
27	2	18
28	3	18
29	4	17
30	5	17
31	6	16
32	7	15

Maskable interrupt statuses are generated upon the receipt of a cell and upon buffer overflow. If a buffer overflow occurs, entire cells are lost.

Cells are written into the Ingress/Egress MCIF buffers without header translation. As an option, the HEC byte location can be overwritten with the PHY device identification. The length of the cell is determined by the CELLLEN[3:0] bits in the Ingress/Egress Input Cell Interface Configuration register and the UPURS in the Ingress/Egress Cell Processor Configuration register. If the UPURS bit is a logic 1, a causation word is prepended to the cell to indicate why the cell was routed to the Ingress/Egress MCIF and provides cell status information.

The causation word has the following format:

CAUSE[15:0]	Definition
Bit 15	PHYID[4]
Bit 14	PHYID[3]
Bit 13	PHYID[2]
Bit 12	PHYID[1]
Bit 11	PHYID[0]
Bit 10	PROV
Bit 9	End_to_End_Point
Bit 8	Segment_End_Point
Bit 7	TimeOut
Bit 6	NNI
Bit 5	VPC
Bit 4	OAM_Type
Bit 3	TYP[3]
Bit 2	TYP[2]
Bit 1	TYP[1]
Bit 0	TYP[0]

PHYID[4:0]: The index of the PHY device associated with the cell.

PROV: Provisioned connection. This bit is a logic 1 if the cell belongs to a provisioned connection. A logic 0 indicates the connection search failed to find a VC Table Record for the cell. The End_to_End_Point, Segment_End_Point, NNI, OAM_Type, and TYP[3:0] fields are undefined if PROV is a logic 0. Also, on cells from the Ingress path the PHYID[4:0] is not valid if PROV is a logic 0.

End_to_End_Point Indicates the connection is provisioned as an OAM flow end point.

Segment_End_Point Indicates the connection is provisioned as an OAM flow segment end point.

TimeOut — (Only valid for the Egress Microprocessor Cell Interface) Indicates the cell was removed from the Backward Cell interface because the head-of-line blocking timer has expired. When this bit is set, only the PHYID and TYP fields are valid.

NNI: — Indicates the connection is associated with a Network-Network Interface (NNI). A logic 0 means the connection belongs to a User-Network Interface (UNI).

VPC — Indicates the connection is provisioned as a Virtual Path Connection (VPC). A logic 0 means the connection is provisioned as a Virtual Channel Connection (VCC).

OAM_Type — A logic 1 identifies a segment OAM cell. A logic 0 identifies an end-to-end OAM cell. This bit is not defined when the TYP[3:0] field is 0000, 1011, 1100 or 1101.

TYP[3:0] — Cell type. This field is encoded as follows:

TYP[3:0]	Cell Type
0000	User
0001	AIS
0010	RDI
0011	Continuity Check
0100	Loopback
0101	Forward Monitoring
0110	Backward Reporting
0111	Reserved
1000	Activate/Deactivate
1001	Undefined OAM
1010	System Management OAM
1011	Forward RM
1100	Backward RM
1101	Invalid PTI/VCI

1110	Reserved
1111	OAM cell with errored CRC-10

The EXTCA bits of the Ingress/Egress MCIF Extract Buffer Control and Status registers are asserted if one or more complete cells are available in the buffer. If DMA control is enabled (DMAEN bit logic 1), the DREQ output is also asserted upon receipt of a cell. The first read of the Ingress/Egress MCIF after either the EXTCA bit or the DREQ is asserted, returns the first word of the cell. Subsequent reads return the remainder of the cell. The sequence of words is the same as for buffer writes (see above). At any time, the read pointer can be returned to the beginning of the cell by setting the RESTART bit. The current cell is discarded upon setting the ABORT bit. The DREQ output is deasserted during the read of the last word of the cell.

8.29 ATLAS DLL Clock Operation

The ATLAS uses a Digital Delay Locked Loop (DLL) to control the skew of internal clock nets. The DLL measures the phase difference between the system clock and the reference clock and generates an internal clock that reduces the phase difference between the system clock and the reference clock to zero. The internally generated clock is a delayed version of the system clock created using a digital delay line.

The ATLAS requires that all input clocks at stable and glitch free. Changing the clock frequency of the device during normal operation can resolute in the device locking-up or performing in a non-consistent manner.

The operation of the DLL defaults to the optimum configuration. Under normal operating conditions no programming of the DLL's is required for correct operation. It is recommended that the device be held in soft-reset, register 0x000, until the RUN bit, in register 0x00C, is set. The RUN bit indicates that all DLL's in the ATLAS are operating correctly and have locked-on to the input clock frequency.

9 NORMAL MODE REGISTER MEMORY MAP

Table 29 Register Memory Map

9.1 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI-ATLAS. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[11]) is low.

For all register accesses, CSB must be low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-ATLAS to determine the programming state of the block.

3. Writeable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-ATLAS operation unless otherwise noted.

Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-ATLAS operates, as intended, reserved register bits must only be written with the value indicated. Similarly, writing to reserved registers should be avoided.

Register 0x000: S/UNI-ATLAS Master Reset and Identity / Load Performance Meters

Bit	Type	Function	Default
15	R/W	RESET	0
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6	R	TYPE[2]	0
5	R	TYPE[1]	0
4	R	TYPE[0]	1
3	R	ID[3]	Note 1
2	R	ID[2]	Note 1
1	R	ID[1]	Note 1
0	R	ID[0]	Note 1

In addition, writing to this register simultaneously loads all the aggregate and per-PHY performance meter registers located at addresses 0x011, 0x012, 0x013, 0x022, 0x023, 0x032, 0x033, 0x042, 0x043, 0x400-0x5FC, 0x600-0x7F9.

ID[3:0]:

The ID bits can be read to provide a binary number indicating the S/UNI-ATLAS feature version.

NOTE 1:
Rev A ID[3:0] = 0000
Rev B ID[3:0] = 0001
Rev C ID[3:0] = 0010

TYPE[2:0]:

The TYPE bits can be read to distinguish the S/UNI-ATLAS from the other members of the S/UNI-ATLAS family of devices.

RESET:

The RESET bit allows the S/UNI-ATLAS to be reset under software control. If the RESET bit is a logic one, the entire S/UNI-ATLAS is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-ATLAS out of reset. Holding the S/UNI-ATLAS in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise, the effect of the software reset is equivalent to that of the hardware reset.

Register 0x001: S/UNI-ATLAS Master Configuration

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6	R/W	BUSYPOL	0
5	R/W	DREQINV	0
4	R/W	SEL1SEC	0
3	R/W	CLKRATE[1]	0
2	R/W	CLKRATE[0]	0
1	R/W	ESTANDBY	1
0	R/W	ISTANDBY	1

ISTANDBY:

The ISTANDBY bit disables Ingress Cell Processing to avoid passing corrupted cells while initializing the S/UNI-ATLAS. When ISTANDBY is a logic 1, the S/UNI-ATLAS makes all bus cycles available for external SRAM access (i.e. access to the Ingress VC Table is given highest priority, and no other processing will interrupt the SRAM bus).

If the ISTANDBY bit is set while cell processing is in progress, the processing of cells currently in the pipeline is completed, but no more cells are transferred into the ingress of the S/UNI-ATLAS.

ESTANDBY:

The ESTANDBY bit disables Egress Cell Processing to avoid passing corrupted cells while initializing the S/UNI-ATLAS. When ESTANDBY is a logic 1, the S/UNI-ATLAS makes all bus cycles available for external SRAM access (i.e. access to the Egress VC Table is given highest priority, and no other processing will interrupt the SRAM bus).

If the ESTANDBY bit is set while cell processing is in progress, the processing of cells currently in the pipeline is completed, but no more cells are transferred into the egress of the S/UNI-ATLAS.

CLKRATE[1:0]:

The CLKRATE[1:0] bits selects between a 25, 50 and 52 MHz clock frequency to allow the generation of an internal 0.5 second clock. The encoding of CLKRATE[1:0] is as follows:

CLKRATE[1:0]	Assumed ISYSCLK frequency
00	25 MHz
01	50 MHz
10	52 MHz
11	Reserved

The CLKRATE[1:0] bits are used to generated an internal 0.5 second clock which is used by the background processes to generate Fault Management Cell and alarms.

SEL1SEC:

The SEL1SEC bit determines the trigger for processing that relies on background processing, such as AIS, RDI and CC cell generation. If the SEL1SEC is a logic 0, the 0.5 second clock is derived from ISYSCLK, which is assumed to be 25, 50 or 52 MHz (determined by the CLKRATE[1:0] setting). If SEL1SEC is a logic 1, processing is initiated on the rising edge of the HALFSECCLK input.

DREQINV:

The DREQINV bit inverts the polarity of the IDREQ and EDREQ primary outputs. If DREQINV is logic 0, the IDREQ and EDREQ outputs are active high. If DREQINV is logic 1, the IDREQ and EDREQ outputs are active low.

BUSYPOL:

The BUSYPOL bit sets the polarity of the BUSYB primary output. If BUSYPOL is logic 0, the BUSYB primary output is active low. If BUSYPOL is logic 1, the BUSYB output is active high.

Register 0x002: Master Interrupt Status #1

Bit	Type	Function	Default
15	R	REG6I	X
14	R	REG5I	X
13	R	REG4I	X
12	R	REG3I	X
11	R	I_XFERI	X
10	R	I_XPOLI	X
9	R	I_POLI	X
8	R	I_END_RDII	X
7	R	I_SEG_RDII	X
6	R	I_END_AISI	X
5	R	I_SEG_AISI	X
4	R	I_END_CCI	X
3	R	I_SEG_CCI	X
2	R	I_OAMERRI	X
1	R	I_PTIVCII	X
0	R	I_INVALI	X

I_INVALI:

The I_INVALI bit indicates that a cell with an unprovisioned VPI/VCI combination or invalid routing bits has been received at the Ingress of the S/UNI-ATLAS. When logic 1, the I_INVALI bit indicates one or more Ingress VC Table searches have not resulted in a match. This bit is cleared when this register is read.

I_PTIVCII

The I_PTIVCII bit indicates a cell with an invalid PTI or VCI field has been received at the Ingress of the S/UNI-ATLAS. When logic 1, the I_PTIVCII bit indicates one or more F5 cells have the PTI field with PTI='111', F4 cells with an invalid VCI field (VCI 7 through 15 and 0) or at least one VP Resource Management cell has been received with PTI not equal to '110'. Also for NNI connections this bit will be set if the PTI field for F4 or F5 OAM cells is not equal to '000' or '010'. This bit is cleared when this register is read.

I_OAMERRI

The I_OAMERRI bit indicates one or more OAM cell with an incorrect OAM Type, Function Type or Error Detection Code field (CRC-10) has been received at the Ingress of the S/UNI-ATLAS. When logic 1, the I_OAMERRI bit indicates one or more errored OAM cells have been received. This bit may also indicate one or more Resource Management cell with an incorrect CRC-10 has been received. This bit is cleared when this register is read.

I_SEG_CCI

The I_Seg_CCI bit indicates that a Segment Continuity Check alarm (in the Ingress VC Table) has changed state. When logic 1, the I_SEG_CCI bit indicates the Segment_CC_Alarm bit in the Ingress VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

I_END_CCI:

The I_END_CCI bit indicates that an End-to-End Continuity Check alarm (in the Ingress VC Table) has changed state. When logic 1, the I_END_CCI bit indicates the End_to_End_CC_Alarm bit in the Ingress VC Table has changed state for one or more virtual connection. This bit is cleared when this register is read.

I_SEG_AISI:

The I_SEG_AISI bit indicates that a Segment AIS alarm (in the Ingress VC Table) has changed state. When logic 1, the I_SEG_AISI bit indicates the Segment AIS Alarm bit in the Ingress VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

I_END_AISI:

The I_END_AISI bit indicates that an End-to-End AIS alarm (in the Ingress VC Table) has changed state. When logic 1, the I_END_AISI bit indicates the End-to-End AIS Alarm bit in the Ingress VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

I_SEG_RDII:

The I_SEG_RDII bit indicates that a Segment RDI alarm (in the Ingress VC Table) has changed state. When logic 1, the I_SEG_RDII bit indicates the Segment RDI Alarm bit in the Ingress VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

I_END_RDII:

The I_END_RDII bit indicates that an End-to-End RDI alarm (in the Ingress VC Table) has changed state. When logic 1, the I_END_RDII bit indicates the End-to-End RDI Alarm bit in the Ingress VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

I_POLI:

The I_POLI bit indicates a non-compliant cell has been received at the Ingress of the S/UNI-ATLAS. When logic 1, the I_POLI bit indicates one or more cells have violated the traffic contract since the last read of this register. This bit is cleared when this register is read.

I_XPOLI:

The excessive policing indication (I_XPOLI) bit becomes a logic 1 upon receipt of a cell belonging to a connection that has at least one non-compliant cell count that has just become greater than 32768 (i.e. the MSB of one or more non-compliant cell counts has just been set). This bit is cleared when this register is read.

I_XFERI:

The I_XFERI bit indicates that the Ingress per-PHY cell counters have been transferred to holding registers and the contents should be read. When logic 1, the I_XFERI bit indicates that either the I_XFER or OVR bit in the Counter Status register has been asserted. The I_XFERI bit is cleared when this register is read.

REG3I:

The REG3I bit indicates that at least one bit in register 0x003, S/UNI-ATLAS Master Interrupt Status #2, is currently asserted.

REG4I:

The REG4I bit indicates that at least one bit in register 0x004, S/UNI-ATLAS Master Interrupt Status #3, is currently asserted.

REG5I:

The REG5I bit indicates that at least one bit in register 0x005, S/UNI-ATLAS Master Interrupt Status #4, is currently asserted.

REG6I:

The REG6I bit indicates that at least one bit in register 0x006, S/UNI-ATLAS Master Interrupt Status #5, is currently asserted.

Register 0x003: Master Interrupt Status #2

Bit	Type	Function	Default
15	R	REG6I	X
14	R	REG5I	X
13	R	REG4I	X
12	R	I_XCOSI	X
11	R	I_COSFULLI	X
10	R	I_PHYXPOLI	X
9	R	I_PHYPOLI	X
8	R	I_BCIFFULLI	X
7	R	I_SRCHERRI	X
6	R	I_PCELLI	X
5	R	I_RPRTYI	X
4	R	I_RSOCI	X
3	R	I_INSRDYI	X
2	R	I_UPCAI	X
1	R	I_UPFOVRI	X
0	R	I_FULLI	X

I_FULLI:

The I_FULLI bit becomes a logic 1 when the Ingress Output Cell Interface has been filled to its 4 cell capacity. This may indicate failure or congestion in the entity connection to the Ingress Output Cell Interface. This bit is cleared when this register is read.

I_UPFOVRI:

The I_UPFOVRI bit is set high when an Ingress Microprocessor Cell Interface extract FIFO overflow occurs. This bit is cleared when this register is read.

I_UPCAI:

The I_UPCAI bit indicates that a cell has been written into the Ingress Microprocessor Cell extract FIFO, and is ready for extraction by an external processor. When logic 1, the I_UPCAI bit indicates that the EXTCA bit in the Ingress Microprocessor Extract FIFO Control and Status register has been asserted. The I_UPCAI bit is cleared when this register is read.

I_INSRDYI:

The I_INSRDYI bit indicates the Ingress Microprocessor Cell Interface insert FIFO is empty and is ready for another cell. This bit is cleared when this register is read.

I_RSOCI:

The I_RSOCI bit is set to logic 1 when the RSOC input to the Ingress Input Cell Interface is sampled high during any position other than the first word of the selected data structure. The write address counter is reset to the first word of the data structure when RSOC is sampled high. This bit is reset immediately after a read to this register.

I_RPRTYI:

The I_RPRTYI bit indicates a parity error has been detected on the RDAT[15:0] data bus. When logic 1, the I_RPRTYI bit indicates a parity error over the RDAT[15:0] data bus. This bit is cleared when this register is read.

I_PCELLI:

The I_PCELLI bit indicates that a physical layer idle cell has been received at the Ingress of the S/UNI-ATLAS. When logic 1, the I_PCELLI bit indicates one or more cells with an all zero VPI and VCI value and a CLP=1 have been received at the Ingress Input Cell Interface. This bit is cleared when this register is read.

I_SRCHERRI:

The search error bit (I_SRCHERRI) indicates that a VPI/VCI search in the Ingress VC Table has failed due to an improperly constructed secondary search table. This bit is set if the secondary search key takes more than 41 cycles. If the I_BADVCtoUP register bit is a logic 1, the cell associated with the failed search is routed to the Ingress Microprocessor Cell Interface Extract FIFO. This bit is cleared when this register is read.

I_BCIFFULLI:

This Ingress Backward OAM Cell Interface Full bit (I_BCIFOVRI) indicates that the Ingress Backward OAM Cell Interface is full. When logic 1, the I_BCIFFULLI bit indicates that the Ingress Backward OAM Cell Interface FIFO is full, and cannot accept any more cells generated by the Egress Cell Processor. This affects how often RDI and Backward Reporting PM cells can be generated and inserted into the Ingress cell flow. If the I_BCIFFULLI interrupt persists, the rate at which cells are allowed from the Ingress BCIF may have to be increased, so that RDI and Backward Reporting PM cells can be generated at the appropriate intervals. This bit is cleared when this register is read.

I_PHYPOLI:

The Ingress PHY Policing Interrupt bit (I_PHYPOLI) indicates that one or more cells have violated one or more per-PHY policing contracts. When logic 1, the I_PHYPOLI bit indicates one or more cells have violated one or more of the 32 PHY policing instances. This bit is cleared when this register is read.

I_PHYXPOLI:

The PHY excessive policing indication (I_PHYXPOLI) bit becomes a logic 1 upon receipt of a cell belonging to a PHY device that has at least one of the per-PHY non-compliant cell counts in excess of 32768 (i.e. the MSB of one or more per-PHY non-compliant cell counts is set). This bit is cleared when this register is read.

I_COSFULLI:

The Ingress Change of State FIFO Full Interrupt bit (I_COSFULLI) indicates that the Ingress Change of State FIFO is full. When logic 1, the I_COSFULLI indicates that the Ingress Change of State FIFO is full, and no more change of state notifications can be written into the FIFO. This suspends a background process until FIFO space becomes free. It is the responsibility of the management software to ensure this FIFO is read often enough to ensure the notification of changes of state are compliant with Bellcore and ITU standards. This bit is cleared when this register is read.

I_XCOSI:

The Ingress Excessive Change of State FIFO Interrupt bit (I_XCOSI) indicates that the Ingress Change of State FIFO is half-full. When logic 1, the I_XCOSI indicates that the Ingress Change of State FIFO is half-full with changes of connection state information. This indicates that the Change of State FIFO should be read quickly to avoid the Change of State FIFO from becoming full. It is the responsibility of the management software to ensure the Change of State FIFO is read often enough to ensure the notification of changes of state are compliant with Bellcore and ITU standards. This bit is cleared when this register is read.

REG4I:

The REG4I bit indicates that at least one bit in Register 0x004, S/UNI-ATLAS Master Interrupt Status #3 is currently asserted.

REG5I:

The REG5I bit indicates that at least one bit in Register 0x005, S/UNI-ATLAS Master Interrupt Status #4 is currently asserted.

REG6I:

The REG6I bit indicates that at least one bit in Register 0x006, S/UNI-ATLAS Master Interrupt Status #5 is currently asserted.

Register 0x004: Master Interrupt Status #3

Bit	Type	Function	Default
15	R	REG6I	X
14	R	REG5I	X
13		Unused	X
12		Unused	X
11	R	E_SPRTYI[3]	X
10	R	E_SPRTYI[2]	X
9	R	E_SPRTYI[1]	X
8	R	E_SPRTYI[0]	X
7	R	I_SPRTYI[7]	X
6	R	I_SPRTYI[6]	X
5	R	I_SPRTYI[5]	X
4	R	I_SPRTYI[4]	X
3	R	I_SPRTYI[3]	X
2	R	I_SPRTYI[2]	X
1	R	I_SPRTYI[1]	X
0	R	I_SPRTYI[0]	X

I_SPRTYI[7:0]:

The I_SPRTYI[7:0] bits indicate a parity error has been detected on the Ingress VC Table, ISD[63:0], data bus. When logic 1, the I_SPRTYI[7:0] bits indicate the following:

I_SPRTYI[7]: Parity error over inputs ISD[63:56]
I_SPRTYI[6]: Parity error over inputs ISD[55:48]
I_SPRTYI[5]: Parity error over inputs ISD[47:40]
I_SPRTYI[4]: Parity error over inputs ISD[39:32]
I_SPRTYI[3]: Parity error over inputs ISD[31:24]
I_SPRTYI[2]: Parity error over inputs ISD[23:16]
I_SPRTYI[1]: Parity error over inputs ISD[15:8]
I_SPRTYI[0]: Parity error over inputs ISD[7:0]

All bits are cleared when this register is read.

E_SPRTYI[3:0]:

The E_SPRTYI[3:0] bits indicate a parity error has been detected on the Egress VC Table, ESD[31:0], data bus. When logic 1, the E_SPRTYI[3:0] bits indicate the following:

E_SPRTYI[3]: Parity error over inputs ESD[31:24]
E_SPRTYI[2]: Parity error over inputs ESD[23:16]
E_SPRTYI[1]: Parity error over inputs ESD[15:8]
E_SPRTYI[0]: Parity error over inputs ESD[7:0].

All bits are cleared when this register is read.

REG5I:

The REG5I bit indicates that at least one bit in Register 0x005, S/UNI-ATLAS Master Interrupt Status #4, is currently asserted.

REG6I:

The REG6I bit indicates that at least one bit in Register 0x006, S/UNI-ATLAS Master Interrupt Status #5, is currently asserted.

Register 0x005: Master Interrupt Status #4

Bit	Type	Function	Default
15	R	REG6I	X
14	R	E_PCELLI	X
13	R	E_IOVRI	X
12	R	E_INSRDYI	X
11	R	E_UPCAI	X
10	R	E_UPFOVRI	X
9	R	E_FULLI	X
8	R	E_End_RDII	X
7	R	E_Seg_RDII	X
6	R	E_End_AISI	X
5	R	E_Seg_AISI	X
4	R	E_END_CCI	X
3	R	E_SEG_CCI	X
2	R	E_OAMERRI	X
1	R	E_PTIVCII	X
0	R	E_XFERI	x

E_XFERI:

The E_XFERI bit indicates that the Egress per-PHY cell counters have been transferred to holding registers and the contents should be read. When logic 1, the E_XFERI bit indicates that either the E_XFER or OVR bit in the Counter Status register has been asserted. The E_XFERI bit is cleared when this register is read.

E_PTIVCII:

The E_PTIVCII bit indicates a cell with an invalid PTI or VCI field has been received at the Egress Cell Processor. When logic 1, the E_PTIVCII bit indicates one or more F5 cells with PTI='111' or one or more F4 cells with an invalid VCI field (0, 7 through 15), or one or more F4 RM cells with PTI not equal to '110' have been received (conditioned by VPRMSEL bit in Register 0x280). An F4 OAM cell is received on an NNI connection and the PTI field does not equal '000' or '010'. This bit is cleared when this register is read.

E_OAMERRI:

The E_OAMERRI bit indicates one or more OAM cell with an incorrect OAM Type, Function Type or Error Detection Code field (CRC-10) has been received at the Egress of the S/UNI-ATLAS. When logic 1, the E_OAMERRI bit indicates one or more errored OAM cells have been received. This bit may also indicate one or more Resource Management cell with an incorrect CRC-10 has been received. This bit is cleared when this register is read.

E_SEG_CCI:

The E_Seg_CCI bit indicates that a Segment Continuity Check alarm (in the Egress VC Table) has changed state. When logic 1, the E_SEG_CCI bit indicates the Segment_CC_Alarm bit in the Egress VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

E_END_CCI:

The E_END_CCI bit indicates that an End-to-End Continuity Check alarm (in the Egress VC Table) has changed state. When logic 1, the E_END_CCI bit indicates the End_to_End_CC_Alarm bit in the Egress VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

E_SEG_AISI:

The E_SEG_AISI bit indicates that a Segment AIS alarm (in the Egress VC Table) has changed state. When logic 1, the E_SEG_AISI bit indicates the Segment AIS Alarm bit in the Egress VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

E_END_AISI:

The E_END_AISI bit indicates that an End-to-End AIS alarm (in the Egress VC Table) has changed state. When logic 1, the E_END_AISI bit indicates the End-to-End AIS Alarm bit in the Egress VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

E_SEG_RDII:

The E_SEG_RDII bit indicates that a Segment RDI alarm (in the Egress VC Table) has changed state. When logic 1, the E_SEG_RDII bit indicates the Segment RDI Alarm bit in the Egress VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

E_END_RDII:

The I_END_RDII bit indicates that an End-to-End RDI alarm (in the Egress VC Table) has changed state. When logic 1, the I_END_RDII bit indicates the End-to-End RDI Alarm bit in the Egress VC Table has changed state for one or more virtual connections. This bit is cleared when this register is read.

E_FULLI:

The E_FULLI bit becomes a logic 1 when the Egress Output Cell Interface has been filled to its 4 cell capacity on any PHY. This may indicate failure or congestion in the entity connection to the Egress Output Cell Interface. This bit is cleared when this register is read.

E_UPFOVRI:

The E_UPFOVRI bit is set high when an Egress Microprocessor Cell Interface extract FIFO overflow occurs. This bit is reset after a read to this register.

E_UPCAI:

The E_UPCAI bit that a cell has been written into the Egress Microprocessor Cell extract FIFO, and is ready for extraction by an external processor. When logic 1, the E_UPCAI bit indicates that the EXTCA bit in the Egress Microprocessor Extract FIFO Control and Status register has been asserted. The E_UPCAI bit is cleared when this register is read.

E_INSRDYI:

The E_INSRDYI bit indicates the Egress Microprocessor Cell Interface insert FIFO is empty and is ready for another cell. This bit is cleared when this register is read.

E_IOVRI:

The E_IOVRI bit indicates that an overflow of the Egress Input Cell Interface occurred. When logic 1, the E_IOVRI indicates a cell was written into the Egress Input Cell Interface while the Cell Available for that PHY was deasserted. That cell will be discarded. This bit is reset when this register is read.

E_PCELLI:

The E_PCELLI bit indicates that a physical layer idle cell has been received at the Egress Input Cell Interface. When logic 1, the E_PCELLI bit indicates one or more cells with an all zero VPI and VCI value and a CLP=1 have been received at the Egress Input Cell Interface. This bit is cleared when this register is read.

REG6I:

The REG6I bit indicates that at least one bit in Register 0x006, S/UNI-ATLAS Master Interrupt Status #5, is currently asserted.

Register 0x006: Master Interrupt Status #5

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6	R	E_SEARCHEI	X
5	R	E_XCOSI	X
4	R	E_COSFULLI	X
3	R	E_BCIFFULLI	X
2	R	E_IWRENBI	X
1	R	E_IPRTYI	X
0	R	E_ISOCI	X

E_ISOCI:

The E_ISOCI bit is set to logic 1 when the ISOC input to the Egress Input Cell Interface is sampled high during any position other than the first word of the selected data structure. The write address counter is reset to the first word of the data structure when ISOC is sampled high. This bit is reset immediately after a read to this register.

E_PRTYI:

The E_IPRTYI bit indicates a parity error has been detected on the IDAT[15:0] data bus. When logic 1, the E_IPRTYI bit indicates a parity error over the IDAT[15:0] data bus. This bit is cleared when this register is read.

E_IWRENBI :

The E_IWRENBI bit indicates more than one of the E_IWRENB[4:1] inputs were asserted simultaneously, or an attempt to write a new cell with a different PHYID occurred before completion of the current cell write. This bit is cleared when this register is read.

E_BCIFFULLI:

The Egress Backward OAM Cell Interface Full bit (E_BCIFFULLI indicates that the Egress Backward OAM Cell Interface is full. When logic 1, the E_BCIFFULLI bit indicates that the Backward OAM Cell Interface FIFO is full, and cannot accept any more cells generated Ingress Cell Processor. This affects how often RDI and Backward Reporting PM cells can be generated and inserted into the Egress cell flow. If the E_BCIFFULLI interrupt persists, the rate at which cells are allowed from the Egress BCIF may have to be increased, so that RDI and Backward Reporting PM cells can be generated at the appropriate intervals. This bit is cleared when this register is read.

E_COSFULLI:

The Egress Change of State FIFO Full Interrupt bit (E_COSFULLI) indicates that the Egress Change of State FIFO is full. When logic 1, the E_COSFULLI indicates that the Egress Change of State FIFO is full, and no more change of state notifications can be written into the FIFO. This suspends a background process until FIFO space becomes free. It is the responsibility of the management software to ensure this FIFO is read often enough to ensure the notification of changes of state are compliant with Bellcore and ITU standards. This bit is cleared when this register is read.

E_XCOSI:

The Egress Excessive Change of State FIFO Interrupt bit (E_XCOSI) indicates that the Egress Change of State FIFO is half-full. When logic 1, the E_XCOSI indicates that the Egress Change of State FIFO is half-full with changes of connection state information. This indicates that the Change of State FIFO should be read quickly to avoid the Change of State FIFO from becoming full. It is the responsibility of the management software to ensure the Change of State FIFO is read often enough to ensure the notification of changes of state are compliant with Bellcore and ITU standards. This bit is cleared when this register is read.

E_SEARCHEI

The Egress VC Table Search Error Interrupt (E_SEARCHEI) indicates that an error occurred in checking the Egress VC Table lookup address odd parity bit. If a parity error is detected, interrupt is asserted. If the BADVCtoUP register bit is a logic 1, the cell associated with the failed search is routed to the Egress Microprocessor Cell Interface Extract FIFO. This bit is cleared when this register is read.

Register 0x007: Master Interrupt Enable #1

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11	R/W	I_XFERE	0
10	R/W	I_XPOLE	0
9	R/W	I_POLE	0
8	R/W	I_END_RDIE	0
7	R/W	I_SEG_RDIE	0
6	R/W	I_END_AISE	0
5	R/W	I_SEG_AISE	0
4	R/W	I_END_CCE	0
3	R/W	I_SEG_CCE	0
2	R/W	I_OAMERRE	0
1	R/W	I_PTIVCIE	0
0	R/W	I_INVALE	0

The above enable bits control the corresponding interrupt status bits in the S/UNI-ATLAS Master Interrupt Status #1 register. When an enable bit is set to logic 1, the INTB output is asserted low when the corresponding interrupt status bit is a logic 1.

Register 0x008: Master Interrupt Enable #2

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12	R/W	I_XCOSE	0
11	R/W	I_COSFULLE	0
10	R/W	I_PHYXPOLE	0
9	R/W	I_PHYPOLE	0
8	R/W	I_BCIFFULLE	0
7	R/W	I_SRCHERRE	0
6	R/W	I_PCELLE	0
5	R/W	I_RPRTYE	0
4	R/W	I_RSOCE	0
3	R/W	I_INSRDYE	0
2	R/W	I_UPCAE	0
1	R/W	I_UPFOVRE	0
0	R/W	I_FULLE	0

The above enable bits control the corresponding interrupt status bits in the S/UNI-ATLAS Master Interrupt Status #2 register. When an enable bit is set to logic 1, the INTB output is asserted low when the corresponding interrupt status bit is a logic 1.

Register 0x009: Master Interrupt Enable #3

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11	R/W	E_SPRYTE[3]	0
10	R/W	E_SPRYTE[2]	0
9	R/W	E_SPRYTE[1]	0
8	R/W	E_SPRYTE[0]	0
7	R/W	I_SPRYTE[7]	0
6	R/W	I_SPRYTE[6]	0
5	R/W	I_SPRYTE[5]	0
4	R/W	I_SPRYTE[4]	0
3	R/W	I_SPRYTE[3]	0
2	R/W	I_SPRYTE[2]	0
1	R/W	I_SPRYTE[1]	0
0	R/W	I_SPRYTE[0]	0

The above enable bits control the corresponding interrupt status bits in the S/UNI-ATLAS Master Interrupt Status #3 register. When an enable bit is set to logic 1, the INTB output is asserted low when the corresponding interrupt status bit is a logic 1.

Register 0x00A: Master Interrupt Enable #4

Bit	Type	Function	Default
15		Unused	X
14	R/W	E_PCELLE	0
13	R/W	E_IOVRE	0
12	R/W	E_INSRDYE	0
11	R/W	E_UPCAE	0
10	R/W	E_UPFOVRE	0
9	R/W	E_FULLE	0
8	R/W	E_END_RDIE	0
7	R/W	E_SEG_RDIE	0
6	R/W	E_END_AISE	0
5	R/W	E_SEG_AISE	0
4	R/W	E_END_CCE	0
3	R/W	E_SEG_CCE	0
2	R/W	E_OAMERRE	0
1	R/W	E_PTIVCIE	0
0	R/W	E_XFERE	0

The above enable bits control the corresponding interrupt status bits in the S/UNI-ATLAS Master Interrupt #4 register. When an enable bit is set to logic 1, the INTB output is asserted low when the corresponding interrupt status bit is a logic 1.

Register 0x00B: Master Interrupt Enable #5

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6	R/W	E_SEARCHE	0
5	R/W	E_XCOSE	0
4	R/W	E_COSFULLE	0
3	R/W	E_BCIFFULLE	0
2	R/W	E_IWRENBE	0
1	R/W	E_IPRTYE	0
0	R/W	E_ISOCE	0

The above enable bits control the corresponding interrupt status bits in the S/UNI-ATLAS Master Interrupt #5 register. When an enable bit is set to logic 1, the INTB output is asserted low when the corresponding interrupt status bit is a logic 1.

Register 0x00C: Master Clock Monitor

Bit	Type	Function	Default
15	R	DLLRUN	X
14	R/W	RSTDLL	0
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5	R	TFCLKA	X
4	R	IFCLKA	X
3	R	ESYSCKLA	X
2	R	OFCLKA	X
1	R	RFCLKA	X
0	R	ISYSCLKA	X

This register provides activity monitoring on S/UNI-ATLAS clocks. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

ISYSCLKA:

The ISYSCLK active (ISYSCKLA) bit monitors for low to high transitions on the ISYSCLK input. ISYSCLKA is set high on a rising edge of ISYSCLK, and is set low when this register is read.

RFCLKA:

The RFCLK active (RFCLKA) bit monitors for low to high transitions on the RFCLK input. RFCLKA is set high on a rising edge of RFCLK, and is set low when this register is read.

OFCLKA:

The OFCLK active (OFCLKA) bit monitors for low to high transitions on the OFCLK input. OFCLKA is set high on a rising edge of OFCLK, and is set low when this register is read.

ESYSCLKA:

The ESYSCLK active (ESYSCLKA) bit monitors for low to high transitions on the ESYSCLK input. ESYSCLKA is set high on a rising edge of ESYSCLK, and is set low when this register is read.

IFCLKA:

The IFCLK active (IFCLKA) bit monitors for low to high transitions on the IFCLK input. IFCLKA is set high on a rising edge of IFCLK, and is set low when this register is read.

TFCLKA:

The TFCLK active (TFCLKA) bit monitors for low to high transitions on the TFCLK input. TFCLKA is set high on a rising edge of TFCLK, and is set low when this register is read.

RSTDLL:

The Reset Delay Locked Loop register bit (RSTDLL) controls the resetting of the ATLAS DLL components. If this bit is logic 1, the RFCLK, ISYSCLK, OFCLK, IFCLK, ESYSCLK and TFCLK DLL components will be reset.

DLLRUN:

The Delay Locked Loop run register bit (DLLRUN). When logic 1, this bit indicates that all DLL components have locked to their input clocks.

Register 0x010: Ingress Input Cell Interface Configuration #1

Bit	Type	Function	Default
15	R/w	RHECUDF	1
14	R/W	RCAINV	0
13	R/W	RCELLPOST[3]	0
12	R/W	RCELLPOST[2]	0
11	R/W	RCELLPOST[1]	0
10	R/W	RCELLPOST[0]	0
9	R/W	RCELLLEN[3]	0
8	R/W	RCELLLEN[2]	0
7	R/W	RCELLLEN[1]	0
6	R/W	RCELLLEN[0]	0
5	R/W	Reserved	0
4	R/W	RPTYP	0
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	RCALEVEL0	1
0	R/W	RFIFORST	0

RFIFORST:

The RFIFORST bit is used to reset the 4-cell FIFO. When RFIFORST is set to logic zero, the FIFO operates normally. When RFIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to RFIFORST.

N.B. It is recommended that, whenever any other bit in this register or the Ingress Input Cell Interface Configuration 2 register is changed, RFIFORST be set to logic one before the change and set to logic zero after.

RCALEVEL0:

The RCALEVEL0 bit determines how the RCA[4:1] signals are interpreted.

If RCALEVEL0 is a logic 1, the ATLAS Ingress Input Cell Interface checks for close compliance to the SCI-PHY cell transfer handshake. If the RCA signal for the PHY whose cell is currently being transferred is deasserted before the end of the cell, the cell will be discarded.

If RCALEVEL0 is a logic 0, the RCA signal may be deasserted early without loss of the cell. Once a cell transfer is initiated, the entire cell will be read contiguously regardless of the state of the RCA signal

RPTYP:

The RPTYP bit selects even or odd parity for the input signal. When set to logic 1, RPRTY is the even parity bit for RDAT[15:0]. When set to logic 0, RPRTY is the odd parity bit for RDAT[15:0].

RCELLLEN[3:0]:

The RCELLLEN[3:0] bits determine the number of words appended to the input cell. When the RBUS8 register bit is a logic 1, the binary RCELLLEN[3:0] value is the maximum number of bytes appended to the basic 53 byte ATM cell. The maximum cell length is 63 bytes; a RCELLLEN[3:0] greater than 10 decimal results in 10 appended bytes.

When RBUS8 is a logic 0, the binary RCELLLEN[3:0] value is the number of words appended to the basic 27 word ATM cell. The maximum cell length is 32 words (i.e. 5 appended words); therefore, RCELLLEN[3:0] should not be set greater than 5 decimal when RBUS8 is logic 0.

RCELLPOST[3:0]:

The RCELLPOST[3:0] bits determine the number of words in the input cell postpend. The numerical difference between RCELLLEN[3:0] and RCELLPOST[3:0] represents the number of words in the prepend. It is inappropriate that RCELLPOST[3:0] exceed RCELLLEN[3:0].

When RBUS8 is a logic 1, the binary RCELLPOST[3:0] value is the number of bytes postpended to the basic 53 byte ATM cell.

When RBUS8 is a logic 0, the binary RCELLPOST[3:0] value is the number of words postpended to the basic 27 word ATM cell.

RCAINV:

The RCAINV bit selects the active polarity of the Ingress RCA[4:1] cell available signals. The default configuration selects RCA[4:1] to be active high. When RCAINV is set to logic 1 the RCA[4:1] signals become active low. If the state of the RCAINV bit has been changed, the Ingress Input Cell Interface must be reset via the FIFORST.

RHECUDF:

The RHECUDF bit determines whether or not the HEC/UDF octets are included in cells transferred over the Ingress Input Cell Interface. When set to logic 1 (default), the HEC and UDF octets are included. When set to logic 0, these octets are omitted. I.e. if RBUS8 is logic 0, the third word of the 27-word ATM cell is omitted and a 26-word cell (plus appended words) is transferred. If RBUS8 is logic 1, the fifth octet of the 53-octet ATM cell is omitted and a 52-octet cell (plus appended octets) is transferred.

Register 0x011: Ingress Physical Layer Cell Counter

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7	R	RPICELL[7]	X
6	R	RPICELL[6]	X
5	R	RPICELL[5]	X
4	R	RPICELL[4]	X
3	R	RPICELL[3]	X
2	R	RPICELL[2]	X
1	R	RPICELL[1]	X
0	R	RPICELL[0]	X

This register provides a count of the Physical Layer idle cells erroneously passed from the PHY layer.

RPICELL[7:0]:

The RPICELL[7:0] bits indicate the number of Physical Layer idle cells presented to the Ingress Input Cell Interface during the last accumulation interval. A Physical Layer cell is defined by a VPI value of zero, a VCI value of zero, a PTI of zero and a CLP value of one. Physical Layer cells should not be present at the ATM Layer.

A write to either address 0x011, 0x012 or 0x013 loads the register with the current counter value and resets the internal 8 bit counter to 1 or 0. The counter reset value is dependent on whether there was a count event during the transfer of the count to the Physical Layer Cell Counter register. The contents of this register are valid within 4 IFCLK cycles of a transfer being triggered by a write to address 0x011, 0x012 or 0x013. If this register is not polled regularly, the count value will saturate at 255.

This counter can also be reset by writing to the Master Reset and Identity/Load Performance Register 0x000. After a write to register 0x000, the Physical Layer Cell Counter register is loaded with the current count value and the counter is reset as described above.

Register 0x012: Ingress Input Cell Counter (LSB)

Bit	Type	Function	Default
15	R	RCELL[15]	X
14	R	RCELL[14]	X
13	R	RCELL[13]	X
12	R	RCELL[12]	X
11	R	RCELL[11]	X
10	R	RCELL[10]	X
9	R	RCELL[9]	X
8	R	RCELL[8]	X
7	R	RCELL[7]	X
6	R	RCELL[6]	X
5	R	RCELL[5]	X
4	R	RCELL[4]	X
3	R	RCELL[3]	X
2	R	RCELL[2]	X
1	R	RCELL[1]	X
0	R	RCELL[0]	X

Register 0x013: Ingress Input Cell Counter (MSB)

Bit	Type	Function	Default
15	R	RCELL[31]	X
14	R	RCELL[30]	X
13	R	RCELL[29]	X
12	R	RCELL[28]	X
11	R	RCELL[27]	X
10	R	RCELL[26]	X
9	R	RCELL[25]	X
8	R	RCELL[24]	X
7	R	RCELL[23]	X
6	R	RCELL[22]	X
5	R	RCELL[21]	X
4	R	RCELL[20]	X
3	R	RCELL[19]	X
2	R	RCELL[18]	X
1	R	RCELL[17]	X
0	R	RCELL[16]	X

RCELL[31:0]:

The RCELL[31:0] bits indicate the number of cells read from the Ingress Input Cell Interface during the last accumulation interval. The count includes all user information and OAM cells, regardless of whether or not the VPI/VCI value is provisioned. The count does not include Physical Layer idle cells (VPI=0, VCI=0, CLP=1) and unassigned cells (VPI=0, VCI=0, CLP=0).

A write to either address 0x011, 0x012 or 0x013 loads the registers with the current counter value and resets the internal 32 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Read Cell Counter registers. The counter should be polled at least every 10 seconds to avoid the counter from saturating at 0xFFFFFFFF. The contents of these registers are valid within 4 RFCLK cycles of a transfer being triggered by a write to address 0x011, 0x012 or 0x013.

This counter can also be reset by writing to the Master Reset and Identity/Load Performance Register 0x000. After a write to register 0x000, the Physical Layer Cell Counter register is loaded with the current count value and the counter is reset as described above.

Register 0x014: Ingress Input Cell Interface Configuration #2

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9	R/W	RBUS8	0
8	R/W	Reserved	0
7		Unused	X
6	R/W	Reserved	0
5	R/W	RNNI	1
4	R/W	RPHYDEV[4]	0
3	R/W	RPHYDEV[3]	0
2	R/W	RPHYDEV[2]	0
1	R/W	RPHYDEV[1]	0
0	R/W	RPHYDEV[0]	0

RPHYDEV[4:0]:

The RPHYDEV[4:0] bits are used when the ATLAS is in Polled mode (RPOLL=1). The ATLAS polls PHY devices using the RADDR[4:0] signals. The RPHYDEV[4:0] bits indicate the number of devices to be polled as follows:

RPHYDEV[4:0]	Meaning
00000	Poll all 32 PHY devices
00001	Poll PHY#1 thru PHY#2
00010	Poll PHY#1 thru PHY#3
:	
11110	Poll PHY#1 thru PHY#31
11111	Poll all 32 PHY devices

RNNI:

The RNNI bit selects whether the first four bits of the ATM cell header are used when determining whether a cell should be discarded because it is unassigned or a physical layer idle cell. When set to logic 1 (default), the NNI format is used and first four bits of the ATM cell header must be zeros for a cell to be identified as an unassigned or physical layer cell. When set to logic 0, the UNI format is used and first four bits of the ATM cell header are ignored.

If a mixture of UNI and NNI cells pass through the Input Cell Interface, this register bit should be set to a logic 1. Any Physical Layer UNI cells which contain non-zero GFC fields shall be passed through the input FIFO and subsequently rejected by the Ingress VC Search Algorithm. This results in an increment of the Invalid Cell Count rather than the Physical Layer Cell count.

RBUS8:

The RBUS8 register bit controls the bus width selection of the Ingress Input Cell Interface. When RBUS8 is logic 1, the 10-bit interface consisting of a start of cell indication, an 8-bit octet bus and a parity bit is selected. When RBUS8 is logic 0, an 18-bit interface consisting of a start of cell indication, 16-bit word bus and a parity bit is selected.

Register 0x020: Ingress Output Cell Interface Configuration #1

Bit	Type	Function	Default
15	R/W	OHECUDF	1
14	R/W	OCAINV	0
13	R/W	OCELLPOST[3]	0
12	R/W	OCELLPOST[2]	0
11	R/W	OCELLPOST[1]	0
10	R/W	OCELLPOST[0]	0
9	R/W	OCELLLEN[3]	0
8	R/W	OCELLLEN[2]	0
7	R/W	OCELLLEN[1]	0
6	R/W	OCELLLEN[0]	0
5	R/W	Reserved	0
4	R/W	OPTYP	0
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	OCALEVEL0	1
0	R/W	OFIFORST	0

OFIFORST:

The OFIFORST bit is used to reset the 4-cell FIFO. When OFIFORST is set to logic zero, the FIFO operates normally. When OFIFORST is set to logic one, the FIFO is immediately emptied and ignores reads and writes. The FIFO remains empty and continues to ignore reads and writes until a logic zero is written to OFIFORST.

N.B. It is recommended that, whenever any other bit in this register or the Ingress Output Cell Interface Configuration 2 register is changed, OFIFORST be set to logic one before the change and set to logic zero after.

OCALEVEL0:

The OCALEVEL0 signal determines what the OCA output indicates when it transitions inactive. When OCALEVEL0 is set to logic 1, a deassertion of the OCA output indicates that the Ingress Output Cell Interface FIFO is empty. When OCALEVEL0 is set to logic 0, a deassertion of the OCA output indicates that the Ingress Output Cell Interface FIFO is near empty and contains only four words.

OPTYP:

The OPTYP bit selects even or odd parity for the output data signal. When set to logic 1, OPRTY is the even parity bit for ODAT[15:0]. When set to logic 0, OPRTY is the odd parity bit for ODAT[15:0].

OCELLLEN[3:0]:

The OCELLLEN[3:0] bits determine the number of words appended to the output cell. When the OBUS8 register bit is a logic 1, the binary OCELLLEN[3:0] value is the maximum number of bytes appended to the basic 53 byte ATM cell. The maximum cell length is 63 bytes; a OCELLLEN[3:0] greater than 10 decimal results in 10 appended bytes.

When OBUS8 is a logic 0, the binary OCELLLEN[3:0] value is the number of words appended to the basic 27 word ATM cell. The maximum cell length is 32 words (i.e. 5 appended words); therefore, OCELLLEN[3:0] should not be set greater than 5 decimal when OBUS8 is logic 0.

OCELLPOST[3:0]:

The OCELLPOST[3:0] bits determine the number of words in the output cell postpend. The numerical difference between OCELLLEN[3:0] and OCELLPOST[3:0] represents the number of words in the prepend. It is inappropriate that OCELLPOST[3:0] exceed OCELLLEN[3:0].

When OBUS8 is a logic 1, the binary OCELLPOST[3:0] value is the number of bytes postpended to the basic 53 byte ATM cell.

When OBUS8 is a logic 0, the binary OCELLPOST[3:0] value is the number of words postpended to the basic 27 word ATM cell.

OCAINV:

The OCAINV bit selects the active polarity of the OCA cell available signal. The default configuration selects OCA to be active high. When OCAINV is set to logic 1 the OCA signal become active low. If the state of the OCAINV bit has been changed, the Ingress Output Cell Interface must be reset via the FIFORST bit in order to properly initialize the OCA output.

OHECUDF:

The HECUDF bit determines whether or not the HEC/UDF octets are included in cells transferred over the Ingress Output Cell Interface. When set to logic 1 (default), the HEC and UDF octets are included. When set to logic 0, these octets are omitted. I.e. if OBUS8 is logic 0, the third word of the 27-word ATM cell is omitted and a 26-word cell (plus appended words) is transferred. If OBUS8 is logic 1, the fifth octet of the 53-octet ATM cell is omitted and a 52-octet cell (plus appended octets) is transferred.

Register 0x022: Ingress Output Cell Counter (LSB)

Bit	Type	Function	Default
15	R	OCELL[15]	X
14	R	OCELL[14]	X
13	R	OCELL[13]	X
12	R	OCELL[12]	X
11	R	OCELL[11]	X
10	R	OCELL[10]	X
9	R	OCELL[9]	X
8	R	OCELL[8]	X
7	R	OCELL[7]	X
6	R	OCELL[6]	X
5	R	OCELL[5]	X
4	R	OCELL[4]	X
3	R	OCELL[3]	X
2	R	OCELL[2]	X
1	R	OCELL[1]	X
0	R	OCELL[0]	X

Register 0x023: Ingress Output Cell Counter (MSB)

Bit	Type	Function	Default
15	R	OCELL[31]	X
14	R	OCELL[30]	X
13	R	OCELL[29]	X
12	R	OCELL[28]	X
11	R	OCELL[27]	X
10	R	OCELL[26]	X
9	R	OCELL[25]	X
8	R	OCELL[24]	X
7	R	OCELL[23]	X
6	R	OCELL[22]	X
5	R	OCELL[21]	X
4	R	OCELL[20]	X
3	R	OCELL[19]	X
2	R	OCELL[18]	X
1	R	OCELL[17]	X
0	R	OCELL[16]	X

OCELL[31:0]:

The OCELL[31:0] bits indicate the number of cells read from the Ingress Output Cell Interface during the last accumulation interval. This counter should be polled at least every 10 seconds to avoid saturation or rollover.

A write to either address 0x022 or 0x023 loads the registers with the current counter value and resets the internal 32 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Read Cell Counter registers. The counter should be polled at least every 10 seconds to avoid the counter from saturating at 0xFFFFFFFF. The contents of these registers are valid within 4 OFCLK cycles of a transfer being triggered by a write to address 0x022 or 0x023.

This counter can also be reset by writing to the Master Reset and Identity/Load Performance Register 0x000. After a write to register 0x000, the Physical Layer Cell Counter register is loaded with the current count value and the counter is reset as described above.

Register 0x024: Ingress Output Cell Interface Configuration #2

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9	R/W	OBUS8	0
8	R/W	Reserved	0
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	1
4	R/W	Reserved	0
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	Reserved	0

OBUS8:

The OBUS8 register bit controls the bus width selection of the Ingress Output Cell Interface. When OBUS8 is logic 1, the 10-bit interface consisting of a start of cell indication, an 8-bit octet bus and a parity bit is selected. When OBUS8 is logic 0, an 18-bit interface consisting of a start of cell indication, 16-bit word bus and a parity bit is selected.

Register 0x030: Egress Input Cell Interface Configuration #1

Bit	Type	Function	Default
15	R/W	IHECUDF	1
14	R/W	ICAINV	0
13	R/W	ICELLPOST[3]	0
12	R/W	ICELLPOST[2]	0
11	R/W	ICELLPOST[1]	0
10	R/W	ICELLPOST[0]	0
9	R/W	ICELLLEN[3]	0
8	R/W	ICELLLEN[2]	0
7	R/W	ICELLLEN[1]	0
6	R/W	ICELLLEN[0]	0
5	R/W	Reserved	0
4	R/W	IPTYP	0
3	R/W	IFIFODP[1]	0
2	R/W	IFIFODP[0]	0
1	R/W	Reserved	0
0	R/W	IFIFORST	0

IFIFORST:

The IFIFORST bit is used to reset the 4-cell FIFO. When IFIFORST is set to logic zero, the FIFO operates normally. When IFIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to IFIFORST.

N.B. It is recommended that, whenever any other bit in this register or the Egress Input Cell Interface Configuration 2 register is changed, IFIFORST be set to logic one before the change and set to logic zero after.

IFIFODP[1:0]:

The IFIFODP[1:0] register field determines the apparent cell depth of all FIFOs for the input interface. This value determines the fill level at which the ICA[x] lines are deasserted. FIFO depth control may be important in systems where the cell latency through the Egress Input Cell Interface must be minimized. Although the Egress Input Cell Interface will deassert ICA[x] once the apparent depth level is reached, cells transferred despite the deassertion of ICA[x] will still be written in the FIFO until the physical storage limit (four cells) is reached. Any further cell writes will be lost. The apparent FIFO cell depth is configured as shown below:

IFIFODP[1]	IFIFODP[0]	APPARENT DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

IPTYP:

The IPTYP bit selects even or odd parity for the input signal. When set to logic 1, IPRTY is the even parity bit for IDAT[15:0]. When set to logic 0, IPRTY is the odd parity bit for IDAT[15:0].

ICELLLEN[3:0]:

The ICELLLEN[3:0] bits determine the number of words appended to the input cell. When the IBUS8 register bit is a logic 1, the binary ICELLLEN[3:0] value is the maximum number of bytes appended to the basic 53 byte ATM cell. The maximum cell length is 63 bytes; a ICELLLEN[3:0] greater than 10 decimal results in 10 appended bytes.

When IBUS8 is a logic 0, the binary ICELLLEN[3:0] value is the number of words appended to the basic 27 word ATM cell. The maximum cell length is 32 words (i.e. 5 appended words); therefore, ICELLLEN[3:0] should not be set greater than 5 decimal when IBUS8 is logic 0.

ICELLPOST[3:0]:

The ICELLPOST[3:0] bits determine the number of words in the input cell postpend. The numerical difference between ICELLLEN[3:0] and ICELLPOST[3:0] represents the number of words in the prepend. It is inappropriate that ICELLPOST[3:0] exceed ICELLLEN[3:0].

When IBUS8 is a logic 1, the binary ICELLPOST[3:0] value is the number of bytes postpended to the basic 53 byte ATM cell.

When IBUS8 is a logic 0, the binary ICELLPOST[3:0] value is the number of words postpended to the basic 27 word ATM cell.

ICAINV:

The CAINV bit selects the active polarity of the Egress ICA[4:1] cell available signals. The default configuration selects ICA[4:1] to be active high. When ICAINV is set to logic 1 the ICA[4:1] signals become active low. If the state of the ICAINV bit has been changed, the Egress Input Cell Interface must be reset via the IFIFORST.

IHECUDF:

The IHECUDF bit determines whether or not the HEC/UDF octets are included in cells transferred over the Egress Input Cell Interface. When set to logic 1 (default), the HEC and UDF octets are included. When set to logic 0, these octets are omitted. I.e. if IBUS8 is logic 0, the third word of the 27-word ATM cell is omitted and a 26-word cell (plus appended words) is transferred. If IBUS8 is logic 1, the fifth octet of the 53-octet ATM cell is omitted and a 52-octet cell (plus appended octets) is transferred.

Register 0x032: Egress Input Cell Counter (LSB)

Bit	Type	Function	Default
15	R	ICELL[15]	X
14	R	ICELL[14]	X
13	R	ICELL[13]	X
12	R	ICELL[12]	X
11	R	ICELL[11]	X
10	R	ICELL[10]	X
9	R	ICELL[9]	X
8	R	ICELL[8]	X
7	R	ICELL[7]	X
6	R	ICELL[6]	X
5	R	ICELL[5]	X
4	R	ICELL[4]	X
3	R	ICELL[3]	X
2	R	ICELL[2]	X
1	R	ICELL[1]	X
0	R	ICELL[0]	X

Register 0x033: Egress Input Cell Counter (MSB)

Bit	Type	Function	Default
15	R	ICELL[31]	X
14	R	ICELL[30]	X
13	R	ICELL[29]	X
12	R	ICELL[28]	X
11	R	ICELL[27]	X
10	R	ICELL[26]	X
9	R	ICELL[25]	X
8	R	ICELL[24]	X
7	R	ICELL[23]	X
6	R	ICELL[22]	X
5	R	ICELL[21]	X
4	R	ICELL[20]	X
3	R	ICELL[19]	X
2	R	ICELL[18]	X
1	R	ICELL[17]	X
0	R	ICELL[16]	X

ICELL[31:0]:

The ICELL[31:0] bits indicate the number of cells read from the Egress Input Cell Interface during the last accumulation interval. The count includes all user information and OAM cells, regardless of whether or not the VPI/VCI value is provisioned. The count also includes any Physical Layer idle cells (VPI=0, VCI=0, CLP=1) and unassigned cells (VPI=0, VCI=0, CLP=0) which are passed through the Egress Input cell interface.

A write to a registers 0x032, 0x033 or 0x000 marks the end of an accumulation interval, loading the register with the current counter value and resetting the counter to 0 or 1 if a countable event occurred during the transfer. The content of this register is valid within 4 IFCLK cycles of a transfer being triggered by a register write operation. The associated counter is incremented after the last octet of the cell is received and will saturate at 2^{32}-1 if the accumulation interval is too long.

Register 0x034: Egress Input Cell Interface Configuration #2

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10	R/W	Reserved	0
9	R/W	IBUS8	0
8	R/W	Reserved	0
7	R/W	Reserved	0
6	R/W	Reserved	1
5	R/W	INNI	1
4	R/W	IPHYDEV[4]	0
3	R/W	IPHYDEV[3]	0
2	R/W	IPHYDEV[2]	0
1	R/W	IPHYDEV[1]	0
0	R/W	IPHYDEV[0]	0

IPHYDEV[4:0]:

The IPHYDEV[4:0] bits are used when the ATLAS is in Polled mode (IPOLL=1). The ATLAS polls PHY devices using the IADDR[4:0] signals. The IPHYDEV[4:0] bits indicate the number of devices which can be polled as follows:

IPHYDEV[4:0]	Meaning
00000	Poll all 32 PHY devices
00001	Poll PHY#1 thru PHY#2
00010	Poll PHY#1 thru PHY#3
:	
11110	Poll PHY#1 thru PHY#31
11111	Poll all 32 PHY devices

INNI:

The INNI bit selects whether the first four bits of the ATM cell header are used when determining whether a cell should be discarded because it is unassigned or a physical layer idle cell. When set to logic 1 (default), the NNI format is used and first four bits of the ATM cell header must be zeros for a cell to be identified as an unassigned or physical layer cell. When set to logic 0, the UNI format is used and first four bits of the ATM cell header are ignored.

If a mixture of UNI and NNI cells pass through the Input Cell Interface, this register bit should be set to a logic 1. Any Physical Layer UNI cells which contain non-zero GFC fields shall be passed through the Egress Input FIFO.

IBUS8:

The IBUS8 register bit controls the bus width selection of the Egress Input Cell Interface. When IBUS8 is logic 1, the 10-bit interface consisting of a start of cell indication, an 8-bit octet bus and a parity bit is selected. When IBUS8 is logic 0, an 18-bit interface consisting of a start of cell indication, 16-bit word bus and a parity bit is selected.

Register 0x040: Egress Output Cell Interface Configuration #1

Bit	Type	Function	Default
15	R/W	THECUDF	1
14	R/W	TCAINV	0
13	R/W	TCELLPOST[3]	0
12	R/W	TCELLPOST[2]	0
11	R/W	TCELLPOST[1]	0
10	R/W	TCELLPOST[0]	0
9	R/W	TCELLLEN[3]	0
8	R/W	TCELLLEN[2]	0
7	R/W	TCELLLEN[1]	0
6	R/W	TCELLLEN[0]	0
5	R/W	Reserved	0
4	R/W	TPTYP	0
3	R/W	TFIFODP[1]	0
2	R/W	TFIFODP[0]	0
1	R/W	Reserved	0
0	R/W	TFIFORST	0

TFIFORST:

The TFIFORST bit is used to reset the 4-cell FIFO. When TFIFORST is set to logic zero, the FIFO operates normally. When TFIFORST is set to logic one, the FIFO is immediately emptied and ignores reads and writes. The FIFO remains empty and continues to ignore reads and writes until a logic zero is written to TFIFORST.

N.B. It is recommended that, whenever any other bit in this register or the Egress Output Cell Interface Configuration 2 register is changed, TFIFORST be set to logic one before the change and set to logic zero after.

TFIFODP[1:0]:

The TFIFODP[1:0] register field determines the apparent cell depth of all FIFOs for the Egress output interface. The FIFO depth control may be important in systems where the cell latency through the Egress portion of the ATLAS. The apparent FIFO cell depth is configured as shown below:

TFIFODP[1]	TFIFODP[0]	APPARENT DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

TPTYP:

The TPTYP bit selects even or odd parity for the output data signal. When set to logic 1, TPRTY is the even parity bit for TDAT[15:0]. When set to logic 0, OPRTY is the odd parity bit for TDAT[15:0].

TCELLLEN[3:0]:

The TCELLLEN[3:0] bits determine the number of words appended to the output cell. When the TBUS8 register bit is a logic 1, the binary TCELLLEN[3:0] value is the maximum number of bytes appended to the basic 53 byte ATM cell. The maximum cell length is 63 bytes; a TCELLLEN[3:0] greater than 10 decimal results in 10 appended bytes.

When TBUS8 is a logic 0, the binary TCELLLEN[3:0] value is the number of words appended to the basic 27 word ATM cell. The maximum cell length is 32 words (i.e. 5 appended words); therefore, TCELLLEN[3:0] should not be set greater than 5 decimal when TBUS8 is logic 0.

TCELLPOST[3:0]:

The TCELLPOST[3:0] bits determine the number of words in the output cell postpend. The numerical difference between TCELLLEN[3:0] and TCELLPOST[3:0] represents the number of words in the prepend. It is inappropriate that TCELLPOST[3:0] exceed TCELLLEN[3:0].

When TBUS8 is a logic 1, the binary TCELLPOST[3:0] value is the number of bytes postpended to the basic 53 byte ATM cell.

When TBUS8 is a logic 0, the binary TCELLPOST[3:0] value is the number of words postpended to the basic 27 word ATM cell.

TCAINV:

The TCAINV bit selects the active polarity of the Egress TCA[4:1] cell available signals. The default configuration selects TCA[4:1] to be active high. When TCAINV is set to logic 1 the TCA[4:1] signals become active low. If the state of the TCAINV bit has been changed, the Egress Output Cell Interface must be reset via the TFIFORST.

THECUDF:

The THECUDF bit determines whether or not the HEC/UDF octets are included in cells transferred over the Egress Output Cell Interface. When set to logic 1 (default), the HEC and UDF octets are included. When set to logic 0, these octets are omitted. I.e. if TBUS8 is logic 0, the third word of the 27-word ATM cell is omitted and a 26-word cell (plus appended words) is transferred. If TBUS8 is logic 1, the fifth octet of the 53-octet ATM cell is omitted and a 52-octet cell (plus appended octets) is transferred.

Register 0x042: Egress Output Cell Counter (LSB)

Bit	Type	Function	Default
15	R	TCELL[15]	X
14	R	TCELL[14]	X
13	R	TCELL[13]	X
12	R	TCELL[12]	X
11	R	TCELL[11]	X
10	R	TCELL[10]	X
9	R	TCELL[9]	X
8	R	TCELL[8]	X
7	R	TCELL[7]	X
6	R	TCELL[6]	X
5	R	TCELL[5]	X
4	R	TCELL[4]	X
3	R	TCELL[3]	X
2	R	TCELL[2]	X
1	R	TCELL[1]	X
0	R	TCELL[0]	X

Register 0x043: Egress Output Cell Counter (MSB)

Bit	Type	Function	Default
15	R	TCELL[31]	X
14	R	TCELL[30]	X
13	R	TCELL[29]	X
12	R	TCELL[28]	X
11	R	TCELL[27]	X
10	R	TCELL[26]	X
9	R	TCELL[25]	X
8	R	TCELL[24]	X
7	R	TCELL[23]	X
6	R	TCELL[22]	X
5	R	TCELL[21]	X
4	R	TCELL[20]	X
3	R	TCELL[19]	X
2	R	TCELL[18]	X
1	R	TCELL[17]	X
0	R	TCELL[16]	X

TCELL[31:0]:

The TCELL[31:0] bits indicate the number of cells transferred from the Egress Output Cell Interface during the last accumulation interval.

A write to a registers 0x042, 0x043 or 0x000 marks the end of an accumulation interval, loading the register with the current counter value and resetting the counter to 0 or 1 if a countable event occurred during the transfer. The content of this register is valid within 4 TFCLK cycles of a transfer being triggered by a register write operation. The associated counter is incremented after the last octet of the cell is sent and will saturate at 2^{32}-1 if the accumulation interval is too long.

Register 0x044: Egress Output Cell Interface Configuration #2

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10	R/W	TBUS8	0
9	R/W	Reserved	0
8	R/W	Reserved	0
7	R/W	Reserved	0
6	R/W	Reserved	1
5	R/W	Reserved	1
4	R/W	TPHYDEV[4]	0
3	R/W	TPHYDEV[3]	0
2	R/W	TPHYDEV[2]	0
1	R/W	TPHYDEV[1]	0
0	R/W	TPHYDEV[0]	0

TPHYDEV[4:0]:

The PHYDEV[4:0] bits are used when the ATLAS is in Polled mode (TPOLL=1). The ATLAS polls PHY devices using the TADDR[4:0] signals. The TPHYDEV[4:0] bits indicate the number of devices to be polled as follows:

TPHYDEV[4:0]	Meaning
00000	Poll all 32 PHY devices
00001	Poll PHY#1 thru PHY#2
00010	Poll PHY#1 thru PHY#3
:	
11110	Poll PHY#1 thru PHY#31
11111	Poll all 32 PHY devices

TBUS8:

The TBUS8 register bit controls the bus width selection of the Egress Output Cell Interface. When TBUS8 is logic 1, the 10-bit interface consisting of a start of cell indication, an 8-bit octet bus and a parity bit is selected. When TBUS8 is logic 0, an 18-bit interface consisting of a start of cell indication, 16-bit word bus and a parity bit is selected.

Register 0x050: Ingress Microprocessor Extract Cell Interface Control and Status

Bit	Type	Function	Default
15	R	I_EXTCA	X
14	R	I_ILEN[2]	X
13	R	I_ILEN[1]	X
12	R	I_ILEN[0]	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4	W	I_ABORT	0
3	W	I_RESTART	0
2	R/W	I_EXTPHYID	0
1	R/W	I_DMAEN	0
0	R/W	I_EXTRST	0

I_EXTRST:

The I_EXTRST is used to reset the Ingress Microprocessor Extract Cell Interface. When I_EXTRST is set to logic 0, the Extract FIFO operates normally. When I_EXTRST is logic 1, the extract FIFO is immediately emptied and ignores writes. The extract FIFO remains empty and continues to ignore writes until a logic 0 is written to I_EXTRST.

I_DMAEN:

The Ingress MCIF DMA Enable (I_DMAEN) bit allows generation of a DMA request upon reception of a cell in the extract FIFO. If IDMAEN is logic 1, the IDREQ output is asserted when a complete cell has been written into the extract FIFO. The first read of the Ingress Microprocessor Cell Data register after IDREQ is asserted returns the first word of the cell. Subsequent reads of the Ingress Microprocessor Cell Data register return the remaining words in the cell. When the cell contents are exhausted, the IDREQ output is deasserted even if more cells are contained in the cell buffer. This eases identification of cell boundaries.

If I_DMAEN is logic 0, the IDREQ output is held deasserted.

I_EXTPHYID:

The I_EXTPHYID bit allows the extraction of the PHY ID in each extracted cell from the Ingress Microprocessor Cell Interface. The HEC byte will be overwritten with the PHY ID associated with the extracted cell. The PHYID consists of a 5-bit number in the range 0 to 31, and is LSB justified within the HEC byte of the cell. A value of 0 represents PHY 1, a value of 1 represents PHY2, etc. up to PHY 32.

If I_EXTPHYID is logic 1, the HEC byte will be overwritten.
If I_EXTPHYID is logic 0, the HEC byte will not be overwritten.

I_RESTART:

The restart cell read (I_RESTART) bit resets the microprocessor cell read pointer. If I_RESTART is set to logic 1 during a cell read, the next word read from the Ingress Microprocessor Cell Data register will be the first word of the current cell. Subsequent reads from the Ingress Microprocessor Cell Data register return the remaining words of the cell.

I_RESTART is not readable, and is cleared upon a read of the Ingress Microprocessor Cell Data register.

I_ABORT:

The read abort (I_ABORT) bit allows the microprocessor to discard a cell without reading the contents. If I_ABORT is logic 1, the current cell being read is purged from the extract FIFO and the IDREQ output will be deasserted.

I_ABORT is not readable, and is cleared upon a read of the Microprocessor Cell Data register.

I_ILEN[2:0]:

The Ingress input cell length (I_ILEN[2:0]) status bits represent the length of the extracted cell currently being read. I_ILEN[2:0] will be valid throughout the transfer of the cell. This status information may be used to control the number of microprocessor reads for each particular cell and would typically be read just prior to reading the cell data. Since valid cell lengths range from 32 words to 27 words, values of these bits are:

I_ILEN[2:0] = 111, cell length = 32 words
I_ILEN[2:0] = 110, cell length = 31 words
…
I_ILEN[2:0] = 010, cell length = 27 words
I_ILEN[2:0] = 001, RESERVED
I_ILEN[2:0] = 000, RESERVED

I_EXTCA:

The Ingress microprocessor cell available (I_EXTCA) status bit indicates that at least one cell is present in the cell extract buffer. I_EXTCA is set to logic 1 when the last word of a cell is received. I_EXTCA is cleared to logic 0 when the last word in the buffer is read by the microprocessor. If multiple cells exist in the buffer, then I_EXTCA will remain at logic 1 until the last word of the last cell is read.

Assertion of the I_EXTCA status bit also results in a maskable interrupt.

Register 0x051: Ingress Microprocessor Insert Cell Interface Control and Status

Bit	Type	Function	Default
15	R	I_INSRDY	X
14		Unused	X
13		Unused	X
12		Unused	X
11	W	I_WRSOC	0
10	R/W	I_PHY[4]	0
9	R/W	I_PHY[3]	0
8	R/W	I_PHY[2]	0
7	R/W	I_PHY[1]	0
6	R/W	I_PHY[0]	0
5	R/W	I_OLEN[2]	0
4	R/W	I_OLEN[1]	0
3	R/W	I_OLEN[0]	0
2	R/W	I_UPHDRX	0
1	R/W	I_CRC10	0
0	R/W	I_INSRST	0

I_INSRST:

The I_INSRST bit is used to reset the Ingress Microprocessor Insert Cell Interface. When I_INSRST is set to logic 0, the insert FIFO operates normally. When I_INSRST is set to logic 1, the insert FIFO is immediately emptied and ignores writes. The insert FIFO remains empty and continues to ignore writes until a logic 0 is written into I_INSRST.

Any transfer from the insert FIFO currently in progress will be aborted.

I_CRC10:

The I_CRC10 bit forces the generation of the Error Detection Code (EDC) for cells written into the Ingress insert FIFO. If I_CRC10 is set to logic 1 prior to assembling the cell in the buffer, the last 10-bits of the cell are overwritten with the I_CRC-10 value calculated over the information field (payload) of the cell. In this case, the 6 MSBs of the last word are overwritten with zeros prior to I_CRC-10 generation and hence 6 zeros will be transmitted along with the valid I_CRC-10.

I_UPHDRX:

The Ingress header translation (I_UPHDRX) bit controls the header processing of the current cell written into the Ingress insert FIFO. If I_UPHDRX was set to logic 1 prior to writing the cell in the buffer, the current cell has its header modified (if header translation is enabled in the Ingress Cell Processor configuration register). The cell is also subject to all other cell processing functions, just as if the cell had been inserted through the Ingress Input Cell Interface. Therefore, the header information must correspond to a provisioned VC, or the cell will be discarded.

If I_UPHDRX is logic 0, the current cell is passed to the output cell interface without modification, with the exception that appended bytes may be added or stripped off to ensure a correct cell length for the selected interface. The cell need not belong to a provisioned connection. The cell is not processed.

I_OLEN[2:0]:

The I_OLEN[2:0] bits indicate the number of words in the inserted cell that the microprocessor is about to write. Since valid cell lengths range from 32 words to 27 words, values of these bits are:

I_OLEN[2:0] = 111, cell length = 32 words.
I_OLEN[2:0] = 110, cell length = 31 words.
…
I_OLEN[2:0] = 010, cell length = 27 words
I_OLEN[2:0] = 001, RESERVED.
I_OLEN[2:0] = 000, RESERVED.

I_PHYID[4:0]:

The Ingress PHY identification bits determine the PHY association of the current cell being written by the microprocessor. The state of the PHY[4:0] when the WRSOC is set selects the PHY device for that cell:

I_PHY[4:0] = 00000, PHY #1/Single PHY.
I_PHY[4:0] = 00001, PHY #2
I_PHY[4:0] = 00010, PHY #3
…
I_PHY[4:0] = 11111, PHY #32.

I_WRSOC:

The Ingress write start of cell (WRSOC) bit must identify the first word of the current cell that the microprocessor is writing. If I_WRSOC is logic 1, the next word written into the Ingress Microprocessor Cell Data register becomes the first word of the cell. Subsequent writes to the Ingress Microprocessor Cell Data register fill the remainder of the cell sequentially and the number of writes should correspond to the programmed I_OLEN[2:0] value. If I_WRSOC is set again before a complete cell is written, the existing contents will be overwritten without transmission.

I_WRSOC is not readable.

I_INSRDY:

The insert buffer ready status (I_INSRDY) bit indicates that the Ingress insert FIFO is ready to accept cell data. I_INSRDY is cleared when entire cell has been written into the FIFO and the cell has been transferred to the Ingress Cell Processor for insertion into the cell stream. Assertion of the I_INSRDY bit results in the assertion of a maskable interrupt.

Register 0x052: Ingress Microprocessor Cell Data

Bit	Type	Function	Default
15	R/W	I_MCD[15]	X
14	R/W	I_MCD[14]	X
13	R/W	I_MCD[13]	X
12	R/W	I_MCD[12]	X
11	R/W	I_MCD[11]	X
10	R/W	I_MCD[10]	X
9	R/W	I_MCD[9]	X
8	R/W	I_MCD[8]	X
7	R/W	I_MCD[7]	X
6	R/W	I_MCD[6]	X
5	R/W	I_MCD[5]	X
4	R/W	I_MCD[4]	X
3	R/W	I_MCD[3]	X
2	R/W	I_MCD[2]	X
1	R/W	I_MCD[1]	X
0	R/W	I_MCD[0]	X

I_MCD[15:0]:

The Ingress MCD[15:0] contains the cell data destined to or read from the Ingress Microprocessor Cell Interface.

For the cell extract FIFO, the I_EXTCA bit and associated maskable interrupt indicate that a cell is available to be read. Alternatively, the assertion of the IDREQ output (if enabled by the I_DMAEN bit) signals the presence of the cell. Reads of this register return the words of the cell starting with the first. If necessary, the read pointer can be reset to the start of the current cell by setting the I_RESTART bit. Alternatively, the read pointer can be reset to the start of the next cell by setting the I_ABORT bit.

In a polled mode, the I_INSRDY register bit indicates that the microprocessor may write another cell. For interrupt driven systems, the I_INSRDYI interrupt status bit and associated maskable interrupt indicate that a cell may be written.

Register 0x060: Egress Microprocessor Extract Cell Interface Control and Status

Bit	Type	Function	Default
15	R	E_EXTCA	X
14	R	E_ILEN[2]	X
13	R	E_ILEN[1]	X
12	R	E_ILEN[0]	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4	W	E_ABORT	0
3	W	E_RESTART	0
2	R/W	E_EXTPHYID	0
1	R/W	E_DMAEN	0
0	R/W	E_EXTRST	0

E_EXTRST:

The E_EXTRST is used to reset the Egress Microprocessor Extract Cell Interface. When E_EXTRST is set to logic 0, the Egress Extract FIFO operates normally. When E_EXTRST is logic 1, the Egress Extract FIFO is immediately emptied and ignores writes. The Egress extract FIFO remains empty and continues to ignore writes until a logic 0 is written to E_EXTRST.

E_DMAEN:

The Egress DMA Enable (E_DMAEN) bit allows generation of a DMA request upon reception of a cell in the extract FIFO. If E_DMAEN is logic 1, the EDREQ output is asserted when a complete cell has been written into the Egress extract FIFO. The first read of the Egress Microprocessor Cell Data register after EDREQ is asserted returns the first word of the cell. Subsequent reads of the Egress Microprocessor Cell Data register return the remaining words in the cell. When the cell contents are exhausted, the EDREQ output is deasserted even if more cells are contained in the cell buffer. This eases identification of cell boundaries.

If E_DMAEN is logic 0, the EDREQ output is held deasserted.

E_EXTPHYID:

The E_EXTPHYID bit allows the extraction of the Egress PHY ID in each extracted cell. The HEC byte will be overwritten with the Egress PHY ID associated with the extracted cell. The Egress PHYID consists of a 5-bit number in the range 0 to 31, and is LSB justified within the HEC byte of the cell. A value of 0 represents PHY 1, a value of 1 represents PHY2, etc. up to PHY 32.

If E_EXTPHYID is logic 1, the HEC byte will be overwritten.
If E_EXTPHYID is logic 0, the HEC byte will not be overwritten.

E_RESTART:

The Egress restart cell read (E_RESTART) bit resets the microprocessor cell read pointer. If E_RESTART is set to logic 1 during a cell read, the next word read from the Egress Microprocessor Cell Data register will be the first word of the current cell. Subsequent reads from the Egress Microprocessor Cell Data register return the remaining words of the cell.

E_RESTART is not readable, and is cleared upon a read of the Egress Microprocessor Cell Data register.

E_ABORT:

The read abort (E_ABORT) bit allows the microprocessor to discard a cell without reading the contents. If E_ABORT is logic 1, the current cell being read is purged from the Egress extract FIFO and the EDREQ output will be deasserted.

E_ABORT is not readable, and is cleared upon a read of the Microprocessor Cell Data register.

E_ILEN[2:0]:

The Egress input cell length (E_ILEN[2:0]) status bits represent the length of the extracted cell currently being read. E_ILEN[2:0] will be valid throughout the transfer of the cell. This status information may be used to control the number of microprocessor reads for each particular cell and would typically be read just prior to reading the cell data. Since valid cell lengths range from 32 words to 27 words, values of these bits are:

E_ILEN[2:0] = 111, cell length = 32 words
E_ILEN[2:0] = 110, cell length = 31 words
…
E_ILEN[2:0] = 010, cell length = 27 words
E_ILEN[2:0] = 001, RESERVED
E_ILEN[2:0] = 000, RESERVED

E_EXTCA:

The Egress microprocessor cell available (E_EXTCA) status bit indicates that at least one cell is present in the Egress cell extract buffer. E_EXTCA is set to logic 1 when the last word of a cell is received. E_EXTCA is cleared to logic 0 when the last word in the buffer is read by the microprocessor. If multiple cells exist in the buffer, then E_EXTCA will remain at logic 1 until the last word of the last cell is read.

Assertion of the E_EXTCA status bit also results in a maskable interrupt.

Register 0x061: Egress Microprocessor Insert Cell Interface Control and Status

Bit	Type	Function	Default
15	R	E_INSRDY	X
14		Unused	X
13		Unused	X
12		Unused	X
11	W	E_WRSOC	0
10	R/W	E_PHY[4]	0
9	R/W	E_PHY[3]	0
8	R/W	E_PHY[2]	0
7	R/W	E_PHY[1]	0
6	R/W	E_PHY[0]	0
5	R/W	E_OLEN[2]	0
4	R/W	E_OLEN[1]	0
3	R/W	E_OLEN[0]	0
2	R/W	E_UPHDRX	0
1	R/W	E_CRC10	0
0	R/W	E_INSRST	0

E_INSRST:

The E_INSRST bit is used to reset the Egress Microprocessor Insert Cell Interface. When E_INSRST is set to logic 0, the Egress insert FIFO operates normally. When E_INSRST is set to logic 1, the Egress insert FIFO is immediately emptied and ignores writes. The Egress insert FIFO remains empty and continues to ignore writes until a logic 0 is written into E_INSRST.

Any transfer from the insert E_FIFO currently in progress will be aborted.

E_CRC10:

The E_CRC10 bit forces the generation of the Error Detection Code (EDC) for cells written into the Egress insert FIFO. If E_CRC10 is set to logic 1 prior to assembling the cell in the buffer, the last 10-bits of the cell are overwritten with the CRC-10 value calculated over the information field (payload) of the cell. In this case, the 6 MSBs of the last word are overwritten with zeros prior to CRC-10 generation and hence 6 zeros will be transmitted along with the valid CRC-10.

E_UPHDRX:

The Egress header translation (E_UPHDRX) bit controls the header processing of the current cell written into the Egress insert FIFO. If E_UPHDRX was set to logic 1 prior to writing the cell in the buffer, the current cell has its header modified (if header translation is enabled in the Egress Cell Processor configuration register). The cell is also subject to all other cell processing functions, just as if the cell had been inserted through the Egress Input Cell Interface. Therefore, the header information must correspond to a provisioned VC, or the cell will be discarded.

If E_UPHDRX is logic 0, the current cell is passed to the Egress output cell interface without modification, with the exception that appended bytes may be added or stripped off to ensure a correct cell length for the selected interface. The cell need not belong to a provisioned connection. The cell is not processed.

E_OLEN[2:0]:

The E_OLEN[2:0] bits indicate the number of words in the inserted cell that the microprocessor is about to write. Since valid cell lengths range from 32 words to 27 words, values of these bits are:

E_OLEN[2:0] = 111, cell length = 32 words.
E_OLEN[2:0] = 110, cell length = 31 words.
…
E_OLEN[2:0] = 010, cell length = 27 words
E_OLEN[2:0] = 001, RESERVED.
E_OLEN[2:0] = 000, RESERVED.

E_PHYID[4:0]:

The Egress PHY identification bits determine the Egress PHY association of the current cell being written by the microprocessor. The state of the E_PHY[4:0] when the WRSOC is set selects the PHY device for that cell:

E_PHY[4:0] = 00000, PHY #1/Single PHY.
E_PHY[4:0] = 00001, PHY #2
E_PHY[4:0] = 00010, PHY #3
…
E_PHY[4:0] = 11111, PHY #32.

E_WRSOC:

The Egress write start of cell (E_WRSOC) bit must identify the first word of the current cell that the microprocessor is writing. If E_WRSOC is logic 1, the next word written into the Egress Microprocessor Cell Data register becomes the first word of the cell. Subsequent writes to the Egress Microprocessor Cell Data register fill the remainder of the cell sequentially and the number of writes should correspond to the programmed E_OLEN[2:0] value. If E_WRSOC is set again before a complete cell is written, the existing contents will be overwritten without transmission.

E_WRSOC is not readable.

E_INSRDY:

The Egress insert buffer ready status (E_INSRDY) bit indicates that the Egress insert FIFO is ready to accept cell data. E_INSRDY is cleared when entire cell has been written into the FIFO and the cell has been transferred to the Egress Cell Processor for insertion into the cell stream. Assertion of the E_INSRDY bit results in the assertion of a maskable interrupt.

Register 0x062: Egress Microprocessor Cell Data

Bit	Type	Function	Default
15	R/W	E_MCD[15]	X
14	R/W	E_MCD[14]	X
13	R/W	E_MCD[13]	X
12	R/W	E_MCD[12]	X
11	R/W	E_MCD[11]	X
10	R/W	E_MCD[10]	X
9	R/W	E_MCD[9]	X
8	R/W	E_MCD[8]	X
7	R/W	E_MCD[7]	X
6	R/W	E_MCD[6]	X
5	R/W	E_MCD[5]	X
4	R/W	E_MCD[4]	X
3	R/W	E_MCD[3]	X
2	R/W	E_MCD[2]	X
1	R/W	E_MCD[1]	X
0	R/W	E_MCD[0]	X

E_MCD[15:0]:

The E_MCD[15:0] contains the cell data destined to or read from the Egress Microprocessor Cell Interface.

For the Egress cell extract FIFO, the E_EXTCA bit and associated maskable interrupt indicate that a cell is available to be read. Alternatively, the assertion of the EDREQ output (if enabled by the E_DMAEN bit) signals the presence of the cell. Reads of this register return the words of the cell starting with the first. If necessary, the read pointer can be reset to the start of the current cell by setting the E_RESTART bit. Alternatively, the read pointer can be reset to the start of the next cell by setting the E_ABORT bit.

In a polled mode, the E_INSRDY register bit indicates that the microprocessor may write another cell. For interrupt driven systems, the E_INSRDYI interrupt status bit and associated maskable interrupt indicate that a cell may be written.

Register 0x070: Ingress RDI Backward OAM Cell Interface Configuration #1

Bit	Type	Function	Default
15	R/W	Reserved	1
14	R/W	Reserved	0
13	R/W	Reserved	0
12	R/W	Reserved	0
11	R/W	Reserved	0
10	R/W	Reserved	0
9	R/W	Reserved	0
8	R/W	Reserved	0
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	IRDIBCIFRST	0

IRDIBCIFRST:

The IRDIBCIFRST bit is used to reset the 4-cell FIFO. When IRDIBCIFRST is set to logic zero, the FIFO operates normally. When IRDIBCIFRST is set to logic one, the FIFO is immediately emptied and ignores reads and writes. The FIFO remains empty and continues to ignore reads and writes until a logic zero is written to IRDIBCIFRST.

N.B. This FIFO must be reset at startup.

Register 0x071: Reserved

Register 0x072: Reserved

Register 0x073: Reserved

Register 0x074: Reserved

Register 0x080: Ingress Backward Reporting OAM Cell Interface Configuration #1

Bit	Type	Function	Default
15	R/W	Reserved	1
14	R/W	Reserved	0
13	R/W	Reserved	0
12	R/W	Reserved	0
11	R/W	Reserved	0
10	R/W	Reserved	0
9	R/W	Reserved	0
8	R/W	Reserved	0
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	IBPMBCIFRST	0

IBPMBCIFRST:

The IBPMBCIFRST bit is used to reset the 16-cell FIFO. When IBPMBCIFRST is set to logic zero, the FIFO operates normally. When IBPMBCIFRST is set to logic one, the FIFO is immediately emptied and ignores reads and writes. The FIFO remains empty and continues to ignore reads and writes until a logic zero is written to IBPMBCIFRST.

N.B. This FIFO must be reset at startup.

Register 0x081: Reserved

Register 0x082: Reserved

Register 0x083: Reserved

Register 0x084: Reserved

Register 0x090: Egress RDI Backward OAM Cell Interface Configuration #1

Bit	Type	Function	Default
15	R/W	Reserved	1
14	R/W	Reserved	0
13	R/W	Reserved	0
12	R/W	Reserved	0
11	R/W	Reserved	0
10	R/W	Reserved	0
9	R/W	Reserved	0
8	R/W	Reserved	0
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	ERDIBCIFRST	0

ERDIBCIFRST:

The ERDIBCIFRST bit is used to reset the 4-cell FIFO. When ERDIBCIFRST is set to logic zero, the FIFO operates normally. When ERDIBCIFRST is set to logic one, the FIFO is immediately emptied and ignores reads and writes. The FIFO remains empty and continues to ignore reads and writes until a logic zero is written to ERDIBCIFRST.

N.B. This FIFO must be reset at startup.

Register 0x091: Reserved

Register 0x092: Reserved

Register 0x093: Reserved

Register 0x094: Reserved

Register 0x0A0: Egress Backward Reporting OAM Cell Interface Configuration #1

Bit	Type	Function	Default
15	R/W	Reserved	1
14	R/W	Reserved	0
13	R/W	Reserved	0
12	R/W	Reserved	0
11	R/W	Reserved	0
10	R/W	Reserved	0
9	R/W	Reserved	0
8	R/W	Reserved	0
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	EBPMBCIFRST	0

EBPMBCIFRST:

The EBPMBCIFRST bit is used to reset the 16-cell FIFO. When EBPMBCIFRST is set to logic zero, the FIFO operates normally. When EBPMBCIFRST is set to logic one, the FIFO is immediately emptied and ignores reads and writes. The FIFO remains empty and continues to ignore reads and writes until a logic zero is written to EBPMBCIFRST.

N.B. This FIFO must be reset at startup.

Register 0x0A1: Reserved

Register 0x0A2: Reserved

Register 0x0A3: Reserved

Register 0x0A4: Reserved

Register 0x0B0: RFCLK Delay Locked Loop Register 1

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	0
4		OVERRIDE	0
3		Unused	X
2		Unused	X
1	R/W	VERN_EN	0
0	R/W	LOCK	0

The DLL Configuration Register controls the basic operation of the DLL.

CAUTION: The following register bits should not be changed after reset. Modifying any of the default values can result in unpredictable operation or no operation at all. It is highly recommend that these register bits remain unchanged.

LOCK:

The LOCK register is used to force the DLL to ignore phase offsets indicated by the phase detector after the lock has been achieved. When LOCK is set to logic zero, the DLL will track phase offsets measured by the phase detector between the RFCLK and the reference clock inputs. When LOCK is set to logic one, the DLL will not change the tap, register 0x0B2, after the phase detector indicates of zero phase offset between the RFCLK and the reference clock inputs for the first time.

VERN_EN:

The vernier enable register (VERN_EN) forces the DLL to ignore the phase detector and use the tap number specified by the VERNIER[7:0] register bits. When VERN_EN is set to logic zero, the DLL operates normally adjusting the phase offset based on the phase detector. When VERN_EN is set to logic one, the delay line uses the tap specified by the VERNIER[7:0] register bits.

OVERRIDE:

The override control (OVERRIDE) disables the DLL operation. When OVERRIDE is set low, the DLL generates the DLLCLK by delaying the RFCLK until the rising edge of the reference clock occurs at the same time as the rising edge of RFCLK. When OVERRIDE is set high, the DLLCLK output is a buffered version of the RFCLK input. This feature provides a back-up strategy in case the DLL does not operate correctly.

Register 0x0B1: RFCLK DLL Register 2

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7	R/W	VERNIER[7]	0
6	R/W	VERNIER[6]	0
5	R/W	VERNIER[5]	0
4	R/W	VERNIER[4]	0
3	R/W	VERNIER[3]	0
2	R/W	VERNIER[2]	0
1	R/W	VERNIER[1]	0
0	R/W	VERNIER[0]	0

The Vernier Control Register provides the delay line tap control when using the vernier option.

VERNIER[7:0]:

The vernier tap register bits VERNIER[7:0] specifies the phase delay through the DLL when using the vernier feature. When VERN_EN is set high, the VERNIER[7:0] registers specify the delay tap used. When VERN_EN is set low, the VERNIER[7:0] register is ignored. A VERNIER[7:0] value of all zeros specifies the delay tap with the minimum delay through the delay line. A VERNIER[7:0] value of all ones specifies the delay tap with the maximum delay through the delay line.

Register 0x0B2: RFCLK DLL Register 3

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7	R	TAP[7]	X
6	R	TAP[6]	X
5	R	TAP[5]	X
4	R	TAP[4]	X
3	R	TAP[3]	X
2	R	TAP[2]	X
1	R	TAP[1]	X
0	R	TAP[0]	X

The DLL Delay Tap Status Register indicates the delay tap used by the DLL to generate the outgoing clock. Writing to this register performs a software reset of the DLL.

TAP[7:0]:

The tap status register bits TAP[7:0] specifies the delay line tap the DLL is using to generate the outgoing clock DLLCLK. When TAP[7:0] is logic zero, the DLL is using the delay line tap with minimum phase delay. When TAP[7:0] is all logic one, the DLL is using the delay line tap with maximum phase delay. TAP[7:0] is invalid when vernier enable VERN_EN is set to one.

Register 0x0B3: RFCLK DLL Register 4

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7	R	SYSCLKI	X
6	R	REFCLKI	X
5	R	ERRORI	X
4	R	CHANGEI	X
3		Unused	X
2	R	ERROR	X
1	R	CHANGE	0
0	R	RUN	0

The DLL Control Status Register provides information of the DLL operation.

RUN:

The DLL lock status register bit RUN indicates the DLL has found a delay line tap in which the phase difference between the rising edge of REFCLK and the rising edge of SYSLCK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1. The RUN register bit is cleared only by a system reset or a software reset (writing to register 0x0B2).

CHANGE:

The delay line tap change register bit CHANGE indicates the DLL has moved to a new delay line tap. CHANGE is set high for eight SYSCLK cycles when the DLL moves to a new delay line tap.

CHANGEI:

The delay line tap change event register bit (CHANGEI) indicates the CHANGE register bit has changed value. When the CHANGE register changes from a logic zero to a logic one, the CHANGEI register bit is set to logic one. The CHANGEI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

REFCLKI:

The reference clock event register bit REFCLKI provides a method to monitor activity on the reference clock. When the REFCLK primary input changes from a logic zero to a logic one, the REFCLKI register bit is set to logic one. The REFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

SYSCLKI:

The system clock event register bit SYSLCKI provides a method to monitor activity on the system clock. When the SYSCLK primary input changes from a logic zero to a logic one, the SYSCLKI register bit is set to logic one. The SYSCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Register 0x0C0: ISYSCLK Delay Locked Loop Register 1

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B0 for a complete description.

Register 0x0C1: ISYSCLK DLL Register 2

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B1 for a complete description.

Register 0x0C2: ISYSCLK DLL Register 3

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B2 for a complete description.

Register 0x0C3: ISYSCLK DLL Register 4

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B3 for a complete description.

Register 0x0D0: OFCLK Delay Locked Loop Register 1

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B0 for a complete description.

Register 0x0D1: OFCLK DLL Register 2

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B1 for a complete description.

Register 0x0D2: OFCLK DLL Register 3

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B2 for a complete description.

Register 0x0D3: OFCLK DLL Register 4

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B3 for a complete description.

Register 0x0E0: IFCLK Delay Locked Loop Register 1

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B0 for a complete description.

Register 0x0E1: IFCLK DLL Register 2

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B1 for a complete description.

Register 0x0E2: IFCLK DLL Register 3

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B2 for a complete description.

Register 0x0E3: IFCLK DLL Register 4

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B3 for a complete description.

Register 0x0F0: ESYSCLK Delay Locked Loop Register 1

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B0 for a complete description.

Register 0x0F1: ESYSCLK DLL Register 2

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B1 for a complete description.

Register 0x0F2: ESYSCLK DLL Register 3

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B2 for a complete description.

Register 0x0F3: ESYSCLK DLL Register 4

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B3 for a complete description.

Register 0x100: TFCLK Delay Locked Loop Register 1

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B0 for a complete description.

Register 0x101: TFCLK DLL Register 2

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B1 for a complete description.

Register 0x102: TFCLK DLL Register 3

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B2 for a complete description.

Register 0x103: TFCLK DLL Register 4

The Operation of this register is identical to the RFCLK Delay Locked Loop. Refer to register 0x0B3 for a complete description.

Register 0x180: Ingress Search Engine Configuration

Bit	Type	Function	Default
15	R/W	PHY[2]	0
14	R/W	PHY[1]	0
13	R/W	PHY[0]	0
12	R/W	BCIFHECUDF	0
11	R/W	Reserved	0
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5	R/W	Reserved	0
4	R/W	DISVERIFY	0
3	R/W	Reserved	0
2	R/W	CNTUNDEF	0
1	R/W	CNTINVPTIVPI	0
0	R/W	VPRMSEL	0

VPRMSEL:

The VPRMSEL bit controls the identification of the VPC Resource Management (VP-RM) cells. If VPRMSEL is a logic 0, VP-RM cells are identified by a VCI=6, the PTI field is ignored. If VPRMSEL is a logic 1, VP-RM cells are identified by a VCI=6 and a PTI=110. If the PTI field is not equal to 110, the cell is flagged as invalid and optionally can be routed to the Ingress Microprocessor Cell Interface by the Ingress Cell Processor.

CNTINVPTIVCI:

The CNTINVPTIVCI controls the counting of cells with invalid PTI or VCI values. If CNTINVPTIVCI is a logic 0, all F5 cells with PTI= '111' and F4 cells with VCI = 0 and/or VCI between 7 to 15, are included in the per-PHY count of Invalid VPI/VCI/PTI cells. Cells with PTI='111' or VCI = 0, 7-15 will always result in the assertion of the I_PTIVCII interrupt regardless of the state of CNTINVPTIVCI.

CNTUNDEF:

If the CNTUNDEF bit is a logic 1, OAM cells with undefined OAM Type and Function Type fields are accumulated in the per-PHY count of errored OAM cells. The I_OAMERRI interrupt is also asserted if CNTUNDEF is logic 1 and an OAM cell with an undefined OAM Type and Function Type field is received. If CNTUNDEF is a logic 0, only OAM cells with CRC-10 errors cause the per-PHY errored OAM cell count to increment.

DISVERIFY:

The Disable Verify bit controls whether or not the secondary search key is used as part of the cell confirmation step.

If this bit is set to logic 1 then, after the VC search is complete, the Secondary search key IS NOT compared to the Verify Field of the VCRA. All cells with a valid Primary Key will be considered part of a valid connection. This bit will typically be set high if the cell is identified completely using only the Primary Key – perhaps as part of an egress routing device.

If this bit is set to logic 0 the binary search is completed with the “confirmation step” which compares the secondary key to the Verify Field of the VCRA.

BCIFHECUDF:

If the BCIFHECUDF bit is logic 1, the HEC and UDF fields are used for the direct lookup index for cells received from the Ingress Backward OAM Cell Interface. This allows the management software to use the HEC and UDF fields to specify an Ingress VC Table address for cells that are inserted into the Ingress cell stream. If this bit is logic 0, the Ingress Search Engine uses the primary and secondary search keys to lookup cells received from the Ingress Backward OAM Cell Interface in exactly the same manner as cells received from the Ingress Input Cell Interface.

PHY[2:0]:

The contents of PHY[2:0] determine the number of PHY ID bits in the Primary Search Key. If less than all five PHY address lines should be considered during the key search (as in the case where only a single PHY interface is used) then PHY[2:0] must be programmed with the values below.

PHY[2]	PHY[1]	PHY[0]	Number of PHY ID bits in Primary Key
1	1	1	Reserved
1	1	0	Reserved
1	0	1	5
1	0	0	4
0	1	1	3
0	1	0	2
0	0	1	1
0	0	0	0 (single PHY interface)

Register 0x181: Ingress VC Table External RAM Address

Bit	Type	Function	Default
15	R/W	SA[15]	0
14	R/W	SA[14]	0
13	R/W	SA[13]	0
12	R/W	SA[12]	0
11	R/W	SA[11]	0
10	R/W	SA[10]	0
9	R/W	SA[9]	0
8	R/W	SA[8]	0
7	R/W	SA[7]	0
6	R/W	SA[6]	0
5	R/W	SA[5]	0
4	R/W	SA[4]	0
3	R/W	SA[3]	0
2	R/W	SA[2]	0
1	R/W	SA[1]	0
0	R/W	SA[0]	0

This register is used in conjunction with the Word Select and Access Control register to access the Ingress VC Table external SRAM.

SA[15:0]:

This register holds the VC Record Address to be used to address the Ingress VC Table external SRAM through Microprocessor initiated accesses. It identifies the desired VC Table entry.

Register 0x182: Ingress VC Table External RAM Access Control

Bit	Type	Function	Default
15	R/W	RWB	0
14	R	BUSY	X
13	R/W	CLRONRD	0
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1		Unused	X
0		Unused	X

This register allows the microprocessor to access the Ingress VC Table external SRAM for data in the VC Record indicated in register 0x181 and perform the operation specified by the RWB bit. Writing to this register initiates a microprocessor access request cycle. The contents of the Ingress VC Table Record Address register should be set to the desired Ingress VC Table Record before this register is written. Write Mask register 0x184 can be used to mask bytes out of the write operation.

Note, the Write Mask register is valid if a single Ingress VC Table row is being accessed. If multiple Ingress VC Table rows are being accessed (i.e. more than one ROW[14:0] signal is active), the ATLAS applies the Write Mask on multiple row accesses. If Masking is not desired for multiple row accesses, perform an extra write to clear the write mask register before the access.

CLRONRD:

If CLRONRD is logic 1, then after a read access of Row 5 of the Ingress VC Table specified in Register 0x181, a write with data bits [47:0] set to all '0' is automatically initiated. Other bits in the words are preserved in the write back.

If CLRONRD is logic 1, then after a read access of Row 6 and Row 9 of the Ingress VC Table specified in Register 0x181, a write with data bits all '0' is automatically initiated.

If CLRONRD = '0', no write back to clear the data bits is initiated.

BUSY:

The BUSY bit is high while a Microprocessor initiated access request to the Ingress VC Table external SRAM is pending. If more than one access to the external SRAM is initiated either through read-write-back, mask write or writing to multiple rows of the Ingress VC Table through write/read caching, the BUSY bit is deasserted only after all the access required has been completed. This register should be polled until the BUSY bit goes low before another microprocessor access request is initiated. A microprocessor access request with 1 row selected is typically completed within 37 ISYSCLK cycles. If the ISTANDBY bit in the ATLAS Master Configuration register is a logic 1, the access time with 1 word selected is reduced to less than 5 ISYSCLK cycles.

RWB:

The RWB bit selects the operation to be performed on the addressed Ingress VC Table external SRAM: when RWB is set to a logic 1, a read from the external SRAM is requested; when RWB is set to a logic 0, a write to the external SRAM is requested.

Register 0x183: Ingress VC Table External SRAM Row Select

Bit	Type	Function	Default
15		Unused	X
14	R/W	Row[14]	0
13	R/W	Row[13]	0
12	R/W	Row[12]	0
11	R/W	Row[11]	0
10	R/W	Row[10]	0
9	R/W	Row[9]	0
8	R/W	Row[8]	0
7	R/W	Row[7]	0
6	R/W	Row[6]	0
5	R/W	Row[5]	0
4	R/W	Row[4]	0
3	R/W	Row[3]	0
2	R/W	Row[2]	0
1	R/W	Row[1]	0
0	R/W	Row[0]	0

This register selects the rows which the microprocessor wants to access from the Ingress VC Table for data in the VC Record indicated in register 0x181 and perform the operation specified by the RWB bit. The contents of the VC Record Address register and this register should be written before Register 0x182 is written.

ROW[14:0]:
ROW[14:0] indicate which of the 15 rows in the VC Record Table indicated by Register 0x181 is to be written or read when a microprocessor access to the Ingress VC Table is to be done. If ROW[x] is set to logic 1, row x of the Ingress VC Table will be written to or read from when Register 0x182 is written. If ROW[14:0] are all set to logic 1, all 15 rows of the Ingress VC Table record address selected in Register 0x181 will be written or read when a external SRAM access is triggered by writing to Register 0x182. The BUSY bit will be asserted until all the rows which are selected are written or read.

Register 0x184: Ingress VC Table Write Mask

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7	R/W	WM[7]	0
6	R/W	WM[6]	0
5	R/W	WM[5]	0
4	R/W	WM[4]	0
3	R/W	WM[3]	0
2	R/W	WM[2]	0
1	R/W	WM[1]	0
0	R/W	WM[0]	0

WM[7:0]:

The write mask (WM[7:0]) is used to select which bytes of the Ingress VC Table row will be written during a write operation. If any of WM[7:0] are a '1' during a write operation, the ISE performs a read-write-back operation when a write is requested. WM[7] controls the mask to bits [63:56] of the Ingress VC Table word and WM[0] controls the mask to bits [7:0] of the Ingress VC Table word. This is to allow the ISE to write to selected fields of a row in the Ingress VC Table.

If WM[7:0] = "00000000" then no fields are masked during the write and therefore no read cycle is required before doing the write. If more than one row is being accessed during a microprocessor initiated SRAM access, then the same WM[7:0] fields will be used for every access. Firmware should ensure that this register is updated before each write access.

If WM[7:0] = 0xFF, a normal read operation will result in a read-write-back operation instead of a simple read. The result is an extra cycle will be taken up, but register contents will remain unchanged.

Register 0x185: Field A Location and Length

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12	R/W	LA[4]	0
11	R/W	LA[3]	0
10	R/W	LA[2]	0
9	R/W	LA[1]	0
8	R/W	LA[0]	0
7		Unused	X
6	R/W	STARTA[6]	0
5	R/W	STARTA[5]	0
4	R/W	STARTA[4]	0
3	R/W	STARTA[3]	0
2	R/W	STARTA[2]	0
1	R/W	STARTA[1]	0
0	R/W	STARTA[0]	0

This register holds the starting location and length of Field A within the Routing Word.

STARTA[6:0]:

STARTA[6:0] forms the binary address of the MSB of the Field A within the Routing Word. STARTA[6] is the MSB of the address.

LA[4:0]:

LA[4:0] gives the length of the Field A in bits. The length is stored in LA[4:0] as binary value with LA[4] as MSB. If no Field A is to be used then LA[4:0] should be set to '00000'. Valid values for this field range from '00000' to '10000.' As a programming example: If a 10 bit Field A should be extracted starting at the 120th bit of the Routing Word, we would set LA ='01010' (length = 10) and STARTA='1110111' (starting address = 119), i.e. write 0x0A77 to this register.

Register 0x186: Field B Location and Length

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11	R/W	LB[3]	0
10	R/W	LB[2]	0
9	R/W	LB[1]	0
8	R/W	LB[0]	0
7		Unused	X
6	R/W	STARTB[6]	0
5	R/W	STARTB[5]	0
4	R/W	STARTB[4]	0
3	R/W	STARTB[3]	0
2	R/W	STARTB[2]	0
1	R/W	STARTB[1]	0
0	R/W	STARTB[0]	0

This register holds the starting location and length of Field B within the Routing Word.

STARTB[6:0]:

STARTB[6:0] forms the binary address of the MSB of the Field B within the Routing Word. STARTB[6] is the MSB of the address.

LB[3:0]:

LB[3:0] gives the length of the Field B in bits. The length is stored in LB[3:0] as binary value with LB[3] as MSB. If no Field B is to be used then LB[3:0] should be set to '0000'. Valid values for this field range from '0000' to '1011.' As a programming example: If a 10 bit Field B should be extracted starting at the 120th bit of the Routing Word, we would set LB ='1010' (length = 10) and STARTB = '1110111' (starting address = 119), i.e. write 0x0A77 to this register.

Register 0x187: Ingress Backward OAM Cell Interface Pacing

Bit	Type	Function	Default
15	R/W	BCP[15]	0
14	R/W	BCP[14]	0
13	R/W	BCP[13]	0
12	R/W	BCP[12]	0
11	R/W	BCP[11]	0
10	R/W	BCP[10]	0
9	R/W	BCP[9]	0
8	R/W	BCP[8]	0
7	R/W	BCP[7]	0
6	R/W	BCP[6]	0
5	R/W	BCP[5]	1
4	R/W	BCP[4]	0
3	R/W	BCP[3]	0
2	R/W	BCP[2]	0
1	R/W	BCP[1]	0
0	R/W	BCP[0]	0

This register sets the number of cell intervals between the transfer of backward cells from the Ingress Backward Cell Interface. A cell interval is defined to be 32 (i.e. assuming cells to be 64 bytes in length) ISYSCLK clocks. This is to prevent excessive insertion of backward OAM cells from the Ingress Backward OAM Cell Interface into the Ingress cell stream by the ATLAS.

BCP[15:0]:

BCP[15:0] sets the number of cell interval between transfers of cells from the Backward Cell Interface. The minimum rate of transfer is 1 in 65535 cell intervals. When BCP[15:0] = 0x0000 back-to-back transfer from the Ingress Backward Cell Interface is possible, if there are no transfer requested from the Ingress Input Cell Interface or the Ingress Microprocessor Cell Interface. The default is set to 1 in 32 cell interval.

Register 0x188: RESERVED

Bit	Type	Function	Default
15		Unused	X
14		Unsued	X
13		Unused	X
12		Unused	X
11		Unused	X
10	R/W	Reserved	1
9	R/W	Reserved	0
8	R/W	Reserved	0
7		Unused	X
6		Unused	X
5		Unused	X
4	R/W	Reserved	0
3	R/W	Reserved	1
2	R/W	Reserved	1
1	R/W	Reserved	0
0	R/W	Reserved	0

This register is reserved.

Register 0x190: Ingress VC Table Data Row 0, Word 0 (LSW) (RAM Data[15:0])

Bit	Type	Function	Default
15	R/W	Row0[15]	0
14	R/W	Row0[14]	0
13	R/W	Row0 [13]	0
12	R/W	Row0 [12]	0
11	R/W	Row0 [11]	0
10	R/W	Row0 [10]	0
9	R/W	Row0 [9]	0
8	R/W	Row0 [8]	0
7	R/W	Row0 [7]	0
6	R/W	Row0 [6]	0
5	R/W	Row0 [5]	0
4	R/W	Row0 [4]	0
3	R/W	Row0 [3]	0
2	R/W	Row0 [2]	0
1	R/W	Row0 [1]	0
0	R/W	Row0 [0]	0

This register contains either the data to be written into the Ingress VC Table Row 0 Word 0 (LSW) external SRAM or the data read from the external SRAM when a read request has been completed. If data is to be written to Ingress VC Table external SRAM Row 0, the LSW word must be written to this register before the Ingress VC Record Address register and the Row Select and Access Control register are written. If data is to be read from Row 0 this register contains the data from Row 0 Word 0 (LSW) after the external SRAM access is completed.

Register 0x191: Ingress VC Table Data Row 0, Word 1 (RAM Data [31:16])

Bit	Type	Function	Default
15	R/W	Row0 [31]	0
14	R/W	Row0 [30]	0
13	R/W	Row0 [29]	0
12	R/W	Row0 [28]	0
11	R/W	Row0 [27]	0
10	R/W	Row0 [26]	0
9	R/W	Row0 [25]	0
8	R/W	Row0 [24]	0
7	R/W	Row0 [23]	0
6	R/W	Row0 [22]	0
5	R/W	Row0 [21]	0
4	R/W	Row0 [20]	0
3	R/W	Row0 [19]	0
2	R/W	Row0 [18]	0
1	R/W	Row0 [17]	0
0	R/W	Row0 [16]	0

This register contains either the data to be written into the Ingress VC Table Row 0 Word 1 external SRAM or the data read from the external SRAM when a read request has been completed. If data is to be written to Ingress VC Table external SRAM Row 0, this word must be written to this register before the Ingress VC Table Record Address register and the Row Select and Access Control register are written. If data is to be read from Row 0 this register contains the data from Row 0 Word 1 after the external SRAM access is completed.

Register 0x192: Ingress VC Table Data Row 0, Word 2 (RAM Data [47:32])

Bit	Type	Function	Default
15	R/W	Row0[47]	0
14	R/W	Row0[46]	0
13	R/W	Row0[45]	0
12	R/W	Row0[44]	0
11	R/W	Row0[43]	0
10	R/W	Row0[42]	0
9	R/W	Row0[41]	0
8	R/W	Row0[40]	0
7	R/W	Row0[39]	0
6	R/W	Row0[38]	0
5	R/W	Row0[37]	0
4	R/W	Row0[36]	0
3	R/W	Row0[35]	0
2	R/W	Row0[34]	0
1	R/W	Row0[33]	0
0	R/W	Row0[32]	0

This register contains either the data to be written into the Ingress VC Table Row 0 Word 2 external SRAM or the data read from the external SRAM when a read request has been completed. If data is to be written to Ingress VC Record external SRAM Row 0, this word must be written to this register before the Ingress VC Table Record Address register and the Row Select and Access Control register are written. If data is to be read from Row 0 this register contains the data from Row 0 Word 2 after the external SRAM access is completed.

Register 0x193: Ingress VC Table Data Row 0, Word 3 (MSW) (RAM Data [63:48])

Bit	Type	Function	Default
15	R/W	Row0[63]	0
14	R/W	Row0[62]	0
13	R/W	Row0[61]	0
12	R/W	Row0[60]	0
11	R/W	Row0[59]	0
10	R/W	Row0[58]	0
9	R/W	Row0[57]	0
8	R/W	Row0[56]	0
7	R/W	Row0[55]	0
6	R/W	Row0[54]	0
5	R/W	Row0[53]	0
4	R/W	Row0[52]	0
3	R/W	Row0[51]	0
2	R/W	Row0[50]	0
1	R/W	Row0[49]	0
0	R/W	Row0[48]	0

This register contains either the data to be written into the Ingress VC Table Row 0 Word 3 external SRAM or the data read from the external SRAM when a read request has been completed. If data is to be written to Ingress VC Table external SRAM Row 0, this word must be written to this register before the Ingress VC Table Record Address register and the Row Select and Access Control register are written. If data is to be read from Row 0 this register contains the data from Row 0 Word 3 (MSW) after the external SRAM access is completed.

Register 0x194: Ingress VC Table Data Row 1, Word 0 (LSW) (RAM Data [15:0])

Register 0x195: Ingress VC Table Data Row 1, Word 1 (RAM Data [31:16])

Register 0x196: Ingress VC Table Data Row 1, Word 2 (RAM Data [47:32])

Register 0x197: Ingress VC Table Data Row 1, Word 3 (MSW) (RAM Data [63:48])

Register 0x198: Ingress VC Table Data Row 2, Word 0 (LSW) (RAM Data [15:0])

Register 0x199: Ingress VC Table Data Row 2, Word 1 (RAM Data [31:16])

Register 0x19A: Ingress VC Table Data Row 2, Word 2 (RAM Data [47:32])

Register 0x19B: Ingress VC Table Data Row 2, Word 3 (MSW) (RAM Data [63:48])

Register 0x19C: Ingress VC Table Data Row 3, Word 0 (LSW) (RAM Data [15:0])

Register 0x19D: Ingress VC Table Data Row 3, Word 1 (RAM Data [31:16])

Register 0x19E: Ingress VC Table Data Row 3, Word 2 (RAM Data [47:32])

Register 0x19F: Ingress VC Table Data Row 3, Word 3 (MSW) (RAM Data [63:48])

Register 0x1A0: Ingress VC Table Data Row 4, Word 0 (LSW) (RAM Data [15:0])

Register 0x1A1: Ingress VC Table Data Row 4, Word 1 (RAM Data [31:16])

Register 0x1A2: Ingress VC Table Data Row 4, Word 2 (RAM Data [47:32])

Register 0x1A3: Ingress VC Table Data Row 4, Word 3 (MSW) (RAM Data [63:48])

Register 0x1A4: Ingress VC Table Data Row 5, Word 0 (LSW) (RAM Data [15:0])

Register 0x1A5: Ingress VC Table Data Row 5, Word 1 (RAM Data [31:16])

Register 0x1A6: Ingress VC Table Data Row 5, Word 2 (RAM Data [47:32])

Register 0x1A7: Ingress VC Table Data Row 5, Word 3 (MSW) (RAM Data [63:48])

Register 0x1A8: Ingress VC Table Data Row 6, Word 0 (LSW) (RAM Data [15:0])

Register 0x1A9: Ingress VC Table Data Row 6, Word 1 (RAM Data [31:16])

Register 0x1AA: Ingress VC Table Data Row 6, Word 2 (RAM Data [47:32])

Register 0x1AB: Ingress VC Table Data Row 6, Word 3 (MSW) (RAM Data [63:48])

Register 0x1AC: Ingress VC Table Data Row 7, Word 0 (LSW) (RAM Data [15:0])

Register 0x1AD: Ingress VC Table Data Row 7, Word 1 (RAM Data [31:16])

Register 0x1AE: Ingress VC Table Data Row 7, Word 2 (RAM Data [47:32])

Register 0x1AF: Ingress VC Table Data Row 7, Word 3 (MSW) (RAM Data [63:48])

Register 0x1B0: Ingress VC Table Data Row 8, Word 0 (LSW) (RAM Data [15:0])

Register 0x1B1: Ingress VC Table Data Row 8, Word 1 (RAM Data [31:16])

Register 0x1B2: Ingress VC Table Data Row 8, Word 2 (RAM Data [47:32])

Register 0x1B3 Ingress VC Table Data Row 8, Word 3 (MSW) (RAM Data [63:48])

Register 0x1B4: Ingress VC Table Data Row 9, Word 0 (LSW) (RAM Data [15:0])

Register 0x1B5: Ingress VC Table Data Row 9, Word 1 (RAM Data [31:16])

Register 0x1B6: Ingress VC Table Data Row 9, Word 2 (RAM Data [47:32])

Register 0x1B7: Ingress VC Table Data Row 9, Word 3 (MSW) (RAM Data [63:48])

Register 0x1B8: Ingress VC Table Data Row 10, Word 0 (LSW) (RAM Data [15:0])

Register 0x1B9: Ingress VC Table Data Row 10, Word 1 (RAM Data [31:16])

Register 0x1BA: Ingress VC Table Data Row 10, Word 2 (RAM Data [47:32])

Register 0x1BB: Ingress VC Table Data Row 10, Word 3 (MSW) (RAM Data [63:48])

Register 0x1BC: Ingress VC Table Data Row 11, Word 0 (LSW) (RAM Data [15:0])

Register 0x1BD: Ingress VC Table Data Row 11, Word 1 (RAM Data [31:16])

Register 0x1BE: Ingress VC Table Data Row 11, Word 2 (RAM Data [47:32])

Register 0x1BF: Ingress VC Table Data Row 11, Word 3 (MSW) (RAM Data [63:48])

Register 0x1C0: Ingress VC Table Data Row 12 Word 0 (LSW) (RAM Data [15:0])

Register 0x1C1: Ingress VC Table Data Row 12 Word 1 (RAM Data [31:16])

Register 0x1C2: Ingress VC Table Data Row 12 Word 2 (RAM Data [47:32])

Register 0x1C3: Ingress VC Table Data Row 12 Word 3 (MSW) (RAM Data [63:48])

Register 0x1C4: Ingress VC Table Data Row 13 Word 0 (LSW) (Ram Data[15:0])

Register 0x1C5: Ingress VC Table Data Row 13 Word 1 (RAM Data [31:16])

Register 0x1C6: Ingress VC Table Data Row 13 Word 2 (RAM Data [47:32])

Register 0x1C7: Ingress VC Table Data Row 13 Word 3 (MSW) (RAM Data [63:48])

Register 0x1C8: Ingress VC Table Data Row 14 Word 0 (LSW) (Ram Data[15:0])

Register 0x1C9: Ingress VC Table Data Row 14 Word 1 (RAM Data [31:16])

Register 0x1CA: Ingress VC Table Data Row 14 Word 2 (RAM Data [47:32])

Register 0x1CB: Ingress VC Table Data Row 14 Word 3 (MSW) (RAM Data [63:48])

Register 0x200: Ingress Cell Processor Configuration 1

Bit	Type	Function	Default
15	R/W	Reserved	0
14	R/W	Reserved	0
13	R/W	UNDEFtoOCIF	0
12	R/W	InactiveToUP	0
11	R/W	COS	0
10	R/W	UPURS	0
9	R/W	VCRASTUFF	0
8	R/W	AUTORDI	0
7	R/W	COUNT	0
6	R/W	PM	0
5	R/W	GPOLICE	0
4	R/W	GFC	0
3	R/W	GUDF	0
2	R/W	GHEC	0
1	R/W	GPREPO	0
0	R/W	GVPIVCI	0

GVPIVCI:

If the GVPIVCI bit is logic 1, VPI/VCI translation is globally enabled. The ATM cell VPI/VCI bytes can be replaced by the contents of the Output Header word of the Ingress VC Table. If the GVPIVCI bit is logic 0, the incoming VPI/VCI combination is passed transparently.

Note that if the connection is F4 (ie. VPC, where the VCI field in the search key is coded as all zeros), then the VCI is passed through transparently.

GPREPO:

If the GPREPO bit is logic 1, substitution of prepend and postpend bytes is globally enabled. Any prepend or postpend bytes of an ATM cell are replaced by the contents of the PrePo1-PrePo10 words of the Ingress VC Table. If GPREPO is logic 0, prepend and postpend bytes pass through transparently.

GHEC:

If the GHEC bit is logic 1, the HEC field of an ATM cell is replaced by the contents of the 8 least significant bits of the Output Header word of the Ingress VC Table. If GHEC is logic 0, the HEC field of an ATM cell is passed transparently.

GUDF:

If the GUDF bit is logic 1, the UDF field of an ATM cell is replaced by the contents of the UDF field in the Ingress VC Table. If GUDF is logic 0, the UDF field of an ATM cell is passed transparently.

GFC:

The GFC bit determines if the GFC field in the ATM header is replaced or passed through unaltered. If GFC is logic 1, the GFC field is passed transparently. If GFC is logic 0, the GFC field is replaced by the contents of the most significant 4 bits of the Output Header field of the Ingress VC Table. The GFC bit has no effect if the connection belongs to a NNI.

GPOLICE:

If the GPOLICE bit is logic 1, cell rate policing is globally enabled on all connections (policing can be disabled on a per-connection basis by clearing the Increment fields, or by setting the Action1 and Action2 fields to zero). If the GPOLICE bit is logic 0, no cell rate policing is performed and no physical memory needs to be provisioned at VC Table locations ISA[19:16]=0011, 0100 and 0101.

PM:

If the PM bit is logic 1, performance monitoring is globally enabled. If the PM bit is logic 0, performance monitoring is globally disabled, all performance monitoring cells are neither terminated nor monitored at end-to-end points and segment end points, and no statistics are maintained at intermediate points.

COUNT:

If the COUNT bit is logic 1, per-connection cell counting is globally enabled. If the COUNT bit is logic 0, the two generic cell counts in the Ingress VC Table are not maintained, and no physical memory need be provided at those locations.

AUTORDI:

The AUTORDI bit enables the generation of segment and end-to-end RDI cells while in an AIS alarm or Continuity alarm state. If AUTORDI is logic 1, an RDI cell is transmitted (and looped from the Ingress Cell Processor to the Egress cell stream) immediately upon the reception of the first AIS cell at a flow end-point (if the ATLAS is an end-to-end point for that connection, an end-to-end RDI cell will be generated, if the ATLAS is a segment end point, a segment RDI cell will be generated, and if the ATLAS is both a segment and end-to-end point, both types of RDI cells will be generated) and once per second thereafter until the AIS state is exited. Similarly, if the CC_RDI bit in the Ingress VC Table is set, RDI cells are generated once per second if no user or CC cells have been received in the last 3.5 +/- 0.5 seconds. RDI cells can also be transmitted if the Send_RDI_segment and Send_RDI_end_to_end bits in the Ingress VC Table are set.

COS:

The Change of State FIFO enable (COS) bit enables the monitoring of changes in connection state in the Ingress direction. If COS is logic 1, all Ingress connections which undergo changes in state (e.g. AIS or CC alarm states) can be logged in a Change of State FIFO. This FIFO is 256 entries deep and holds a copy of the per-connection Status field of the Ingress VC Table. Using this feature eliminates the need to periodically poll each connection to determine if any changes in state have occurred. If the COS FIFO becomes full, background processes which monitor for changes in connection state will be suspended until such time as the FIFO becomes able to accept notifications of changes in state. Therefore, it is the responsibility of the management software to ensure the COS FIFO is read often enough so that changes in state remain compliant with the Bellcore and ITU standards.

If COS is logic 0, the COS FIFO is disabled, and the background processes will not be suspended. If COS is logic 0, it is the responsibility of the management software to poll each connection to determine changes in connection state (as reflected in the Status field of the Ingress VC Table) and notify higher layers of any changes in state.

The updating of the COS FIFO can be enabled/disabled on a per-connection basis with the COS_enable bit of the Configuration field of the Ingress VC Table.

VCRAstuff:

If the VCRAstuff bit is logic 1, all cells routed to the Ingress Microprocessor Cell Interface have the HEC and UDF bytes replaced with the Ingress VC Table Record address. This enables a microprocessor to immediately determine the location of an Ingress VC Table Record in its data structure. This feature is provided to enable high speed processing of cells. The EXTPHYID bit of the Ingress Microprocessor Cell Interface Extract FIFO Control and Status register takes precedence over the VCRAstuff bit. If the EXTPHYID is set, the HEC byte location of extracted cells will contain the PHY identification regardless of the state of the VCRAstuff bit.

UPURS:

The Ingress Microprocessor User Reason Symbol (UPURS) bit allows a causation word to be prepended to the cell extracted to the Ingress Microprocessor Interface. This allows an external microprocessor to immediately determine the reason a cell was routed to the Ingress Microprocessor Cell Interface. The extracted cell length will be 1 greater than the input cell length. Hence, this feature cannot be used if the input cell length is 32-words.

InactiveToUP:

When InactiveToUP is high, all cells received on connections whose Active bit is logic 0 in the Ingress VC Table are copied to the Ingress Microprocessor Cell Interface. Regardless of the state of this bit, all cells received on inactive connections are dropped by the ICP (i.e. not sent to the Ingress Output Cell Interface).

UNDEFtoOCIF:

When UNDEFtoOCIF is high, all OAM cells with an undefined OAM Type or Function Type value are passed through the Output Cell interface (OCIF) at flow end points. If UNDEFtoOCIF is low undefined OAM cells are not passed through the OCIF. The setting of this bit does not effect the action of copying cells to the Microprocessor Cell Interface. The UNDEFtoOCIF allows the use of proprietary OAM cell types which can be processed after the ATLAS.

Register 0x201: Ingress PHY Policing 1

Bit	Type	Function	Default
15	R/W	PolicePHY15	0
14	R/W	PolicePHY14	0
13	R/W	PolicePHY13	0
12	R/W	PolicePHY12	0
11	R/W	PolicePHY11	0
10	R/W	PolicePHY10	0
9	R/W	PolicePHY9	0
8	R/W	PolicePHY8	0
7	R/W	PolicePHY7	0
6	R/W	PolicePHY6	0
5	R/W	PolicePHY5	0
4	R/W	PolicePHY4	0
3	R/W	PolicePHY3	0
2	R/W	PolicePHY2	0
1	R/W	PolicePHY1	0
0	R/W	PolicePHY0	0

PolicePHYx:

The PolicePHYx bits enable the ATLAS per-PHY policing for PHYs 0 through 15. If PolicePHYx is logic 1, the per-PHY policing is enabled on PHYx. All connections associated with PHYx may have per-PHY policing enabled. The PHY Police bit in the Ingress VC Table must also be set to logic 1 for a connection to be per-PHY policed as well as policed by the per-connection leaky buckets. If PolicePHYx is logic 0, per-PHY policing for PHYx is disabled.

If per-PHY policing is enabled, it is the responsibility of the management software to setup the internal per-PHY Policing RAM.

Register 0x202: Ingress PHY Policing 2

Bit	Type	Function	Default
15	R/W	PolicePHY31	0
14	R/W	PolicePHY30	0
13	R/W	PolicePHY29	0
12	R/W	PolicePHY28	0
11	R/W	PolicePHY27	0
10	R/W	PolicePHY26	0
9	R/W	PolicePHY25	0
8	R/W	PolicePHY24	0
7	R/W	PolicePHY23	0
6	R/W	PolicePHY22	0
5	R/W	PolicePHY21	0
4	R/W	PolicePHY20	0
3	R/W	PolicePHY19	0
2	R/W	PolicePHY18	0
1	R/W	PolicePHY17	0
0	R/W	PolicePHY16	0

PolicePHYx:

The PolicePHYx bits enable the ATLAS per-PHY policing for PHYs 16 through 31. If PolicePHYx is logic 1, the per-PHY policing is enabled on PHYx. All connections associated with PHYx may have per-PHY policing enabled. The PHY Police bit in the Ingress VC Table must also be set to logic 1 for a connection to be per-PHY policed as well as policed by the per-connection leaky buckets. If PolicePHYx is logic 0, per-PHY policing for PHYx is disabled.

If per-PHY policing is enabled, it is the responsibility of the management software to setup the internal per-PHY Policing RAM.

Register 0x203: Ingress PHY Policing RAM Address and Access Control

Bit	Type	Function	Default
15	R/W	RWB	0
14	R	BUSY	X
13	R/W	CLRONRD	0
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6	R/W	PHYRow[1]	0
5	R/W	PHYRow[0]	0
4	R/W	PHYAddr[4]	0
3	R/W	PHYAddr[3]	0
2	R/W	PHYAddr[2]	0
1	R/W	PHYAddr[1]	0
0	R/W	PHYAddr[0]	0

PHYAddr[4:0]:

The PHYAddr[4:0] bits indicate which of the per-PHY RAM locations is going to be accessed. PHYAddr[4:0]=00000 holds the policing parameters and non-compliant cell counts for PHY 1, and PHYAddr[4:0]=11111 holds the policing parameters and non-compliant cell counts for PHY31.

PHYRow[1:0]:

The PHYRow[1:0] bits indicate which row of the per-PHY Policing RAM at PHYAddr[4:0] that is going to be accessed. If PHYRow[1:0] =00, the first row of the per-PHY Policing RAM is accessed. If PHYRow[1:0] = 11, the fourth row of the per-PHY Policing RAM is accessed.

CLRONRD:

If the CLRONRD bit is logic 1, then the per-PHY non-compliant cell counts are cleared after a read access to a per-PHY Policing RAM location is performed. If CLRONRD is logic 0, then a clearing write is not performed when the per-PHY non-compliant cell counts are accessed.

BUSY:

After a read or write access is initiated, the BUSY bit is asserted until the access has been completed. Typically, a read or write access will be completed within 37 ISYSCLK cycles.

RWB:

This bit indicates whether a read or write access is to be performed. If logic 1, a read access is initiated when this register is written to. If logic 0, a write access is initiated.

Register 0x204: Ingress PHY Policing RAM Data (LSW)

Bit	Type	Function	Default
15	R/W	PHYPoliceData[15]	0
14	R/W	PHYPoliceData[14]	0
13	R/W	PHYPoliceData[13]	0
12	R/W	PHYPoliceData[12]	0
11	R/W	PHYPoliceData[11]	0
10	R/W	PHYPoliceData[10]	0
9	R/W	PHYPoliceData[9]	0
8	R/W	PHYPoliceData[8]	0
7	R/W	PHYPoliceData[7]	0
6	R/W	PHYPoliceData[6]	0
5	R/W	PHYPoliceData[5]	0
4	R/W	PHYPoliceData[4]	0
3	R/W	PHYPoliceData[3]	0
2	R/W	PHYPoliceData[2]	0
1	R/W	PHYPoliceData[1]	0
0	R/W	PHYPoliceData[0]	0

PHYPoliceData[15:0]:

This is the least significant 16-bits of data to be written into the per-PHY Policing RAM, or the data read from the RAM when a read request has been completed. If data are to be written into the RAM, then this register must be written to before the PHY Policing Access and Control register is written. If data are to be read, then the BUSY bit of the PHY Policing Access and Control register must be deasserted before these data are valid.

Register 0x205: Ingress PHY Policing RAM Data (MSW)

Bit	Type	Function	Default
15	R/W	PHYPoliceData[31]	0
14	R/W	PHYPoliceData[30]	0
13	R/W	PHYPoliceData[29]	0
12	R/W	PHYPoliceData[28]	0
11	R/W	PHYPoliceData[27]	0
10	R/W	PHYPoliceData[26]	0
9	R/W	PHYPoliceData[25]	0
8	R/W	PHYPoliceData[24]	0
7	R/W	PHYPoliceData[23]	0
6	R/W	PHYPoliceData[22]	0
5	R/W	PHYPoliceData[21]	0
4	R/W	PHYPoliceData[20]	0
3	R/W	PHYPoliceData[19]	0
2	R/W	PHYPoliceData[18]	0
1	R/W	PHYPoliceData[17]	0
0	R/W	PHYPoliceData[16]	0

PHYPoliceData[31:16]:

This is the most significant 16-bits of data to be written into the per-PHY Policing RAM, or the data read from the RAM when a read request has been completed. If data are to be written into the RAM, then this register must be written to before the PHY Policing Access and Control register is written. If data are to be read, then the BUSY bit of the PHY Policing Access and Control register must be deasserted before these data are valid.

Register 0x206: Ingress PHY Policing Configuration 1 & 2

Bit	Type	Function	Default
15	R/W	Config2GCRA[7]	0
14	R/W	Config2GCRA[6]	0
13	R/W	Config2GCRA[5]	0
12	R/W	Config2GCRA[4]	0
11	R/W	Config2GCRA[3]	0
10	R/W	Config2GCRA[2]	0
9	R/W	Config2GCRA[1]	0
8	R/W	Config2GCRA[0]	0
7	R/W	Config1GCRA[7]	0
6	R/W	Config1GCRA[6]	0
5	R/W	Config1GCRA[5]	0
4	R/W	Config1GCRA[4]	0
3	R/W	Config1GCRA[3]	0
2	R/W	Config1GCRA[2]	0
1	R/W	Config1GCRA[1]	0
0	R/W	Config1GCRA[0]	0

Config1GCRA[7:0]:

The following table indicates upon which cell streams the per-PHY Policing instance acts (if the PHY Policing Configuration bit in the per-PHY Policing RAM is set to PHYPoliceConfig[1:0]=00):

Cell Type	RM		Segment OAM		End-to-End OAM		User	
CLP Bit	0	1	0	1	0	1	0	1
Reg Bit	Config1 GCRA[0]	Config1 GCRA[1]	Config1 GCRA[2]	Config1 GCRA[3]	Config1 GCRA[4]	Config1 GCRA[5]	Config1 GCRA[6]	Config1 GCRA[7]

A logic 1 written into any of the Config1GCRA1[7:0] register bits enables the per-PHY policing on that particular cell stream.

Config2GCRA[7:0]:

These register bits indicate the cell streams upon which the per-PHY Policing instance acts (if the PHY Policing Configuration bit in the per-PHY Policing RAM is set to PHYPoliceConfig[1:0]=01). These register bits are programmed in the same manner as listed above.

Register 0x207: Ingress PHY Policing Configuration 3 & 4

Bit	Type	Function	Default
15	R/W	Config4GCRA[7]	0
14	R/W	Config4GCRA[6]	0
13	R/W	Config4GCRA[5]	0
12	R/W	Config4GCRA[4]	0
11	R/W	Config4GCRA[3]	0
10	R/W	Config4GCRA[2]	0
9	R/W	Config4GCRA[1]	0
8	R/W	Config4GCRA[0]	0
7	R/W	Config3GCRA[7]	0
6	R/W	Config3GCRA[6]	0
5	R/W	Config3GCRA[5]	0
4	R/W	Config3GCRA[4]	0
3	R/W	Config3GCRA[3]	0
2	R/W	Config3GCRA[2]	0
1	R/W	Config3GCRA[1]	0
0	R/W	Config3GCRA[0]	0

Config3GCRA[7:0]:

These register bits indicate the cell streams upon which the per-PHY Policing instance acts (if the PHY Policing Configuration bit in the per-PHY Policing RAM is set to PHYPoliceConfig[1:0]=10). These register bits are programmed in the same manner as listed above.

Config4GCRA[7:0]:

These register bits indicate the cell streams upon which the per-PHY Policing instance acts (if the PHY Policing Configuration bit in the per-PHY Policing RAM is set to PHYPoliceConfig[1:0]=11). These register bits are programmed in the same manner as listed above.

Register 0x208: Ingress Connection Policing Configuration 1

Bit	Type	Function	Default
15	R/W	GCRA2[7]	0
14	R/W	GCRA2[6]	0
13	R/W	GCRA2[5]	0
12	R/W	GCRA2[4]	0
11	R/W	GCRA2[3]	0
10	R/W	GCRA2[2]	0
9	R/W	GCRA2[1]	0
8	R/W	GCRA2[0]	0
7	R/W	GCRA1[7]	0
6	R/W	GCRA1[6]	0
5	R/W	GCRA1[5]	0
4	R/W	GCRA1[4]	0
3	R/W	GCRA1[3]	0
2	R/W	GCRA1[2]	0
1	R/W	GCRA1[1]	0
0	R/W	GCRA1[0]	0

This register configuration is selected if the per-connection PolicingConfiguration[2:0]=000.

GCRA1[7:0]:

The following table indicates upon which cell streams the first policing instance acts:

Cell Type	RM		Segment OAM		End-to-End OAM		User	
CLP Bit	0	1	0	1	0	1	0	1
Reg Bit	GCRA1 [0]	GCRA1 [1]	GCRA1 [2]	GCRA1 [3]	GCRA1 [4]	GCRA1 [5]	GCRA1 [6]	GCRA1 [7]

A logic 1 written to any of the GCRA1[7:0] bits enables GCRA1 policing for that particular cell stream. For example, to enable cell rate policing for GCRA1 on the user CLP=0+1 cell stream, the register configuration would be GCRA1[7:0]=11000000. If GCRA1[7:0] = 00000000, the first GCRA policing instance is globally disabled.

GCRA2[7:0]:

These register bits control upon which cell streams the second GCRA instance acts. These register bits are programmed in exactly the same manner as described above.

Register 0x209: Ingress Connection Policing Configuration 2

Register 0x20A: Ingress Connection Policing Configuration 3

Register 0x20B: Ingress Connection Policing Configuration 4

Register 0x20C: Ingress Connection Policing Configuration 5

Register 0x20D: Ingress Connection Policing Configuration 6

Register 0x20E: Ingress Connection Policing Configuration 7

Register 0x20F: Ingress Connection Policing Configuration 8

Register 0x210: Ingress Policing Configuration and Non-Compliant Cell Counting

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13	R/W	PHYNCOUNT3[1]	0
12	R/W	PHYNCOUNT3[0]	0
11	R/W	PHYNCOUNT2[1]	0
10	R/W	PHYNCOUNT2[0]	0
9	R/W	PHYNCOUNT1[1]	0
8	R/W	PHYNCOUNT1[0]	0
7	R/W	NCOUNT3[1]	0
6	R/W	NCOUNT3[0]	0
5	R/W	NCOUNT2[1]	0
4	R/W	NCOUNT2[0]	0
3	R/W	NCOUNT1[1]	0
2	R/W	NCOUNT1[0]	0
1	R/W	POLQNTM[1]	0
0	R/W	POLQNTM[0]	0

POLQNTM:

The POLQNTM[1:0] bits set the time quantum for policing functions for all connections and policing instances (per-PHY and per-connection).

POLQNTM[1:0]	ISYSCLK period
00	1 times ISYSCLK period
01	2 times ISYSCLK period
10	4 times ISYSCLK period
11	8 times ISYSCLK period

NCOUNT1[1:0]:

The NCOUNT1[1:0] bits determine how the per-connection Non-Compliant cell count #1 of the Ingress VC Table is defined:

NCOUNT1[1:0]	Definition
00	Non-compliant CLP=0 cells.
01	Non-compliant CLP=0+1 cells.
10	Discarded CLP=0 cells.
11	Discarded CLP=0+1 cells.

NCOUNT2[1:0]:

The NCOUNT2[1:0] bits determine how the per-connection Non-Compliant Cell Count #2 of the Ingress VC Table is defined:

NCOUNT2[1:0]	Definition
00	Non-compliant CLP=0 cells.
01	Non-compliant CLP=0+1 cells.
10	Discarded CLP=0 cells.
11	Discarded CLP=0+1 cells.

NCOUNT3[1:0]:

The NCOUNT3[1:0] bits determine how the per-connection Non-Compliant Cell Count #3 of the Ingress VC Table is defined:

NCOUNT3[1:0]	Definition
00	Non-compliant CLP=0 cells.
01	Non-compliant CLP=0+1 cells.
10	Tagged CLP=0 cells which are not discarded.
11	Discarded CLP=0+1 cells.

PHYNCOUNT1[1:0]

The PHYNCOUNT1[1:0] bits determine how the per-PHY Non-Compliant Cell Count #1 of the PHY Policing RAM is defined:

PHYNCOUNT1[1:0]	Definition
00	Non-compliant CLP=0 cells.
01	Non-compliant CLP=0+1 cells.
10	Discarded CLP=0 cells.

11	Discarded CLP=0+1 cells.

PHYNCOUNT2[1:0]

The PHYNCOUNT2[1:0] bits determine how the per-PHY Non-Compliant Cell Count #2 of the PHY Policing RAM is defined:

PHYNCOUNT2[1:0]	Definition
00	Non-compliant CLP=0 cells.
01	Non-compliant CLP=0+1 cells.
10	Discarded CLP=0 cells.
11	Discarded CLP=0+1 cells.

PHYNCOUNT3[1:0]:

The PHYNCOUNT3[1:0] bits determine how the per-PHY Non-Compliant Cell Count #3 of the PHY Policing RAM is defined:

PHYNCOUNT3[1:0]	Definition
00	Non-compliant CLP=0 cells.
01	Non-compliant CLP=0+1 cells.
10	Tagged CLP=0 cells which are not discarded.
11	Discarded CLP=0+1 cells.

Register 0x211: Ingress Performance Monitoring RAM Record Address

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7	R/W	PM Bank	0
6	R/W	PM Addr[6]	0
5	R/W	PM Addr[5]	0
4	R/W	PM Addr[4]	0
3	R/W	PM Addr[3]	0
2	R/W	PM Addr[2]	0
1	R/W	PM Addr[1]	0
0	R/W	PM Addr[0]	0

PM Bank:

The PM Bank bit determines which bank of PM data will be accessed. If this bit is logic 0, the PM Addr[6:0] field will access the desired data for the first bank of internal PM RAM. If this bit is logic 1, the PM Addr[6:0] field will access the desired data for the second bank of internal PM Ram.

PM Addr[6:0]:

This field specifies which of the 128 possible PM Sessions to access. The PM Bank bit determines whether Bank 1 or Bank 2 of a particular PM Address will be selected.

Register 0x212: Ingress Performance Monitoring RAM Word Select and Access Control

Bit	Type	Function	Default
15	R/W	RWB	0
14	R	BUSY	X
13	R/W	CLRONRD	0
12	R/W	WM[9]	0
11	R/W	WM[8]	0
10	R/W	WM[7]	0
9	R/W	WM[6]	0
8	R/W	WM[5]	0
7	R/W	WM[4]	0
6	R/W	WM[3]	0
5	R/W	WM[2]	0
4	R/W	WM[1]	0
3	R/W	WM[0]	0
2	R/W	PM Row[2]	0
1	R/W	PM Row[1]	0
0	R/W	PM Row[0]	0

PM Row[2:0]:

This field determines which row of internal PM data will be accessed. If the first row is desired (i.e. Row 0), the setting this field to PM Row[2:0] = '000' will access this row. If the eighth row is desired (i.e. Row 7), then setting this field to PM Row[2:0]='111' will access this row.

WM[9:0]:

The write mask (WM[7:0]) is used to select which bytes of the Ingress PM Internal RAM data will be written during a write operation. If any of WM[9:0] are '1' during a write operation, the ICP performs a read-write-back operation when a write is requested. WM[9] controls the mask to bits [79:72] of the Ingress PM RAM Data, and WM[0] controls the mask to bits [7:0] of the Ingress PM RAM Data. This allows the ICP to write to selected fields in a row of the Ingress PM Ram Data.

CLRONRD:

If CLRONRD is logic 1, after a read access of rows PMADDR[2:0] = 011,100,101,110, or 111 of the Ingress PM RAM is specified in this register, a clearing write of the row will be initiated. The Fwd SECBC (running count) and Bwd SECBC (copied) will be preserved.

If CLRONRD is logic 0, no write back to clear the data bits is initiated.

BUSY:

The BUSY bit is high while a Microprocessor initiated access request to the Ingress PM RAM data is pending the BUSY bit is deasserted only after all the access required has been completed. This register should be polled until the BUSY bit goes low before another microprocessor access request is initiated. A microprocessor access request is typically completed within 35 ISYSCLK cycles

RWB:

The RWB bit selects the operation to be performed on the addressed Ingress PM Ram Data: when RWB is set to a logic 1, a read from the internal SRAM is requested; when RWB is set to a logic 0, a write to the internal SRAM is requested.

Register 0x213: Ingress Performance Monitoring RAM Data Word 0 (LSW)

Bit	Type	Function	Default
15	R/W	PMData[15]	0
14	R/W	PMData[14]	0
13	R/W	PMData[13]	0
12	R/W	PMData[12]	0
11	R/W	PMData[11]	0
10	R/W	PMData[10]	0
9	R/W	PMData[9]	0
8	R/W	PMData[8]	0
7	R/W	PMData[7]	0
6	R/W	PMData[6]	0
5	R/W	PMData[5]	0
4	R/W	PMData[4]	0
3	R/W	PMData[3]	0
2	R/W	PMData[2]	0
1	R/W	PMData[1]	0
0	R/W	PMData[0]	0

This register contains either the data to be written into the Ingress PM RAM Data Word 0 (LSW) or the data read from the internal Ingress PM RAM when a read request has been completed. If data is to be written to Ingress PM RAM Data, the LSW word be written to this register before the Ingress PM RAM Select and Access Control register are written. If data is to be read from the Ingress PM RAM, this register contains the data from Word 0 (LSW) after the internal SRAM access is completed.

Register 0x214: Ingress Performance Monitoring RAM Data Word 1

Bit	Type	Function	Default
15	R/W	PMData[31]	0
14	R/W	PMData[30]	0
13	R/W	PMData[29]	0
12	R/W	PMData[28]	0
11	R/W	PMData[27]	0
10	R/W	PMData[26]	0
9	R/W	PMData[25]	0
8	R/W	PMData[24]	0
7	R/W	PMData[23]	0
6	R/W	PMData[22]	0
5	R/W	PMData[21]	0
4	R/W	PMData[20]	0
3	R/W	PMData[19]	0
2	R/W	PMData[18]	0
1	R/W	PMData[17]	0
0	R/W	PMData[16]	0

This register contains either the data to be written into the Ingress PM RAM Data Word 1 or the data read from the internal Ingress PM RAM when a read request has been completed. If data is to be written to Ingress PM RAM Data Word 1, the word must be written to this register before the Ingress PM RAM Select and Access Control register are written. If data is to be read from the Ingress PM RAM this register contains the data from Word 1 after the internal SRAM access is completed.

Register 0x215: Ingress Performance Monitoring RAM Data Word 2

Bit	Type	Function	Default
15	R/W	PMData[47]	0
14	R/W	PMData[46]	0
13	R/W	PMData[45]	0
12	R/W	PMData[44]	0
11	R/W	PMData[43]	0
10	R/W	PMData[42]	0
9	R/W	PMData[41]	0
8	R/W	PMData[40]	0
7	R/W	PMData[39]	0
6	R/W	PMData[38]	0
5	R/W	PMData[37]	0
4	R/W	PMData[36]	0
3	R/W	PMData[35]	0
2	R/W	PMData[34]	0
1	R/W	PMData[33]	0
0	R/W	PMData[32]	0

This register contains either the data to be written into the Ingress PM RAM Data Word 2 or the data read from the internal Ingress PM RAM when a read request has been completed. If data is to be written to Ingress PM RAM Data Word 2, the word must be written to this register before the Ingress PM RAM Select and Access Control register are written. If data is to be read from the Ingress PM RAM this register contains the data from Word 2 after the internal SRAM access is completed.

Register 0x216: Ingress Performance Monitoring RAM Data Word 3

Bit	Type	Function	Default
15	R/W	PMData[63]	0
14	R/W	PMData[62]	0
13	R/W	PMData[61]	0
12	R/W	PMData[60]	0
11	R/W	PMData[59]	0
10	R/W	PMData[58]	0
9	R/W	PMData[57]	0
8	R/W	PMData[56]	0
7	R/W	PMData[55]	0
6	R/W	PMData[54]	0
5	R/W	PMData[53]	0
4	R/W	PMData[52]	0
3	R/W	PMData[51]	0
2	R/W	PMData[50]	0
1	R/W	PMData[49]	0
0	R/W	PMData[48]	0

This register contains either the data to be written into the Ingress PM RAM Data Word 3 or the data read from the internal Ingress PM RAM when a read request has been completed. If data is to be written to Ingress PM RAM Data Word 3, the word must be written to this register before the Ingress PM RAM Select and Access Control register are written. If data is to be read from the Ingress PM RAM this register contains the data from Word 3 after the internal SRAM access is completed.

Register 0x217: Ingress Performance Monitoring RAM Data Word 4 (MSW)

Bit	Type	Function	Default
15	R/W	PMData[79]	0
14	R/W	PMData[78]	0
13	R/W	PMData[77]	0
12	R/W	PMData[76]	0
11	R/W	PMData[75]	0
10	R/W	PMData[74]	0
9	R/W	PMData[73]	0
8	R/W	PMData[72]	0
7	R/W	PMData[71]	0
6	R/W	PMData[70]	0
5	R/W	PMData[69]	0
4	R/W	PMData[68]	0
3	R/W	PMData[67]	0
2	R/W	PMData[66]	0
1	R/W	PMData[65]	0
0	R/W	PMData[64]	0

This register contains either the data to be written into the Ingress PM RAM Data Word 4 (MSW) or the data read from the internal Ingress PM RAM when a read request has been completed. If data is to be written to Ingress PM RAM Data Word 4, the word must be written to this register before the Ingress PM RAM Select and Access Control register are written. If data is to be read from the Ingress PM RAM this register contains the data from Word 4 after the internal SRAM access is completed.

Register 0x218: Ingress Performance Monitoring Threshold A1

Bit	Type	Function	Default
15	R/W	MERROR[3]	0
14	R/W	MERROR[2]	0
13	R/W	MERROR[1]	0
12	R/W	MERROR[0]	0
11	R/W	MMISINS[11]	0
10	R/W	MMISINS[10]	0
9	R/W	MMISINS[9]	0
8	R/W	MMISINS[8]	0
7	R/W	MMISINS[7]	0
6	R/W	MMISINS[6]	0
5	R/W	MMISINS[5]	0
4	R/W	MMISINS[4]	0
3	R/W	MMISINS[3]	0
2	R/W	MMISINS[2]	0
1	R/W	MMISINS[1]	0
0	R/W	MMISINS[0]	0

This is the first of four Threshold Registers. These threshold registers are addressed by the Threshold_Select[1:0] field of the PM Configuration field of the Ingress PM RAM data. Note, these thresholds apply to both Forward Monitoring and Backward Reporting cells.

MMISINS[11:0]:

MMISINS[11:0] is the binary representation of the threshold of misinserted cells per Performance Monitoring block required to declare a Severely Errored Cell Block of Misinserted Cells (SECB Misinserted). The number of misinserted cells is not counted if this threshold is exceeded (the SECB Misinserted counter will be incremented instead). If MMISINS[11:0] is a binary zero, SECB Misinserted is not declared as a result of excessive misinserted cells.

MERROR[3:0]:

MERROR[3:0] is the binary representation of the threshold of BIP-16 violations per Performance Monitoring block required to declare a Severely Errored Cell Block for Errored cells (SECB Errored). Errored cell counts are not accumulated if this threshold is exceeded (the SECB Errored count will be incremented instead). If MERROR[3:0] is a binary zero, the SECB Errored cell count is not declared as a result of excessive BIP-16 violations.

Register 0x219: Ingress Performance Monitoring Threshold A2

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11	R/W	MLOST[11]	0
10	R/W	MLOST[10]	0
9	R/W	MLOST[9]	0
8	R/W	MLOST[8]	0
7	R/W	MLOST[7]	0
6	R/W	MLOST[6]	0
5	R/W	MLOST[5]	0
4	R/W	MLOST[4]	0
3	R/W	MLOST[3]	0
2	R/W	MLOST[2]	0
1	R/W	MLOST[1]	0
0	R/W	MLOST[0]	0

This is the first of four Threshold Registers. These threshold registers are addressed by the Threshold_Select[1:0] field of the PM Configuration field of the Ingress PM RAM data.

The threshold given below applies to both received Forward Monitoring and Backward Reporting cells.

MLOST[11:0]:

MLOST[11:0] is the binary representation of the threshold of lost cells per Performance Monitoring block required to declare a Severely Errored Cell Block of Lost Cells (SECB Lost). The number of lost cells is not counted if this threshold is exceeded (the SECB Lost counter will be incremented instead). If MLOST[11:0] is a binary zero, SECB Lost is not declared as a result of excessive lost cells.

Register 0x21A: Ingress Performance Monitoring Threshold B1

Register 0x21B: Ingress Performance Monitoring Threshold B2

Register 0x21C: Ingress Performance Monitoring Threshold C1

Register 0x21D: Ingress Performance Monitoring Threshold C2

Register 0x21E: Ingress Performance Monitoring Threshold D1

Register 0x21F: Ingress Performance Monitoring Threshold D2

Register 0x220: Ingress Cell Processor Routing Configuration

Bit	Type	Function	Default
15	R/W	CRC10toUP	0
14	R/W	DROPCRC10	0
13	R/W	ACTDEtoOCIF	0
12	R/W	SYSMANtoOCIF	0
11	R/W	DROPINVPTIVCI	0
10	R/W	DROPBRM	0
9	R/W	DROPFRM	0
8	R/W	BADVCtoUP	0
7	R/W	BRMtoUP	0
6	R/W	FRMtoUP	0
5	R/W	ACTDEtoUP	0
4	R/W	INVPTIVCItoUP	0
3	R/W	UNDEFtoUP	0
2	R/W	SYSMANtoUP	0
1	R/W	DROPCRCERM	0
0	R/W	PMtoUP	0

PMtoUP:

If this bit is logic 1, all Performance Monitoring OAM cells are copied to the Ingress Microprocessor Cell Interface at flow end-points. Regardless of the state of this bit, all PM OAM cells are output to the Ingress Output Cell Interface if the ATLAS is not an end-point for that Ingress connection.

DROPCRCERM:

If this bit is logic 1, all Forward and Backward RM cells with an incorrect CRC-10 are discarded. If this bit is logic 0, then all Forward and Backward RM cells are output to the Ingress Output Cell Interface regardless of whether their CRC-10 is correct or not.

SYSMANtoUP:

If this bit is logic 1, all System Management OAM cells are copied to the Ingress Microprocessor Cell Interface at flow end-points. Regardless of the state of this bit, all System Management OAM cells are output to the Ingress Output Cell Interface if the ATLAS is not an end-point for that Ingress connection.

UNDEFtoUP:

If the UNDEFtoUP bit is logic 1, all OAM cells with an undefined OAM Type or Function Type value are copied to the Ingress Microprocessor Cell Interface at flow end-points. Regardless of the state of this bit, all OAM cells with an undefined OAM Type or Function Type value are output to the Ingress Output Cell Interface if the ATLAS is not an end point for that Ingress connection.

INVPTIVCItoUP:

If the INVPTIVCItoUP bit is logic 1, all F5 (VCC) cells with an invalid PTI field (PTI=111) and all F4 (VPC) cells with an invalid VCI field (VCI 7 through 15) are copied to the Ingress Microprocessor Cell Interface. The DROPINVPTIVCI register bit determines whether cells with invalid PTI or VCI fields are passed to the Ingress Output Cell Interface.

ACTDEtoUP:

If the ACTDEtoUP bit is logic 1, all activate/deactivate OAM cells are copied to the Ingress Microprocessor Cell Interface at flow end-points. If the ATLAS is not a flow end-point for the connection, the Activate/Deactivate cells are not copied to the Ingress Microprocessor Cell Interface Regardless of the state of this bit, all activate/deactivate cells are passed to the Ingress Output Cell Interface if the ATLAS is not an end point for that Ingress connection.

FRMtoUP:

If the FRMtoUP bit is logic 1, all forward RM cells are copied to the Ingress Microprocessor Cell Interface. Forward RM cells are identified by a zero in the DIR bit position of the payload in conjunction with PTI=110 for VC-RM cells and by VCI=6 for VP-RM cells. If the VPRMSEL register bit of the Ingress Search Engine configuration register is logic 1, VP-RM cells are further qualified by PTI=110.

BRMtoUP:

If the BRMtoUP bit is logic 1, all Backward RM cells are copied to the Ingress Microprocessor Cell Interface. Backward RM cells are identified by a one in the DIR bit position of the payload in conjunction with PTI=110 for VC-RM cells and VCI=6 for VP-RM cells. If the VPRMSEL register bit of the Ingress Search Engine configuration register is logic 1, VP-RM cells are further qualified by PTI=110.

BADVCtoUP:

If the BADVCtoUP bit is logic 1, all cells with an unprovisioned VPI/VCI are routed to the Ingress Microprocessor Cell Interface. If this bit is logic 0, those cells are discarded by the ATLAS.

DROPFRM:

If the DROPFRM bit is logic 1, all forward RM cells are dropped (i.e. not output to the Ingress Output Cell Interface). Regardless of the state of this bit, forward RM cells can be routed to the Ingress Microprocessor Cell Interface if the FRMtoUP bit is set.

DROPBRM:

If the DROPBRM bit is logic 1, all backward RM cells are dropped (i.e. not output to the Ingress Output Cell Interface). Regardless of the state of this bit, backward RM cells can be routed to the Ingress Microprocessor Cell Interface if the BRMtoUP bit is set.

DROPINVPTIVCI:

If this bit is logic 1, all F4 (VCC) cells with PTI=111 and all F5 (VPC) cells with a VCI of 7 through 15 are not routed to the Ingress Output Cell Interface. If DROPINVPTIVCI is logic 0, these cells are passed transparently.

SYSMANtoOCIF:

If the SYSMANtoOCIF bit is logic 1, all System Management cells are routed to the Ingress Output Cell Interface. If the SYSMANtoOCIF is logic 0, then at flow end-points, all System Management cells are dropped. Regardless of the state of this bit, all System Management cells are routed to the Ingress Output Cell Interface if the ATLAS is not a flow end-point for that connection.

ACTDEtoOCIF:

If the ACTDEtoOCIF bit is logic 1, all Activate/Deactivate cells are routed to the Ingress Output Cell Interface. If ACTDEtoOCIF is logic 0, then at flow end points, all Activate/Deactivate cells are dropped. Regardless of the state of this bit, all Activate/Deactivate cells are routed to the Ingress Output Cell Interface if the ATLAS is not a flow end point for that Ingress connection.

DROPCRC10:

If the DROPCRC10 bit is logic 1, all OAM cells with an errored CRC-10 are dropped (i.e. not routed to the Ingress Output Cell Interface). Regardless of the state of this bit, if the ATLAS is a flow end-point, all OAM cells with an errored CRC-10 are dropped.

CRC10toUP:

If the CRC10toUP bit is logic 1, all OAM cells or RM cells with an errored CRC-10 are copied to the Ingress Microprocessor Cell Interface. Regardless of the state of this bit, the DROPCRC10 bit determines whether or not the ATLAS will route errored OAM cells to the Ingress Output Cell Interface.

Register 0x221: Ingress OAM Cell Generation Configuration

Bit	Type	Function	Default
15	R/W	AISCCP[15]	0
14	R/W	AISCCP[14]	0
13	R/W	AISCCP[13]	0
12	R/W	AISCCP[12]	0
11	R/W	AISCCP[11]	0
10	R/W	AISCCP[10]	0
9	R/W	AISCCP[9]	0
8	R/W	AISCCP[8]	0
7	R/W	AISCCP[7]	0
6	R/W	AISCCP[6]	0
5	R/W	AISCCP[5]	1
4	R/W	AISCCP[4]	0
3	R/W	AISCCP[3]	0
2	R/W	AISCCP[2]	0
1	R/W	AISCCP[1]	0
0	R/W	AISCCP[0]	0

AISCCP[15:0]:

AISCCP[15:0] sets the number of cell intervals between generation of AIS or CC cells into the Ingress Output Cell Interface. This is to prevent an excessive number of AIS/CC cells to be generated back-to-back by the ATLAS. A cell interval is defined to be 32 (i.e. assuming cells to be of 64 bytes) ISYSCLK clocks. The minimum rate of transfer is 1 in 65535 cell intervals. When AISCCP[15:0] = 0x0000 back-to-back generation of AIS/CC cells into the Ingress Output Cell Interface is possible. The default is set to 1 in 32 cell intervals.

Register 0x222: Ingress per-PHY AIS Cell Generation Control 1

Bit	Type	Function	Default
15	R/W	AIS15	0
14	R/W	AIS14	0
13	R/W	AIS13	0
12	R/W	AIS12	0
11	R/W	AIS11	0
10	R/W	AIS10	0
9	R/W	AIS9	0
8	R/W	AIS8	0
7	R/W	AIS7	0
6	R/W	AIS6	0
5	R/W	AIS5	0
4	R/W	AIS4	0
3	R/W	AIS3	0
2	R/W	AIS2	0
1	R/W	AIS1	0
0	R/W	AIS0	0

AISx:

AISx enables the generation of AIS cells for PHY x, where x is from 0 to 15. If AISx is a logic 1, end-to-end AIS cells are generated to the Ingress Output Cell Interface once per second (nominally) for every connection associated with PHYx which is not an end-to-end point. If AISx is a logic 0, AIS cell generation on a per-PHY basis is disabled. The PHYID[4:0] field in the Ingress VC Table identifies a connection's associated PHY.

Register 0x223: Ingress per-PHY AIS Cell Generation Control 2

Bit	Type	Function	Default
15	R/W	AIS31	0
14	R/W	AIS30	0
13	R/W	AIS29	0
12	R/W	AIS28	0
11	R/W	AIS27	0
10	R/W	AIS26	0
9	R/W	AIS25	0
8	R/W	AIS24	0
7	R/W	AIS23	0
6	R/W	AIS22	0
5	R/W	AIS21	0
4	R/W	AIS20	0
3	R/W	AIS19	0
2	R/W	AIS18	0
1	R/W	AIS17	0
0	R/W	AIS16	0

AISx:

AISx enables the generation of AIS cells for PHY x, where x is from 16 to 31. If AISx is a logic 1, end-to-end AIS cells are generated to the Ingress Output Cell Interface once per second (nominally) for every connection associated with PHYx which is not an end-to-end point. If AISx is a logic 0, AIS cell generation on a per-PHY basis is disabled. The PHYID[4:0] field in the Ingress VC Table identifies a connection's associated PHY.

Register 0x224: Ingress per-PHY RDI Cell Generation Control 1

Bit	Type	Function	Default
15	R/W	RDI15	0
14	R/W	RDI14	0
13	R/W	RDI13	0
12	R/W	RDI12	0
11	R/W	RDI11	0
10	R/W	RDI10	0
9	R/W	RDI9	0
8	R/W	RDI8	0
7	R/W	RDI7	0
6	R/W	RDI6	0
5	R/W	RDI5	0
4	R/W	RDI4	0
3	R/W	RDI3	0
2	R/W	RDI2	0
1	R/W	RDI1	0
0	R/W	RDI0	0

RDIx:

RDIx enables the generation of RDI cells on a per-PHY basis for PHY x, where x is from 0 to 15. If RDIx is a logic 1, RDI cells for every connection (which is configured as an end-to-end point) associated with PHY x, are generated once per second (nominally) to the Egress Output Cell Interface (through the Egress Backward OAM Cell Interface). If RDIx is a logic 0, RDI cell generation on a per-PHY basis is disabled. The PHYID[4:0] field in the Ingress VC Table identifies a connection's associated PHY.

If RDIx is logic 1, only end-to-end RDI cells are generated.

Register 0x225: Ingress per-PHY RDI Cell Generation Control 2

Bit	Type	Function	Default
15	R/W	RDI31	0
14	R/W	RDI30	0
13	R/W	RDI29	0
12	R/W	RDI28	0
11	R/W	RDI27	0
10	R/W	RDI26	0
9	R/W	RDI25	0
8	R/W	RDI24	0
7	R/W	RDI23	0
6	R/W	RDI22	0
5	R/W	RDI21	0
4	R/W	RDI20	0
3	R/W	RDI19	0
2	R/W	RDI18	0
1	R/W	RDI17	0
0	R/W	RDI16	0

RDIx:

RDIx enables the generation of RDI cells on a per-PHY basis for PHY x, where x is from 16 to 31. If RDIx is a logic 1, RDI cells for every connection (which is configured as an end-to-end point) associated with PHY x, are generated once per second (nominally) to the Egress Output Cell Interface (through the Egress Backward OAM Cell Interface). If RDIx is a logic 0, RDI cell generation on a per-PHY basis is disabled. The PHYID[4:0] field in the Ingress VC Table identifies a connection's associated PHY.

If RDIx is logic 1, only end-to-end RDI cells are generated.

Register 0x226: Ingress OAM Defect Type0 and 1

Bit	Type	Function	Default
15	R/W	DT2[7]	0
14	R/W	DT2[6]	1
13	R/W	DT2[5]	1
12	R/W	DT2[4]	0
11	R/W	DT2[3]	1
10	R/W	DT2[2]	0
9	R/W	DT2[1]	1
8	R/W	DT2[0]	0
7	R/W	DT1[7]	0
6	R/W	DT1[6]	1
5	R/W	DT1[5]	1
4	R/W	DT1[4]	0
3	R/W	DT1[3]	1
2	R/W	DT1[2]	0
1	R/W	DT1[1]	1
0	R/W	DT1[0]	0

DT1[7:0] and DT2[7:0]:

This register contains the Defect Type data that is inserted into generated AIS cells. The Defect Type field is inserted into generated RDI cells when the Send_RDI_Segment or Send_RDI_End_to_End bits are logic 1 (i.e. forced insertion of RDI cells rather than generation of RDI cells as a result of AUTORDI) or when an RDI cell is generated as a result of the CC_RDI function. The selection DT0-DT15 is selected on a per-VC basis, controlled by the Defect Type[3:0] bits in the Ingress VC Table.

Register 0x227: Ingress OAM Defect Type 2 and 3

Register 0x228: Ingress OAM Defect Type 4 and 5

Register 0x229: Ingress OAM Defect Type 6 and 7

Register 0x22A: Ingress OAM Defect Type 8 and 9

Register 0x22B: Ingress OAM Defect Type 10 and 11

Register 0x22C: Ingress OAM Defect Type 12 and 13

Register 0x22D: Ingress OAM Defect Type 14 and 15

Register 0x22E: Ingress OAM Defect Location Octets 0 & 1

Bit	Type	Function	Default
15	R/W	DL[15]	0
14	R/W	DL[14]	1
13	R/W	DL[13]	1
12	R/W	DL[12]	0
11	R/W	DL[11]	1
10	R/W	DL[10]	0
9	R/W	DL[9]	1
8	R/W	DL[8]	0
7	R/W	DL[7]	0
6	R/W	DL[6]	1
5	R/W	DL[5]	1
4	R/W	DL[4]	0
3	R/W	DL[3]	1
2	R/W	DL[2]	0
1	R/W	DL[1]	1
0	R/W	DL[0]	0

DL[15:0]:

This register contains the Defect Location data LSB which is inserted into generated AIS cells. The Defect Location is also inserted into RDI cells when the Send_RDI_Segment or Send_RDI_End_to_End register bits are asserted (i.e. forced insertion of RDI cells rather than generation of RDI cells as a -result of AUTORDI) and when RDI cells are generated as a result of the CC_RDI process. This is the least significant 16-bits of the Defect Location field. Note the Defect Location defaults to 6A6A6A6A6A6A6A6A6A6A6A6A6A6A6A6A hex.

Register 0x22F: Ingress Defect Location Octets 2 & 3

Register 0x230: Ingress Defect Location Octets 4 & 5

Register 0x231: Ingress Defect Location Octets 6 & 7

Register 0x232: Ingress Defect Location Octets 8 & 9

Register 0x233: Ingress Defect Location Octets 10 & 11

Register 0x234: Ingress Defect Location Octets 12 & 13

Register 0x235: Ingress Defect Location Octets 14 & 15

Register 0x236: Ingress Cell Counting Configuration 1

Bit	Type	Function	Default
15	R/W	COUNT2[7]	0
14	R/W	COUNT2[6]	0
13	R/W	COUNT2[5]	0
12	R/W	COUNT2[4]	0
11	R/W	COUNT2[3]	0
10	R/W	COUNT2[2]	0
9	R/W	COUNT2[1]	0
8	R/W	COUNT2[0]	0
7	R/W	COUNT1[7]	0
6	R/W	COUNT1[6]	0
5	R/W	COUNT1[5]	0
4	R/W	COUNT1[4]	0
3	R/W	COUNT1[3]	0
2	R/W	COUNT1[2]	0
1	R/W	COUNT1[1]	0
0	R/W	COUNT1[0]	0

This register is addressed when the Count_Type bit of the Ingress VC Table is set to logic 0.

COUNT1[7:0]:

The COUNT1[7:0] controls which cells the Ingress Cell Processor includes in its first per-connection 32-bit cell count. The COUNT1[7:0] field is programmed as follows:

Cell Type	Cells with PTI=111 (F5 only) and VCI = 7 to 15 (F4 only)		RM Cells		OAM Cells		User Cells	
CLP Bit	0	1	0	1	0	1	0	1
Register Bit	COUNT1 [0]	COUNT1 [1]	COUNT1 [2]	COUNT1 [3]	COUNT1 [4]	COUNT1 [5]	COUNT1 [6]	COUNT1 [7]

A logic 1 written to any of the COUNT1[7:0] bits enables counting on that particular stream. For example, to enable counting of CLP=0+1 User and OAM cells only, the register configuration would be COUNT1[7:0] = 0xF0. If COUNT1[7:0] = 0x00, the first generic cell count for all connections is disabled.

COUNT2[7:0]:

The COUNT2[7:0] register bits controls which cells the Ingress Cell Processor includes in its second per-connection 32-bit cell count. The COUNT2[7:0] field is programmed exactly the same as the COUNT1[7:0] field.

Register 0x237: Ingress Cell Counting Configuration 2

Bit	Type	Function	Default
15	R/W	COUNT2[7]	0
14	R/W	COUNT2[6]	0
13	R/W	COUNT2[5]	0
12	R/W	COUNT2[4]	0
11	R/W	COUNT2[3]	0
10	R/W	COUNT2[2]	0
9	R/W	COUNT2[1]	0
8	R/W	COUNT2[0]	0
7	R/W	COUNT1[7]	0
6	R/W	COUNT1[6]	0
5	R/W	COUNT1[5]	0
4	R/W	COUNT1[4]	0
3	R/W	COUNT1[3]	0
2	R/W	COUNT1[2]	0
1	R/W	COUNT1[1]	0
0	R/W	COUNT1[0]	0

This register is addressed when the COUNT bit of the Ingress VC Table is set to logic 1.

COUNT1[7:0]:

The COUNT1[7:0] controls which cells the Ingress Cell Processor includes in its first per-connection 32-bit cell count. The COUNT1[7:0] field is programmed as follows:

Cell Type	Cells with PTI=111 (F5) or VCI=7 to 15 (F4) (See note 1)		RM Cells		OAM Cells		User Cells (see note 2)	
CLP Bit	0	1	0	1	0	1	0	1
Register Bit	COUNT1 [0]	COUNT1 [1]	COUNT1 [2]	COUNT1 [3]	COUNT1 [4]	COUNT1 [5]	COUNT1 [6]	COUNT1 [7]

A logic 1 written to any of the COUNT1[7:0] bits enables counting on that particular stream. For example, to enable counting of CLP=0+1 User and OAM cells only, the register configuration would be COUNT1[7:0] = 0xF0. If COUNT1[7:0] = 0x00, the first generic cell count for all connections is disabled.

Note 1: Cells in this category which are declared as user cells in the F4 PM Flow VCI Map or F5 PM Flow PTI map are counted as user cells rather than in this category. Physical Layer cells are always counted in this category.
Note 2: User cells includes cells from any PTI/VCI which is marked as a user cell in the F4 PM Flow VCI Map or F5 PM Flow PTI map, other than F4 RM cells for F4 connections or F5 RM cells for F5 connections. Cells with VCI=1, 2, or 5 are always counted in this category.

COUNT2[7:0]:

The COUNT2[7:0] register bits controls which cells the Ingress Cell Processor includes in its second per-connection 32-bit cell count. The COUNT2[7:0] field is programmed in exactly the manner as the COUNT1[7:0] field.

Register 0x238: Ingress Cell Processor Configuration 2

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10	R/W	IAISCOPY	0
9	R/W	F4SAISF5EAIS	0
8	R/W	F4SAISF5ERDI	0
7	R/W	F4EAISF5EAIS	0
6	R/W	F4EAISF5SRDI	0
5	R/W	ForceCC	0
4	R/W	Alternate_Count	0
3	R/W	BCIFP1P2	0
2	R/W	MFL	0
1	R/W	BCIFHECUDF	0
0	R/W	CounterWrap	0

CounterWrap:

If CounterWrap is logic 1, the per-connection Ingress VC Table counts do not saturate at all ones, rather, they rollover. If CounterWrap is logic 0, these counts saturate at all ones. It is the responsibility of the management software to ensure the per-connection counts are polled often enough to avoid saturation or rollover.

BCIFHECUDF:

If this bit is logic 1, the HEC field of the Output Header word and the UDF field of the Ingress VC Table are used to overwrite the HEC/UDF fields of generated RDI and Backward Monitoring PM cells which are looped inside the ATLAS. If both BCIFHECUDF and BCIFP1P2 are logic 0, the Ingress VC Table Record Address overwrites the HEC/UDF fields of the generated RDI and Backward Monitoring PM cells.

MFL

The Maximum Frame Length (MFL) bit determines whether or not the MFL conformance test is performed when the Guaranteed Frame Rate (GFR) policing is enabled. If MFL is logic 1,

the MFL test is used, and the Maximum Frame Length field of the Ingress VC Table (at ISA[19:16]=1010) is used to denote the maximum permissible frame length. If MFL is logic 0, the Maximum Frame Length conformance test is performed using the Maximum Frame Length Count value programmed in the Maximum Frame Length Count register, and no physical RAM need be populated for the Maximum Frame Length field. If the Maximum Frame Length field of the Ingress VC Table is set to all zeros, this disables the MFL conformance test when MFL is a logic 1. If MFL is a logic 0, the MFL conformance test can be disabled by setting the Maximum Frame Length Count (MFLC[10:0]) to all ones.

BCIFP1P2:

If this bit is logic 1 and BCIFHECUDF is logic 0, the Prepo1 and Prepo2 fields of the Ingress VC Table are used to overwrite the HEC/UDF fields of generated RDI and Backward Reporting PM cells sent to the Backward OAM Cell Interface. BCIFHECUDF takes precedence over BCIFP1P2. If both BCIFHECUDF and BCIFP1P2 are logic 0, the Ingress VC Table Record Address overwrites the HEC/UDF fields of the generated RDI and Backward Reporting PM cells.

Alternate_Count:

The Alternate_Count bit determines at which row, the per-connection cell counts in the Ingress VC Table are incremented. If the Alternate_Count bit is logic 0, the ATLAS maintains the per-connection cell counts for the Ingress VC Table at ISA[19:16]=0110. If the Alternate_Count is logic 1, the counts are maintained at ISA[19:16]=1001. It is the responsibility of the management software to ensure the count locations are cleared before the ATLAS begins incrementing at these locations.

ForceCC:

The ForceCC bit controls whether or not the insertion of CC cells is dependent on the user cell traffic. If ForceCC is logic 0, CC cells are only generated if the CC_Activate_Segment or CC_Activate_End_to_End per-connection bits are logic 1 and if no user cells have been transmitted within one second (nominal). If ForceCC is logic 1, CC cells are generated at a rate of once per second (nominal) if the CC_Activate_Segment or CC_Activate_End_to_End bits are logic 1.

F4EAISF5SRDI:

The F4EAISF5SRDI register bit controls the generation of F5 Segment RDI cells upon the reception of an F4 End-to-End AIS cell. When this bit is logic 1, a segment VC-RDI cell will be generated when an end-to-end VPC-AIS cell is terminated at a VPC end-to-end point and an associated VCC segment end-point is switched from that VPC. If this bit is logic 0, a segment VC-RDI cell will not be generated in this circumstance.

F4EAISF5EAIS:

The F4EAISF5EAIS register bit controls the generation of F5 End-to-End AIS cells upon the reception of an F4 End-to-End AIS cell. When this bit is logic 1, an end-to-end VC-AIS cell will be generated when an end-to-end VPC-AIS cell is terminated at a VPC end-to-end point, and an associated VCC segment end-point is switched from that VPC. If this bit is logic 0, an end-to-end VC-AIS cell will not be generated in this circumstance.

F4SAISF5ERDI:

The F4SAISF5ERDI register bit controls the generation of F5 end-to-end RDI cells upon the reception of an F4 segment AIS cell. If this bit is logic 1, an end-to-end VC-RDI cell will be generated when a segment VPC-AIS cell is terminated at a VPC segment end-point. If this bit is logic 0, an end-to-end VC-RDI cell will not be generated in this circumstance.

F4SAISF5EAIS:

The F4SAISF5EAIS register bit controls the generation of F5 end-to-end AIS cells upon the reception of an F4 segment AIS cell. If this bit is logic 1, an end-to-end VC-AIS cell will be generated when a segment VPC-AIS cell is terminated at a VPC segment end-point. If this bit is logic 0, an end-to-end AIS cell will not be generated in this circumstance.

IAISCOPY:

If the IAISCOPY register bit is logic 1, the ATLAS copies the Defect Location and Defect Type fields of all received segment and end-to-end AIS cells to the Ingress VC Table. These fields are used when segment or end-to-end RDI cells are generated as a result of the AUTORDI process. If IAISCOPY is logic 0, then the fields are not copied to the Ingress VC Table, and RAM need not be populated for these locations. If these rows are not provisioned, then the RDI cells will contain the local defect type selected by the Defect_Type field in the configuration field of the Ingress VC Table, and will contain the default 0x6A6A pattern in the defect location field.

Register 0x239: Maximum Frame Length Count Register

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10	R/W	MFLC[10]	1
9	R/W	MFLC[9]	1
8	R/W	MFLC[8]	1
7	R/W	MFLC[7]	1
6	R/W	MFLC[6]	1
5	R/W	MFLC[5]	1
4	R/W	MFLC[4]	1
3	R/W	MFLC[3]	1
2	R/W	MFLC[2]	1
1	R/W	MFLC[1]	1
0	R/W	MFLC[0]	1

MFLC[10:0]:

The Maximum Frame Length Count, MFLC[10:0] is provided as an alternative to the Maximum Frame Length field of the Ingress VC Table. If the MFL bit of the Ingress Cell Processor Configuration 2 register is set to logic 0, the MFLC[10:0] is used in place of the Maximum Frame Length field when performing the MFL Conformance Test of the Generic Frame Rate policing. If the MFL bit is set to logic 0, the MFL Conformance test can be disabled by setting the MFLC[10:0] to all ones.

Register 0x23A: Ingress VC Table Change of Connection Status Data (LSW)

Bit	Type	Function	Default
15	R	COSDATA[15]	X
14	R	COSDATA[14]	X
13	R	COSDATA[13]	X
12	R	COSDATA[12]	X
11	R	COSDATA[11]	X
10	R	COSDATA[10]	X
9	R	COSDATA[9]	X
8	R	COSDATA[8]	X
7	R	COSDATA[7]	X
6	R	COSDATA[6]	X
5	R	COSDATA[5]	X
4	R	COSDATA[4]	X
3	R	COSDATA[3]	X
2	R	COSDATA[2]	X
1	R	COSDATA[1]	X
0	R	COSDATA[0]	X

COSDATA[15:0]:

This register contains the 16-bit connection ID of a connection in the Ingress VC Table which has undergone a change in connection state. This is the least significant 16-bits of data in the Ingress Change of State FIFO.

The COSDATA[15:0] data are valid if the COSVALID bit is logic 1 and BUSY bit is logic 0 in register 0x23B.

The COS FIFO read pointer is incremented when this register is read.

Register 0x23B: Ingress VC Table Change of Connection Status Data (MSW)

Bit	Type	Function	Default
15	R	COSFULL	X
14	R	COSVALID	X
13	R	BUSY	X
12		Unused	X
11		Unused	X
10		Unused	X
9	R	COSDATA[25]	X
8	R	COSDATA[24]	X
7	R	COSDATA[23]	X
6	R	COSDATA[22]	X
5	R	COSDATA[21]	X
4	R	COSDATA[20]	X
3	R	COSDATA[19]	X
2	R	COSDATA[18]	X
1	R	COSDATA[17]	X
0	R	COSDATA[16]	X

COSDATA[25:16]:

The COS[25:16] field contains the End-point information and Status field of a connection whose address is identified by the COS[15:0] register. COSDATA[25] is the Segment End-Point bit (if this bit is logic 1, the connection is configured as a segment end-point), COSDATA[24] is the End-to-End Point bit (if this bit is logic 1, the connection is configured as an end-to-end point), COSDATA[23:16] is the Status field (LSB justified with COSDATA[23:21] set to logic 0) of the connection. The presence of data in this register indicates that the connection has undergone a change in connection state. This is the most significant 8-bits of the Ingress Change of State FIFO.

The COSVALID and BUSY register bits indicate whether or not the data in this register are valid. The COS FIFO read pointer is updated when the Ingress VC Table Change of Connection Status Data LSW register is read.

BUSY:

If BUSY is logic 1, the COS FIFO read-pointer is being updated. When BUSY is asserted, the COSVALID bit is undefined. When BUSY is deasserted, the state of the COSVALID bit is defined.

COSVALID:

If this bit is logic 1, the data in this register and the Ingress VC Table Change of Connection Status Data (LSW) are valid. The COSVALID bit is defined only when the BUSY bit is logic 0.

COSFULL:

If this register bit is logic 1, the Ingress Change of State FIFO is full, and no more change of connection state data can be written into the FIFO. This will suspend the Ingress background process, which monitors the connection for changes in the connection state. It is the responsibility of the management software to ensure this register is read often enough to ensure the notification of changes in connection state are compliant to Bellcore and ITU standards.

Register 0x23C: Ingress Cell Processor F4-PM Flow VCI map

Bit	Type	Function	Default
15	R/W	VCI_15	0
14	R/W	VCI_14	0
13	R/W	VCI_13	0
12	R/W	VCI_12	0
11	R/W	VCI_11	0
10	R/W	VCI_10	0
9	R/W	VCI_9	0
8	R/W	VCI_8	0
7	R/W	VCI_7	0
6	R/W	VCI_6	0
5	R/W	VCI_5	1
4		Unused	X
3		Unused	X
2	R/W	VCI_2	1
1	R/W	VCI_1	1
0	R/W	VCI_0	0

VCI_x:

This register maps which VCI values are included in F4 Performance Monitoring flows maintained by the Ingress Cell Processor. This register is provided to guard against possible changes in ITU and Bellcore standards.

Setting any of these register bits to logic 1 ensures they will be included in F4 PM flows.

Register 0x23D: Ingress Cell Processor F5-PM Flow PTI map

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8	R/W	F5RM_F4PM	1
7	R/W	PTI_7	0
6	R/W	PTI_6	0
5		Unused	X
4		Unused	X
3	R/W	PTI_3	1
2	R/W	PTI_2	1
1	R/W	PTI_1	1
0	R/W	PTI_0	1

PTI_x:

This register maps which PTI values are included in F5 Performance Monitoring flows maintained by the Ingress Cell Processor. This register is provided to guard against possible changes in ITU and Bellcore standards.

Setting any of these register bits to logic 1 ensures they will be included in F5 PM flows.

F5RM_F4PM:

This bit determines whether or not F5 RM cells (Forward and Backward) and included in F4 PM flows. If this bit is logic 0, then F5 RM cells are not included (i.e. they are not considered to be user cells) in F4 PM flows. If this bit is logic 1 (default), then F5 RM cells are included in F4 PM flows.

Register 0x23E: Ingress Paced Fwd PM Cell Generation

Bit	Type	Function	Default
15	R/W	FWDPMP[15]	0
14	R/W	FWDPMP[14]	0
13	R/W	FWDPMP[13]	0
12	R/W	FWDPMP[12]	0
11	R/W	FWDPMP[11]	0
10	R/W	FWDPMP[10]	0
9	R/W	FWDPMP[9]	0
8	R/W	FWDPMP[8]	0
7	R/W	FWDPMP[7]	0
6	R/W	FWDPMP[6]	0
5	R/W	FWDPMP [5]	1
4	R/W	FWDPMP [4]	0
3	R/W	FWDPMP [3]	0
2	R/W	FWDPMP [2]	0
1	R/W	FWDPMP [1]	0
0	R/W	FWDPMP [0]	0

FWDPMP [15:0]:

FWDPM[15:0] sets the number of cell intervals between generation of successive Forward Monitoring PM cells into the Ingress cell stream. This is to prevent an excessive number of Forward Monitoring PM cells to be generated simultaneously by the ATLAS. A cell interval is defined to be 32 (i.e. assuming cells to be of 64 bytes) ISYSCLK clocks. The minimum rate of transfer is 1 in 65536 cell intervals. When FWDPMP[15:0] = 0x0000 back-to-back generation of Fwd PM cells into the Ingress cell stream is possible. The default is set to 1 in 32 cell interval.

Register 0x23F Ingress VC Table Maximum Index

Bit	Type	Function	Default
15	R/W	MAX[15]	0
14	R/W	MAX[14]	0
13	R/W	MAX[13]	0
12	R/W	MAX[12]	0
11	R/W	MAX[11]	0
10	R/W	MAX[10]	0
9	R/W	MAX[9]	0
8	R/W	MAX[8]	0
7	R/W	MAX[7]	0
6	R/W	MAX[6]	0
5	R/W	MAX[5]	0
4	R/W	MAX[4]	0
3	R/W	MAX[3]	0
2	R/W	MAX[2]	0
1	R/W	MAX[1]	0
0	R/W	MAX[0]	0

MAX[15:0]:

The MAX[15:0] bits represent the current maximum Ingress VC Table index (ISA[15:0]). It is used by the background processes of the Ingress VC Table as the first connection upon which the background processes act. The index decrements with each subsequent connection serviced. An accurate value in this location maximizes the efficiency of the ATLAS. Fixing this register guarantees that all 65535 connections will be serviced by the background processes. **Do not set MAX[15:0] to a value greater than supported by the depth of SRAM provisioned.**

Setting MAX[15:0] to all zeros effectively halts the background tasks for all locations except ISA[15:0]=0x0000.

Register 0x240: Ingress per-PHY APS Indication 1

Bit	Type	Function	Default
15	R/W	APS15	1
14	R/W	APS14	1
13	R/W	APS13	1
12	R/W	APS12	1
11	R/W	APS11	1
10	R/W	APS10	1
9	R/W	APS9	1
8	R/W	APS8	1
7	R/W	APS7	1
6	R/W	APS6	1
5	R/W	APS5	1
4	R/W	APS4	1
3	R/W	APS3	1
2	R/W	APS2	1
1	R/W	APS1	1
0	R/W	APS0	1

APSx:

The APSx register bits indicate that automatic protection switching for PHY x exists. If APSx is logic 1, then when a segment VP-AIS cell is terminated, an end-to-end VP-AIS cell will not be generated. If APSx is logic 0, then when a segment VP-AIS cell is terminated, an end-to-end VP-AIS cell will be generated (assuming that end-to-end VPC-AIS cells are not being received). The PHYID[4:0] field in the Ingress VC Table identifies the PHY device associated with a connection.

Register 0x241: Ingress per-PHY APS Indication 2

Bit	Type	Function	Default
15	R/W	APS31	1
14	R/W	APS30	1
13	R/W	APS29	1
12	R/W	APS28	1
11	R/W	APS27	1
10	R/W	APS26	1
9	R/W	APS25	1
8	R/W	APS24	1
7	R/W	APS23	1
6	R/W	APS22	1
5	R/W	APS21	1
4	R/W	APS20	1
3	R/W	APS19	1
2	R/W	APS18	1
1	R/W	APS17	1
0	R/W	APS16	1

APSx:

The APSx register bits indicate that automatic protection switching for PHY x exists. If APSx is logic 1, then when a segment VP-AIS cell is terminated, an end-to-end VP-AIS cell will not be generated. If APSx is logic 0, then when a segment VP-AIS cell is terminated, and end-to-end VP-AIS cell will be generated. The PHYID[4:0] field in the Ingress VC Table identifies the PHY device associated with a connection.

Register 0x280: Egress Cell Processor Configuration #1

Bit	Type	Function	Default
15	R/W	BADVCtoUP	0
14	R/W	CounterWrap	0
13	R/W	HBTOtoUP	0
12	R/W	UPURS	0
11	R/W	VCRAstuff	0
10	R/W	COS	0
9	R/W	AUTORDI	0
8	R/W	COUNT	0
7	R/W	PM	0
6	R/W	GFC	0
5	R/W	GVPIVCI	0
4	R/W	PHYIDinHEC	0
3	R/W	AddrParityEn	0
2	R/W	CNTUNDEF	0
1	R/W	GENPHYID_0	0
0	R/W	VPRMSEL	0

VPRMSEL:

The VPRMSEL bit controls the identification of the VPC Resource Management (VP-RM) cells. If VPRMSEL is a logic 0, VP-RM cells are identified by a VCI=6, the PTI field is ignored. If VPRMSEL is a logic 1, VP-RM cells are identified by a VCI=6 and a PTI=110. If the PTI field is not equal to 110, the cell is flagged as invalid and optionally can be routed to the Egress Microprocessor Cell Interface by the downstream block.

GENPHYID_0:

If the GENPHYID_0 bit is a logic 1, generated OAM cells (AIS, CC, PM) will be transmitted to PHY 0, independent of the PHYID field in the Egress VC Table. This assumes that all incoming cells are destined for PHY 0.

If the GENPHYID_0 bit is a logic 0, generated OAM cells will take their PHYID from the Egress VC Table.

CNTUNDEF:

If the CNTUNDEF bit is a logic 1, OAM cells with undefined OAM Type and Function Type fields are included in the count of Errored OAM cells. This also results in the assertion of the E_OAMERRI interrupt. If CNTUNDEF is a logic 0, only OAM cells with CRC-10 errors are included in the per-PHY count of Errored OAM cells. The assertion of the E_OAMERRI interrupt will also be suppressed in this case.

AddrParityEn:

If AddrParityEn is logic 1, then parity protection is enabled over the connection lookup address. This assumes that parity exists in the external SRAM, and is connected appropriately to the ESD[31:0] and ESP[3:0] pins. The BadVCtoUP bit (this register) describes what happens to a cell if a parity error occurs. If AddrParityEn is logic 0, parity protection is disabled and external SRAM parity is not required.

PHYIDinHEC:

If PHYIDinHEC is logic 1, the HEC byte of input cells is substituted with the contents of the PHYID field in the Egress VC Table (LSB justified with the 3 MSBs set to logic 0). Generated RDI and Backward Reporting PM cells also have their HEC byte overwritten in this manner. If PHYIDinHEC is logic 0, the HEC byte of input cells is passed transparently.

GVPIVCI:

If GVPIVCI is logic 1, Egress header translation (of the VPI/VCI fields) is globally enabled. The VPI/VCI bytes of ATM cells are replaced with the VPI/VCI fields in the Egress VC Table. If the connection is an F4 (the VCI field in the search key is coded as all zeros), then the VCI field is passed through transparently. If GVPIVCI is logic 0, the incoming VPI/VCI fields are passed through unaltered.

GFC:

The GFC bit determines if the GFC field in the ATM cell header is overwritten or passed through unaltered. If GFC is logic 1, the GFC field in the incoming cell is passed transparently. If GFC is logic 0, the GFC field is replaced by the contents of the Egress VC Table. The GFC bit has no effect if the connection belongs to a NNI.

PM:

If the PM bit is logic 1, performance monitoring is globally enabled. If the PM bit is logic 0, all performance monitoring cells are ignored at end-to-end points and segment-end points, and no statistics are maintained at intermediate points.

COUNT:

If the COUNT bit is logic 1, per-connection cell counting is globally enabled. If the COUNT bit is logic 0, the two generic cell counts in the Egress VC Table are not maintained, and no physical memory need be provided at those locations.

AUTORDI:

The AUTORDI bit enables the generation of segment and end-to-end RDI cells while in an AIS alarm or Continuity alarm state. If AUTORDI is logic 1, an RDI cell is transmitted (and looped from the Egress Cell Processor to the Ingress cell stream) immediately upon the reception of the first AIS cell at a flow end-point (if the ATLAS is an end-to-end point for that connection, an end-to-end RDI cell will be generated, if the ATLAS is a segment end point, a segment RDI cell will be generated, and if the ATLAS is both a segment and end-to-end point, both types of RDI cells will be generated) and once per second thereafter until the AIS state is exited. Similarly, if the CC_RDI bit in the Egress VC Table is set, RDI cells are generated once per second if no user or CC cells have been received in the last 3.5 +/- 0.5 seconds. RDI cells can also be transmitted if the Send_RDI_segment and Send_RDI_end_to_end bits in the Egress VC Table are set (this is independent of the AUTORDI bit).

COS:

The Change of State FIFO enable (COS) bit enables the monitoring of changes in connection state in the Egress direction. If COS is logic 1, all egress connections which undergo changes in state (e.g. AIS or CC alarm states) can be logged in a Change of State FIFO. This FIFO is 256 entries deep and holds a copy of the per-connection Status field of the Egress VC Table. Using this feature eliminates the need to periodically poll each connection to determine if any changes in state have occurred. If the COS FIFO becomes full, background processes which monitor for changes in connection state will be suspended until such time as the FIFO becomes able to accept notifications of changes in state. Therefore, it is the responsibility of the management software to ensure the COS FIFO is read often enough so that changes in state remain compliant with the Bellcore and ITU standards.

If COS is logic 0, the COS FIFO is disabled, and the background processes will not be suspended. If COS is logic 0, it is the responsibility of the management software to poll each connection to determine changes in connection state (as reflected in the Status field of the Egress VC Table) and notify higher layers of any changes in state.

The updating of the COS FIFO can be enabled/disabled on a per-connection basis with the COS_enable bit of the of the Egress VC Table at row ESA[19:16] = 0001..

VCRAstuff:

If the VCRAstuff bit is logic 1, all cells routed to the Egress Microprocessor Cell Interface have the HEC and UDF bytes replaced with the Egress VC Table Record address. This enables a microprocessor to immediately determine the location of an Egress VC Record in its data structure. This feature is provided to enable high speed processing of cells. The EXTPHYID bit of the Egress Microprocessor Cell Interface Extract FIFO Control and Status register takes precedence over the VCRAstuff bit. If the EXTPHYID is set, the HEC byte location of extracted cells will contain the PHY identification regardless of the state of the VCRAstuff bit.

UPURS:

The Egress Microprocessor User Reason Symbol (UPURS) bit allows a causation word to be prepended to the cell extracted to the Egress Microprocessor Interface. This allows an external microprocessor to immediately determine the reason a cell was routed to the Egress Microprocessor Cell Interface. The extracted cell length will be 1 greater than the input cell length. If the input cell length is 32, and the UPURS bit is logic one, the first word of the cell (prepend or postpend) will be overwritten with the causation word.

HBTOtoUP:

If the HBTOtoUP bit is logic 1, then if the cell at the head of the Egress Backward OAM Cell Interface times out due to a malfunctioning PHY, this cell will be copied to the Egress Microprocessor Cell Interface for logging and possible insertion in the future. If the HBTOtoUP is logic 0, then any cell at the head of the Egress Backward OAM Cell Interface which times out due to a malfunctioning PHY will be discarded.

CounterWrap:

The CounterWrap bit controls the saturation or rollover of Egress VC Table counts. If the CounterWrap bit is logic 1, then all counts in the Egress VC Table will rollover. If the CounterWrap bit is logic 0, then all counts in the Egress VC Table will saturate at all ones and never rollover. It is the responsibility of the management software to ensure the Egress VC Table counts are polled often enough to ensure they never rollover or saturate.

BADVCtoUP:

If the BadVCtoUP bit is logic 1, then a connection lookup error (parity error in the connection address) will cause the cell to be copied to the Egress Microprocessor Cell Interface. If the BadVCtoUP bit is logic 0, then a lookup error will result in the cell being discarded.

Register 0x281: Egress Cell Processor Routing Configuration

Bit	Type	Function	Default
15	R/W	CRC10toUP	0
14	R/W	DROPCRC10	0
13	R/W	ACTDEtoOCIF	0
12	R/W	SYSMANtoOCIF	0
11	R/W	DROPINVPTIVCI	0
10	R/W	DROPBRM	0
9	R/W	DROPFRM	0
8	R/W	INACTIVEtoUP	0
7	R/W	BRMtoUP	0
6	R/W	FRMtoUP	0
5	R/W	ACTDEtoUP	0
4	R/W	INVPTIVCItoUP	0
3	R/W	UNDEFtoUP	0
2	R/W	SYSMANtoUP	0
1	R/W	DROPCRCERM	0
0	R/W	PMtoUP	0

PMtoUP:

If this bit is logic 1, all Performance Monitoring OAM cells are copied to the Egress Microprocessor Cell Interface at flow end-points. Regardless of the state of this bit, all PM OAM cells are output to the Egress Output Cell Interface if the ATLAS is not an end-point for that Egress connection.

DROPCRCERM:

If this bit is logic 1, all Forward and Backward RM cells are discarded as a result of an incorrect CRC-10. If this bit is logic 0, then all Forward and Backward RM cells are output to the Egress Output Cell Interface regardless of whether their CRC-10 is correct or not.

SYSMANtoUP:

If this bit is logic 1, all System Management OAM cells are copied to the Egress Microprocessor Cell Interface at flow end-points. If this bit is logic 0, System Management OAM cells are not copied to the Egress Microprocessor Cell Interface at flow end-points. Regardless of the state of this bit, all System Management OAM cells are output to the Egress Output Cell Interface if the ATLAS is not an end-point for that Egress connection.

UNDEFtoUP:

If the UNDEFtoUP bit is logic 1, all OAM cells with an undefined OAM Type or Function Type value are copied to the Egress Microprocessor Cell Interface at flow end-points. Regardless of the state of this bit, all OAM cells with an undefined OAM Type or Function Type value are output to the Egress Output Cell Interface if the ATLAS is not an end point for that Egress connection.

INVPTIVCItoUP:

If the INVPTIVCItoUP bit is logic 1, all F5 (VCC) cells with an invalid PTI field (PTI=111) and all F4 (VPC) cells with an invalid VCI field (VCI 7 through 15) are copied to the Egress Microprocessor Cell Interface. The DROPINVPTIVCI register bit determines whether cells with invalid PTI or VCI fields are passed to the Egress Output Cell Interface.

ACTDEtoUP:

If the ACTDEtoUP bit is logic 1, all activate/deactivate OAM cells are copied to the Egress Microprocessor Cell Interface at flow end-points. If the ATLAS is not a flow end-point for the connection, the Activate/Deactivate cells are not copied to the Egress Microprocessor Cell Interface. Regardless of the state of this bit, all activate/deactivate cells are passed to the Egress Output Cell Interface if the ATLAS is not an end point for that Egress connection.

FRMtoUP:

If the FRMtoUP bit is logic 1, all forward RM cells are copied to the Egress Microprocessor Cell Interface. Forward RM cells are identified by a zero in the DIR bit position of the payload in conjunction with PTI=110 for VC-RM cells and by VCI=6 for VP-RM cells. If the VPRMSEL register bit of the Egress Cell Processor configuration register is logic 1, VP-RM cells are further qualified by PTI=110.

BRMtoUP:

If the BRMtoUP bit is logic 1, all Backward RM cells are copied to the Egress Microprocessor Cell Interface. Backward RM cells are identified by a one in the DIR bit position of the payload in conjunction with PTI=110 for VC-RM cells and VCI=6 for VP-RM cells. If the VPRMSEL register bit of the Egress Cell Processor configuration register is logic 1, VP-RM cells are further qualified by PTI=110.

INACTIVEtoUP:

If the INACTIVEtoUP bit is logic 1, all cells whose direct index lookup has an Egress VC Table record with the Active bit equal to 0 are copied to the Egress Microprocessor Cell Interface. Any received cell for which the Egress VC Table record has an Active bit equal to 0 are unconditionally dropped (i.e. not sent to the Egress Output Cell Interface).

DROPFRM:

If the DROPFRM bit is logic 1, all forward RM cells are dropped (i.e. not output to the Egress Output Cell Interface). Regardless of the state of this bit, forward RM cells can be routed to the Egress Microprocessor Cell Interface if the FRMtoUP bit is set.

DROPBRM:

If the DROPBRM bit is logic 1, all backward RM cells are dropped (i.e. not output to the Egress Output Cell Interface). Regardless of the state of this bit, backward RM cells can be routed to the Egress Microprocessor Cell Interface if the BRMtoUP bit is set.

DROPINVPTIVCI:

If this bit is logic 1, all F4 (VCC) cells with PTI=111 and all F5 (VPC) cells with a VCI of 7 through 15 are not routed to the Egress Output Cell Interface. If DROPINVPTIVCI is logic 0, these cells are passed transparently.

SYSMANtoOCIF:

If this bit is logic 1, all System Management OAM cells are not discarded at flow-end points, they are output to the Egress Output Cell Interface. If this bit is logic 0, System Management OAM cells are discarded at flow end-points. Regardless of the state of this bit, all System Management cells are routed to the Egress Output Cell Interface if the ATLAS is not a flow end-point for that connection.

ACTDEtoOCIF:

If the ACTDEtoOCIF bit is logic 1, all Activate/Deactivate cells are routed to the Egress Output Cell Interface. If ACTDEtoOCIF is logic 0, then at flow end points, all Activate/Deactivate cells are dropped. Regardless of the state of this bit, all Activate/Deactivate cells are routed to the Egress Output Cell Interface if the ATLAS is not a flow end point for that Egress connection.

DROPCRC10:

If the DROPCRC10 bit is logic 1, all OAM cells with an errored CRC-10 are dropped (i.e. not routed to the Egress Output Cell Interface). Regardless of the state of this bit, if the ATLAS is a flow end-point, all OAM cells with an errored CRC-10 are dropped.

CRC10toUP:

If the CRC10toUP bit is logic 1, all OAM cells and RM cells with an errored CRC-10 are copied to the Egress Microprocessor Cell Interface. Regardless of the state of this bit, the DROPCRC10 bit determines whether or not the ATLAS will route errored OAM cells to the Egress Output Cell Interface.

Register 0x282: Egress Cell Processor Direct Lookup Index Configuration 1

Bit	Type	Function	Default
15	R/W	PHY[2]	0
14	R/W	PHY[1]	0
13	R/W	PHY[0]	0
12	R/W	LA[4]	0
11	R/W	LA[3]	0
10	R/W	LA[2]	0
9	R/W	LA[1]	0
8	R/W	LA[0]	0
7	R/W	BCIFHECUDF	0
6	R/W	STARTA[6]	0
5	R/W	STARTA[5]	0
4	R/W	STARTA[4]	0
3	R/W	STARTA[3]	0
2	R/W	STARTA[2]	0
1	R/W	STARTA[1]	0
0	R/W	STARTA[0]	0

This register holds the starting location and length of the Lookup index within the Routing Word. The Egress routing word consists of a PHYID field which is appended to the field specified by the LA[4:0] and the STARTA[6:0], and the LB[4:0] and STARTB[6:0] fields. The PHYID forms the MSB of the index, the field specified by the LB[4:0] and STARTB[6:0] fields is the next portion of the index and finally, the LA[3:0] and STARTA[6:0] fields specify the LSB of the index. If the combined fields are less than 16-bits, the index is LSB justified and the MSBs are padded with zeros to form a 16-bit index.

STARTA[6:0]:

STARTA[6:0] forms the binary address of the LSB of the Lookup index within (fieldA) the Routing Word. STARTA[6] is the MSB of the address.

LA[4:0]:

LA[4:0] gives the fieldA length of the Lookup index in bits. The length is stored in LA[4:0] as binary value with LA[4] as MSB. Valid values for this field range from '00000' to '10000.' As a programming example: If a 10 bit Lookup index should be extracted starting at the 120th bit of the Routing Word, we would set LA ='01010' (length = 10) and STARTA='1110111' (starting address = 119, ending address = 110), i.e. write 0x0A77 to this register.

BCIFHECUDF:

If the BCIFHECUDF bit is logic 1, the HEC and UDF fields are used for the direct lookup index for cells received from the Egress Backward OAM Cell Interface. This allows the management software to use the HEC and UDF fields to specify an Egress VC Table address for cells that are inserted into the Egress cell stream. If this bit is logic 0, the Egress Cell Processor uses the Lookup index field to lookup cells received from the Egress Backward OAM Cell Interface in exactly the same manner as cells received from the Egress Input Cell Interface.

PHY[2:0]:

The contents of PHY[2:0] determine the number of PHY ID bits in Lookup Index. If less than all five PHY address lines should be considered during the index search (as in the case where only a single PHY interface is used) then PHY[2:0] must be programmed with the values below.

PHY[2]	PHY[1]	PHY[0]	Number of PHY ID bits in Primary Key
1	1	1	Reserved
1	1	0	Reserved
1	0	1	5
1	0	0	4
0	1	1	3
0	1	0	2
0	0	1	1
0	0	0	0 (single PHY interface)

Register 0x283: Egress Cell Processor Direct Lookup Index Configuration 2

Bit	Type	Function	Default
15	R/W	LBtoUPXLAT	0
14	R/W	ForceCC	0
13	R/W	EAISCOPY	0
12	R/W	LB[4]	0
11	R/W	LB[3]	0
10	R/W	LB[2]	0
9	R/W	LB[1]	0
8	R/W	LB[0]	0
7	R/W	Alternate_Count	0
6	R/W	STARTB[6]	0
5	R/W	STARTB[5]	0
4	R/W	STARTB[4]	0
3	R/W	STARTB[3]	0
2	R/W	STARTB[2]	0
1	R/W	STARTB[1]	0
0	R/W	STARTB[0]	0

STARTB[6:0]

STARTB[6:0] forms the binary address of the second portion of the Lookup index within the Routing Word. STARTB[6] is the MSB of the address.

LB[4:0]:

LB[4:0] gives the length of the Lookup index in bits. The length is stored in LB[4:0] as binary value with LB[4] as MSB. Valid values for this field range from ‘00000’ to ‘10000.’ As a programming example: If a 10 bit Lookup index should be extracted starting at the 120th bit of the Routing Word, we would set LB =’01010’ (length = 10) and STARTB=’1110111’ (starting address = 119), i.e. write 0x0A77 to this register.

Alternate_Count:

The Alternate_Count bit determines at which row, the per-connection cell counts in the Egress VC Table are incremented. If the Alternate_Count bit is logic 0, the ATLAS maintains the per-connection cell counts for the Egress VC Table at EAD[19:16]=0100 and 0101. If the Alternate_Count is logic 1, the counts are maintained at EAD [19:16]=0110 and 0111. It is the responsibility of the management software to ensure the count locations are cleared before the ATLAS begins incrementing at these locations.

EAISCOPY:

If the EAISCOPY register bit is logic 1, the ATLAS copies the Defect Location and Defect Type fields of all received segment and end-to-end AIS cells to the Egress VC Table. These fields are used when segment or end-to-end RDI cells are generated as a result of the AUTORDI process. If EAISCOPY is logic 0, then the fields are not copied to the Egress VC Table, and RAM need not be populated for these locations. If these rows are not provisioned, then the RDI cells will contain the local defect type selected by the Defect_Type field in the configuration field of the Egress VC Table, and will contain the default 0x6A6A pattern in the defect location field.

ForceCC:

The ForceCC bit controls whether or not the insertion of CC cells is dependent on the user cell traffic. If ForceCC is logic 0, CC cells are only generated if the CC_Activate_Segment or CC_Activate_End_to_End per-connection bits are logic 1 and if no user cells have been transmitted in within one second (nominal). If ForceCC is logic 1, CC cells are generated at a rate of once per second (nominal) if the CC_Activate_Segment or CC_Activate_End_to_End bits are logic 1.

LBtoUPXLAT:

The LBtoUPXLAT bit determines whether or not Loopback cells which are copied to the Egress Microprocessor Cell Interface have their cell header translated. If this bit is logic 1, all loopback cells which are copied to the Egress MCIF have their header replaced by the contents of the Egress VC Table (VPI, VCI (if appropriate), HEC and UDF fields). If this bit is logic 0, then loopback cells which are copied to the Egress MCIF are not header translated. Note, all other cells which are routed to the Egress MCIF do not have their headers translated.

Register 0x284: Egress Cell Processor F4-PM Flow VCI map

Bit	Type	Function	Default
15	R/W	VCI_15	0
14	R/W	VCI_14	0
13	R/W	VCI_13	0
12	R/W	VCI_12	0
11	R/W	VCI_11	0
10	R/W	VCI_10	0
9	R/W	VCI_9	0
8	R/W	VCI_8	0
7	R/W	VCI_7	0
6	R/W	VCI_6	0
5	R/W	VCI_5	1
4		Unused	X
3		Unused	X
2	R/W	VCI_2	1
1	R/W	VCI_1	1
0	R/W	VCI_0	0

VCI_x:

This register maps which VCI values are included in F4 Performance Monitoring flows maintained by the Egress Cell Processor. This register is provided to guard against possible changes in ITU and Bellcore standards.

Setting any of these register bits to logic 1 ensures they will be included in F4 PM flows.

VCI_15 down to VCI_7 are also used in processing cells in a VPC to determine whether these cells are user traffic or invalid traffic for routing/counting purposes. These settings do not affect the assertion of the INV_PTIVCII output.

Register 0x285: Egress Cell Processor F5-PM Flow PTI map

Bit	Type	Function	Default
15	R/W	SINGLEPHY622	0
14	R/W	UNDEFtoOCIF	0
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8	R/W	F5RM_F4PM	1
7	R/W	PTI_7	0
6	R/W	PTI_6	0
5		Unused	X
4		Unused	X
3	R/W	PTI_3	1
2	R/W	PTI_2	1
1	R/W	PTI_1	1
0	R/W	PTI_0	1

PTI_x:

This register maps which PTI values are included in F5 Performance Monitoring flows maintained by the Egress Cell Processor. This register is provided to guard against possible changes in ITU and Bellcore standards.

Setting any of these register bits to logic 1 ensures they will be included in F5 PM flows.

F5RM_F4PM:

This bit determines whether or not F5 RM cells (Forward and Backward) and included in F4 PM flows. If this bit is logic 0, then F5 RM cells are not included (i.e. considered to be user cells) in F4 PM flows. If this bit is logic 1 (default), then F5 RM cells are included in F4 PM flows.

UNDEFtoOCIF:

If the UNDEFtoOCIF bit is logic 1, all Undefined OAM cells are routed to the Egress Output Cell Interface. If UNDEFtoOCIF is logic 0, then at flow end points, all Undefined OAM cells

are dropped. Regardless of the state of this bit, all Undefined OAM cells are routed to the Egress Output Cell Interface if the ECP is not a flow end point for that Egress connection. The setting of this bit does not effect the action of copying cells to the Microprocessor Cell Interface. The UNDEFtoOCIF allows the use of proprietary OAM cell types which can be processed after the ATLAS.

SINGLEPHY622:

If the system using the ATLAS contains a single, 622 Mbit/s PHY device, this bit must be set to a logic 1. This bit is necessary to ensure maximum throughput when PM is enabled. In other modes of operation, this bit should be set to a logic 0.

Register 0x286: Egress Backward OAM Cell Interface Pacing

Bit	Type	Function	Default
15	R/W	BCP[15]	0
14	R/W	BCP[14]	0
13	R/W	BCP[13]	0
12	R/W	BCP[12]	0
11	R/W	BCP[11]	0
10	R/W	BCP[10]	0
9	R/W	BCP[9]	0
8	R/W	BCP[8]	0
7	R/W	BCP[7]	0
6	R/W	BCP[6]	0
5	R/W	BCP[5]	1
4	R/W	BCP[4]	0
3	R/W	BCP[3]	0
2	R/W	BCP[2]	0
1	R/W	BCP[1]	0
0	R/W	BCP[0]	0

This register sets the number of cell intervals between the transfer of backward OAM cells from the Egress Backward Cell Interface. A cell interval is defined to be 32 (i.e. assuming cells to be 64 bytes in length) clocks. This is to prevent excessive insertion of backward OAM cells from the Egress Backward OAM Cell Interface into the Egress cell stream by the ATLAS.

BCP[15:0]:

BCP[15:0] sets the number of cell interval between transfers of cells from the Backward Cell Interface. The minimum rate of transfer is 1 in 65535 cell intervals. When BCP[15:0] = 0x0000 back-to-back transfer from the Egress Backward Cell Interface is possible, if there are no transfer requested from the Egress Input Cell Interface or the Egress Microprocessor Cell Interface. The default is set to 1 in 32 cell interval.

Register 0x287: Egress Backward OAM Cell Interface Head-of-Line Time Out

Bit	Type	Function	Default
15	R/W	HBTO[15]	0
14	R/W	HBTO[14]	0
13	R/W	HBTO[13]	0
12	R/W	HBTO[12]	0
11	R/W	HBTO[11]	0
10	R/W	HBTO[10]	0
9	R/W	HBTO[9]	0
8	R/W	HBTO[8]	0
7	R/W	HBTO[7]	0
6	R/W	HBTO[6]	0
5	R/W	HBTO[5]	0
4	R/W	HBTO[4]	0
3	R/W	HBTO[3]	0
2	R/W	HBTO[2]	0
1	R/W	HBTO[1]	0
0	R/W	HBTO[0]	0

HBTO[15:0]:

HBTO[15:0] sets the timeout limit before a cell at the head of the Backward Cell Interface FIFO is discarded. This is to prevent a malfunctioning PHY holding a Backward Reporting PM cell or RDI cell at the head of the FIFO, thus blocking all others cells that follow. The unit is in cell periods, where a cell period is considered to be 32 ESYSCLK cycles. Default is set to all zeros, which disables this timeout feature.

Register 0x288: Egress Paced AIS/CC Cell Generation

Bit	Type	Function	Default
15	R/W	AISCCP[15]	0
14	R/W	AISCCP[14]	0
13	R/W	AISCCP[13]	0
12	R/W	AISCCP[12]	0
11	R/W	AISCCP[11]	0
10	R/W	AISCCP[10]	0
9	R/W	AISCCP[9]	0
8	R/W	AISCCP[8]	0
7	R/W	AISCCP[7]	0
6	R/W	AISCCP[6]	0
5	R/W	AISCCP[5]	1
4	R/W	AISCCP[4]	0
3	R/W	AISCCP[3]	0
2	R/W	AISCCP[2]	0
1	R/W	AISCCP[1]	0
0	R/W	AISCCP[0]	0

AISCCP[15:0]:

AISCCP[15:0] sets the number of cell interval between generation of AIS or CC cells into the Egress Output Cell Interface. This is to prevent an excessive number of AIS/CC cells to be generated back-to-back by the ATLAS. A cell interval is defined to be 32 (i.e. assuming cells to be of 64 bytes) ESYSCLK clocks. The minimum rate of transfer is 1 in 65535 cell intervals. When AISCCP[15:0] = 0x0000 back-to-back generation of AIS/CC cells into the Egress Output Cell Interface is possible. The default is set to 1 in 32 cell interval.

Register 0x289: Egress Paced Fwd PM Cell Generation

Bit	Type	Function	Default
15	R/W	FWDPMP[15]	0
14	R/W	FWDPMP[14]	0
13	R/W	FWDPMP[13]	0
12	R/W	FWDPMP[12]	0
11	R/W	FWDPMP[11]	0
10	R/W	FWDPMP[10]	0
9	R/W	FWDPMP[9]	0
8	R/W	FWDPMP[8]	0
7	R/W	FWDPMP[7]	0
6	R/W	FWDPMP[6]	0
5	R/W	FWDPMP [5]	1
4	R/W	FWDPMP [4]	0
3	R/W	FWDPMP [3]	0
2	R/W	FWDPMP [2]	0
1	R/W	FWDPMP [1]	0
0	R/W	FWDPMP [0]	0

FWDPMP [15:0]:

FWDPM[15:0] sets the number of cell intervals between generation of successive Forward Monitoring PM cells into the Egress cell stream. This is to prevent an excessive number of Forward Monitoring PM cells to be generated simultaneously by the ATLAS. A cell interval is defined to be 32 (i.e. assuming cells to be of 64 bytes) ESYSCLK clocks. The minimum rate of transfer is 1 in 65535 cell intervals. When FWDPMP[15:0] = 0x0000 back-to-back generation of Fwd PM cells into the Egress cell stream is possible. The default is set to 1 in 32 cell interval.

Register 0x28A: Egress per-PHY AIS Cell Generation Control 1

Bit	Type	Function	Default
15	R/W	AIS15	0
14	R/W	AIS14	0
13	R/W	AIS13	0
12	R/W	AIS12	0
11	R/W	AIS11	0
10	R/W	AIS10	0
9	R/W	AIS9	0
8	R/W	AIS8	0
7	R/W	AIS7	0
6	R/W	AIS6	0
5	R/W	AIS5	0
4	R/W	AIS4	0
3	R/W	AIS3	0
2	R/W	AIS2	0
1	R/W	AIS1	0
0	R/W	AIS0	0

AISx:

AISx enables the generation of AIS cells for PHY x, where x is from 0 to 15. If AISx is logic 1, AIS cells for every connection associated with PHYx, are generated once per second (nominally) to the Egress Output Cell Interface. If AISx is a logic 0, AIS cell generation on a per-PHY basis is disabled. The PHYID[4:0] field in the Egress VC Table identifies a connection's associated PHY.

If AISx is logic 1, only end-to-end AIS cells are generated. End-to-end AIS cells will not be generated on connections which are configured as end-to-end points.

Register 0x28B: Egress per-PHY AIS Cell Generation Control 2

Bit	Type	Function	Default
15	R/W	AIS31	0
14	R/W	AIS30	0
13	R/W	AIS29	0
12	R/W	AIS28	0
11	R/W	AIS27	0
10	R/W	AIS26	0
9	R/W	AIS25	0
8	R/W	AIS24	0
7	R/W	AIS23	0
6	R/W	AIS22	0
5	R/W	AIS21	0
4	R/W	AIS20	0
3	R/W	AIS19	0
2	R/W	AIS18	0
1	R/W	AIS17	0
0	R/W	AIS16	0

AISx:

AISx enables the generation of AIS cells for PHY x, where x is from 16 to 31. If AISx is logic 1, AIS cells for every connection associated with that PHY device are generated once per second (nominally) to the Egress Output Cell Interface. If AISx is a logic 0, AIS cell generation on a per-PHY basis is disabled. The PHYID[4:0] field in the Egress VC Table identifies a connection's associated PHY.

If AISx is logic 1, only end-to-end AIS cells are generated. End-to-end AIS cells will not be generated on connections which are configured as end-to-end points.

Register 0x28C: Egress per-PHY RDI Cell Generation Control 1

Bit	Type	Function	Default
15	R/W	RDI15	0
14	R/W	RDI14	0
13	R/W	RDI13	0
12	R/W	RDI12	0
11	R/W	RDI11	0
10	R/W	RDI10	0
9	R/W	RDI9	0
8	R/W	RDI8	0
7	R/W	RDI7	0
6	R/W	RDI6	0
5	R/W	RDI5	0
4	R/W	RDI4	0
3	R/W	RDI3	0
2	R/W	RDI2	0
1	R/W	RDI1	0
0	R/W	RDI0	0

RDIx:

RDIx enables the generation of RDI cells on a per-PHY basis for PHY x, where x is from 0 to 15. If RDIx is a logic 1, RDI cells for every connection associated with PHY x, are generated once per second (nominally) to the Ingress Output Cell Interface (through the Ingress Backward OAM Cell Interface). If RDIx is a logic 0, RDI cell generation on a per-PHY basis is disabled. The PHYID[4:0] field in the Egress VC Table identifies a connection's associated PHY. RDI cells are only generated for connection end-points associated with the PHY x when RDIx is logic 1.

If RDIx is logic 1, only end-to-end RDI cells are generated.

Register 0x28D: Egress per-PHY RDI Cell Generation Control 2

Bit	Type	Function	Default
15	R/W	RDI31	0
14	R/W	RDI30	0
13	R/W	RDI29	0
12	R/W	RDI28	0
11	R/W	RDI27	0
10	R/W	RDI26	0
9	R/W	RDI25	0
8	R/W	RDI24	0
7	R/W	RDI23	0
6	R/W	RDI22	0
5	R/W	RDI21	0
4	R/W	RDI20	0
3	R/W	RDI19	0
2	R/W	RDI18	0
1	R/W	RDI17	0
0	R/W	RDI16	0

RDIx:

RDIx enables the generation of RDI cells on a per-PHY basis for PHY x, where x is from 0 to 15. If RDIx is a logic 1, RDI cells for every connection (which is configured as an end-to-end point) associated with PHY x, are generated once per second (nominally) to the Ingress Output Cell Interface (through the Ingress Backward OAM Cell Interface). If RDIx is a logic 0, RDI cell generation on a per-PHY basis is disabled. The PHYID[4:0] field in the Egress VC Table identifies a connection's associated PHY.

If RDIx is logic 1, only end-to-end RDI cells are generated.

Register 0x28E: Egress per-PHY APS Indication 1

Bit	Type	Function	Default
15	R/W	APS15	1
14	R/W	APS14	1
13	R/W	APS13	1
12	R/W	APS12	1
11	R/W	APS11	1
10	R/W	APS10	1
9	R/W	APS9	1
8	R/W	APS8	1
7	R/W	APS7	1
6	R/W	APS6	1
5	R/W	APS5	1
4	R/W	APS4	1
3	R/W	APS3	1
2	R/W	APS2	1
1	R/W	APS1	1
0	R/W	APS0	1

APSx:

The APSx register bits indicate that automatic protection switching for PHY x exists. If APSx is logic 1, then when a segment VP-AIS cell is terminated, an end-to-end VP-AIS cell will not be generated. If APSx is logic 0, then when a segment VP-AIS cell is terminated, and end-to-end VP-AIS cell will be generated (assuming that end-to-end VPC-AIS cells are not being received on that connection). The PHYID[4:0] field in the Egress VC Table identifies the PHY device associated with a connection.

Register 0x28F: Egress per-PHY APS Indication 2

Bit	Type	Function	Default
15	R/W	APS31	1
14	R/W	APS30	1
13	R/W	APS29	1
12	R/W	APS28	1
11	R/W	APS27	1
10	R/W	APS26	1
9	R/W	APS25	1
8	R/W	APS24	1
7	R/W	APS23	1
6	R/W	APS22	1
5	R/W	APS21	1
4	R/W	APS20	1
3	R/W	APS19	1
2	R/W	APS18	1
1	R/W	APS17	1
0	R/W	APS16	1

APSx:

The APSx register bits indicate that automatic protection switching for PHY x exists. If APSx is logic 1, then when a segment VP-AIS cell is terminated, an end-to-end VP-AIS cell will not be generated. If APSx is logic 0, then when a segment VP-AIS cell is terminated, and end-to-end VP-AIS cell will be generated (assuming that end-to-end VPC-AIS cells are not being received on that connection). The PHYID[4:0] field in the Egress VC Table identifies the PHY device associated with a connection.

Register 0x290: Egress VC Table Counting Configuration 1

Bit	Type	Function	Default
15	R/W	COUNT2[7]	0
14	R/W	COUNT2[6]	0
13	R/W	COUNT2[5]	0
12	R/W	COUNT2[4]	0
11	R/W	COUNT2[3]	0
10	R/W	COUNT2[2]	0
9	R/W	COUNT2[1]	0
8	R/W	COUNT2[0]	0
7	R/W	COUNT1[7]	0
6	R/W	COUNT1[6]	0
5	R/W	COUNT1[5]	0
4	R/W	COUNT1[4]	0
3	R/W	COUNT1[3]	0
2	R/W	COUNT1[2]	0
1	R/W	COUNT1[1]	0
0	R/W	COUNT1[0]	0

This register is addressed when the Count_Type bit of the Egress VC Table is set to logic 0.

COUNT1[7:0]:

The COUNT1[7:0] controls which cells the Egress Cell Processor includes in its first per-connection 32-bit cell count. The COUNT1[7:0] field is programmed as follows:

Cell Type	Cells with PTI=111 (F5) or VCI=7 to 15 (F4) (See note 1)		RM Cells		OAM Cells		User Cells (see note 2)	
CLP Bit	0	1	0	1	0	1	0	1
Register Bit	COUNT1 [0]	COUNT1 [1]	COUNT1 [2]	COUNT1 [3]	COUNT1 [4]	COUNT1 [5]	COUNT1 [6]	COUNT1 [7]

A logic 1 written to any of the COUNT1[7:0] bits enables counting on that particular stream. For example, to enable counting of CLP=0+1 User and OAM cells only, the register configuration would be COUNT1[7:0] = 0xF0. If COUNT1[7:0] = 0x00, the first generic cell count for all connections is disabled.

Note 1: Cells in this category which are declared as user cells in the F4 PM Flow VCI Map or F5 PM Flow PTI map are counted as user cells rather than in this category. Physical layer cells are always counted in this category. F4 RM cells that have PTI /= '110' (when VPRMSEL='1') are counted here instead of as RM cells. F4 OAM cells that have PTI /= '000','010' and are received on an NNI connection are counted here instead of as OAM cells.

Note 2: User cells includes cells from any PTI/VCI which are marked as a user cell in the F4 PM Flow VCI Map or F5 PM Flow PTI map, other than F4 RM cells for F4 connections or F5 RM cells for F5 connections. Cells with VCI=1, 2, or 5 are always counted in this category.

COUNT2[7:0]:

The COUNT2[7:0] register bits controls which cells the Egress Cell Processor includes in its second per-connection 32-bit cell count. The COUNT2[7:0] field is programmed in exactly the manner as the COUNT1[7:0] field.

Register 0x291: Egress VC Table Counting Configuration 2

Bit	Type	Function	Default
15	R/W	COUNT2[7]	0
14	R/W	COUNT2[6]	0
13	R/W	COUNT2[5]	0
12	R/W	COUNT2[4]	0
11	R/W	COUNT2[3]	0
10	R/W	COUNT2[2]	0
9	R/W	COUNT2[1]	0
8	R/W	COUNT2[0]	0
7	R/W	COUNT1[7]	0
6	R/W	COUNT1[6]	0
5	R/W	COUNT1[5]	0
4	R/W	COUNT1[4]	0
3	R/W	COUNT1[3]	0
2	R/W	COUNT1[2]	0
1	R/W	COUNT1[1]	0
0	R/W	COUNT1[0]	0

This register is addressed when the Count_Type bit of the Egress VC Table is set to logic 1.

COUNT1[7:0]:

The COUNT1[7:0] controls which cells the Egress Cell Processor includes in its first per-connection 32-bit cell count. The COUNT1[7:0] field is programmed as follows:

Cell Type	Cells with PTI=111 (F5) or VCI = 7 to 15 (F4)		RM Cells		OAM Cells		User Cells	
CLP Bit	0	1	0	1	0	1	0	1
Register Bit	COUNT1 [0]	COUNT1 [1]	COUNT1 [2]	COUNT1 [3]	COUNT1 [4]	COUNT1 [5]	COUNT1 [6]	COUNT1 [7]

A logic 1 written to any of the COUNT1[7:0] bits enables counting on that particular stream. For example, to enable counting of CLP=0+1 User and OAM cells only, the register configuration would be COUNT1[7:0] = 0xF0. If COUNT1[7:0] = 0x00, the first generic cell count for all connections is disabled.

Note 1: Cells in this category which are declared as user cells in the F4 PM Flow VCI Map or F5 PM Flow PTI map are counted as user cells rather than in this category. Physical layer cells are always counted in this category. F4 RM cells that have PTI /= '110' (when VPRMSEL='1') are counted here instead of as RM cells. F4 OAM cells that have PTI /= '000','010' and are received on an NNI connection are counted here instead of as OAM cells.

Note 2: User cells includes cells from any PTI/VCI which is marked as a user cell in the F4 PM Flow VCI Map or F5 PM Flow PTI map, other than F4 RM cells for F4 connections or F5 RM cells for F5 connections. Cells with VCI=1, 2, or 5 are always counted in this category.

COUNT2[7:0]:

The COUNT2[7:0] register bits controls which cells the Egress Cell Processor includes in its second per-connection 32-bit cell count. The COUNT2[7:0] field is programmed exactly the same as the COUNT1[7:0] field.

Register 0x292: Egress OAM Defect Type 0 and 1

Bit	Type	Function	Default
15	R/W	DT2[7]	0
14	R/W	DT2[6]	1
13	R/W	DT2[5]	1
12	R/W	DT2[4]	0
11	R/W	DT2[3]	1
10	R/W	DT2[2]	0
9	R/W	DT2[1]	1
8	R/W	DT2[0]	0
7	R/W	DT1[7]	0
6	R/W	DT1[6]	1
5	R/W	DT1[5]	1
4	R/W	DT1[4]	0
3	R/W	DT1[3]	1
2	R/W	DT1[2]	0
1	R/W	DT1[1]	1
0	R/W	DT1[0]	0

DT1[7:0] and DT2[7:0]:

This register contains the Defect Type data that is inserted into generated AIS cells. The Defect Type field is inserted into generated RDI cells when the Send_RDI_Segment or Send_RDI_End_to_End bits are logic 1 (i.e. forced insertion of RDI cells rather than generation of RDI cells as a result of AUTORDI) or when an RDI cell is generated as a result of the CC_RDI function. The selection DT1-DT16 is selected on a per-VC basis, controlled by the Defect Type[3:0] bits in the Egress VC Table.

Register 0x293: Egress OAM Defect Type 2 and 3

Register 0x294: Egress OAM Defect Type 4 and 5

Register 0x295: Egress OAM Defect Type 6 and 7

Register 0x296: Egress OAM Defect Type 8 and 9

Register 0x297: Egress OAM Defect Type 10 and 11

Register 0x298: Egress OAM Defect Type 12 and 13

Register 0x299: Egress OAM Defect Type 14 and 15

Register 0x29A: Egress Cell Processor OAM Defect Location Octet 0 & 1

Bit	Type	Function	Default
15	R/W	DL[15]	0
14	R/W	DL[14]	1
13	R/W	DL[13]	1
12	R/W	DL[12]	0
11	R/W	DL[11]	1
10	R/W	DL[10]	0
9	R/W	DL[9]	1
8	R/W	DL[8]	0
7	R/W	DL[7]	0
6	R/W	DL[6]	1
5	R/W	DL[5]	1
4	R/W	DL[4]	0
3	R/W	DL[3]	1
2	R/W	DL[2]	0
1	R/W	DL[1]	1
0	R/W	DL[0]	0

DL[15:0]:

This register contains the Defect Location data LSB which is inserted into generated AIS cells. The Defect Location is also inserted into RDI cells when the Send_RDI_Segment or Send_RDI_End_to_End register bits are asserted (i.e. forced insertion of RDI cells rather than generation of RDI cells as a result of AUTORDI), and when RDI cells are generated as a result of the CC_RDI process. This is the least significant 16-bits of the Defect Location field.

Register 0x29B: Egress Cell Processor OAM Defect Location Octet 2 & 3

Register 0x29C: Egress Cell Processor OAM Defect Location Octet 4 & 5

Register 0x29D: Egress Cell Processor OAM Defect Location Octet 6 & 7

Register 0x29E: Egress Cell Processor OAM Defect Location Octet 8 & 9

Register 0x29F: Egress Cell Processor OAM Defect Location Octet 10 & 11

Register 0x2A0: Egress Cell Processor OAM Defect Location Octet 12 &13

Register 0x2A1: Egress Cell Processor OAM Defect Location Octet 14 & 15

Register 0x2A2: Egress Performance Monitoring Threshold A1

Bit	Type	Function	Default
15	R/W	MERROR[3]	0
14	R/W	MERROR[2]	0
13	R/W	MERROR[1]	0
12	R/W	MERROR[0]	0
11	R/W	MLOST[11]	0
10	R/W	MLOST[11]	0
9	R/W	MLOST[9]	0
8	R/W	MLOST[8]	0
7	R/W	MLOST[7]	0
6	R/W	MLOST[6]	0
5	R/W	MLOST[5]	0
4	R/W	MLOST[4]	0
3	R/W	MLOST[3]	0
2	R/W	MLOST[2]	0
1	R/W	MLOST[1]	0
0	R/W	MLOST[0]	0

This is the first of four Threshold Registers. These threshold registers are addressed by the Threshold_Select[1:0] field of the PM Configuration field of the Egress PM RAM data. The threshold registers are used for both Forward Monitoring and Backward Reporting cell counts.

MERROR[3:0]:

MERROR[3:0] is the binary representation of the threshold of BIP-16 violations per Performance Monitoring block required to declare a Severely Errored Cell Block for Errored cells (SECB Errored). Errored cell counts are not accumulated if the SECB Errored count is incremented. If MERROR[3:0] is a binary zero, the SECB Errored cell count is not declared as a result of excessive BIP-16 violations.

This threshold applies to both received Forward Monitoring and Backward Reporting cells.

MLOST[11:0]:

MLOST[11:0] is the binary representation of the threshold of lost cells per Performance Monitoring block required to declare a Severely Errored Cell Block of Lost Cells (SECB Lost). The number of lost cells is not counted if this threshold is exceeded (the SECB Lost counter will be incremented instead). If MLOST[11:0] is a binary zero, SECB Lost is not declared as a result of excessive lost cells.

Register 0x2A3: Egress Performance Monitoring Threshold A2

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11	R/W	MMISINS[11]	0
10	R/W	MMISINS[10]	0
9	R/W	MMISINS[9]	0
8	R/W	MMISINS[8]	0
7	R/W	MMISINS[7]	0
6	R/W	MMISINS[6]	0
5	R/W	MMISINS[5]	0
4	R/W	MMISINS[4]	0
3	R/W	MMISINS[3]	0
2	R/W	MMISINS[2]	0
1	R/W	MMISINS[1]	0
0	R/W	MMISINS[0]	0

This is the first of four Threshold Registers. These threshold registers are addressed by the Threshold_Select[1:0] field of the PM Configuration field of the Egress PM RAM data.

The thresholds given below apply to both received Forward Monitoring and Backward Reporting cells.

MMISINS[11:0]:

MMISINS[11:0] is the binary representation of the threshold of misinserted cells per Performance Monitoring block required to declare a Severely Errored Cell Block of Misinserted Cells (SECB Misinserted). The number of misinserted cells is not counted if this threshold is exceeded (the SECB Misinserted counter will be incremented instead). If MMISINS[11:0] is a binary zero, SECB Misinserted is not declared as a result of excessive misinserted cells.

Register 0x2A4: Egress Performance Monitoring Threshold B1

Register 0x2A5: Egress Performance Monitoring Threshold B2

Register 0x2A6: Egress Performance Monitoring Threshold C1

Register 0x2A7: Egress Performance Monitoring Threshold C2

Register 0x2A8: Egress Performance Monitoring Threshold D1

Register 0x2A9: Egress Performance Monitoring Threshold D2

Register 0x2AA Egress VC Table Maximum Index

Bit	Type	Function	Default
15	R/W	MAX[15]	0
14	R/W	MAX[14]	0
13	R/W	MAX[13]	0
12	R/W	MAX[12]	0
11	R/W	MAX[11]	0
10	R/W	MAX[10]	0
9	R/W	MAX[9]	0
8	R/W	MAX[8]	0
7	R/W	MAX[7]	0
6	R/W	MAX[6]	0
5	R/W	MAX[5]	0
4	R/W	MAX[4]	0
3	R/W	MAX[3]	0
2	R/W	MAX[2]	0
1	R/W	MAX[1]	0
0	R/W	MAX[0]	0

MAX[15:0]:

The MAX[15:0] bits represent the current maximum Egress VC Table index (ESA[15:0]). It is used by the background processes of the Egress VC Table as the first connection upon which the background processes act. The index is decremented with each subsequent connection serviced. An accurate value in this location maximizes the efficiency of the ATLAS. Fixing this register guarantees that all 65536 connections will be serviced by the background processes. Do not set MAX[15:0] to a value greater than supported by the depth of SRAM provisioned.

Setting MAX[15:0] to all zeros effectively disables the background tasks for all locations except ESA[15:0]=0x0000.

Register 0x2AB: Egress VC Table Record Address

Bit	Type	Function	Default
15	R/W	EAD[15]	0
14	R/W	EAD[14]	0
13	R/W	EAD[13]	0
12	R/W	EAD[12]	0
11	R/W	EAD[11]	0
10	R/W	EAD[10]	0
9	R/W	EAD[9]	0
8	R/W	EAD[8]	0
7	R/W	EAD[7]	0
6	R/W	EAD[6]	0
5	R/W	EAD[5]	0
4	R/W	EAD[4]	0
3	R/W	EAD[3]	0
2	R/W	EAD[2]	0
1	R/W	EAD[1]	0
0	R/W	EAD[0]	0

This register is used in conjunction with the Word Select and Access Control register to access the Egress VC Table external SRAM.

EAD[15:0]:

This register holds the VC Record Address to be used to address the Egress VC Table external SRAM through Microprocessor initiated accesses. It identifies the desired VC Table entry.

Register 0x2AC: Egress VC Table Write Mask and Access Control

Bit	Type	Function	Default
15	R/W	RWB	0
14	R	BUSY	X
13	R/W	CLRONRD	0
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3	R/W	WM[3]	0
2	R/W	WM[2]	0
1	R/W	WM[1]	0
0	R/W	WM[0]	0

This register allows the microprocessor to access the Egress VC Table external SRAM for data in the VC Record indicated in register 0x2AB and perform the operation specified by the RWB bit. Writing to this register initiates a microprocessor access request cycle. The contents of the Egress VC Table Record Address register and the Egress VC Table Row Select register should be set to the desired Egress VC Table Record before this register is written.

WM[3:0]:

The write mask (WM[3:0]) is used to select which bytes of the Egress VC Table row will be written during a write operation. If any of WM[3:0] are a '0' during a write operation (except for the case where all of the WM[3:0] bits are '0', as described in the next paragraph), the ECP performs a read-write-back operation when a write is requested. WM[3] controls the mask to bits [31:24] of the Egress VC Table word and WM[0] controls the mask to bits [7:0] of the Egress VC Table word. This is to allow the ECP to write to selected fields in a row of the Egress VC Table.

If WM[3:0] = "0000" or "1111" then the entire row is written. Note, there is no such operation as "mask the entire row", since this means there is no need for a write operation.

Examples of valid writes are:

Write to bits 31:24 WM[3:0] = 1000
Write to bits 23:16 WM[3:0] = 0100
Write to bits 15:8 WM[3:0] = 0010
Write to bits 7:0 WM[3:0] = 0001
Write to bits 31:16 WM[3:0] = 1100
Write to bits 31:8 WM[3:0] = 1110
Wrte entire row WM[3:0] = 0000 or WM[3:0] = 1111

Note, if more than one row is being accessed during a microprocessor initiated SRAM access, then the WM[3:0] fields are ignored.

CLRONRD:

If CLRONRD is logic 1, after a read access of row 4, 5, 6 or 7 of the Egress VC Table specified in register 0x2AD, a clearing write (with data bits [31:0] set to all '0') is automatically initiated. If CLRONRD is logic 0, no write back to clear the data bits is initiated.

Programming Note: When the CLRONRD bit is logic 1, to perform a Clear-On-Read operation on **any single row** in rows 4-7, an additional read from any row in rows 0 to 3 is required. For example, to perform a Clear-On-Read to row 4, select both rows 4 and 0. Reads to rows 0 to 3 with the Clear-On-Read enabled do not clear the row, so that the extra read has no effect on the table contents. If more than one row are accessed simultaneously, then no additional rows need to be read.

BUSY:

The BUSY bit is high while a Microprocessor initiated access request to the Egress VC Table external SRAM is pending. If more than one access to the external SRAM is initiated either through read-write-back, mask write or writing to multiple rows of the Egress VC Table through write/read caching, the BUSY bit is deasserted only after all the access required has been completed. This register should be polled until the BUSY bit goes low before another microprocessor access request is initiated. A microprocessor access request with 1 word selected is typically completed within 35 ESYSCLK cycles. If the ESTANDBY bit in the ATLAS Master Configuration register is a logic 1, the access time with 1 word selected is reduced to less than 5 ESYSCLK cycles.

RWB:

The RWB bit selects the operation to be performed on the addressed Egress VC Table external SRAM: when RWB is set to a logic 1, a read from the external SRAM is requested; when RWB is set to a logic 0, a write to the external SRAM is requested.

Register 0x2AD: Egress VC Table Row Select

Bit	Type	Function	Default
15	R/W	ROW[15]	0
14	R/W	ROW[14]	0
13	R/W	ROW[13]	0
12	R/W	ROW[12]	0
11	R/W	ROW[11]	0
10	R/W	ROW[10]	0
9	R/W	ROW[9]	0
8	R/W	ROW[8]	0
7	R/W	ROW[7]	0
6	R/W	ROW[6]	0
5	R/W	ROW[5]	0
4	R/W	ROW[4]	0
3	R/W	ROW[3]	0
2	R/W	ROW[2]	0
1	R/W	ROW[1]	0
0	R/W	ROW[0]	0

ROW[15:0]:

ROW[15:0] indicate which of the 16 rows in the Egress VC Record Table is to be written or read when a microprocessor access to the external SRAM is to be performed. If ROW[x] is set to '1', row x of the VC Record Table will be written or read. If ROW[15:0] are all set, all 16 rows of the Egress VC Record Address select in Register 0x2AB will be written or read when a external SRAM access is triggered by writing to register 0x2AC. The BUSY bit will be asserted until all the rows that are selected are written or read.

Register 0x2AE: Egress VC Table Record Row 0, Word 0 (LSW) RAM Data

Bit	Type	Function	Default
15	R/W	ROW0[15]	0
14	R/W	ROW0[14]	0
13	R/W	ROW0[13]	0
12	R/W	ROW0[12]	0
11	R/W	ROW0[11]	0
10	R/W	ROW0[10]	0
9	R/W	ROW0[9]	0
8	R/W	ROW0[8]	0
7	R/W	ROW0[7]	0
6	R/W	ROW0[6]	0
5	R/W	ROW0[5]	0
4	R/W	ROW0[4]	0
3	R/W	ROW0[3]	0
2	R/W	ROW0[2]	0
1	R/W	ROW0[1]	0
0	R/W	ROW0[0]	0

This register contains either the data to be written into the Egress VC Table Row 0 Word 0 (LSW) external SRAM or the data read from the external SRAM when a read request has been completed. If data is to be written to Egress VC Table external SRAM Row 0, the LSW word must be written to this register before the Egress VC Record Address register and the Row Select and Access Control registers are written. If data is to be read from Row 0 this register contains the data from Row 0 Word 0 (LSW) after the external SRAM access is completed.

Register 0x2AF: Egress VC Table Record Row 0, Word 1 (MSW) RAM Data

Bit	Type	Function	Default
15	R/W	ROW0[31]	0
14	R/W	ROW0[30]	0
13	R/W	ROW0[29]	0
12	R/W	ROW0[28]	0
11	R/W	ROW0[27]	0
10	R/W	ROW0[26]	0
9	R/W	ROW0[25]	0
8	R/W	ROW0[24]	0
7	R/W	ROW0[23]	0
6	R/W	ROW0[22]	0
5	R/W	ROW0[21]	0
4	R/W	ROW0[20]	0
3	R/W	ROW0[19]	0
2	R/W	ROW0[18]	0
1	R/W	ROW0[17]	0
0	R/W	ROW0[16]	0

This register contains either the data to be written into the Egress VC Table Row 0 Word 1 external SRAM or the data read from the external SRAM when a read request has been completed. If data is to be written to Egress VC Table external SRAM Row 0, the MSW word must be written to this register before the Egress VC Table Record Address register and the Row Select and Access Control register are written. If data is to be read from Row 0 this register contains the data from Row 0 Word 1 (MSW) after the external SRAM access is completed.

Register 0x2B0: Egress VC Table Record Row 1, Word 0 (LSW) RAM Data

Register 0x2B1: Egress VC Table Record Row 1, Word 1 (MSW) RAM Data

Register 0x2B2: Egress VC Table Record Row 2, Word 0 (LSW) RAM Data

Register 0x2B3: Egress VC Table Record Row 2, Word 1 (MSW) RAM Data

Register 0x2B4: Egress VC Table Record Row 3, Word 0 (LSW) RAM Data

Register 0x2B5: Egress VC Table Record Row 3, Word 1 (MSW) RAM Data

Register 0x2B6: Egress VC Table Record Row 4, Word 0 (LSW) RAM Data

Register 0x2B7: Egress VC Table Record Row 4, Word 1 (MSW) RAM Data

Register 0x2B8: Egress VC Table Record Row 5, Word 0 (LSW) RAM Data

Register 0x2B9: Egress VC Table Record Row 5, Word 1 (MSW) RAM Data

Register 0x2BA: Egress VC Table Record Row 6, Word 0 (LSW) RAM Data

Register 0x2BB: Egress VC Table Record Row 6, Word 1 (MSW) RAM Data

Register 0x2BC: Egress VC Table Record Row 7, Word 0 (LSW) RAM Data

Register 0x2BD: Egress VC Table Record Row 7, Word 1 (MSW) RAM Data

Register 0x2BE: Egress VC Table Record Row 8 Word 0 (LSW) RAM Data

Register 0x2BF: Egress VC Table Record Row 8 Word 1 (MSW) RAM Data

Register 0x2C0: Egress VC Table Record Row 9 Word 0 (LSW) RAM Data

Register 0x2C1: Egress VC Table Record Row 9 Word 1 (MSW) RAM Data

Register 0x2C2: Egress VC Table Record Row 10 Word 0 (LSW) RAM Data

Register 0x2C3: Egress VC Table Record Row 10 Word 1 (MSW) RAM Data

Register 0x2C4: Egress VC Table Record Row 11 Word 0 (LSW) RAM Data

Register 0x2C5: Egress VC Table Record Row 11 Word 1 (MSW) RAM Data

Register 0x2C6: Egress VC Table Record Row 12 Word 0 (LSW) RAM Data

Register 0x2C7: Egress VC Table Record Row 12 Word 1 (MSW) RAM Data

Register 0x2C8: Egress VC Table Record Row 13 Word 0 (LSW) RAM Data

Register 0x2C9: Egress VC Table Record Row 13 Word 1 (MSW) RAM Data

Register 0x2CA: Egress VC Table Record Row 14 Word 0 (LSW) RAM Data

Register 0x2CB: Egress VC Table Record Row 14 Word 1 (MSW) RAM Data

Register 0x2CC: Egress VC Table Record Row 15 Word 0 (LSW) RAM Data

Register 0x2CD: Egress VC Table Record Row 15 Word 1 (MSW) RAM Data

Register 0x2CE: Egress Performance Monitoring RAM Record Address

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7	R/W	PM Bank	0
6	R/W	PM Addr[6]	0
5	R/W	PM Addr[5]	0
4	R/W	PM Addr[4]	0
3	R/W	PM Addr[3]	0
2	R/W	PM Addr[2]	0
1	R/W	PM Addr[1]	0
0	R/W	PM Addr[0]	0

PM Bank:

The PM Bank bit determines which bank of PM data will be accessed. If this bit is logic 0, the PM Addr[6:0] field will access the desired data for the first bank of internal PM RAM. If this bit is logic 1, the PM Addr[6:0] field will access the desired data for the second bank of internal PM Ram.

PM Addr[6:0]:

This field specifies which of the 128 possible PM Sessions to access. The PM Bank bit determines whether Bank 1 or Bank 2 of a particular PM Address will be selected.

Register 0x2CF: Egress Performance Monitoring RAM Row Select and Access Control

Bit	Type	Function	Default
15	R/W	RWB	0
14	R	BUSY	X
13	R/W	CLRONRD	0
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2	R/W	PM Row[2]	0
1	R/W	PM Row[1]	0
0	R/W	PM Row[0]	0

PM Row[2:0]:

This field determines which row of internal PM data will be accessed. If the first row is desired (i.e. Row 0), the setting this field to PM Row[2:0] = '000' will access this row. If the eighth row is desired (i.e. Row 7), then setting this field to PM Row[2:0]='111' will access this row.

CLRONRD:

If CLRONRD is logic 1, after a read access of rows 3,4,5,6, or 7 of the Ingress PM RAM is specified in this register, a clearing write of the row will be initiated. The Fwd SECBC (running count) and Bwd SECBC (copied) will be preserved.

If CLRONRD is logic 0, no write back to clear the data bits is initiated.

BUSY:

The BUSY bit is high while a Microprocessor initiated access request to the Egress PM RAM data is pending the BUSY bit is deasserted only after all the access required has been completed. This register should be polled until the BUSY bit goes low before another microprocessor access request is initiated. A microprocessor access request is typically completed within 35 ESYSCLK cycles. If the ESTANDBY bit in the ATLAS Master Configuration register is a logic 1, the access time is reduced to less than 5 ESYSCLK cycles.

RWB:

The RWB bit selects the operation to be performed on the addressed Egress PM Ram Data: when RWB is set to a logic 1, a read from the internal SRAM is requested; when RWB is set to a logic 0, a write to the internal SRAM is requested.

Register 0x2D0: Egress Performance Monitoring RAM Write Mask

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9	R/W	WM[9]	0
8	R/W	WM[8]	0
7	R/W	WM[7]	0
6	R/W	WM[6]	0
5	R/W	WM[5]	0
4	R/W	WM[4]	0
3	R/W	WM[3]	0
2	R/W	WM[2]	0
1	R/W	WM[1]	0
0	R/W	WM[0]	0

WM[9:0]:

The write mask (WM[9:0]) is used to select which bytes of the Egress PM Internal RAM data will be written during a write operation. If any of WM[9:0] are logic 1 during a write operation, the ECP performs a read-write-back operation when a write is requested, so the value of that byte is not changed in the internal RAM. WM[9] controls the mask to bits [79:72] of the Egress PM RAM Data, and WM[0] controls the mask to bits [7:0] of the Egress PM RAM Data. This allows the ECP to write to selected fields in a row of the Egress PM Ram Data.

Register 0x2D1: Egress Performance Monitoring RAM Data Word 0 (LSW)

Bit	Type	Function	Default
15	R/W	PMData[15]	0
14	R/W	PMData[14]	0
13	R/W	PMData[13]	0
12	R/W	PMData[12]	0
11	R/W	PMData[11]	0
10	R/W	PMData[10]	0
9	R/W	PMData[9]	0
8	R/W	PMData[8]	0
7	R/W	PMData[7]	0
6	R/W	PMData[6]	0
5	R/W	PMData[5]	0
4	R/W	PMData[4]	0
3	R/W	PMData[3]	0
2	R/W	PMData[2]	0
1	R/W	PMData[1]	0
0	R/W	PMData[0]	0

This register contains either the data to be written into the Egress PM RAM Data Word 0 (LSW) or the data read from the internal Egress PM RAM when a read request has been completed. If data is to be written to Egress PM RAM Data, the LSW word must be written to this register before the Egress PM RAM Select and Access Control register are written. If data is to be read from the Egress PM RAM, this register contains the data from Word 0 (LSW) after the internal SRAM access is completed.

Register 0x2D2: Egress Performance Monitoring RAM Data Word 1

Bit	Type	Function	Default
15	R/W	PMData[31]	0
14	R/W	PMData[30]	0
13	R/W	PMData[29]	0
12	R/W	PMData[28]	0
11	R/W	PMData[27]	0
10	R/W	PMData[26]	0
9	R/W	PMData[25]	0
8	R/W	PMData[24]	0
7	R/W	PMData[23]	0
6	R/W	PMData[22]	0
5	R/W	PMData[21]	0
4	R/W	PMData[20]	0
3	R/W	PMData[19]	0
2	R/W	PMData[18]	0
1	R/W	PMData[17]	0
0	R/W	PMData[16]	0

This register contains either the data to be written into the Egress PM RAM Data Word 1 or the data read from the internal Egress PM RAM when a read request has been completed. If data is to be written to Egress PM RAM Data Word 1, the word must be written to this register before the Egress PM RAM Select and Access Control register are written. If data is to be read from the Egress PM RAM this register contains the data from Word 1 after the internal SRAM access is completed.

Register 0x2D3: Egress Performance Monitoring RAM Data Word 2

Bit	Type	Function	Default
15	R/W	PMData[47]	0
14	R/W	PMData[46]	0
13	R/W	PMData[45]	0
12	R/W	PMData[44]	0
11	R/W	PMData[43]	0
10	R/W	PMData[42]	0
9	R/W	PMData[41]	0
8	R/W	PMData[40]	0
7	R/W	PMData[39]	0
6	R/W	PMData[38]	0
5	R/W	PMData[37]	0
4	R/W	PMData[36]	0
3	R/W	PMData[35]	0
2	R/W	PMData[34]	0
1	R/W	PMData[33]	0
0	R/W	PMData[32]	0

This register contains either the data to be written into the Egress PM RAM Data Word 2 or the data read from the internal Egress PM RAM when a read request has been completed. If data is to be written to Egress PM RAM Data Word 2, the word to be written must be written to this register before the Egress PM RAM Select and Access Control register are written. If data is to be read from the Egress PM RAM this register contains the data from Word 2 after the internal SRAM access is completed.

Register 0x2D4: Egress Performance Monitoring RAM Data Word3

Bit	Type	Function	Default
15	R/W	PMData[63]	0
14	R/W	PMData[62]	0
13	R/W	PMData[61]	0
12	R/W	PMData[60]	0
11	R/W	PMData[59]	0
10	R/W	PMData[58]	0
9	R/W	PMData[57]	0
8	R/W	PMData[56]	0
7	R/W	PMData[55]	0
6	R/W	PMData[54]	0
5	R/W	PMData[53]	0
4	R/W	PMData[52]	0
3	R/W	PMData[51]	0
2	R/W	PMData[50]	0
1	R/W	PMData[49]	0
0	R/W	PMData[48]	0

This register contains either the data to be written into the Egress PM RAM Data Word 3 or the data read from the internal Egress PM RAM when a read request has been completed. If data is to be written to Egress PM RAM Data Word 3, the word to be written must be written to this register before the Egress PM RAM Select and Access Control register are written. If data is to be read from the Egress PM RAM this register contains the data from Word 3 after the internal SRAM access is completed.

Register 0x2D5: Egress Performance Monitoring RAM Data Word 4 (MSW)

Bit	Type	Function	Default
15	R/W	PMData[79]	0
14	R/W	PMData[78]	0
13	R/W	PMData[77]	0
12	R/W	PMData[76]	0
11	R/W	PMData[75]	0
10	R/W	PMData[74]	0
9	R/W	PMData[73]	0
8	R/W	PMData[72]	0
7	R/W	PMData[71]	0
6	R/W	PMData[70]	0
5	R/W	PMData[69]	0
4	R/W	PMData[68]	0
3	R/W	PMData[67]	0
2	R/W	PMData[66]	0
1	R/W	PMData[65]	0
0	R/W	PMData[64]	0

This register contains either the data to be written into the Egress PM RAM Data Word 4 (MSW) or the data read from the internal Egress PM RAM when a read request has been completed. If data is to be written to Egress PM RAM Data Word 4, the word to be written must be written to this register before the Egress PM RAM Select and Access Control register are written. If data is to be read from the Egress PM RAM this register contains the data from Word 4 after the internal SRAM access is completed.

Register 0x2D6: Egress VC Table Change of Connection Status Data (LSW)

Bit	Type	Function	Default
15	R	COSDATA[15]	X
14	R	COSDATA[14]	X
13	R	COSDATA[13]	X
12	R	COSDATA[12]	X
11	R	COSDATA[11]	X
10	R	COSDATA[10]	X
9	R	COSDATA[9]	X
8	R	COSDATA[8]	X
7	R	COSDATA[7]	X
6	R	COSDATA[6]	X
5	R	COSDATA[5]	X
4	R	COSDATA[4]	X
3	R	COSDATA[3]	X
2	R	COSDATA[2]	X
1	R	COSDATA[1]	X
0	R	COSDATA[0]	X

COSDATA[15:0]:

This register contains the 16-bit connection ID of a connection in the Egress VC Table which has undergone a change in connection state. This is the least significant 16-bits of data in the Egress Change of State FIFO.

This data is only valid when the COSVALID bit in register 0x2D7 is logic 1.

The COS FIFO read-pointer is incremented upon a read of this register.

Register 0x2D7: Egress VC Table Change of Connection Status Data (MSW)

Bit	Type	Function	Default
15	R	COSFULL	X
14	R	COSVALID	X
13	R	BUSY	X
12		Unused	X
11		Unused	X
10		Unused	X
9	R	COSDATA[25]	X
8	R	COSDATA[24]	X
7	R	COSDATA[23]	X
6	R	COSDATA[22]	X
5	R	COSDATA[21]	X
4	R	COSDATA[20]	X
3	R	COSDATA[19]	X
2	R	COSDATA[18]	X
1	R	COSDATA[17]	X
0	R	COSDATA[16]	X

COSDATA[25:16]:

The COS[25:16] field contains the Status field of a connection whose address is identified by the COS[15:0] register. COSDATA[25] is the Segment End-Point bit (if this bit is logic 1, the connection is configured as a segment end-point), COSDATA[25] is the End-to-End point bit (if this bit is logic 1, the connection is configured as an end-to-end point), COSDATA[23:16] is the Status field (LSB justified with COSDATA[23:15] set to logic 0) of the connection. The presence of data in this register indicates that the connection has undergone a change in connection state. This is the most significant 8-bits of the Egress Change of State FIFO.

Each time the Egress VC Table Change of Connection Status Data LSW register is read, the FIFO read pointer is incremented. The COSVALID register bit indicates whether or not the data in this register are valid.

BUSY:

If this bit is logic 1, the read-pointer of the COS FIFO is being updated. The COSVALID bit is not defined while BUSY is asserted. When BUSY is deasserted, the state of the COSVALID bit is defined.

COSVALID:

If this bit is logic 1, the data in this register and the Egress VC Table Change of Connection Status Data (LSB) are valid. The state of the COSVALID bit is not defined while the BUSY bit is asserted (the BUSY bit is asserted while the COS FIFO read-pointer is being updated). When BUSY is deasserted, the state of the COSVALID bit is defined.

COSFULL:

If this register bit is logic 1, the Egress Change of State FIFO is full, and no more change of connection state data can be written into the FIFO. This will suspend the Egress background process which monitors connection for change in connection state. It is the responsibility of the management software to ensure this register is read often enough to ensure the monitoring and notifications of changes in connection state are compliant to Bellcore and ITU standards.

Register 0x400: Ingress Per-PHY Counter Configuration

Bit	Type	Function	Default
15	R	BUSY	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1	R/W	Clear_On_Read	0
0	R/W	CounterWrap	0

CounterWrap:

If this bit is logic 1, all Ingress per-PHY counts do not saturate at all ones, rather, they rollover. It is the responsibility of the management software to ensure the per-PHY counts are polled often enough to ensure they do not saturate nor rollover. If this bit is logic 0, all per-PHY counts saturate at all ones.

Clear_On_Read:

If this bit is logic 1, all Ingress per-PHY counts are cleared (i.e. reset to zero) when a read of the Ingress per-PHY counts in initiated. If this bit is logic 0, the Ingress per-PHY counts are not reset to zero after a read is initiated.

BUSY:

This BUSY bit is high while a Microprocessor initiated access request to the Ingress per-PHY counts is pending. The BUSY bit is deasserted only after all the access required has been completed. This register should be polled until the BUSY bit goes low before another

microprocessor access request is initiated. A microprocessor access request is typically completed within 39 ISYSCLK cycles.

Register 0x401: PHY1 Ingress Counter Status

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9	R	UNKVPIVCICH	X
8	R	GFCCH	X
7	R	INVALIDCH	X
6	R	OAMERRCH	X
5	R	RMCH	X
4	R	OAMCH	X
3	R	CLP1CH	X
2	R	CLP0CH	X
1	R	XFER	X
0	R	OVR	X

This register contains status information indicating when counter data has been transferred into the holding registers and indicating whether the holding registers have been overrun. It also indicates if any of the counts are non-zero.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 indicates that a previous transfer (indicated by XFER being a logic 1) has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register. The XFERI bit of the Master Interrupt Status #1 register is set when the OVR bit is asserted.

XFER:

The XFER bit indicates that a transfer of counter data has occurred. A logic 1 in this bit position indicates that a latch request, initiated by writing to one of the counter register

locations was received and a transfer of the counter values has occurred. A logic 0 indicates that no transfer has occurred. The XFER bit is cleared by reading this register. The XFERI bit of the Master Interrupt Status #1 register is set when the XFER bit is asserted.

CLP0CH:

The CLP0CH bit is set to logic 1 if the CLP0 cell count register contains a non-zero value.

CLP1CH:

The CLP1CH bit is set to logic 1 if the CLP1 cell count register contains a non-zero value.

OAMCH:

The OAMCH bit is set to logic 1 if the OAM cell count register contains a non-zero value.

RMCH:

The RMCH bit is set to logic 1 if the RM cell count register contains a non-zero value.

OAMERRCH:

The OAMERRCH bit is set to logic 1 if the Errored OAM cell count register contains a non-zero value.

INVALIDCH:

The INVALIDCH bit is set to logic 1 if the Invalid cell count register contains a non-zero value.

GFCCH:

The GFCCH bit is set to logic 1 if the count of received cells with non-zero GFC register contains a non-zero value.

UNKVPIVCICH:

The UNKVPIVCICH bit is set to logic 1 if the last unknown VPI.VCI has changed.

Register 0x402: PHY1 Ingress CLP0 Cell Count (LSB)

Bit	Type	Function	Default
15	R	CLP0[15]	X
14	R	CLP0[14]	X
13	R	CLP0[13]	X
12	R	CLP0[12]	X
11	R	CLP0[11]	X
10	R	CLP0[10]	X
9	R	CLP0[9]	X
8	R	CLP0[8]	X
7	R	CLP0[7]	X
6	R	CLP0[6]	X
5	R	CLP0[5]	X
4	R	CLP0[4]	X
3	R	CLP0[3]	X
2	R	CLP0[2]	X
1	R	CLP0[1]	X
0	R	CLP0[0]	X

CLP0[15:0]:

This register contains the least significant 16-bits of the count of CLP=0 cells received in the Ingress direction of PHY 1 that have been received since the last time the count was transferred. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ISYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Ingress per-PHY CLP0 Cell Counters are incremented whether or not the VC is identified in a valid search or the active bit is set.Register 0x403: PHY1 Ingress CLP0 Cell Count (MSB)

Bit	Type	Function	Default
15	R	CLP0[31]	X
14	R	CLP0[30]	X
13	R	CLP0[29]	X
12	R	CLP0[28]	X
11	R	CLP0[27]	X
10	R	CLP0[26]	X
9	R	CLP0[25]	X
8	R	CLP0[24]	X
7	R	CLP0[23]	X
6	R	CLP0[22]	X
5	R	CLP0[21]	X
4	R	CLP0[20]	X
3	R	CLP0[19]	X
2	R	CLP0[18]	X
1	R	CLP0[17]	X
0	R	CLP0[16]	X

CLP0[31:16]:

This register contains the most significant 16-bits of the count of CLP=0 cells received in the Ingress direction of PHY 1 that have been received since the last time the count was transferred. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ISYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Ingress per-PHY CLP0 Cell Counters are incremented whether or not the VC is identified in a valid search or the active bit is set.

Register 0x404: PHY1 Ingress CLP1 Cell Count (LSB)

Bit	Type	Function	Default
15	R	CLP1[15]	X
14	R	CLP1[14]	X
13	R	CLP1[13]	X
12	R	CLP1[12]	X
11	R	CLP1[11]	X
10	R	CLP1[10]	X
9	R	CLP1[9]	X
8	R	CLP1[8]	X
7	R	CLP1[7]	X
6	R	CLP1[6]	X
5	R	CLP1[5]	X
4	R	CLP1[4]	X
3	R	CLP1[3]	X
2	R	CLP1[2]	X
1	R	CLP1[1]	X
0	R	CLP1[0]	X

CLP1[15:0]:

This register contains the least significant 16-bits of the count of CLP=1 cells received in the Ingress direction of PHY 1 that have been received since the last time the count was transferred. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ISYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Ingress per-PHY CLP1 Cell Counters are incremented whether or not the VC is identified in a valid search or the active bit is set.

Register 0x405: PHY1 Ingress CLP1 Cell Count (MSB)

Bit	Type	Function	Default
15	R	CLP1[31]	X

Bit	Type	Function	Default
14	R	CLP1[30]	X
13	R	CLP1[29]	X
12	R	CLP1[28]	X
11	R	CLP1[27]	X
10	R	CLP1[26]	X
9	R	CLP1[25]	X
8	R	CLP1[24]	X
7	R	CLP1[23]	X
6	R	CLP1[22]	X
5	R	CLP1[21]	X
4	R	CLP1[20]	X
3	R	CLP1[19]	X
2	R	CLP1[18]	X
1	R	CLP1[17]	X
0	R	CLP1[16]	X

CLP1[31:16]:

This register contains the most significant 16-bits of the count of CLP=1 cells received in the Ingress direction of PHY 1 that have been received since the last time the count was transferred. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ISYSCLK cycles and simultaneously the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost. The Ingress per-PHY CLP1 Cell Counters are incremented whether or not the VC is identified in a valid search or the active bit is set.

Register 0x406: PHY1 Ingress Valid OAM Cell Count

Bit	Type	Function	Default
15	R	OAMCNT[15]	X
14	R	OAMCNT[14]	X
13	R	OAMCNT[13]	X
12	R	OAMCNT[12]	X
11	R	OAMCNT[11]	X

Bit	Type	Function	Default
10	R	OAMCNT[10]	X
9	R	OAMCNT[9]	X
8	R	OAMCNT[8]	X
7	R	OAMCNT[7]	X
6	R	OAMCNT[6]	X
5	R	OAMCNT[5]	X
4	R	OAMCNT[4]	X
3	R	OAMCNT[3]	X
2	R	OAMCNT[2]	X
1	R	OAMCNT[1]	X
0	R	OAMCNT[0]	X

OAMCNT[15:0]:

This register contains the count valid OAM cells received in the Ingress direction of PHY 1 that have been received since the last time the count was transferred. The counter will be incremented for all OAM cells belonging to provisioned connections for which no error was detected. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ISYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Ingress per-PHY Valid OAM Cell Counters are only incremented when a VC is identified in a valid search (i.e. the search did not time out and the validation step passed).

Register 0x407: PHY1 Ingress Valid RM Cell Count

Bit	Type	Function	Default
15	R	RMCNT[15]	X
14	R	RMCNT[14]	X
13	R	RMCNT[13]	X
12	R	RMCNT[12]	X
11	R	RMCNT[11]	X
10	R	RMCNT[10]	X
9	R	RMCNT[9]	X
8	R	RMCNT[8]	X
7	R	RMCNT[7]	X
6	R	RMCNT[6]	X
5	R	RMCNT[5]	X
4	R	RMCNT[4]	X
3	R	RMCNT[3]	X
2	R	RMCNT[2]	X
1	R	RMCNT[1]	X
0	R	RMCNT[0]	X

RMCNT[15:0]:

This register contains the count of valid RM cells received in the Ingress direction of PHY 1 that have been received since the last time the count was transferred. The counter will be incremented for all RM cells belonging to provisioned connections for which no error was detected. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ISYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Ingress per-PHY Valid RM Cell Counters are only incremented when a VC is identified in a valid search (i.e. the search did not time out and the validation step passed).

Register 0x408: PHY1 Ingress Errored OAM/RM Cell Count

Bit	Type	Function	Default
15	R	EOAMRM[15]	X
14	R	EOAMRM[14]	X
13	R	EOAMRM[13]	X
12	R	EOAMRM[12]	X
11	R	EOAMRM[11]	X
10	R	EOAMRM[10]	X
9	R	EOAMRM[9]	X
8	R	EOAMRM[8]	X
7	R	EOAMRM[7]	X
6	R	EOAMRM[6]	X
5	R	EOAMRM[5]	X
4	R	EOAMRM[4]	X
3	R	EOAMRM[3]	X
2	R	EOAMRM[2]	X
1	R	EOAMRM[1]	X
0	R	EOAMRM[0]	X

EOAMRM[15:0]:

This register contains the count Errored OAM and RM cells received in the Ingress direction of PHY 1 that have been received since the last time the count was transferred. The count records OAM cells with CRC-10 errors, invalid OAM Type or an invalid Function Type field. The count will also capture RM cells with CRC-10 errors. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ISYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Ingress per-PHY Errored OAM/RM Cell Counters are only incremented when a VC is identified in a valid search (i.e. the search did not time out and the validation step passed).

Register 0x409: PHY1 Ingress Invalid VPI/VCI/PTI Cell Count

Bit	Type	Function	Default
15	R	INVALIDCNT[15]	X
14	R	INVALIDCNT[14]	X
13	R	INVALIDCNT[13]	X
12	R	INVALIDCNT[12]	X
11	R	INVALIDCNT[11]	X
10	R	INVALIDCNT[10]	X
9	R	INVALIDCNT[9]	X
8	R	INVALIDCNT[8]	X
7	R	INVALIDCNT[7]	X
6	R	INVALIDCNT[6]	X
5	R	INVALIDCNT[5]	X
4	R	INVALIDCNT[4]	X
3	R	INVALIDCNT[3]	X
2	R	INVALIDCNT[2]	X
1	R	INVALIDCNT[1]	X
0	R	INVALIDCNT[0]	X

INVALIDCNT[15:0]:

The INVALIDCNT[15:0] bits represent the number of cells with invalid headers that have been received since the last time the count was transferred. The count includes the following types of errors:

1. A F5 cell containing PTI = '111'
2. A F4 cell with a VCI = {0,7 to 15}.
3. A VP RM cell with PTI not equal to '110'.
4. An improperly constructed secondary search table (search takes more 41 cycles).
5. A cell with an unprovisioned VPI/VCI or invalid routing bits.

When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ISYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

Register 0x40A: PHY1 Ingress Non-Zero GFC Cell Count

Bit	Type	Function	Default
15	R	NZGFC[15]	X
14	R	NZGFC[14]	X
13	R	NZGFC[13]	X
12	R	NZGFC[12]	X
11	R	NZGFC[11]	X
10	R	NZGFC[10]	X
9	R	NZGFC[9]	X
8	R	NZGFC[8]	X
7	R	NZGFC[7]	X
6	R	NZGFC[6]	X
5	R	NZGFC[5]	X
4	R	NZGFC[4]	X
3	R	NZGFC[3]	X
2	R	NZGFC[2]	X
1	R	NZGFC[1]	X
0	R	NZGFC[0]	X

NZGFC[15:0]:

This register contains the count of cells with a Non-Zero GFC field received in the Ingress direction of PHY 1 since the last time the count was transferred. The count will also capture RM cells with CRC-10 errors. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ISYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Ingress per-PHY Non-Zero GFC Cell Counters are only incremented when a VC is identified in a valid search (i.e. the search did not time out and the validation step passed). Register 0x40B: PHY1 Ingress Last Unknown VPI.VCI (VCI value)

Bit	Type	Function	Default
15	R	LUNKVCI[15]	X
14	R	LUNKVCI[14]	X
13	R	LUNKVCI[13]	X
12	R	LUNKVCI[12]	X
11	R	LUNKVCI[11]	X
10	R	LUNKVCI[10]	X
9	R	LUNKVCI[9]	X
8	R	LUNKVCI[8]	X
7	R	LUNKVCI[7]	X
6	R	LUNKVCI[6]	X
5	R	LUNKVCI[5]	X
4	R	LUNKVCI[4]	X
3	R	LUNKVCI[3]	X
2	R	LUNKVCI[2]	X
1	R	LUNKVCI[1]	X
0	R	LUNKVCI[0]	X

LUNKVCI[15:0]:

This register contains the VCI value of the last cell which was not provisioned or failed the search. This register is overwritten when a new unknown VPI/VCI is found. When this register is updated the UNKVPIVCICH register bit is set to logic one and the I_SRCHERRI interrupt register bit is set to logic one. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ISYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

Register 0x40C: PHY1 Ingress Last Unknown VPI.VCI (VPI value)

Bit	Type	Function	Default
15	R	Unused	X
14	R	Unused	X
13	R	Unused	X
12	R	Unused	X
11	R	LUNKVPI[11]	X
10	R	LUNKVPI[10]	X
9	R	LUNKVPI[9]	X
8	R	LUNKVPI[8]	X
7	R	LUNKVPI[7]	X
6	R	LUNKVPI[6]	X
5	R	LUNKVPI[5]	X
4	R	LUNKVPI[4]	X
3	R	LUNKVPI[3]	X
2	R	LUNKVPI[2]	X
1	R	LUNKVPI[1]	X
0	R	LUNKVPI[0]	X

LUNKVPI[11:0]:

This register contains the VPI value of the last cell which was not provisioned or failed the search. This register is overwritten when a new unknown VPI/VCI is found. When this register is updated the UNKVPIVCICH register bit is set to logic one and the I_SRCHERRI interrupt register bit is set to logic one. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ISYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

Register 0x410: PHY2 Reserved

Register 0x411: PHY2 Ingress Counter Status

Register 0x412: PHY2 Ingress CLP0 Cell Count (LSB)

Register 0x413: PHY2 Ingress CLP0 Cell Count (MSB)

Register 0x414: PHY2 Ingress CLP1 Cell Count (LSB)

Register 0x415: PHY2 Ingress CLP1 Cell Count (MSB)

Register 0x416: PHY2 Ingress Valid OAM Cell Count

Register 0x417: PHY2 Ingress Valid RM Cell Count

Register 0x418: PHY2 Ingress Errored OAM/RM Cell Count

Register 0x419: PHY2 Ingress Invalid VPI/VCI/PTI Cell Count

Register 0x41A: PHY2 Ingress Non-Zero GFC Cell Count

Register 0x41B: PHY2 Ingress Last Unknown VPI.VCI (VCI value)

Register 0x41C: PHY2 Ingress Last Unknown VPI.VCI (VPI value)

Register 0x420-0x42C: PHY3 Ingress Status and Counts

Register 0x430-0x43C: PHY4 Ingress Status and Counts

Register 0x440-0x44C: PHY5 Ingress Status and Counts

Register 0x450-0x45C: PHY6 Ingress Status and Counts

Register 0x460-0x46C: PHY7 Ingress Status and Counts

Register 0x470-0x47C: PHY8 Ingress Status and Counts

Register 0x480-0x48C: PHY9 Ingress Status and Counts

Register 0x490-0x49C: PHY10 Ingress Status and Counts

Register 0x4A0-0x4AC: PHY11 Ingress Status and Counts

Register 0x4B0-0x4BC: PHY12 Ingress Status and Counts

Register 0x4C0-0x4CC: PHY13 Ingress Status and Counts

Register 0x4D0-0x4DC: PHY14 Ingress Status and Counts

Register 0x4E0-0x4EC: PHY15 Ingress Status and Counts

Register 0x4F0-0x4FC: PHY16 Ingress Status and Counts

Register 0x500-0x50C: PHY17 Ingress Status and Counts

Register 0x510-0x51C: PHY18 Ingress Status and Counts

Register 0x520-0x52C: PHY19 Ingress Status and Counts

Register 0x530-0x53C: PHY20 Ingress Status and Counts

Register 0x540-0x54C: PHY21 Ingress Status and Counts

Register 0x550-0x55C: PHY22 Ingress Status and Counts

Register 0x560-0x56C: PHY23 Ingress Status and Counts

Register 0x570-0x57C: PHY24 Ingress Status and Counts

Register 0x580-0x58C: PHY25 Ingress Status and Counts

Register 0x590-0x59C: PHY26 Ingress Status and Counts

Register 0x5A0-0x5AC: PHY27 Ingress Status and Counts

Register 0x5B0-0x5BC: PHY28 Ingress Status and Counts

Register 0x5C0-0x5CC: PHY29 Ingress Status and Counts

Register 0x5D0-0x5DC: PHY30 Ingress Status and Counts

Register 0x5E0-0x5EC: PHY31 Ingress Status and Counts

Register 0x5F0-0x5FC: PHY32 Ingress Status and Counts

Register 0x600: Egress Per-PHY Counter Configuration

Bit	Type	Function	Default
15	R	BUSY	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1	R/W	Clear_On_Read	0
0	R/W	CounterWrap	0

CounterWrap:

If this bit is logic 1, all Egress per-PHY counts do not saturate at all ones, rather, they rollover. It is the responsibility of the management software to ensure the per-PHY counts are polled often enough to ensure they do not saturate nor rollover. If this bit is logic 0, all per-PHY counts saturate at all ones.

Clear_On_Read:

If this bit is logic 1, all Egress per-PHY counts are cleared (i.e. reset to zero) when a read of the Egress per-PHY counts is initiated. If this bit is logic 0, the Egress per-PHY counts are not cleared after a read is initiated.

BUSY:

This BUSY bit is high while a Microprocessor initiated access request to the Egress per-PHY counts is pending. The BUSY bit is deasserted only after all the access required has been completed. This register should be polled until the BUSY bit goes low before another

microprocessor access request is initiated. A microprocessor access request is typically completed within 39 ESYSCLK cycles.

Register 0x601: PHY1 Egress Counter Status

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7	R	INVALIDCH	X
6	R	OAMERRCH	X
5	R	RMCH	X
4	R	OAMCH	X
3	R	CLP1CH	X
2	R	CLP0CH	X
1	R	XFER	X
0	R	OVR	X

This register contains status information indicating when counter data has been transferred into the holding registers and indicating whether the holding registers have been overrun. It also indicates if any of the counts are non-zero.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 indicates that a previous transfer (indicated by XFER being a logic 1) has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register. The XFERI bit of the Master Interrupt Status #1 register is set when the OVR bit is asserted.

XFER:

The XFER bit indicates that a transfer of counter data has occurred. A logic 1 in this bit position indicates that a latch request, initiated by writing to one of the counter register

locations was received and a transfer of the counter values has occurred. A logic 0 indicates that no transfer has occurred. The XFER bit is cleared by reading this register. The XFERI bit of the Master Interrupt Status #1 register is set when the XFER bit is asserted.

CLP0CH:

The CLP0CH bit is set to logic 1 if the CLP0 cell count register contains a non-zero value.

CLP1CH:

The CLP1CH bit is set to logic 1 if the CLP1 cell count register contains a non-zero value.

OAMCH:

The OAMCH bit is set to logic 1 if the OAM cell count register contains a non-zero value.

RMCH:

The RMCH bit is set to logic 1 if the RM cell count register contains a non-zero value.

OAMERRCH:

The OAMERRCH bit is set to logic 1 if the Errored OAM cell count register contains a non-zero value.

INVALIDCH:

The INVALVPIVCICH bit is set to logic 1 if the Invalid VPI/VCI/PTI cell count register contains a non-zero value.

Register 0x602: PHY1 Egress CLP0 Cell Count (LSB)

Bit	Type	Function	Default
15	R	CLP0[15]	X
14	R	CLP0[14]	X
13	R	CLP0[13]	X
12	R	CLP0[12]	X
11	R	CLP0[11]	X
10	R	CLP0[10]	X
9	R	CLP0[9]	X
8	R	CLP0[8]	X
7	R	CLP0[7]	X
6	R	CLP0[6]	X
5	R	CLP0[5]	X
4	R	CLP0[4]	X
3	R	CLP0[3]	X
2	R	CLP0[2]	X
1	R	CLP0[1]	X
0	R	CLP0[0]	X

CLP0[15:0]:

This register contains the least significant 16-bits of the count of CLP=0 cells received in the Egress direction of PHY 1 that have been received since the last time the count was transferred. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ESYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Egress per-PHY CLP0 Cell Counters are incremented whether or not the active bit is set.

Register 0x603: PHY1 Egress CLP0 Cell Count (MSB)

Bit	Type	Function	Default
15	R	CLP0[31]	X
14	R	CLP0[30]	X
13	R	CLP0[29]	X
12	R	CLP0[28]	X
11	R	CLP0[27]	X
10	R	CLP0[26]	X
9	R	CLP0[25]	X
8	R	CLP0[24]	X
7	R	CLP0[23]	X
6	R	CLP0[22]	X
5	R	CLP0[21]	X
4	R	CLP0[20]	X
3	R	CLP0[19]	X
2	R	CLP0[18]	X
1	R	CLP0[17]	X
0	R	CLP0[16]	X

CLP0[31:16]:

This register contains the most significant 16-bits of the count of CLP=0 cells received in the Egress direction of PHY 1 that have been received since the last time the count was transferred. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ESYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Egress per-PHY CLP0 Cell Counters are incremented whether or not the active bit is set.

Register 0x604: PHY1 Egress CLP1 Cell Count (LSB)

Bit	Type	Function	Default
15	R	CLP1[15]	X
14	R	CLP1[14]	X
13	R	CLP1[13]	X
12	R	CLP1[12]	X
11	R	CLP1[11]	X
10	R	CLP1[10]	X
9	R	CLP1[9]	X
8	R	CLP1[8]	X
7	R	CLP1[7]	X
6	R	CLP1[6]	X
5	R	CLP1[5]	X
4	R	CLP1[4]	X
3	R	CLP1[3]	X
2	R	CLP1[2]	X
1	R	CLP1[1]	X
0	R	CLP1[0]	X

CLP1[15:0]:

This register contains the least significant 16-bits of the count of CLP=1 cells received in the Egress direction of PHY 1 that have been received since the last time the count was transferred. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ESYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Egress per-PHY CLP1 Cell Counters are incremented whether or not the active bit is set.

Register 0x605: PHY1 Egress CLP1 Cell Count (MSB)

Bit	Type	Function	Default
15	R	CLP1[31]	X
14	R	CLP1[30]	X
13	R	CLP1[29]	X
12	R	CLP1[28]	X
11	R	CLP1[27]	X
10	R	CLP1[26]	X
9	R	CLP1[25]	X
8	R	CLP1[24]	X
7	R	CLP1[23]	X
6	R	CLP1[22]	X
5	R	CLP1[21]	X
4	R	CLP1[20]	X
3	R	CLP1[19]	X
2	R	CLP1[18]	X
1	R	CLP1[17]	X
0	R	CLP1[16]	X

CLP1[31:16]:

This register contains the most significant 16-bits of the count of CLP=1 cells received in the Egress direction of PHY 1 that have been received since the last time the count was transferred. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ESYSCLK cycles and simultaneously the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Egress per-PHY CLP1 Cell Counters are incremented whether or not the active bit is set.

Register 0x606: PHY1 Egress Valid OAM Cell Count

Bit	Type	Function	Default
15	R	OAMCNT[15]	X
14	R	OAMCNT[14]	X
13	R	OAMCNT[13]	X
12	R	OAMCNT[12]	X
11	R	OAMCNT[11]	X
10	R	OAMCNT[10]	X
9	R	OAMCNT[9]	X
8	R	OAMCNT[8]	X
7	R	OAMCNT[7]	X
6	R	OAMCNT[6]	X
5	R	OAMCNT[5]	X
4	R	OAMCNT[4]	X
3	R	OAMCNT[3]	X
2	R	OAMCNT[2]	X
1	R	OAMCNT[1]	X
0	R	OAMCNT[0]	X

OAMCNT[15:0]:

This register contains the count valid OAM cells received in the Egress direction of PHY 1 since the last time the count was transferred. The counter will be incremented for all OAM cells belonging to provisioned connections for which no error was detected. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ESYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Egress per-PHY Valid OAM Cell Counters are only incremented when the VC is marked as active and the VC Table address parity check passes, if enabled.

Register 0x607: PHY1 Egress Valid RM Cell Count

Bit	Type	Function	Default
15	R	RMCNT[15]	X

Bit	Type	Function	Default
14	R	RMCNT[14]	X
13	R	RMCNT[13]	X
12	R	RMCNT[12]	X
11	R	RMCNT[11]	X
10	R	RMCNT[10]	X
9	R	RMCNT[9]	X
8	R	RMCNT[8]	X
7	R	RMCNT[7]	X
6	R	RMCNT[6]	X
5	R	RMCNT[5]	X
4	R	RMCNT[4]	X
3	R	RMCNT[3]	X
2	R	RMCNT[2]	X
1	R	RMCNT[1]	X
0	R	RMCNT[0]	X

RMCNT[15:0]:

This register contains the count of valid RM cells received in the Egress direction of PHY 1 since the last time the count was transferred. The counter will be incremented for all RM cells belonging to provisioned connections for which no error was detected. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ESYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Egress per-PHY Valid OAM Cell Counters are only incremented when the VC is marked as active and the VC Table address parity check passes, if enabled.

Register 0x608: PHY1 Egress Errored OAM/RM Cell Count

Bit	Type	Function	Default
15	R	EOAMRM[15]	X
14	R	EOAMRM[14]	X
13	R	EOAMRM[13]	X
12	R	EOAMRM[12]	X

Bit	Type	Function	Default
11	R	EOAMRM[11]	X
10	R	EOAMRM[10]	X
9	R	EOAMRM[9]	X
8	R	EOAMRM[8]	X
7	R	EOAMRM[7]	X
6	R	EOAMRM[6]	X
5	R	EOAMRM[5]	X
4	R	EOAMRM[4]	X
3	R	EOAMRM[3]	X
2	R	EOAMRM[2]	X
1	R	EOAMRM[1]	X
0	R	EOAMRM[0]	X

EOAMRM[15:0]:

This register contains the count Errored OAM and RM cells received in the Egress direction of PHY 1 since the last time the count was transferred. The count records OAM cells with CRC-10 errors, invalid OAM Type or an invalid Function Type field. The count will also capture RM cells with CRC-10 errors. When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ESYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Egress per-PHY Valid OAM Cell Counters are only incremented when the VC is marked as active and the VC Table address parity check passes, if enabled.

Register 0x609: PHY1 Egress Invalid VCI/PTI Cell Count

Bit	Type	Function	Default
15	R	INVALIDCNT[15]	X
14	R	INVALIDCNT[14]	X
13	R	INVALIDCNT[13]	X
12	R	INVALIDCNT[12]	X
11	R	INVALIDCNT[11]	X
10	R	INVALIDCNT[10]	X

Bit	Type	Function	Default
9	R	INVALIDCNT[9]	X
8	R	INVALIDCNT[8]	X
7	R	INVALIDCNT[7]	X
6	R	INVALIDCNT[6]	X
5	R	INVALIDCNT[5]	X
4	R	INVALIDCNT[4]	X
3	R	INVALIDCNT[3]	X
2	R	INVALIDCNT[2]	X
1	R	INVALIDCNT[1]	X
0	R	INVALIDCNT[0]	X

INVALIDCNT[15:0]:

The INVALIDCNT[15:0] bits represent the number of cells with invalid headers that have been received since the last time the count was transferred. The count includes the following types of errors:
1. An F5 cell containing PTI = '111'
2. An F4 cell with a VCI = {0,7 to 15}.
3. A VP RM cell with PTI not equal to '110' and the VPRMSEL register bit is set.
4. An F4 OAM cell is received on an NNI connection and the PTI field does not equal ‘000’ or ‘010’.

When this count is transferred (by writing to register 0x000), the internally accumulated values are transferred to this register within 39 ESYSCLK cycles and simultaneously, the internal counter is reset to begin a new cycle of accumulation. This transfer and reset are carried out in a manner that ensures that coincident events are not lost.

The Egress per-PHY Valid OAM Cell Counters are only incremented when the VC is marked as active and the VC Table address parity check passes, if enabled.

Register 0x610: PHY2 Reserved

Register 0x611: PHY2 Egress Counter Status

Register 0x612: PHY2 Egress CLP0 Cell Count (LSB)

Register 0x613: PHY2 Egress CLP0 Cell Count (MSB)

Register 0x614: PHY2 Egress CLP1 Cell Count (LSB)

Register 0x615: PHY2 Egress CLP1 Cell Count (MSB)

Register 0x616: PHY2 Egress Valid OAM Cell Count

Register 0x617: PHY2 Egress Valid RM Cell Count

Register 0x618: PHY2 Egress Errored OAM/RM Cell Count

Register 0x619: PHY2 Egress Invalid VCI/PTI Cell Count

Register 0x620-0x629: PHY3 Egress Status and Counts

Register 0x630-0x639: PHY4 Egress Status and Counts

Register 0x640-0x649: PHY5 Egress Status and Counts

Register 0x650-0x659: PHY6 Egress Status and Counts

Register 0x660-0x669: PHY7 Egress Status and Counts

Register 0x670-0x679: PHY8 Egress Status and Counts

Register 0x680-0x689: PHY9 Egress Status and Counts

Register 0x690-0x699: PHY10 Egress Status and Counts

Register 0x6A0-0x6A9: PHY11 Egress Status and Counts

Register 0x6B0-0x6B9: PHY12 Egress Status and Counts

Register 0x6C0-0x6C9: PHY13 Egress Status and Counts

Register 0x6D0-0x6D9: PHY14 Egress Status and Counts

Register 0x6E0-0x6E9: PHY15 Egress Status and Counts

Register 0x6F0-0x6F9: PHY16 Egress Status and Counts

Register 0x700-0x709: PHY17 Egress Status and Counts

Register 0x710-0x719: PHY18 Egress Status and Counts

Register 0x720-0x729: PHY19 Egress Status and Counts

Register 0x730-0x739: PHY20 Egress Status and Counts

Register 0x740-0x749: PHY21 Egress Status and Counts

Register 0x750-0x759: PHY22 Egress Status and Counts

Register 0x760-0x769: PHY23 Egress Status and Counts

Register 0x770-0x779: PHY24 Egress Status and Counts

Register 0x780-0x789: PHY25 Egress Status and Counts

Register 0x790-0x799: PHY26 Egress Status and Counts

Register 0x7A0-0x7A9: PHY27 Egress Status and Counts

Register 0x7B0-0x7B9: PHY28 Egress Status and Counts

Register 0x7C0-0x7C9: PHY29 Egress Status and Counts

Register 0x7D0-0x7D9: PHY30 Egress Status and Counts

Register 0x7E0-0x7E9: PHY31 Egress Status and Counts

Register 0x7F0-0x7F9: PHY32 Egress Status and Counts

10 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-ATLAS. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[11]) is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI-ATLAS are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the S/UNI-ATLAS also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be via the JTAG test port.

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x800: Master Test

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-ATLAS test features. Note, PMCTST, DBCTRL and HIZDATA are not reset to zero by a reset of the S/UNI-ATLAS.

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-ATLAS . While the HIZIO bit is a logic one, all output pins of the S/UNI-ATLAS except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

IOTST:

Note, the IOTST bit is NOT used in the S/UNI-ATLAS.

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the S/UNI-ATLAS for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test

mode 0 registers to manipulate the outputs of the block and consequentially the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-ATLAS to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the S/UNI-ATLAS for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-ATLAS microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

10.1 Test Mode 0 Details

In test mode 0, the S/UNI-ATLAS allows the logic levels on the device inputs to be read through the microprocessor interface and allows the device outputs to be forced to either logic level through the microprocessor interface. The IOTST bit in the Master Test register must be set to logic one to access the device I/O.

10.2 JTAG Test Port

The S/UNI-ATLAS JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 30 Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 31 Identification Register

Length	32 bits
Version number	1H
Part Number	7324H
Manufacturer's identification code	0CDH

Length	32 bits
Device identification	173240CDH

Boundary Scan Register

Table 32 Boundary Scan Register

The least significant bit is the first bit to be scanned in on TDI and scanned out on TDO.

Length - 316 bits

Pin/Enable	Type	Boundary Scan Register Bit	Pin/Enable	Type	Boundary Scan Register Bit
intb	o	1	raddr[2]/rrdenb[4]	o	138
idreq	o	2	raddr[1]/rrdenb[3]	o	139
edreq	o	3	raddr[0]/rrdenb[2]	o	140
busyb	o	4	rrdenb[1]	o	141
d[15:0]	i/o	5:20	rca[1]	i	142
For d[15:0]	en	21	rfclk	i	143
rstb	i	22	rsoc	i	144
csb	i	23	rpoll	i	145
wrb	i	24	rprty	i	146
rdb	i	25	rdat[15:0]	i	147:162
ale	i	26	isp[7:0]	i/o	163:170
a[11:0]	i	27:38	For isp[7:0]	en	171
esp[3:0]	i/o	39:42	isd[63:0]	i/o	172:235
For esp[3:0]	en	43	For isd[63:0]	en	236
esd[31:0]	i/o	44:75	half_sec_clk	i	237
For esd[31:0]	en	76	isysclk	i	238
esysclk	i	77	isrwb	o	239
esrwb	o	78	isoeb	o	240
esoeb	o	79	isadsb	o	241
esadsb	o	80	isa[19:0]	o	242:261
esa[19:0]	o	81:100	odat[15:0]	o	262:277
tdat[15:0]	o	101:116	oprty	o	278
tprty	o	117	osoc	o	279
tpoll	i	118	oca	o	280
tfclk	i	119	ofclk	i	281
tsoc	o	120	ordenb	i	282

tca[1]	i	121	otsen	i	283
twrenb[1]	o	122	iavalid/ica[4]	i/o	284
taddr[0]/twrenb[2]	o	123	For iavalid/ica[4]	en	285
taddr[1]/twrenb[3]	o	124	iaddr[4]/ica[3]	i/o	286
taddr[2]/twrenb[4]	o	125	For iaddr[4]/ica[3]	en	287
taddr[3]/tca[2]	i/o	126	iaddr[3]/ica[2]	i/o	288
For taddr[3]/tca[2]	en	127	For iaddr[3]/ica[2]	en	289
taddr[4]/tca[3]	i/o	128	iaddr[2]/iwrenb[4]	i	290
For taddr[4]/tca[3]	en	129	iaddr[1]/iwrenb[3]	i	291
tavalid/tca[4]	i/o	130	iaddr[0]/iwrenb[2]	i	292
For tavalid/tca[4]	en	131	iwrenb[1]	i	293
ravalid/rca[4]	i/o	132	ica[1]	o	294
For ravalid/rca[4]	en	133	ipoll	i	295
raddr[4]/rca[3]	i/o	134	ifclk	i	296
For raddr[4]/rca[3]	en	135	isoc	i	297
raddr[3]/rca[2]	i/o	136	iprty	i	298
For raddr[3]/rca[2]	en	137	idat[0:15]	i	299:314
			hiz (Trisates ALL output and Bidirection pins, when set high)	en	315
			obus_oeb (enable for odat[15:0], osoc, oprty	en	316

Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 22 Input Observation Cell (IN_CELL)

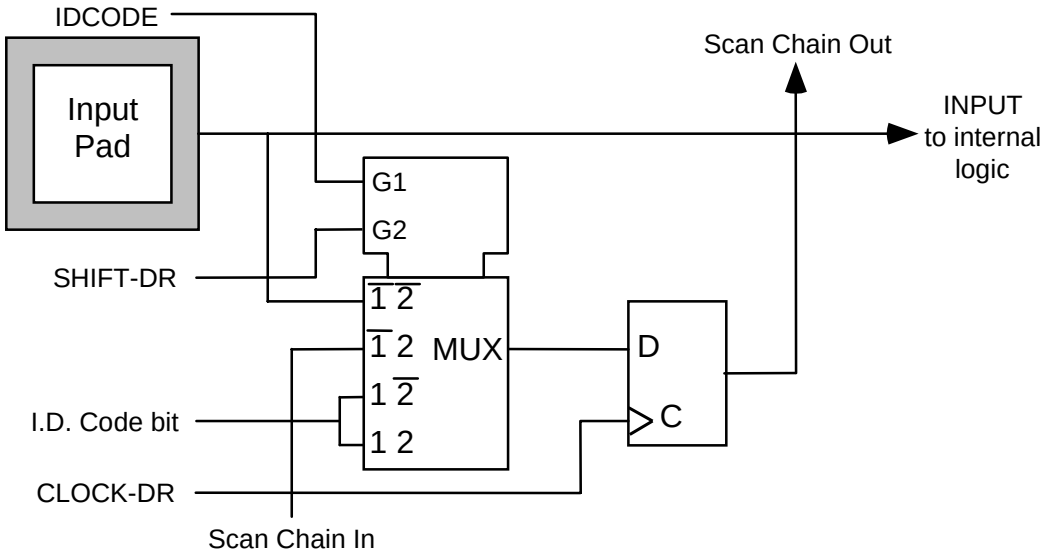


Figure 23 Output Cell (OUT_CELL)

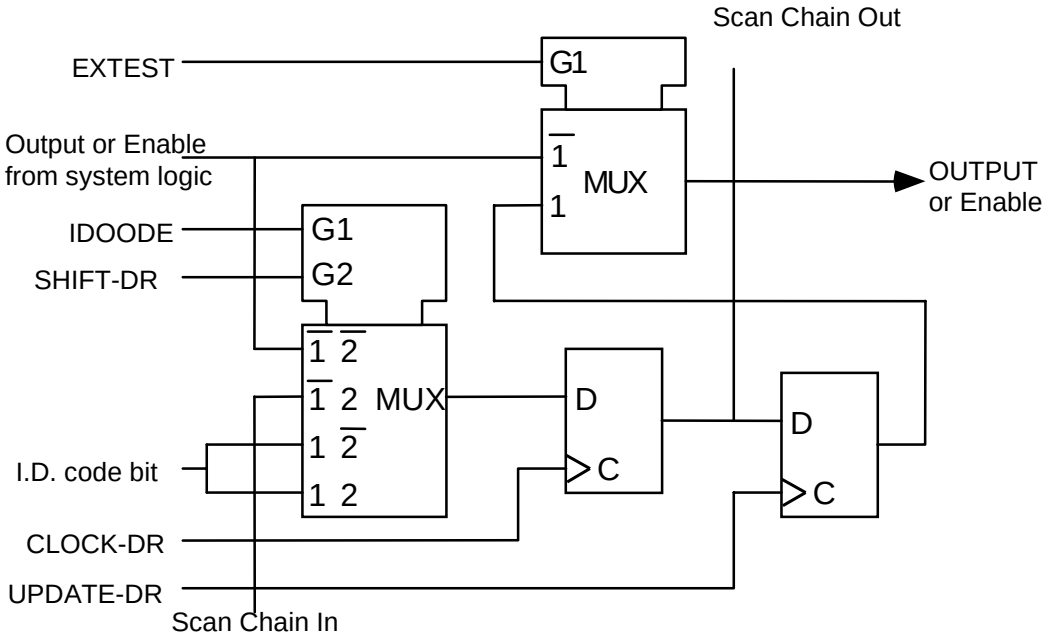


Figure 24 Bi-directional Cell (IO_CELL)

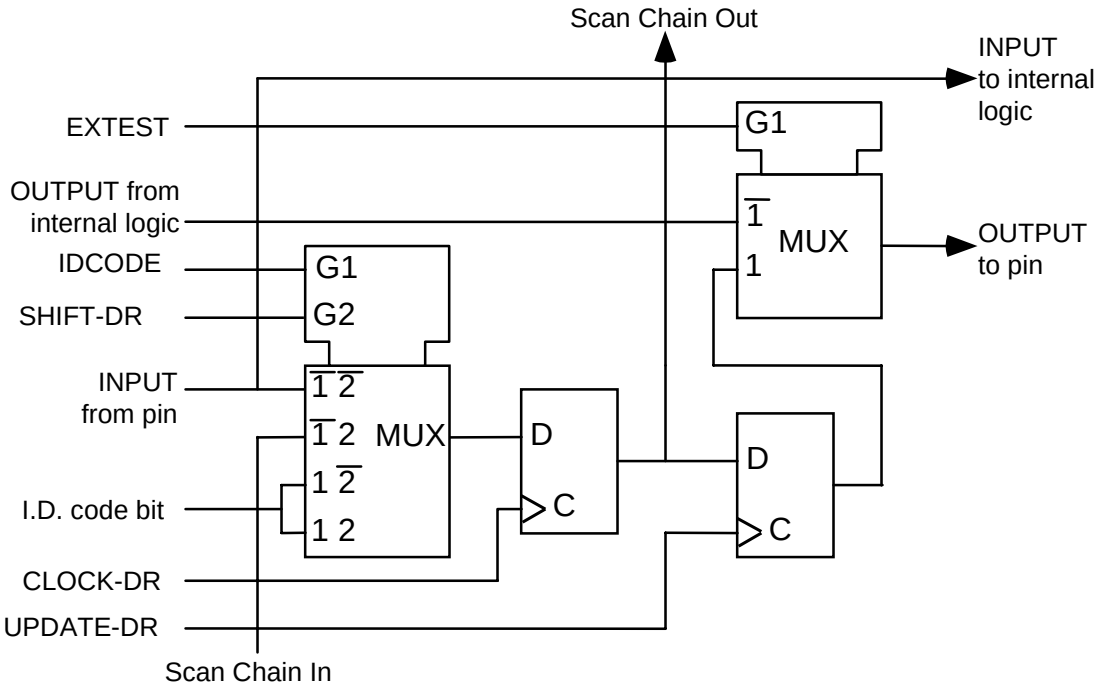
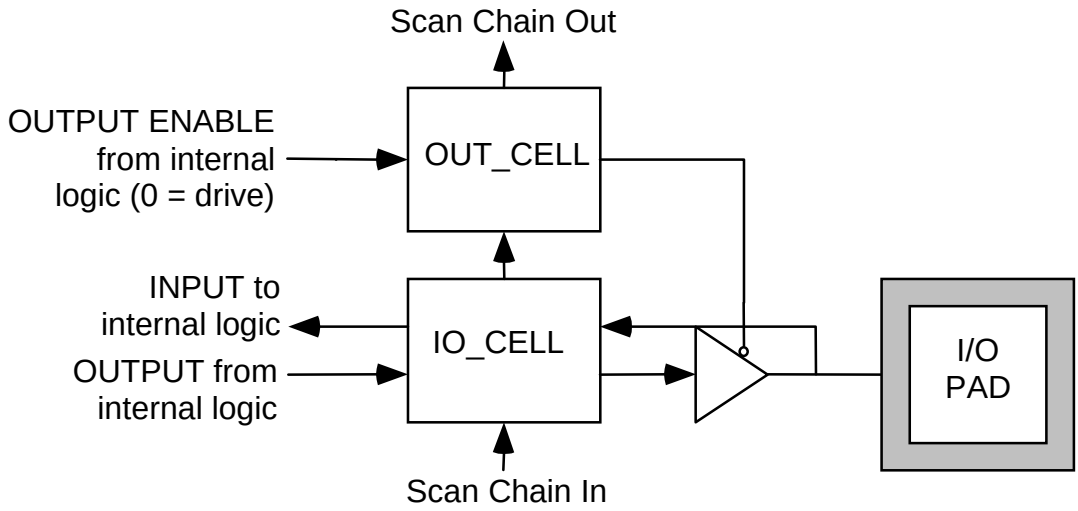


Figure 25 Layout of Output Enable and Bi-directional Cells



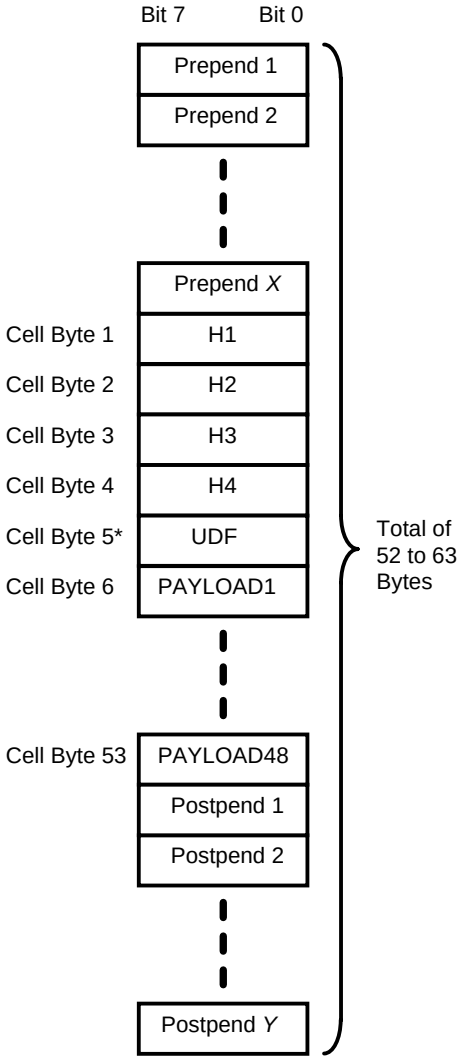
11 OPERATION

11.1 SCI-PHY Extended Cell Format

The SCI-PHY extended cell format is a recent enhancement of the SCI-PHY bus standard described in the "Saturn Compliant Interface for ATM Devices" document (PMC-940102). The extension allows for the appending of up to 10 bytes of additional information.

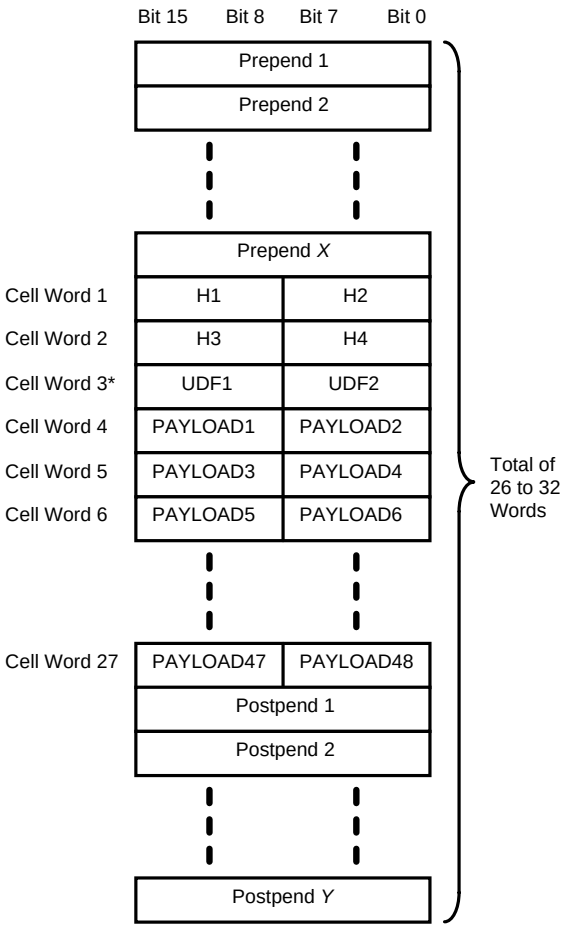
Figure 26 and Figure 27 illustrate the 8 bit wide and 16 bit wide data structures. The length of the prepend and postpend are independently programmable for each interface.

Figure 26 Eight Bit Wide Cell Format



* CELL BYTE 5 MAY OPTIONALLY BE OMITTED.

Figure 27 Sixteen Bit Wide Cell Format



* CELL WORD 3 MAY OPTIONALLY BE OMITTED.

11.2 Synchronous Static RAMs

11.2.1 Ingress VC-Table SRAM

The Ingress VC Table is a 15-row 64 bit data structure which contains context information for up to 65536 connections. The Ingress VC Table is used for connection identification, connection configuration and cell processing functions. The connection identification fields of the VC Table are located in the first two rows of the structure, and the remaining rows are used for connection configuration and cell processing.

The Ingress VC Table is stored externally to the S/UNI-ATLAS in SRAM (Static Ram). The ingress SRAM data bus is 72 bits wide (8 bytes plus byte parity), with an address space of 20 bits (1M).

This creates enough context address space for 64K VCs. The entire SRAM space does not have to be populated however. If fewer than 64K VCs are required, or a subset of ATLAS features are used, then SRAM may be saved. However, additional glue logic may be required to achieve the savings in SRAM.

The ATLAS uses synchronous flow-through non-pipelined fast static random access memory. Any combination of SRAM that provides the full 64-bit data path plus 8-bits of parity can be used. If more than one bank of SRAM is used some address decoding will be required. The Atlas can use the more common synchronous Burst type SRAMs, but the Atlas does not use the burst features. Some of the available SRAMs are shown in the table below.

11.2.2 Egress VC-Table SRAM

The Egress VC table is a 16-row 32-bit data structure which contains context information for up to 65536 connections. The Egress VC Table is used for connection identification, connection configuration and cell processing functions. The connection identification field of the Egress VC Table record is located in the first row of the structure, and the remaining rows are used for connection configuration and cell processing.

The Egress VC Table is stored external to the S/UNI-ATLAS in SRAM. The egress SRAM data bus is 36 bits wide (4 bytes plus byte parity), with an address space of 20 bits (1M). This allows for 64K connections, as with the Ingress VC Table. If less than 64K connections are required, or a subset of ATLAS features is used, then SRAM may be saved.

The Egress VC-Table interface requires synchronous flow-through non-pipelined fast static random access memory. Any combination of SRAM that provides the full 32-bit data path plus 4-bits of parity can be used. If more than one bank of SRAM is used some address decoding will be required. The ATLAS can use the more common synchronous Burst type SRAMs, but the ATLAS does not use the burst features. Some of the available SRAMs are shown in the table below.

Table 33 Atlas VC-Table Available SRAM types

Vendor	Device	Configuration	Access Time	Max. Frequency
Cypress	CY7C1031-10	64K x 18	12 ns	66 MHz
Motorola	MCM67B618A-9	64K x 18	9 ns	75 MHz
Motorola	MCM63F737-9	128K x 36	9 ns	75 MHz
Motorola	MCM63F819-9	256K x 18	9 ns	75 MHz
Motorola	MCM69F536C-9	32K x 36	9 ns	75 MHz
SGS-Thompson	M67H618-10	64K x 18	10 ns	66 MHz
Samsung	KM718B86-9	64K x 18	9 ns	66 MHz

11.3 ATM Cell Processing

11.3.1 OAM Cell Format

The automatic OAM cell handling in the Atlas supports only a subset of the available information fields. The processing of particular fields within some OAM cells is not practical in the Atlas. Cells can be dropped to the Microprocessor Cell Interface for external processing if required. This section describes the processing of received OAM cells and the coding of fields in the generated OAM cells.

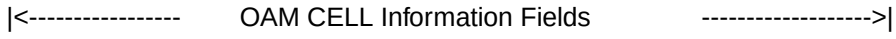
Depending on the setting of the bits in the Ingress OAM Generation Configuration Register, the associated cell type can be copied to the Microprocessor Cell Interface for OAM flows terminated at connection end points. This allows for external processing of the OAM cell types which are not processed by the Atlas. The Atlas can also be configured to drop OAM cells that are also processed.

The table below list the OAM cells which are currently defined and the action that the Atlas takes with each type. Any type which is not listed will be processed as an undefined OAM cell and can be copied to the microprocessor if the UNDEFtoUP bit, in register 0x220 and 0x281, is set and/or to the Output Cell Interface if the UNDEFtoOCIF bit, in register 0x200 and 0x285 is set. If the cell is not copied to the microprocessor cell interface, than at connection end points the cell will be discarded.

Table 34 OAM Type and Function type identifiers

OAM type	Coding	Function type	Coding	Atlas Action
Fault management	0001 0001 0001 0001	AIS RDI CC LB	0000 0001 0100 1000	Processed/generated Processed/generated Processed/generated Copied to OCIF/Micro Only
Performance management	0010 0010	FPM Backward reporting	0000 0001	Processed/generated Processed/generated
APS Co-ordination protocol	0101	Group protection Individual protection	0000 0001	Copied to OCIF/Micro Only Copied to OCIF/Micro Only
Activation/deactivation	1000 1000 1000	FPM and associated BR CC FPM	0000 0001 0010	Copied to OCIF/Micro Only Copied to OCIF/Micro Only Copied to OCIF/Micro Only
System management	1111	Not Standardised	NA	Copied to OCIF/Micro Only

Figure 28 Common OAM Cell Format



Header	OAM type	Function Type	Function specific field	Reserved for future use	EDC (CRC-10)
5 octets	4 bits	4 bits	45 octets	6 bits	10 bits

The Header of the cell carriers the connection information. The Atlas uses the information in the VC Table when generating OAM cells. The Reserved field is set to all zeros.

The Error Detection Code (EDC) is verified for all received OAM cells. The polynomial represented by the 48 octet information field is divided by x10+x9+x5+x4+x+1. All OAM cells which have an all zeros remainder are processed. Cells with an incorrect EDC are discarded.

The specific fields for each type of OAM cell that the Atlas modifies or processes are shown below for each type of cell that the Atlas processes. If the field is marked as “Don’t Care” than the Atlas does not operate on that field. Where appropriate, the register or VC-Table field that modifies the OAM specific field is given.

Figure 29 Specific fields for AIS/RDI fault management cell

Defect type (Register 0x226-0x22D)	Defect location (Register 0x22E-0x235)	Reserved for future use (6AH)
1 octet	16 octets	28 octets

The Atlas allows a total of 16 Defect types to be entered into the Defect Type field of AIS/RDI cells. The value of the field is selectable on a per-VC basis. The Defect location field is programmable and is common to all generated AIS/RDI cells.

There are currently no fields that are specific to the continuity check function, and hence the function specific field is encoded 6AH.

The Atlas does not process any fields in the Loopback cell.

Figure 30 Specific fields for the FPM cell

MCSN/FPM (PM Table)	TUC-0+1 (PM Table)	BEDC-0+1 (PM Table)	TUC-0 (PM Table)	TSTP (Don’t Care)	Reserved for future use (6AH)
8 bits	16 bits	16 bits	16 bits	32 bits	34 octets

The following is with referance to the figure for FPM Specific fields. The Monitoring Cell Sequence Number (MCSN) is incremented with each generated FPM cell for the connection. The Total User Cell (TUC 0+1) number is incremented with each user cell received (CLP = 0 or 1) and is never reset. The Total User Cell (TUC 0) number is incremented with each user cell received (CLP = 0 only) and is never reset. The Block error detection code (CLP = 0 or 1) BEDC contains the BIP-16 value calculated over all user cells since the last forward monitoring cell.

Figure 31 Specific fields for the BR cell

MCSN/ BR (PM Table)	TUC-0+1 (PM Table)	Reserved (6AH)	TUC-0 (PM Table)	TSTP (Don't Care)	Reserved (6AH)	Fwd MCSN (PM Table)	SECBC (PM Table)	TRCC-0 (PM Table)	BLER-0+1 (PM Table)	TRCC-0+1 (PM Table)
8 bits	16 bits	16 bits	16 bits	32 bits	27 octets	8 bits	8 bits	16 bits	8 bits	16 bits

In the figure for BR cell specific fields, the Monitoring Cell Sequence Number (MCSN) is incremented with each generated BR cell for the connection. The Total User Cell CLP = 0 or 1 (TUC 0+1) field is copied from the most recent received BR cell. The field is used with the next received BR cell 's TUC 0+1 to determine the number of cells transmitted by the forward monitoring source point between successive FPM cells. The Total User Cell CLP = 0 only (TUC 0) operates identically to the TUC 0+1 except that the only cells with CLP = 0 are counted. The Forward Monitoring Cell Sequence Number (RMCSN) contains the the MCSN copied from the paired FPM cell. The Severely Errored Cell Block Count (SECBC) is copied from the SECBC field of received Backwards Reporting cells. The total Received Cell count related to CLP = 0 or 1 (TRCC 0+1) and CLP = 0 (TRCC 0) fields carries the current value of a running counter of received user cells.

The Atlas does not process any fields in Activation/Deactivation cells.

11.4 Ingress VC Identification Search Algorithm

Within the constraints imposed by the Primary and Secondary Search Table coding rules, numerous search algorithms are supported. The building of a search data structure is a software function and is normally performed by the supervising microcontroller. A shadow data structure is required by the microcontroller to enact the modifications to the data structure. (It is possible to avoid using a shadow data structure, but efficiency is reduced by the need to perform searches through multiple SRAM accesses via the ATLAS, each taking up to 800 ns. Also, diagnostic possibilities are reduced.)

The algorithm presented below has the following features that optimize it for VC identification:

1. Only those bits in the Secondary Search Key required to make a unique identification are examined. This minimizes the average search time.

2. The number of VC Table entries bound the number of nodes in the Secondary Search Table. Therefore, the depth of memory required for the Secondary Search Table is equal to that required for the VC Table.

3. Nodes can be added or deleted on the fly without corrupting a binary search in progress.

A C-language example of the algorithm will be made available.

11.4.1 Overview

The VC search algorithm maps the cell's PHY identifier, VCI, VPI and selected portions of appended bytes to a 16-bit VC Table address. Effectively, it performs the operation of a Content Addressable Memory (CAM). The data structure created to support the VC identification is designed around maximizing the efficiency of the process.

It is the Select field in the Secondary Search Table which makes the search efficient, because it allows each branching decision to be made based on only the first bit in which two branches differ. That is, as two values are compared, starting with the MSB (most significant bit) and moving to the LSB (least significant bit), the two can be fully discriminated based on the first bit in which they differ. No other bits after that bit, regardless of how much they differ, need to be considered. Because not all bits are examined in the binary search, the search is concluded with a confirmation step that compares the Secondary Search Key against the VPI/VCI of the candidate VC Table.

The following sections describe the search table initialization, connection addition and connection removal processes. Refer to the VC Identification section of the Functional Description section for definitions of the Primary and Secondary Search Keys, for an overview of the search process and for a definition of the data structures.

11.4.1.1 Initialization

The following are the microcontroller actions required to initialize the Search Tables and VC Tables:

1. Set the STANDBY bit of the Master Configuration register (0x001) if not already set by an asynchronous reset.

2. Write zeros (null pointer) to every Primary Search Table location (the least significant 16 bits of offset ISA[19:16] = 0000).

3. Clear the “Active” bit of the configuration field (bit 55 of offset ISA[19:16] = 0010) of all VC Table entries.

4. Clear the STANDBY bit of the Master Configuration register (0x001).

The remaining SRAM locations can be initialized when required.

11.4.1.2Adding a Connection

The following are the microcontroller actions required to provision a connection:

1. Determine the next available VC Table address. Initialize the contents of the VC Table Record via the Microprocessor RAM Address and Data registers (0x190 through 0x1CB). Care should be taken to set the following fields appropriately:

   All counts should be set to zero.

   The "Status" and “Internal Status” fields should be set to all zero’s.

   The "Active" bit of the "Configuration" field should be set to one.

2. Perform a binary search to determine the insertion point. The last pointer accessed in the search shall be the one modified, be it a Primary Search Table entry, left branch or right branch.

3. Find a free Secondary Search Table entry and initialize it. The only exception to this is when a single VC Table Record exists in a tree, in which case the solitary Secondary Search Table entry is modified.

The value of the "Select" is set to the index of the most significant bit which differs between the new VC and the "nearest" existing VC, which was found in step 2. A few insights need highlighting:

1. If there is an overlap between Primary and Secondary Search keys (eg. the Primary key is the VPI), the intersecting bits are excluded from the binary search based on the fact they will always be the same in both keys.

2. Due to fact that the Primary Search key includes the PHY identification, NNI and UNI connections will never reside in the same binary tree. Therefore, the "Select" determination algorithm needs to start its bit comparison at the correct bit (the first bit of the ATM header for NNI and the fifth bit of the ATM header for UNI) to ensure a valid search tree.

3. Perform a SRAM write (via the Microprocessor RAM Address and Data registers) to incorporate the new Secondary Search Table entry in the existing tree structure. This step must be performed last to ensure a binary search in progress is not corrupted.

Five distinct types of insertions are possible based on the existing tree structure:

1. The binary tree is empty. In this case, the null primary search table pointer is modified to point to a newly created Secondary Search Table entry. Because no bits within the Secondary Search Key are required, both the left and right branches of the Secondary Search Table entry point to the same VC Table Record. The "select" field should be set to zero.

Key to data structure diagrams:

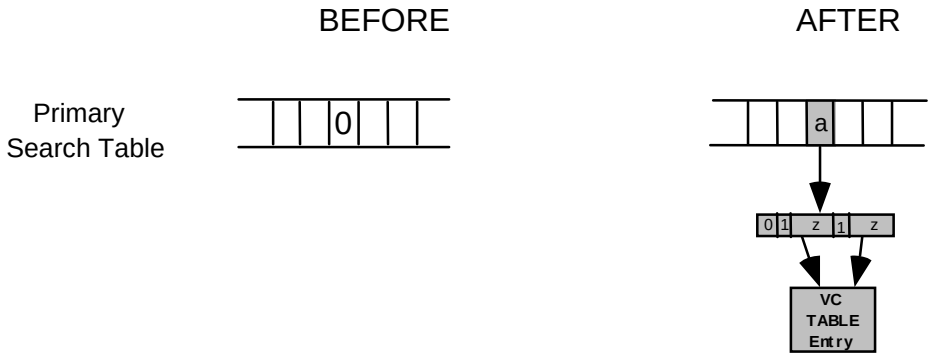
a, b, c - pointers to Secondary Search Table entries

w, x, y, z - pointers to VC Table entries

k,m,n - "select" field contents

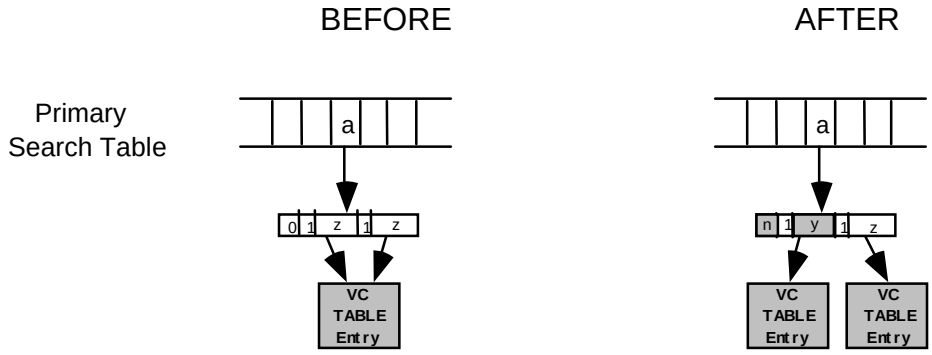
The shaded boxes indicate those fields which have been created or modified.

Figure 32 Connection Insertion when binary tree is empty



2. The binary tree contains only a single VC Table Record. Modify the "select" field to index the most significant bit of the Secondary Search Key that differs between the new and existing connection. Modify the left or right branch, as appropriate, to point to the newly created VC Table Record.

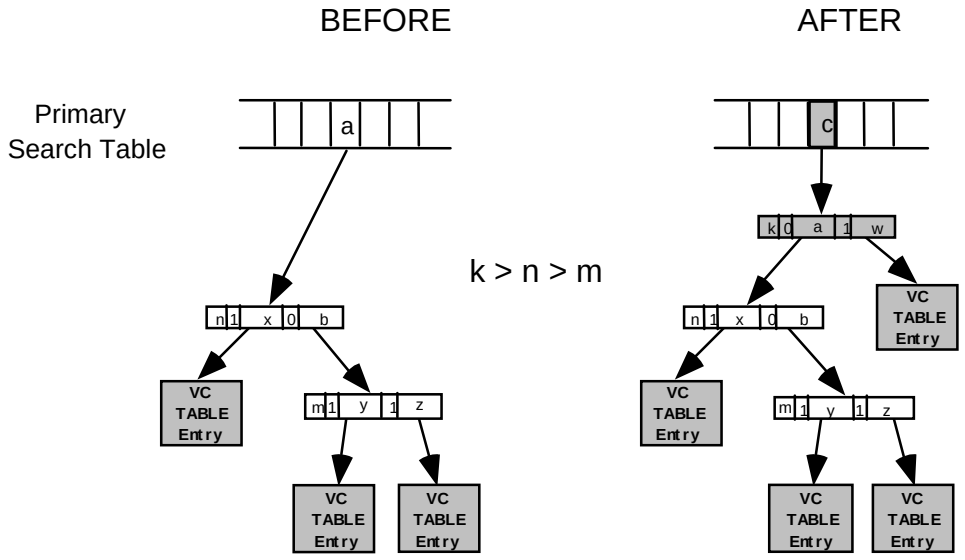
Figure 33 Connection insertion when binary tree contains only single VC record.



The diagram illustrates the case where the new VC has a one in the decision bit position and the existing VC has a zero in the same bit position. If the new VC had a zero in the decision bit position, the right branch would have been modified instead.

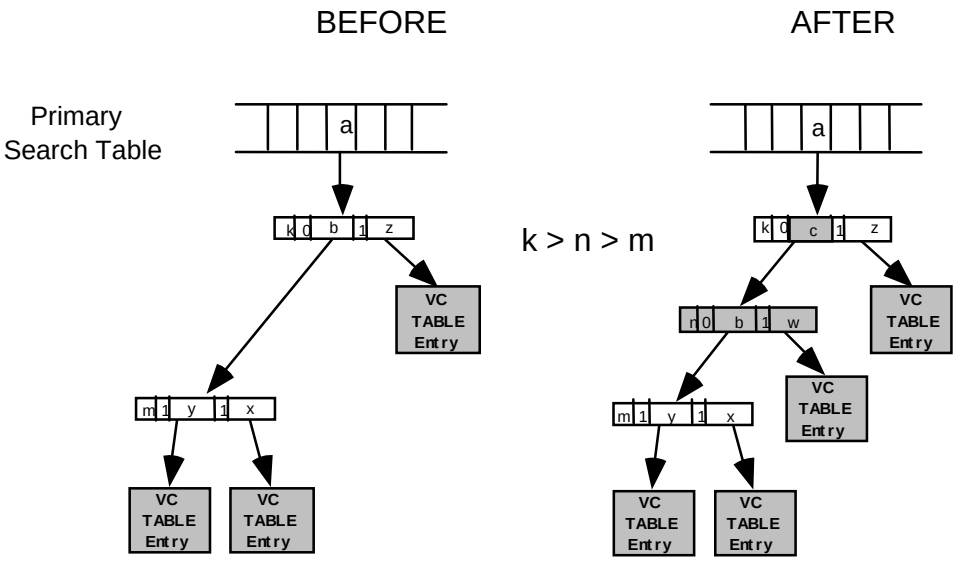
3. The insertion point is at the root of the tree. This occurs when the new decision bit index is greater any of the indices currently in the search tree. In this case, the Primary Search Table entry is modified to point to the newly created Secondary Search Table entry. The New Secondary Search Table entry points to the new VC Table Record and the old tree root.

Figure 34 Connection insertion at the root of the tree.



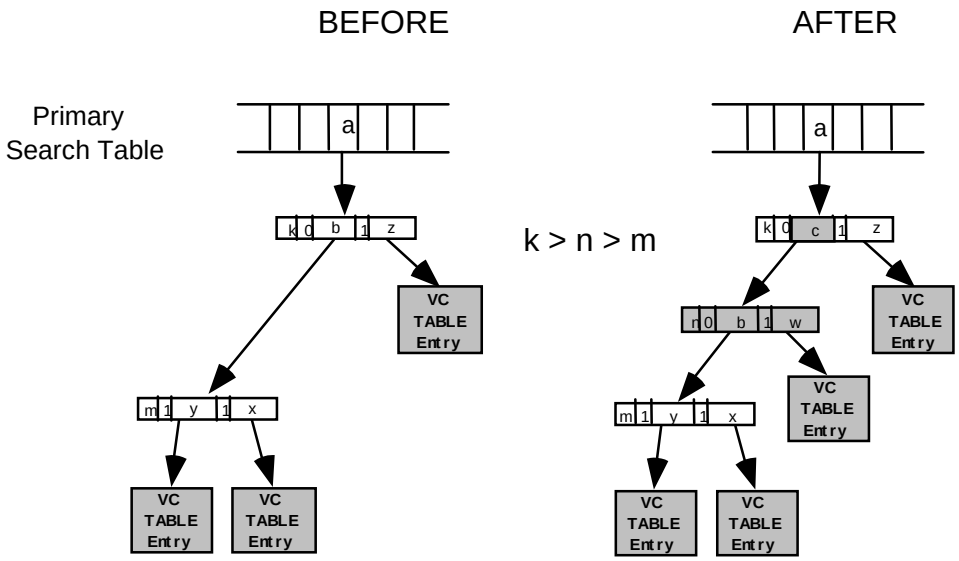
4. The insertion point is in the middle of the binary tree. The new Secondary Search Table entry points to the new VC Table Record and an existing node in the tree. The parent of the existing node is modified to point to the new Secondary Search Table entry in the final step of the insertion.

Figure 35 Connection insertion in the middle of the binary tree.



5. The new Secondary Search Table entry is inserted at a leaf. The search for a candidate insertion point ends on a node which already points to a VC Table Record. The new Secondary Search Table entry points to the existing VC Table Record and the new VC Table Record. The existing Secondary Search Table entry is modified to point to the new Secondary Search Table entry in the final step of the insertion.

Figure 36 New secondary search table entry inserted at a leaf.



11.4.1.3Removing a Connection

The following are the microcontroller actions required to remove a connection:

1. Find the location of the Secondary Search Table entry pointing to the connection's VC Table Record.

2. Modify the parent node (be it the Primary Table entry or another Secondary Search Table entry) of the Secondary Search Table entry being removed to point to the node remaining after the connection removal. The only exception to this is when two VC Table entries exist in a tree, in which case the solitary Secondary Search Table entry is modified. The VC is now considered unprovisioned and any cells belonging to the VC will be discarded.

3. Tag the removed Secondary Search Table entry as free.

4. Read the final statistics for the connection from the VC Table Record. Clear the "Active" bit of the CONFIG VC Table Record field and tag the record as free.

The connection removal process examples are not illustrated because the results are exactly the reverse of the connection provisioning. (Swap the "BEFORE" and "AFTER" labels.)

11.4.2 Ingress Performance Monitoring Activation / Deactivation

When performance monitoring is activated on a connection, there are a number of steps required:

1. Select a PM Session (an address in a selected bank)
2. Set the Fwd_PM0 and Bwd_PM0 bits. The reception of the first Fwd/Bwd PM cells will initiate a clear of the associated counts.
3. If configuring PM as a source point, all counters associated with Fwd PM generation must be cleared.
4. Set this PM address in the VC Table, and set the proper PM Active bit.

When performance monitoring is deactivated on a connection, only the proper PM Active bit needs to be cleared.

11.5 Egress VC Table Operation

The Egress path in the ATLAS does not perform a search on incoming cells. Instead the Egress path does a simple one-for-one look-up function. The index for the look-up must be part of the cell. The location and length of the index is programmable.

11.5.1 Initialization Procedure

Upon start-up, at a minimum, the external SRAM (VC Tables) should be initialized. This is done in the following manner:

1 Set the ESTANDBY input to ensure dedicated access to the RAMs

2 Clear the ACTIVE bit in all locations in each supported VC Table entry. This is done by:

i. Clear all Egress VC Table Record Row registers, 0x2AE-0x2D.

ii. On each pass cycle the value of the Egress VC Table Record Address, register 0x2AB, from 0->MAXVC.

iii. Write a 0x0001 to the Egress VC Table Row Select (only activate row 0).

iv. Set the RWB bit to logic 0 and the WM[3:0] field = “0000” in the Egress VC Table Write Mask and Access Control register 0x2AC.

v. Wait until the BUSY bit in register 0x2AC is cleared before continuing.

This ensures that the ECP does not mistakenly believe that a given connection has been activated. Once this is complete, connections can be activated/deactivated as needed.

11.5.2 Connection Setup

When a connection is activated, the following VC Table bits need to be initialized:

Table 35 VC Table Connection Setup

Field/Bits	Initial Value
Activation Field	1XX
Connection Identifier Field	User Defined
Status	0000000
Configuration Field	User Defined
OAM Configuration Field	User Defined
Internal Status / Send_Seg_CC_Count	1
Internal Status / Send_End_CC_Count	1
Internal Status / Seg_CC_Count	11
Internal Status / End_CC_Count	11
Internal Status / Seg_RDI_Count	11
Internal Status / End_RDI_Count	11
Internal Status / Seg_AIS_Count	11
Internal Status / End_AIS_Count	11
PHYID	User Defined
VPC Pointer	User Defined
Cell Counts	All zeroes

Nothing needs to be done to the Defect Location / Defect Type fields, because these fields are updated upon receipt of an end-end AIS cell.

11.5.2.1 Connection Tear-Down

When a connection is deactivated, only the ACTIVE bit needs to be cleared. The remainder of the fields will be re-initialized by the management software when a connection is activated.

11.5.3 Egress Performance Monitoring Activation / Deactivation

When performance monitoring is activated on a connection, there are a number of steps required:

1. Select a PM Session (an address in a selected bank)

2. Set the Fwd_PM0 and Bwd_PM0 bits. The reception of the first Fwd/Bwd PM cells will initiate a clear of the associated counts.

3. If configuring PM as a source point, all counters associated with Fwd PM generation must be cleared.

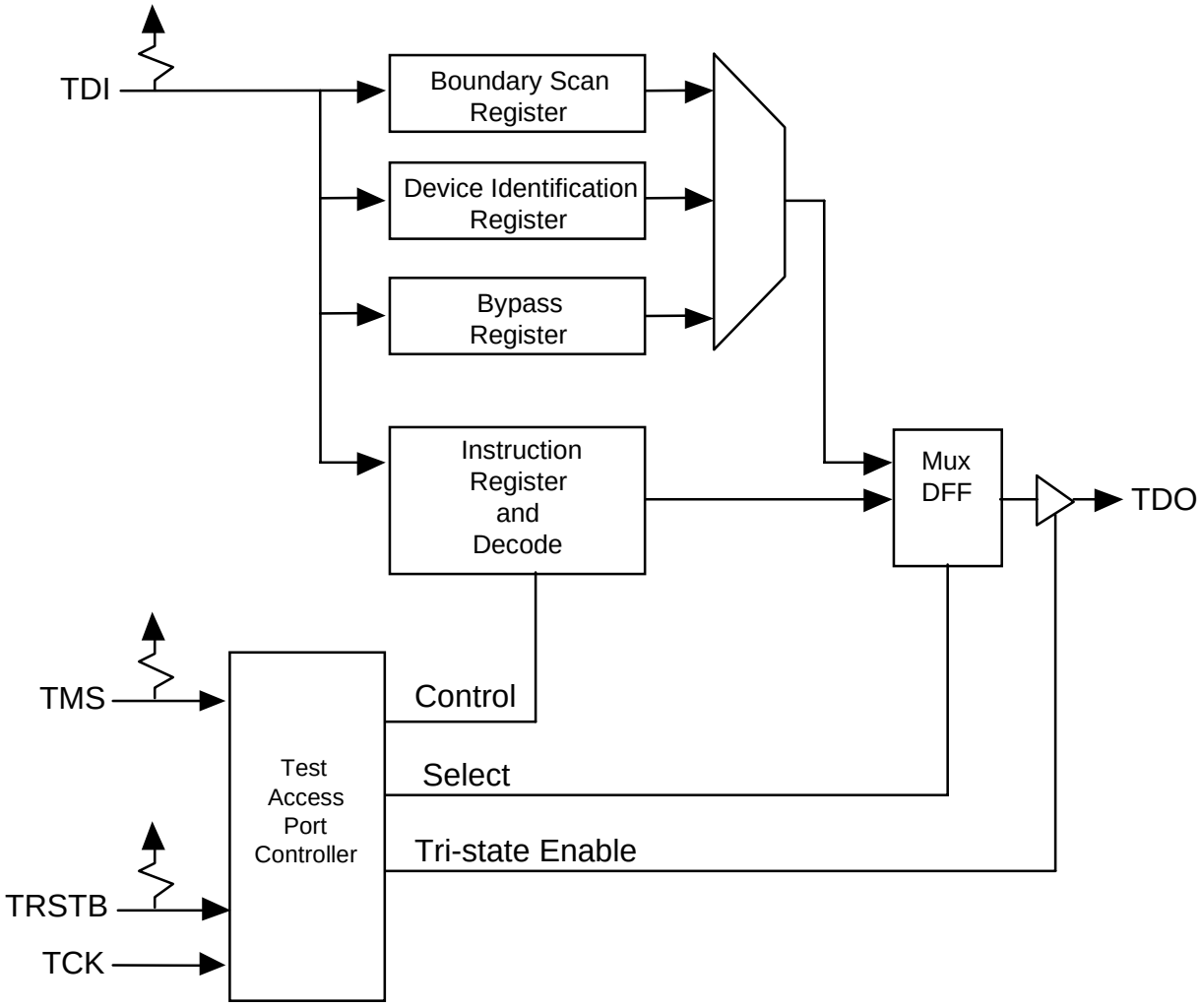
4. Set this PM address in the VC Table, and set the proper PM Active bit.

When performance monitoring is deactivated on a connection, only the proper PM Active bit needs to be cleared.

11.6 JTAG Support

The S/UNI-ATLAS supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 37 Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data

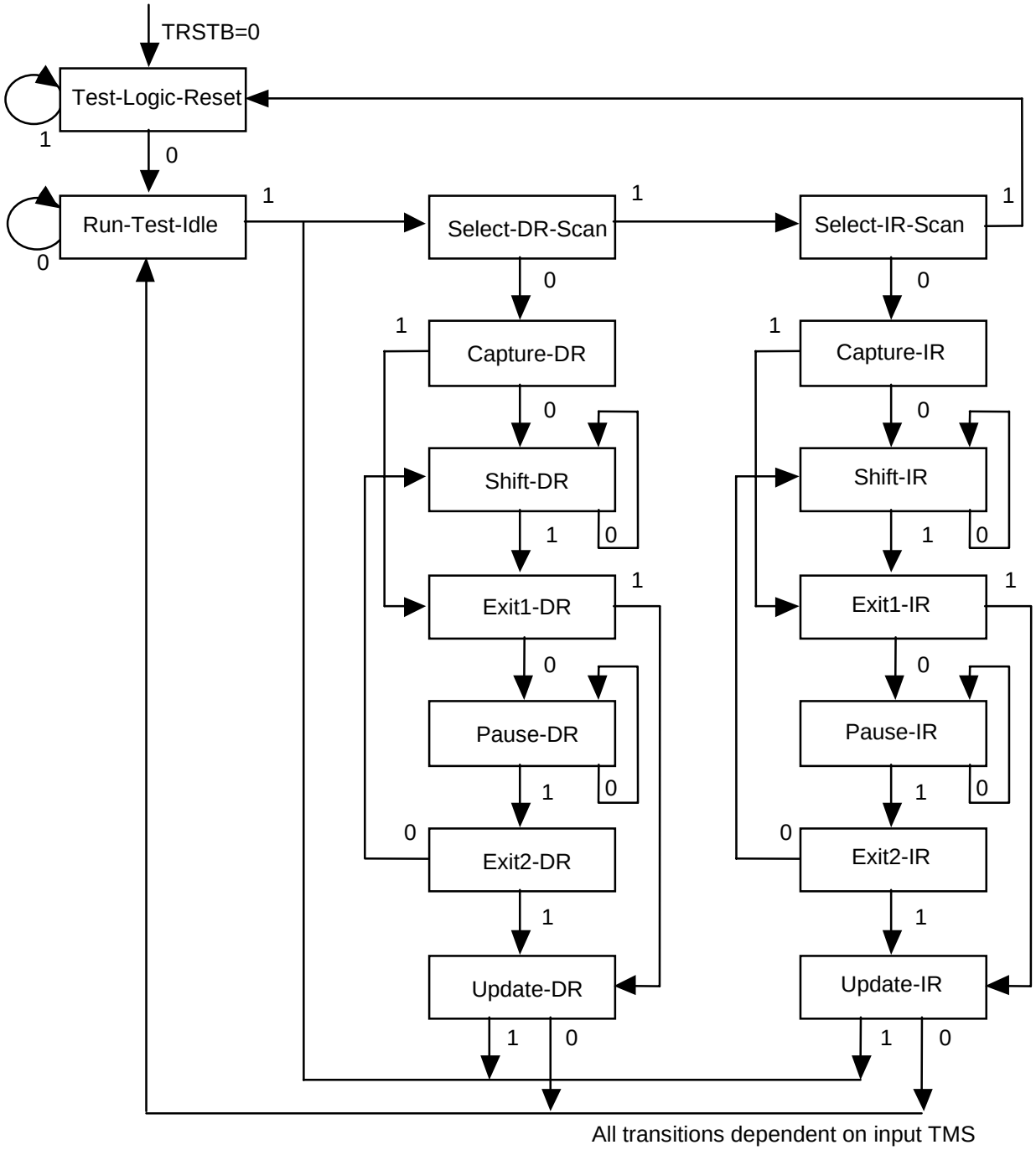
registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

11.6.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 38 TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

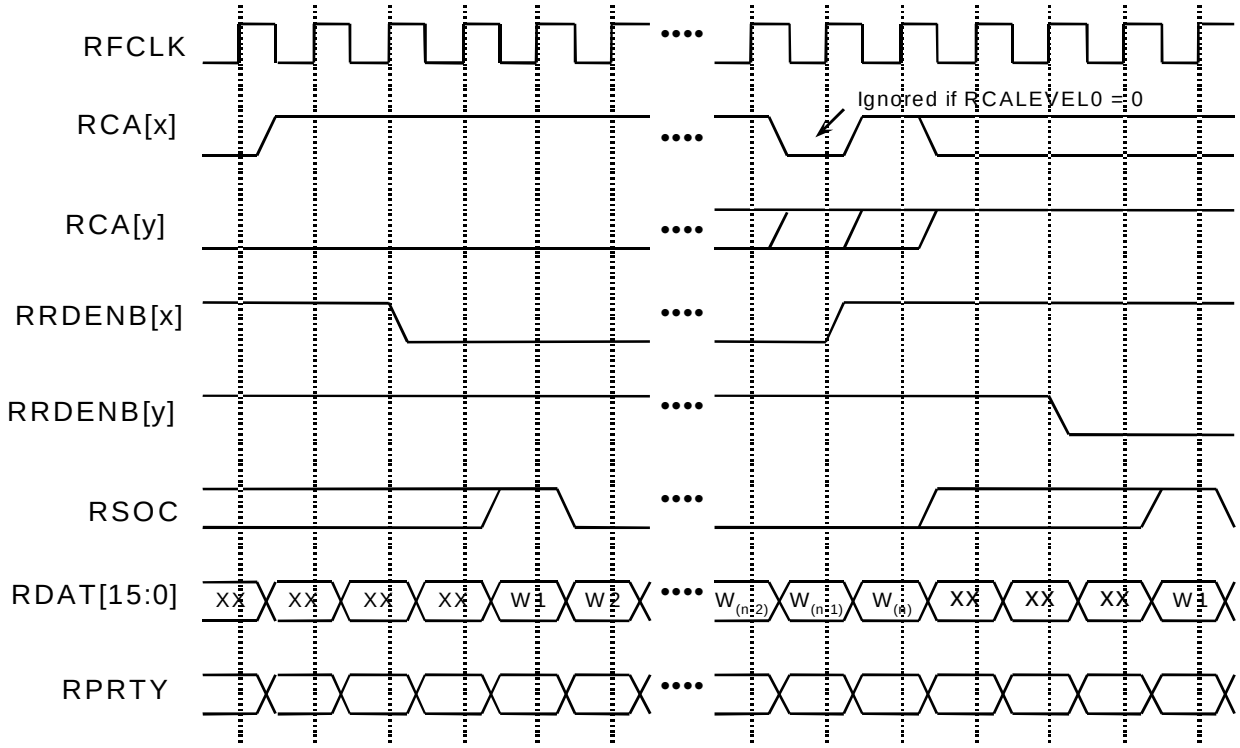
STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

12 FUNCTIONAL TIMING

12.1 Ingress Input Cell Interface

Figure 39 Ingress Input Cell Interface (RPOLL=0)



The Ingress Input Cell Interface diagram above illustrates the operation of the interface when it arbitrates accesses for a single or multiple PHYs under the non-polled (RPOLL=0) operating condition. If operating with a single PHY interface, only the RCA[1] and RRDENB[1] control signals are active. When there is room for another entire cell in the ATLAS Ingress Input Cell Interface FIFO and when one of the RCA[4:1] inputs indicates that there is a cell available, the ATLAS will respond by asserting the associated RRDENB[4:1] output. The ATLAS only supports cell-level handshaking; RRDENB[x] remains asserted until the entire cell is written into the FIFO. Once a transfer has been initiated, all bytes are assumed to be valid and RCA[x] is ignored until the end of the cell if the RCALEVEL0 bit of the Ingress Input Cell Configuration register is a logic 0. If RCALEVEL0 is a logic 1, an early deassertion of RCA[x] is considered to be a violation in the SCI-PHY/Utopia protocol, and the cell is discarded.

There is a minimum of three clock cycles between one RRDENB[x] being deasserted at the end of a cell and another RRDENB[y] being asserted at the start of the next cell.

RSOC is expected to be high during the first word of the data structure. The length of the data structure and the position of the ATM cell within the data structure are set by the RCELLLEN[3:0] and RCELLPOST[3:0] bits of the Ingress Input Cell Interface Configuration register. It is not necessary for RSOC to be present each cell; the input cell write address is generated by an internal counter that

flywheels in the absence of RSOC. If RSOC is sampled high during any but the first word of the cell, an interrupt may be generated (RSOCI) and the input cell write address counter is reset to the first word of the cell.

Figure 40 Ingress Input Cell Interface (RPOLL=1) Example 1

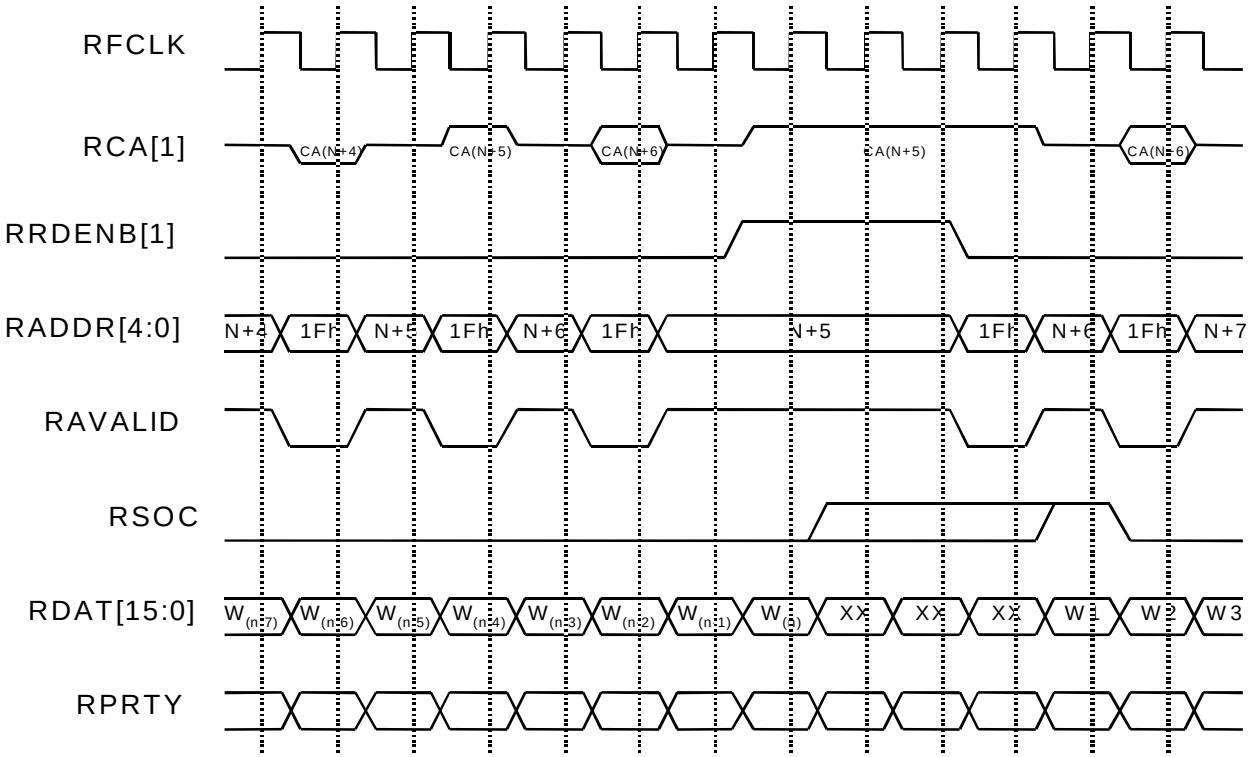
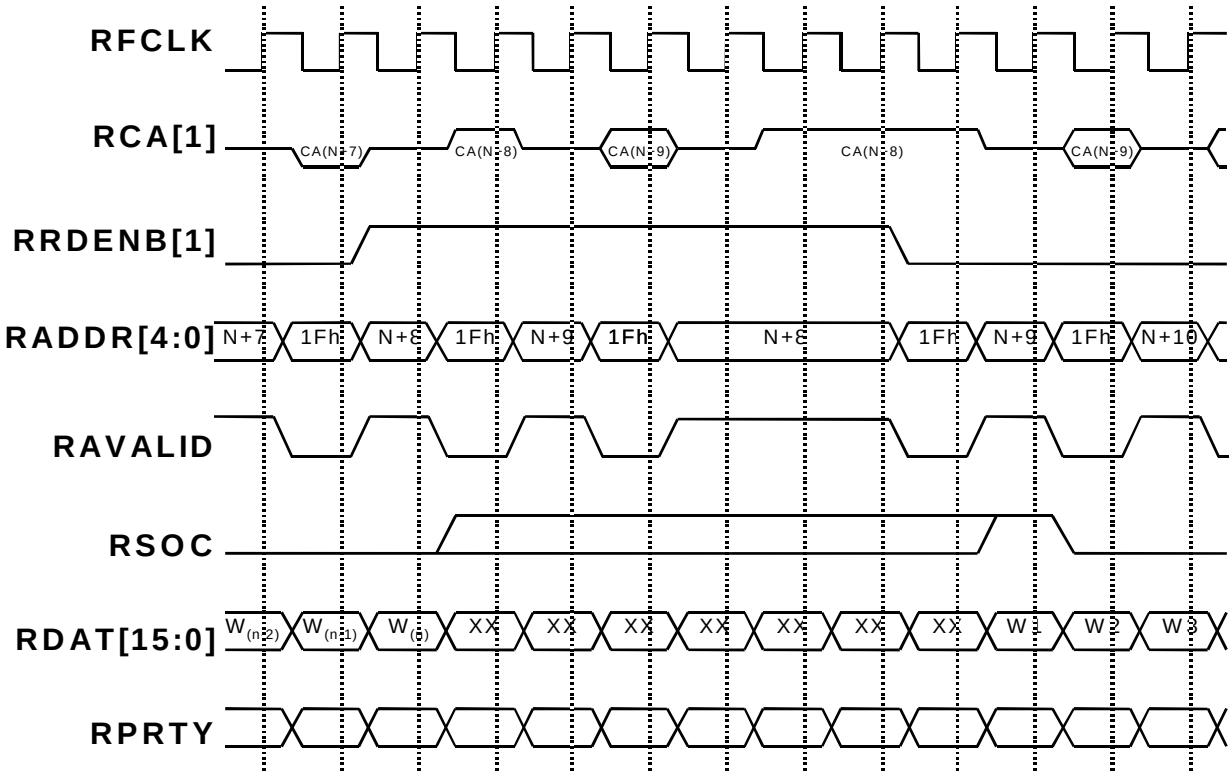


Figure 41 Ingress Input Cell Interface (RPOLL=1) Example 2



The above two figures illustrate the operation of the Ingress Input Cell Interface when it arbitrates accesses for up to 32 PHYs using addressed polling (RPOLL=1). The RCA[1] and RRDENB[1] control signals are active.

The PHY devices are polled cyclically beginning with PHY#(N+1), where N is the PHY ID of the cell currently being transferred. They first PHY device to respond to polling with an available cell indication is selected for transfer of the next cell. If no PHY device responds with an available cell indication, the polling cycle repeats. If the polling cycle repeats while the current cell is being transferred, however, the PHYID of the cell being transferred (i.e. N) is omitted from the polling sequence. This is because PHY devices compliant with the Utopia Level 1 interface (which can be used in polling mode with external glue logic) cannot indicate availability of a subsequent cell while they are simultaneously transferring a cell. Once transfer of the current cell is complete, PHY #N is re-inserted into the polling sequence.

When a PHY device with an available cell is found, polling ceases and the PHY device is selected for transfer of the next cell. If the PHY is found while a cell is being transferred, its ID is output on the RADDR[4:0] address bus, and held until the start of the next cell transfer. The PHY devices recognizes that it has been selected to send the next cell to the ATLAS by the presence of its ID on RADDR[4:0] during the clock cycle prior to RRDENB[1] being asserted. After RRDENB[1] is asserted (i.e. at the start of the next cell transfer), the polling process starts again.

Figure 40 shows an example in which the first PHY to be found with a cell available is PHY #(N+5) and the successful poll occurs during a cell transfer. The value N+5 is therefore output on RADDR[4:0] and held until the start of the next cell transfer. Note that because of the pipelined nature of the polling process, PHY#(N+6) is unavoidably polled before PHY#(N+5) is selected. The polling reply from PHY#(N+6) is ignored. If, for any reason, PHY#(N+5) de-asserts RCA[1] before the start of the next cell transfer, the polling process starts over.

Figure 41 shows a second example in which the first PHY to be found with a cell available is PHY#(N+8) and the successful poll occurs after the previous cell transfer has been completed. In this case, the value N+8 is output on RADDR[4:0] for three clock cycles after which RRDENB[1] is asserted to initiate transfer of the next cell. (Three clock cycles is the minimum required to re-sample RCA[1] and confirm that the cell is still available, i.e. that the PHY has not deasserted the cell available). Again, because of the pipelined nature of the polling process, PHY#(N+9) is unavoidably polled before PHY#(N+8) is selected.

12.2 Ingress Output Cell Interface

Figure 42 Ingress Output Cell Interface (OTSEN=0)

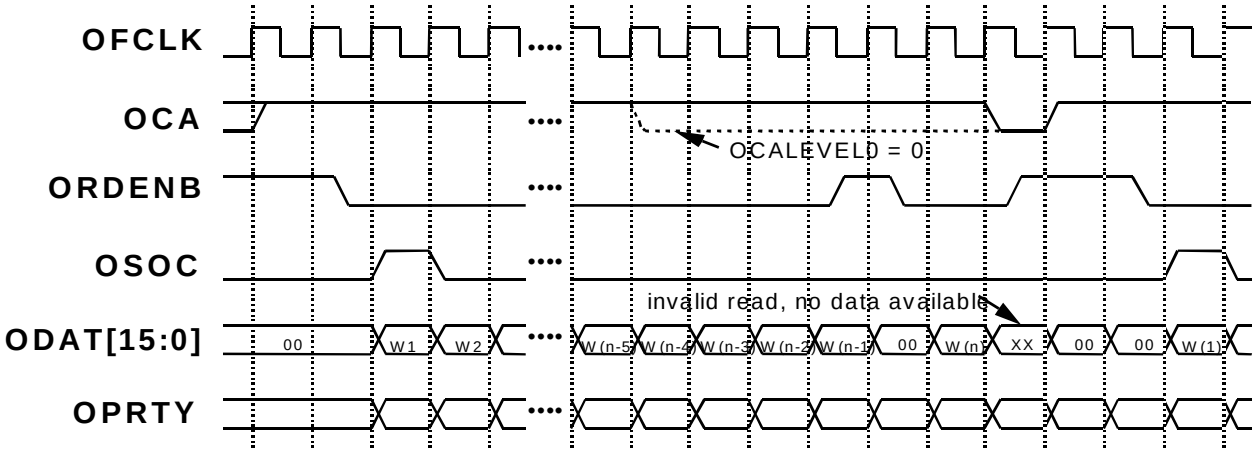


Figure 42 illustrates the Ingress Output Cell Interface functional timing diagram when output tristating is disabled. The diagram also illustrates the case where OCAINV is a logic 0; the sense of the OCA output may be inverted by setting OCAINV to a logic 1.

The ATLAS indicates a cell is available by asserting the output cell available, OCA. OCA remains high until the FIFO is near empty (four words remaining), empty or an error condition is detected. Selection of empty and near empty is made using the OCALEVEL0 bit in the Ingress Output Cell Interface Configuration register. For the near empty option, OCA transitions low four words before the last word of the last cell is read from the FIFO. OCA remains low for a minimum of one OFCLK clock cycle and then can transition high to indicate that there are additional cells available.

Note that if the Output Cell Interface is not near empty, OCA will remain asserted, such that cells can be read out back-to-back.

Figure 43 Ingress Output Cell Interface (OTSEN=1)

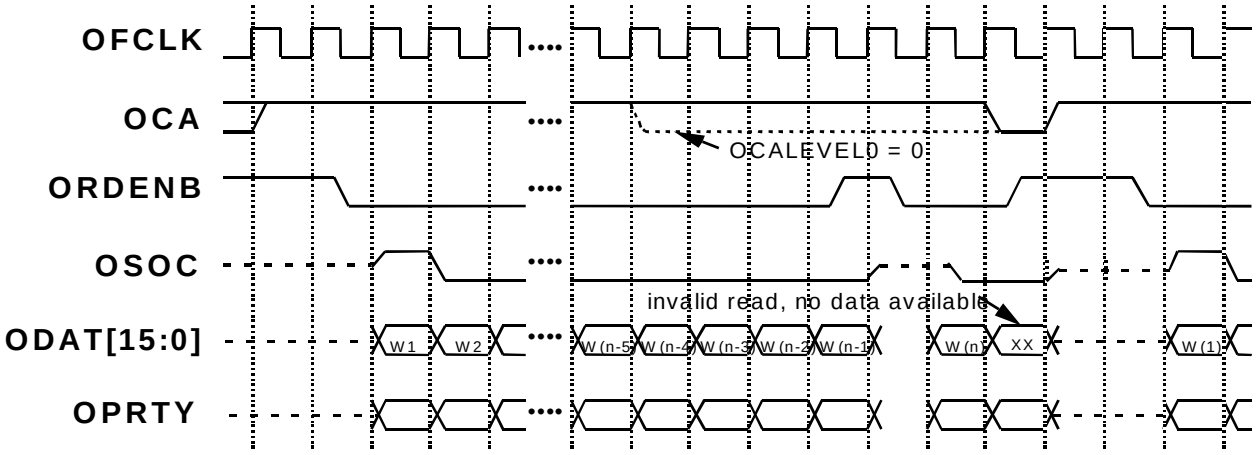


Figure 43 illustrates the functional timing relationship of the Ingress Output Cell Interface with tristating enabled (OTSEN=1). The functional behavior is identical to that when OTSEN=0, however, OSOC, ODAT[15:0], and OPRTY are tristated in the cycle after ORDENB is deasserted.

12.3 Egress Input Cell Interface

Figure 44 Egress Input Cell Interface (IPOLL=0)

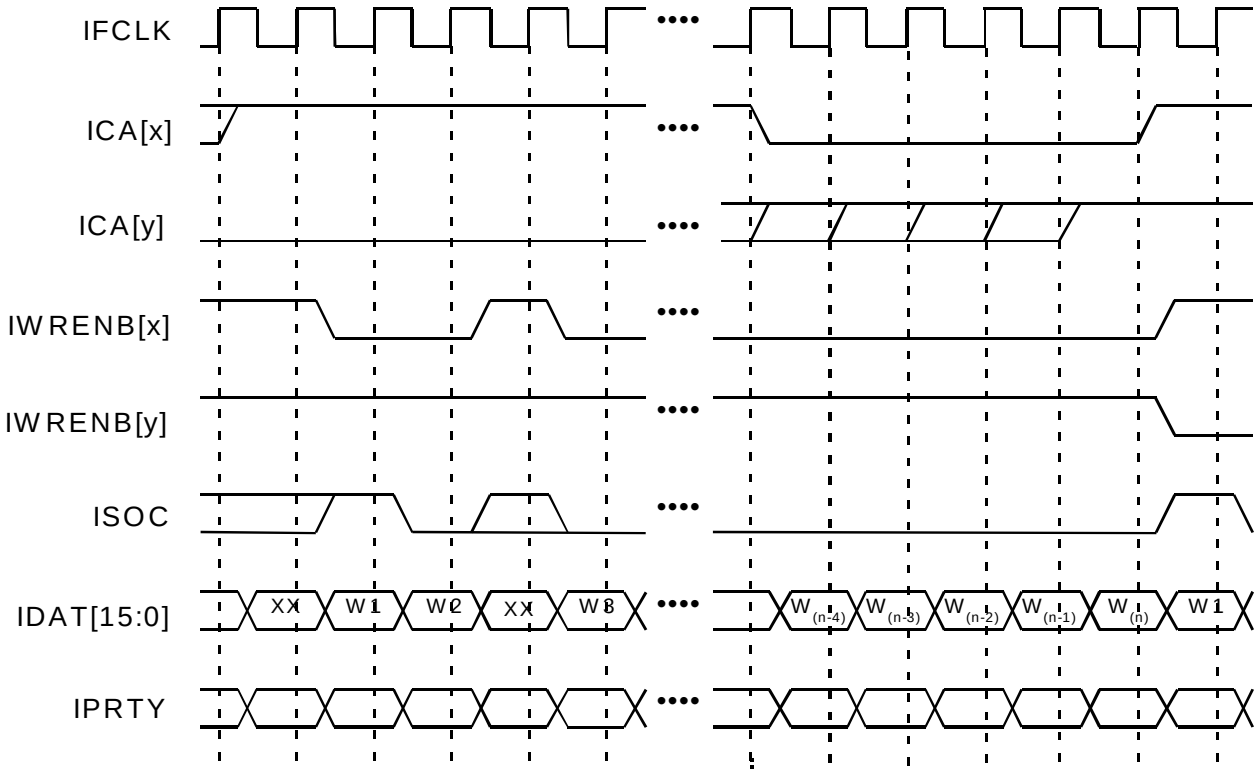


Figure 44 shows the operation of the Egress Input Cell Interface when operating in direct mode, the ATLAS asserts one or more of the cell available outputs, ICA[4:1], to indicate that there is space available to store a cell in the corresponding FIFO(s. ICA[x] remains asserted until the FIFO can accept at most four writes to complete the current cell and is deasserted to indicate that the apparent FIFO depth has been reached. After sampling the asserted ICA[x] output, the Tx-Master device chooses to write a cell for PHY[x] by asserting IWRENB[x] (active low) and simultaneously driving IDAT[15:0] with the words/octets of the cell data structure, asserting ISOC to mark the beginning of a cell data structure. At any time, the Tx-Master device can pause the transfer by de-asserting IWRENB[x] for one or more cycles.

Although the Tx-Master may receive multiple asserted ICA[4:1] signals from the Tx-Slave interface, it shall never assert more than one IWRENB[4:1] lines simultaneously, or assert a different IWRENB[4:1] signal in the middle of a transfer. The IWRENBI interrupt will be generated when this condition is detected. If two or more IWRENB[x] lines are asserted at the start of the transfer, the ATLAS will service that with the lowest numeric index (i.e. IWRENB[1] has the highest priority). If a change in the IWRENB[4:1] lines is detected while a transfer is in progress, it will be ignored unless ISOC is also asserted, in which case the partial cell will be discarded (restoring the various counters for that FIFO) and a new cell transfer for the PHY having the highest priority will be started. This situation will cause the generation of both the ISOCI and IWRENBI interrupts.

Due to pipelining within the ATLAS Egress Input Cell Interface, it is possible that ICA[x] may be deasserted more than 4 cycles before the end of a cell if the Tx-Master device pauses the cell transfer in the cycle where the fifth to last word/octet could have been transferred. In this situation a Tx-Master device supporting octet-level handshaking will transfer 4 more words/octets and then wait for ICA[x] to be reasserted before transferring the last octet. Thus, the cell transfer will be suspended until an additional cell slot is freed in the FIFO and will pause indefinitely if the apparent FIFO depth is set to 1. For this reason, the Tx-Master device connected to the Egress Input Cell Interface must be a true cell-level handshaking device.

Although present for both cell transfers illustrated in this example, it is not necessary for ISOC to be present for each cell; the input cell write address is generated by an internal counter that flywheels in the absence of ISOC. If ISOC is sampled high during any byte other than the first byte of the data structure, the input cell write address counter is reset to the first byte of the data structure and an error condition is signaled on the ISOCI output. However, the ATLAS will still respond to all other control signals necessary to complete the transfer.

Figure 45 Egress Input Cell Interface Polled Mode (IPOLL=1)

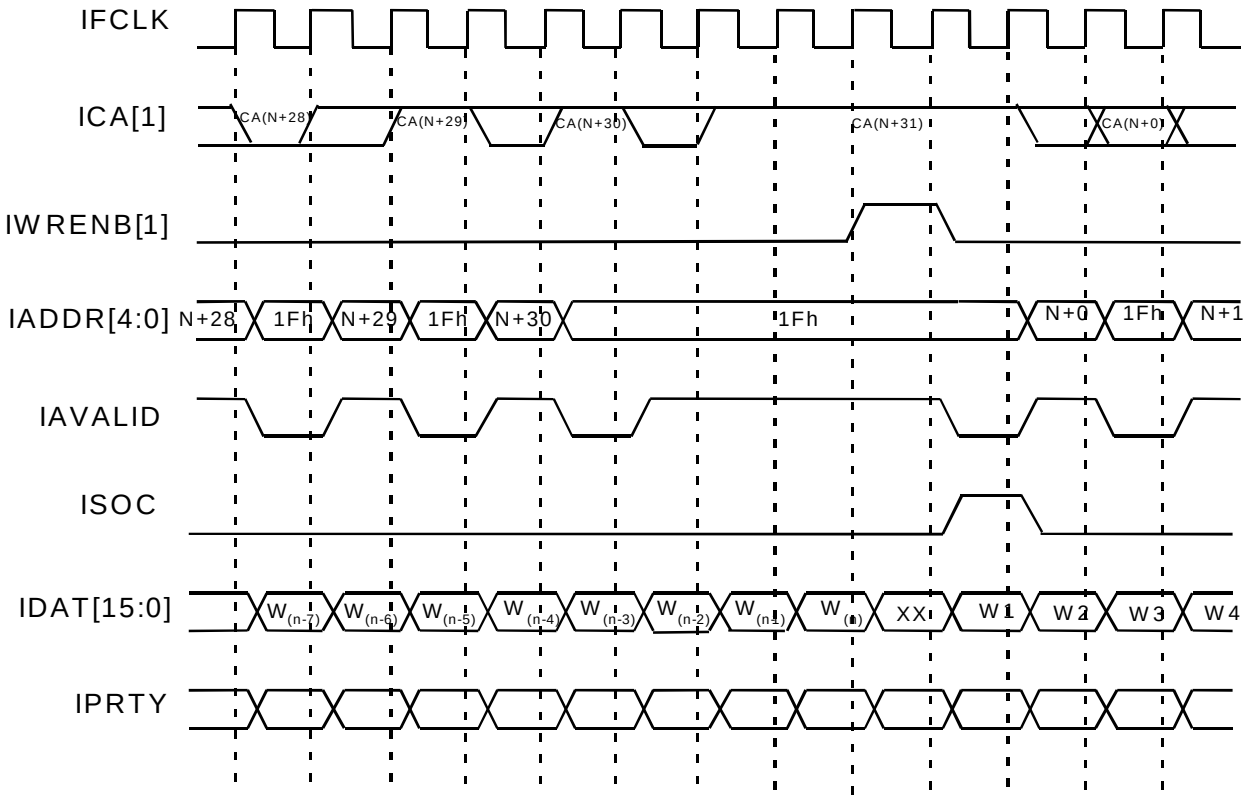


Figure 45 shows the Egress Input Cell Interface configured for polling with 32 PHYs. In this example, each PHY in the Egress Input Cell Interface is polled using the IADDR[4:0] and IAVALID signal while the IWRENB[1] signal is low. As the transfer is completed, the Tx-master device drives IWRENB[1] high and IAVALID is asserted while selecting the PHY for the next transfer by driving its address on the IADDR[4:0] bus in the cycle before IWRENB[1] is driven low. The ATLAS will respond to all polled addresses that have been programmed into the PHYDEV[4:0] bits of the Egress Input Cell Interface Configuration 2 register and return a deasserted ICA when polling an unconfigured PHY. Note that, in the above example, device PHY N+31 corresponds to address 0x1F (PHY#32) and is the last PHY to be polled. After the polling cycle is completed, the master leaves the bus on '1F' (the standard idle value during gap cycles) and then selects PHY#32 by asserting IWRENB[1]. Also note that IAVALID may be tied high when fewer than 32 PHYs are polled, in which case IADDR should be driven to '1F' when an address is not being polled or selected.

12.4 Egress Output Cell Interface

Figure 46 Egress Output Cell Interface Direct Mode (TPOLL=0)

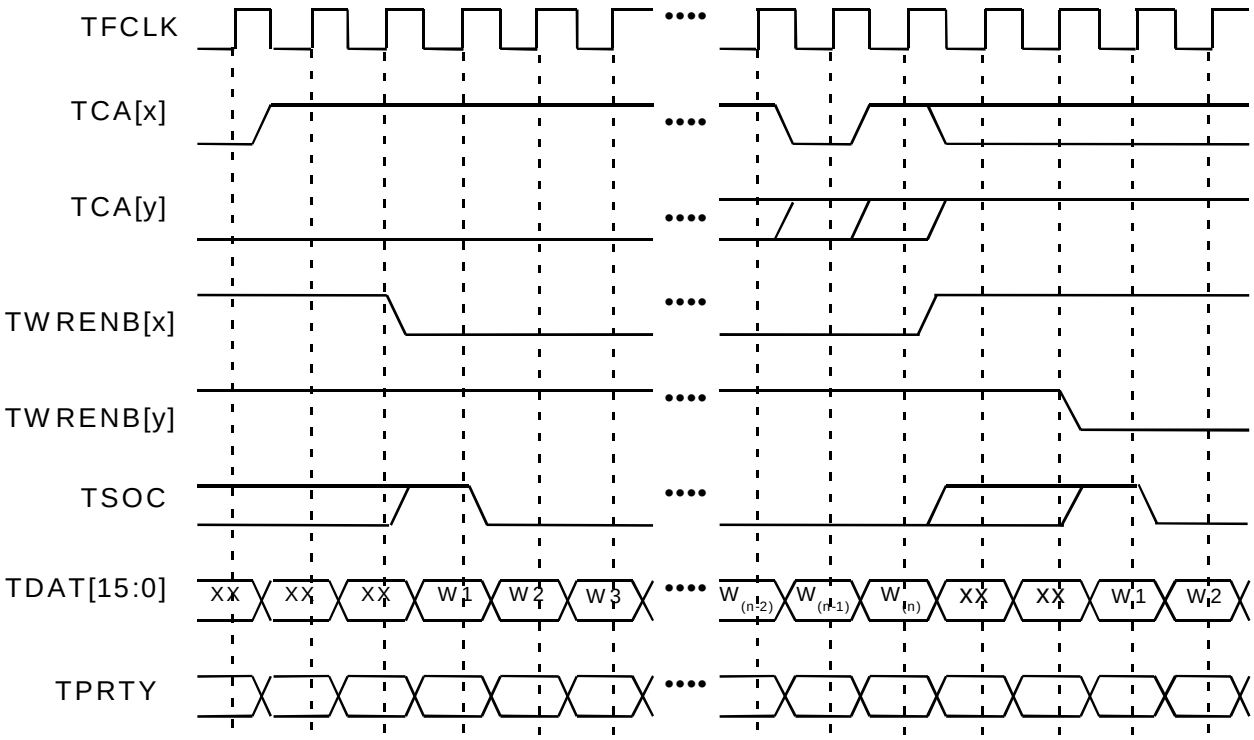


Figure 46 illustrates the operation of the ATLAS Egress Output Cell Interface in direct mode (TPOLL=0). In this mode, each PHY device is connected to its own TCA and TWRENB lines and the Egress Output Cell Interface does not poll the PHYs but instead monitors the TCA's using a round robin priority scheme to arbitrate when cell transfers can be performed for more than one PHY (to ensure fairness). When the Egress Output Cell FIFO has a cell in the associated FIFO and TCA[x] signal is asserted the output interface will assert the appropriate TWRENB to start the transfer.

Figure 47 Egress Output Cell Interface Polled Mode (TPOLL=1)

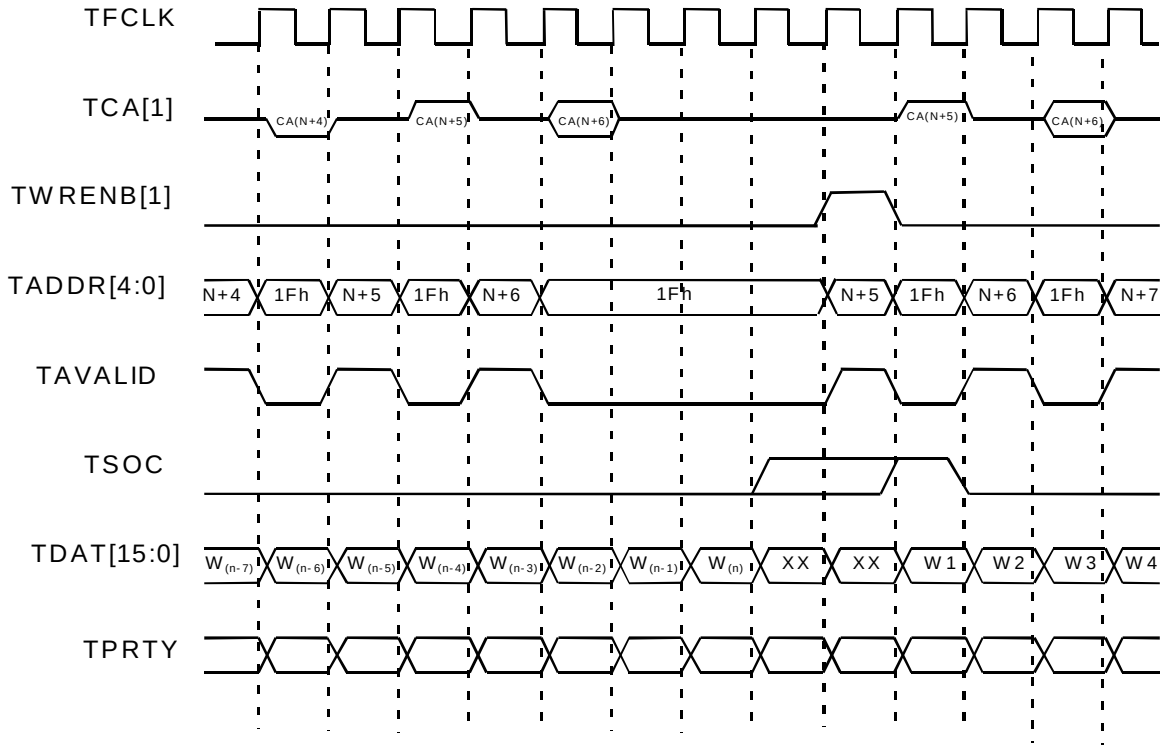


Figure 47 illustrates the operation of the ATLAS Egress Output Cell Interface in Tx-Master polled mode. The PHY devices for which a cell is available in the corresponding FIFO are polled cyclically beginning with the PHY following that for which a transfer is in progress. The polling continues until a PHY is found to assert TCA[1] The polling sequence is then interrupted in order to select the PHY#N. PHY#N is then excluded from the polling sequence until the transfer is almost completed and the 'early warning' TCA status is available. This is because PHY devices compliant with the UTOPIA Level 1 interface (which can be used in polling mode with external glue logic) cannot indicate availability of a subsequent cell while they are simultaneously transferring a cell until 4 cycles before the end of a cell transfer. Once transfer of the current cell is almost complete, PHY#N is re-inserted into the polling sequence so that it may be polled in the 4 cycles before the end of the transfer. (If the number of PHY devices being polled, as given by the PHYDEV[4:0] configuration bits of the Egress Output Cell Interface Configuration 2 register, is large and the Egress Output Cell Interface is operating using word transfers, more time may be required to poll all the PHY devices than to transfer a cell over the interface, in which case cell transfer will complete before PHY#N is due to be polled, in which case the temporary exclusion of PHY#N will not be apparent.)

When the output FIFO is ready to send a cell, polling ceases and the PHY device is selected for transfer of the next cell. The PHY device recognizes that it has been selected to receive the next cell from the Egress Output Cell Interface by the presence of its ID on TADDR[4:0] during the clock cycle prior to TWRENB[1] being asserted low . After TWRENB[1] is asserted low (i.e. at the start of the next cell transfer), the polling process starts again.

13 ABSOLUTE MAXIMUM RATINGS

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 36 Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.3V to +7.0V
Voltage on Any Pin	-0.3V to V_{DD}+0.3V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±10 mA
Absolute Maximum Junction Temperature	+150°C

14 D.C. CHARACTERISTICS

Tc = -40°C to Tj = +120°C, VDD = 3.3 V ±10%

(Typical Conditions: T_C = 25°C, V_{DD} = 3.3 V)

Table 37 D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage (TTL/CMOS)			0.8	Volts	Guaranteed Input LOW Voltage
V_{IL}	Input Low Voltage (CMOS Only)			$0.3V_{dd}$	Volts	Guaranteed Input LOW Voltage Notes 7
V_{IH}	Input High Voltage (TTL/CMOS)	2.0			Volts	Guaranteed Input HIGH Voltage
V_{IH}	Input High Voltage (CMOS Only)	$0.3V_{dd}$			Volts	Guaranteed Input HIGH Voltage Notes 7
V_{OL}	Output or Bi-directional Low Voltage (TTL/CMOS)			0.4	Volts	V_{DD} = min, I_{OL} = -2 mA, Notes 3
V_{OH}	Output or Bi-directional High Voltage (TTL/CMOS)	2.4			Volts	V_{DD} = max, I_{OH} = 2 mA, Notes 3
I_{ILPU}	Input Low Current (Pull ups)	+10	+45	+100	µA	V_{IL} = GND, Notes 1, 3, 6
I_{IHPU}	Input High Current (Pull ups)	-10		+10	µA	V_{IH} = V_{DD}, Notes 1, 3, 6
I_{IL}	Input Low Current	-10		+10	µA	V_{IL} = GND, Notes 2, 3

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input High Current	-10		+10	µA	$V_{IH} = V_{DD}$, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	
C_{OUT}	Output Capacitance		5		pF	
C_{IO}	Bidirectional Capacitance		5		pF	
I_{DDOP}	Operating Current Processing Cells			1500	mA	V_{DD} = 3.6 V, Outputs Unloaded, All Clocks at 50 MHz.

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Pins d[15:0], a[11:0], ale, csb, rdb, wrb, rstb, halfsecclk, tdi, tck, tms, trstb.
5. Pins d[15:0], intb, idreq, edreq, busyb, tdo.
6. Pins tdi, tck, tms, trstb, ale, rstb.
7. Pins RFCLK, OFCLK, IFCLK,TFCLK, ESYSCLK and ISYSCLK.

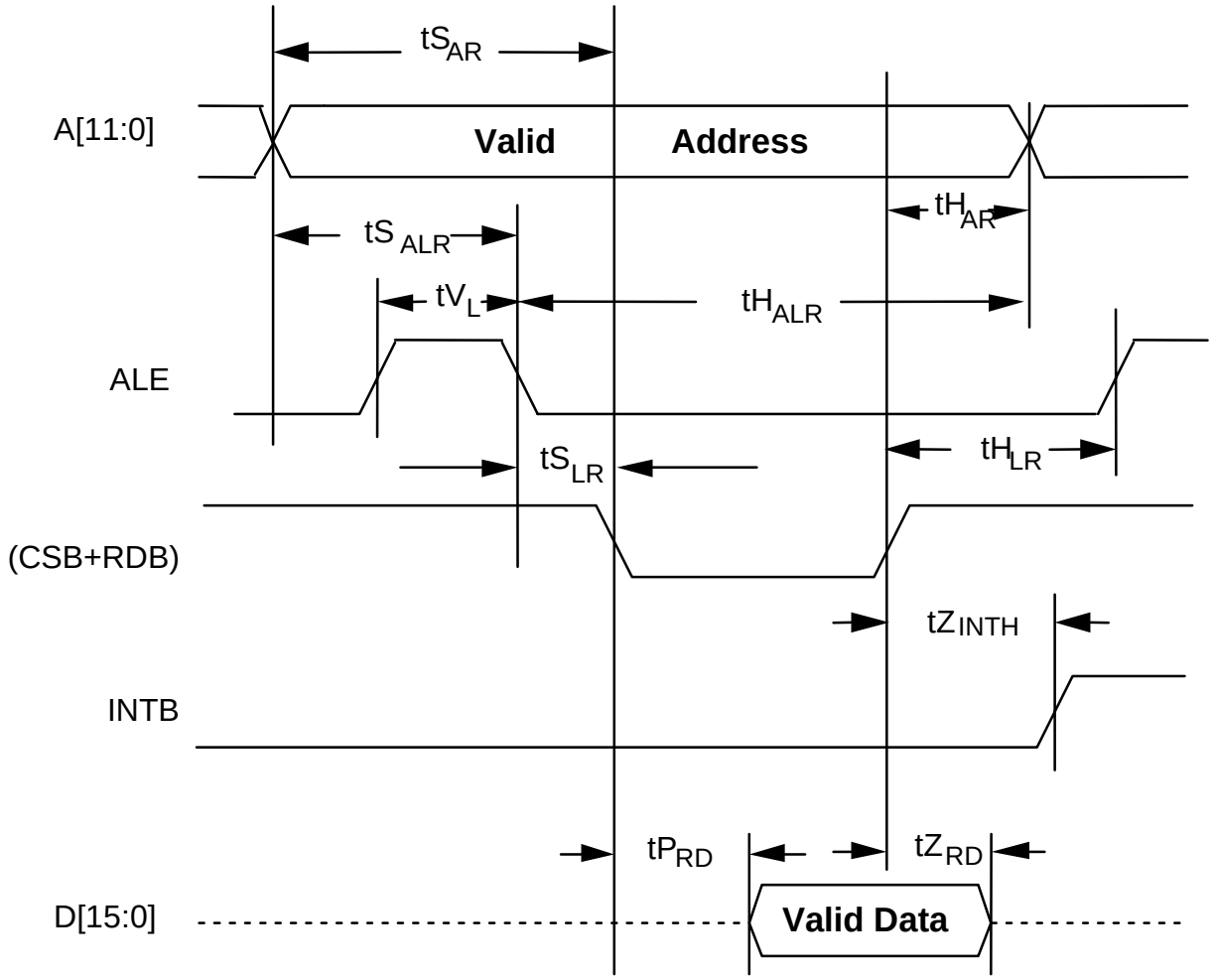
15 A.C. TIMING CHARACTERISTICS

(T_j = -40°C to +120°C, V_{DD} = 3.3 V ±10%, VDD <= BIAS <= 5.5V)

Table 38 Microprocessor Interface Read Access

Symbol	Parameter	Min	Typ	Max	Units
tSAR	Address to Valid Read Set-up Time	10			ns
tHAR	Address to Valid Read Hold Time	5			ns
tSALR	Address to Latch Set-up Time		10		Ns
tHALR	Address to Latch Hold Time		10		ns
tVL	Valid Latch Pulse Width	20			ns
tSLR	Latch to Read Set-up		0		ns
tHLR	Latch to Read Hold		5		ns
tPRD	Valid Read to Valid Data Propagation Delay			50	ns
tZRD	Valid Read Negated to Output Tri-state			20	ns
tZINTH	Valid Read Negated to Output Tri-state			50	ns

Figure 48 Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point o\ the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALR, tHALR, tVL, and tSLR are not applicable.

5. Parameter tHAR is not applicable if address latching is used.

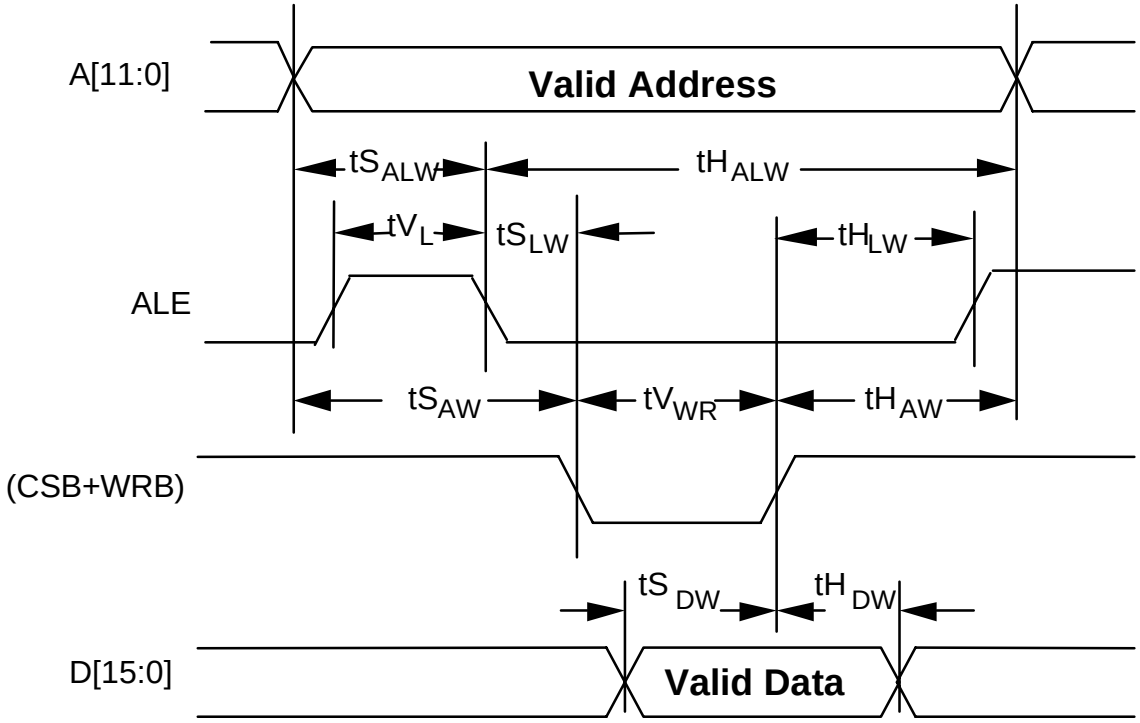
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 39 Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tSAW	Address to Valid Write Set-up Time	10		ns
tSDW	Data to Valid Write Set-up Time	20		ns
tSALW	Address to Latch Set-up Time	10		ns
tHALW	Address to Latch Hold Time	10		ns
tVL	Valid Latch Pulse Width	20		ns
tSLW	Latch to Write Set-up	0		ns
tHLW	Latch to Write Hold	5		ns
tHDW	Data to Valid Write Hold Time	5		ns
tHAW	Address to Valid Write Hold Time	5		ns
tVWR	Valid Write Pulse width	40		ns

Figure 49 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALW, tHALW, tVL, and tSLW are not applicable.

3. Parameter tHAW is not applicable if address latching is used.

4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 40 Egress Input Cell Interface

(T_J = -40°C to +120°C, V_{DD} = 3.3 V ±10% except where specified)

Symbol	Description	Min	Typ	Max	Units	Notes
	IFCLK Frequency	24.5		52	%	1
	IFCLK Duty Cycle	40		60	%	
t_{setup}	Set-up time to IFCLK: IWRENB[4:1], IADDR[4:0], IDAT[15:0], IPRTY, ISOC	3			ns	
t_{setup}	IAVALID		3		ns	
t_{hold}	Hold time from IFCLK: IWRENB[4:1], IADDR[4:0], IDAT[15:0], IPRTY, ISOC	1			ns	2
t_{hold}	Hold time from IFCLK: IWRENB[4:1], IADDR[4:0], IDAT[15:0], IPRTY, ISOC	1.5			ns	3
t_{hold}	IAVALID		1		ns	2
t_{hold}	IAVALID		1.5		ns	3
t_{prop}	Propagation Delay Time from IFCLK: ICA[4:1] C_L = 50 pF C_L = 20 pF	1 1		12 11	ns ns	

Notes:

1. Over the IFCLK frequency range 25 MHz to 52 Mhz T_j = -40°C to +120°C. Over the IFCLK frequency range 24.5 to 25 MHz T_j = -20°C to +120°C.
2. IFCLK = 52 MHz to 40 MHz.
3. IFCLK = 40 MHz to 24.5 MHz.

Figure 50 Egress Input Cell Interface Timing

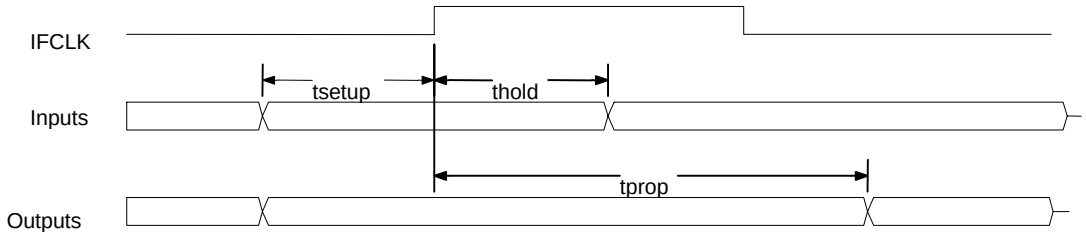


Table 41 Ingress Output Cell Interface

(T_J = -40°C to +120°C, V_{DD} = 3.3 V ±10% except where specified)

Symbol	Description	Min	Max	Units	Notes
	OFCLK Frequency	24.5	52	MHz	1
	OFCLK Duty Cycle	40	60	%	
t_{setup}	Set-up time to OFCLK: ORDENB	3		ns	
t_{hold}	Hold time from OFCLK: ORDENB	1		ns	2
t_{hold}	Hold time from OFCLK: ORDENB	1.5		ns	3
t_{prop}	Propagation Delay Time from OFCLK: OSOC, OCA, OPRTY, ODAT[15:0]				
	C_L = 50 pF	1	12	ns	
	C_L = 20 pF	1	10	ns	

Notes:

1. Over the OFCLK frequency range 25 MHz to 52 Mhz T_j = -40°C to +120°C. Over the OFCLK frequency range 24.5 to 25 MHz T_j = -20°C to +120°C.
2. OFCLK = 52 MHz to 40 MHz.
3. OFCLK = 40 MHz to 24.5 MHz.

Figure 51 Ingress Output Cell Interface Timing

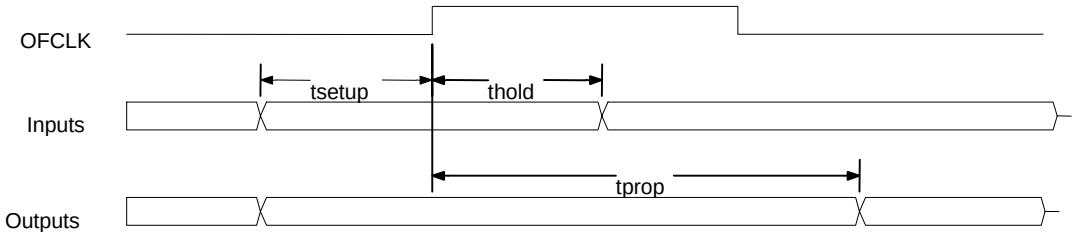


Table 42 Ingress Input Cell Interface

(T_J = -40°C to +120°C, V_{DD} = 3.3 V ±10% except where specified)

Symbol	Description	Min	Max	Units	Notes
	RFCLK Frequency	24.5	52	MHz	1
	RFCLK Duty Cycle	40	60	%	
t_{setup}	Set-up time to RFCLK: RPRTY, RDAT[15:0], RCA[4:1], RSOC	3		ns	
t_{hold}	Hold time from RFCLK: RPRTY, RDAT[15:0], RCA[4:1], RSOC	1		ns	2
t_{hold}	Hold time from RFCLK: RPRTY, RDAT[15:0], RCA[4:1], RSOC	1.5		ns	3
t_{prop}	Propagation Delay Time from RFCLK: RRDENB[4:1], RADDR[4:0], RAVALID				
	C_L = 50 pF	1	12	ns	ns
	C_L = 20 pF	1	10	ns	ns

Notes:

1. Over the RFCLK frequency range 25 MHz to 52 Mhz T_j = -40°C to +120°C. Over the RFCLK frequency range 24.5 to 25 MHz T_j = -20°C to +120°C.
2. RFCLK = 52 MHz to 40 MHz.
3. RFCLK = 40 MHz to 24.5 MHz.

Figure 52 Ingress Input Cell Interface Timing

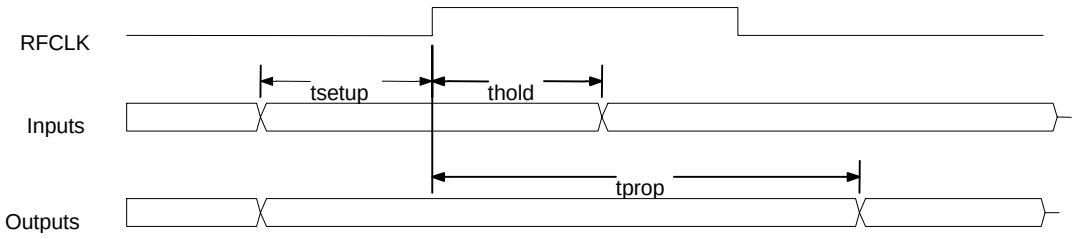


Table 43 Egress Output Cell Interface

(T_J = -40°C to +120°C, V_{DD} = 3.3 V ±10% except where specified)

Symbol	Description	Min	Max	Units	Notes
	TFCLK Frequency	24.5	52	MHz	1
	TFCLK Duty Cycle	40	60	%	
t_{setup}	Set-up time to TFCLK: TCA[4:1]	3		ns	
t_{hold}	Hold time from TFCLK: TCA[4:1]	1		ns	2
t_{hold}	Hold time from TFCLK: TCA[4:1]	1.5		ns	3
t_{prop}	Propagation Delay Time from TFCLK: TDAT[15:0], TPRTY, TSOC, TADDR[4:0], TWRENB[4:1], TAVALID C_L = 50 pF C_L = 20 pF	 1 1	 12 10	 ns ns	

Notes:

1. Over the TFCLK frequency range 25 MHz to 52 Mhz T_j = -40°C to +120°C. Over the TFCLK frequency range 24.5 to 25 MHz T_j = -20°C to +120°C.
2. TFCLK = 52 MHz to 40 MHz.
3. TFCLK = 40 MHz to 24.5 MHz.

Figure 53 Egress Output Cell Interface Timing

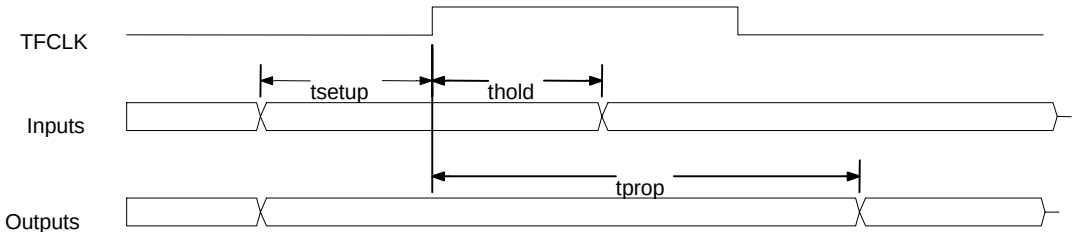


Table 44 Ingress SRAM Interface

(T_J = -40°C to +120°C, V_{DD} = 3.3 V ±10% except where specified)

Symbol	Description	Min	Max	Units	Notes
	ISYSCLK Frequency	24.5	52	MHz	1
	ISYSCLK Duty Cycle	40	60	%	
t_{setup}	Set-up time to ISYSCLK: ISD[63:0]	4		ns	
t_{setup}	Set-up time to ISYSCLK: ISP[7:0]	4.5		ns	
t_{hold}	Hold time from ISYSCLK: ISD[63:0], ISP[7:0]	2		ns	
t_{prop}	Propagation Delay Time from ISYSCLK: ISOEB				
	C_L = 50 pF	2	14	ns	
	C_L = 20 pF	2	12	ns	
t_{prop}	Propagation Delay Time from ISYSCLK: ISD[63:0], ISP[7:0]				
	C_L = 50 pF	1	14	ns	
	C_L = 20 pF	1	13	ns	
t_{prop}	Propagation Delay Time from ISYSCLK: ISADSB, ISRWB, ISA[19:0]				
	C_L = 50 pF	1	14	ns	
	C_L = 20 pF	1	12	ns	

Notes:

1. Over the ISYSCLK frequency range 25 MHz to 52 Mhz T_j = -40°C to +120°C. Over the ISYSCLK frequency range 24.5 to 25 MHz T_j = -20°C to +120°C.

Figure 54 Ingress SRAM Interface Timing

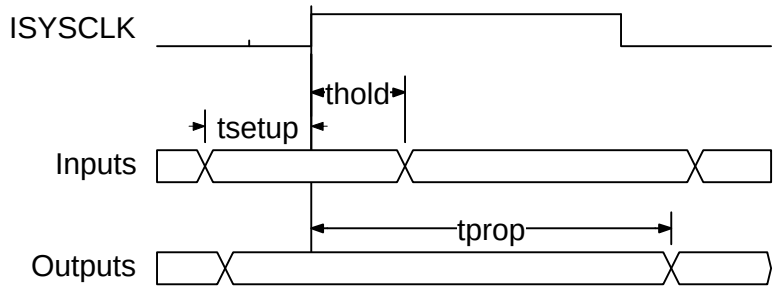


Table 45 Egress SRAM Interface

(T_J = -40°C to +120°C, V_{DD} = 3.3 V ±10% except where specified)

Symbol	Description	Min	Max	Units	Notes
	ESYSCLK Frequency	24.5	52	MHz	1
	ESYSCLK Duty Cycle	40	60	%	
t_{setup}	Set-up time to ESYSCLK: ESD[31:0], ESP[3:0]	4		ns	
t_{hold}	Hold time from ESYSCLK: ESD[31:0], ESP[3:0]	2		ns	
t_{prop}	Propagation Delay Time from ESYSCLK: ESOEB				
	C_L = 50 pF				
	C_L = 20 pF	2	14	ns	
		2	12	ns	
t_{prop}	Propagation Delay Time from ESYSCLK: ESD[31:0], ESP[3:0]				
	C_L = 50 pF	1	14	ns	
	C_L = 20 pF	1	13	ns	
t_{prop}	Propagation Delay Time from ESYSCLK: ESADSB, ESRWB, ESA[19:0]				
	C_L = 50 pF	1	14	ns	
	C_L = 20 pF	1	12	ns	

Notes:

1. Over the ESYSCLK frequency range 25 MHz to 52 Mhz T_j = -40°C to +120°C. Over the ESYSCLK frequency range 24.5 to 25 MHz T_j = -20°C to +120°C.

Figure 55 Egress SRAM Interface Timing

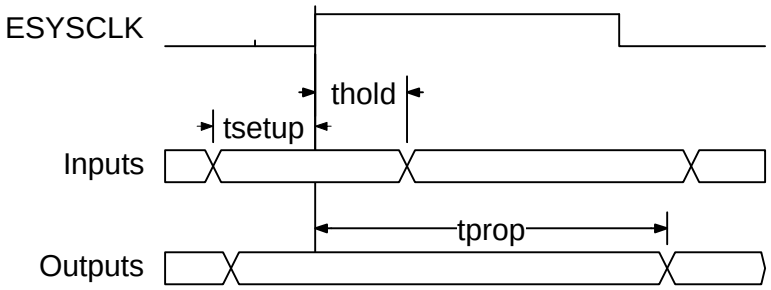
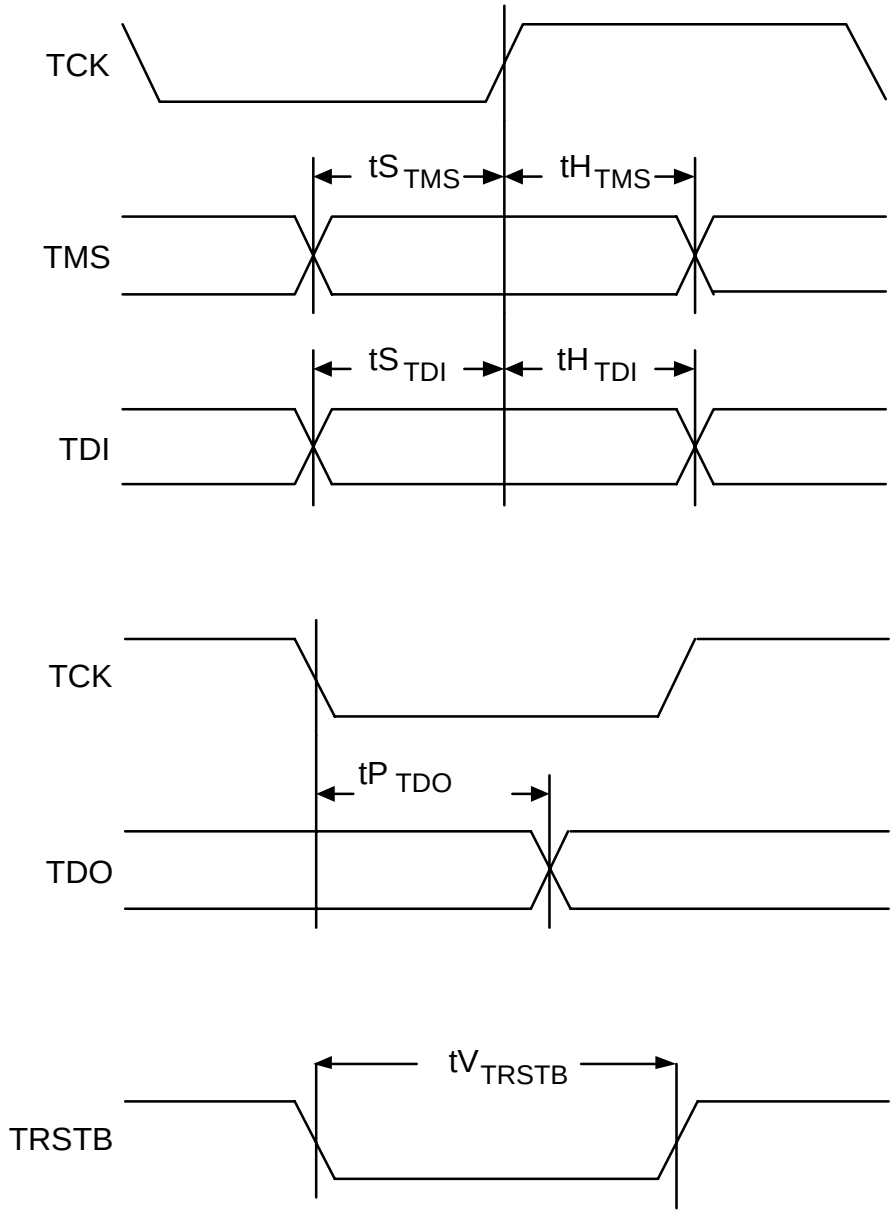


Table 46 JTAG Port Interface

(T_J = -40°C to +120°C, V_{DD} = 3.3 V ±10% except where specified)

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
tSTMS	TMS Set-up time to TCK	50		ns
tHTMS	TMS Hold time to TCK	50		ns
tSTDI	TDI Set-up time to TCK	50		ns
tHTDI	TDI Hold time to TCK	50		ns
tPTDO	TCK Low to TDO Valid	2	50	ns
tVTRSTB	TRSTB Pulse Width	100		ns

Figure 56 JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Output propagation delays are measured with a 50 pF load on the outputs unless otherwise specified.

3. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to the +/- 300mV of the termination voltage on the output. The test load is 50Ohm in parallel with 10pF to GND.

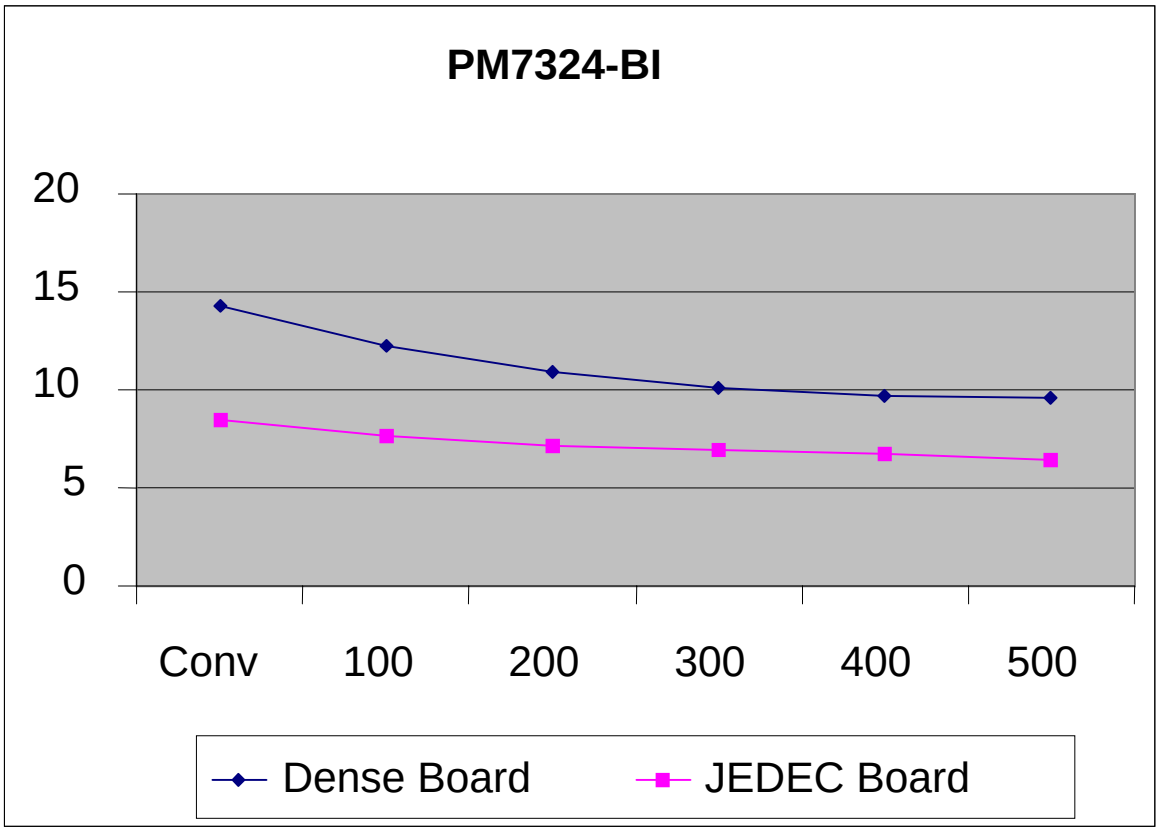
Table 47 Ordering Information

Part No.	Description
PM7324-BI	432 Super Ball Grid Array (SBGA)

Table 48 Thermal Information

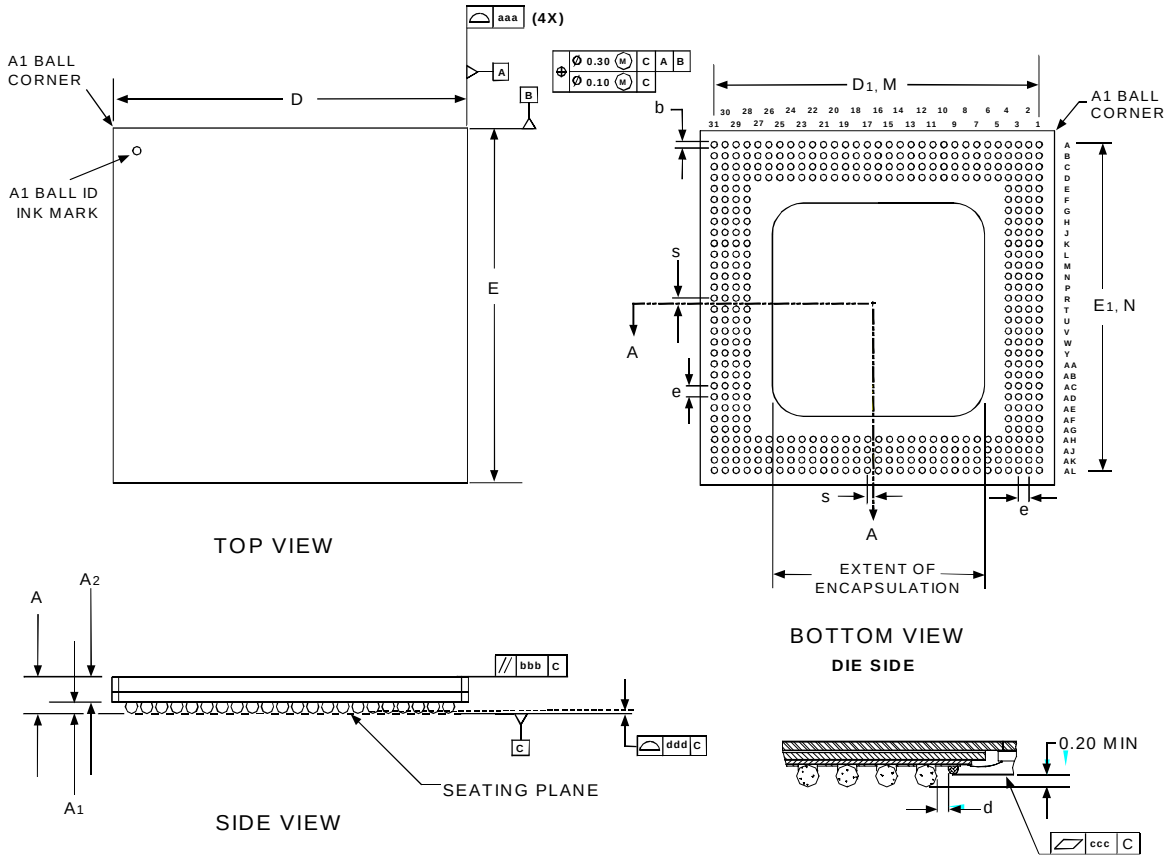
Part No.	Case Temperature	Theta Ja	Theta Jc
PM7324-BI	-40°C to 85°C	14.3 °C/W	1 °C/W

Figure 57 ATLAS THETA JA vs. Air Flow Graph



16 MECHANICAL INFORMATION

Figure 58 432 PIN SBGA – 40 x 40 MM BODY -(B SUFFIX)



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ccc DENOTES FLATNESS.
5) DIMENSION ddd DENOTES COPLANARITY.

PACKAGE TYPE : 432 THERMALLY ENHANCED BALL GRID ARRAY - SBGA																
BODY SIZE : 40 x 40 x 1.54 MM																
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	d	e	aaa	bbb	ccc	ddd	S
Min.	1.30	0.50	0.80	39.90	38.00	39.90	38.00		0.60	0.5	-	-	-	-		-
Nom	1.51	0.60	0.91	40.00	38.10	40.00	38.10	31x31	0.75	-	1.27	-	-	-		0.00
Max.	1.70	0.70	1.00	40.10	38.20	40.10	38.20		0.90	-	-	0.20	0.25	0.20	0.20	-

NOTES:

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