

Octal registered transceivers

74F543, 74F544

74F543 Octal registered transceiver, non-inverting (3-State)
 74F544 Octal registered transceiver, inverting (3-State)

FEATURES

- Combines 74F245 and 74F373 type functions in one chip
- 8-bit octal transceiver with D-type latch
- 74F543 Non-inverting
74F544 Inverting
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 20mA and source 3mA
- B outputs sink 64mA and source 15mA
- 3-State outputs for bus-oriented applications
- 74F543 available in SSOP Type II package

DESCRIPTION

The 74F543 and 74F544 Octal Registered Transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. While the 74F543 has non-inverting data path, the 74F544 inverts data in both directions. The A outputs are guaranteed to sink 24mA, while the B outputs are rated for 64mA.

FUNCTIONAL DESCRIPTION

The 74F543 and 74F544 contain two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{EAB}$) input must be Low in order to enter data from A0 - A7 or take data from B0 - B7, as indicated in the Function Table. With $\overline{EAB}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent Low-to-High transition for the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches. Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F543	6.0ns	80mA
74F544	6.5ns	95mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$	DRAWING NUMBER
24-pin plastic skinny DIP (300mil)	N74F543N, N74F544N	SOT222
24-pin plastic SOL	N74F543D, N74F544D	SOT137-1
24-pin plastic SSOP Type II	74F543DB	SOT340-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

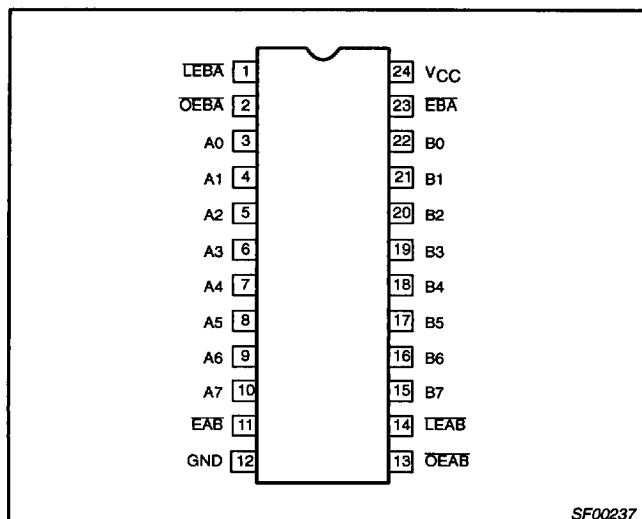
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F543 74F544	A0 - A7	Port A, 3-State inputs	3.5/1.0	70 μ A/0.6mA
	B0 - B7	Port B, 3-State inputs	3.5/1.0	70 μ A/0.6mA
	$\overline{OEAB}$	A-to-B Output Enable input (Active Low)	1.0/1.0	20 μ A/0.6mA
	$\overline{OEBA}$	B-to-A Output Enable input (Active Low)	1.0/1.0	20 μ A/0.6mA
	$\overline{EAB}$	A-to-B Enable input (Active Low)	1.0/2.0	20 μ A/1.2mA
	$\overline{EBA}$	B-to-A Enable input (Active Low)	1.0/2.0	20 μ A/1.2mA
	$\overline{LEAB}$	A-to-B Latch Enable input (Active Low)	1.0/1.0	20 μ A/0.6mA
	$\overline{LEBA}$	B-to-A Latch Enable input (Active Low)	1.0/1.0	20 μ A/0.6mA
74F543	A0 - A7	Port A, 3-State outputs	150/40	3.0mA/24mA
	B0 - B7	Port B, 3-State outputs	750/106.7	15mA/64mA
74F544	$\overline{A0} - \overline{A7}$	Port $\overline{A}$, 3-State outputs	150/40	3.0mA/24mA
	$\overline{B0} - \overline{B7}$	Port $\overline{B}$, 3-State outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST Unit Load is defined as: 20 μ A in the High State and 0.6mA in the Low state.

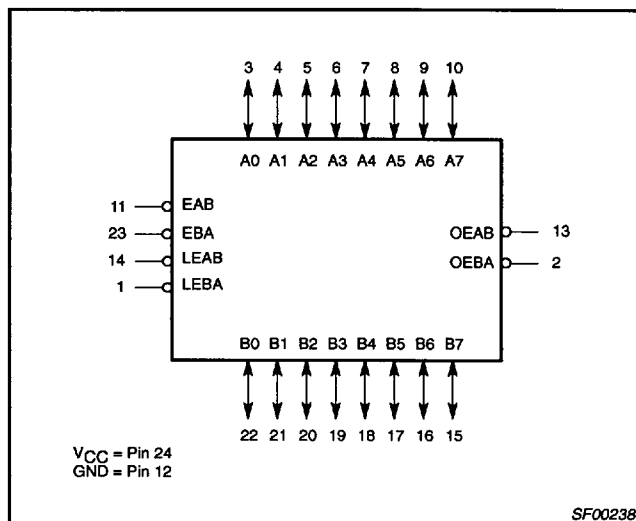
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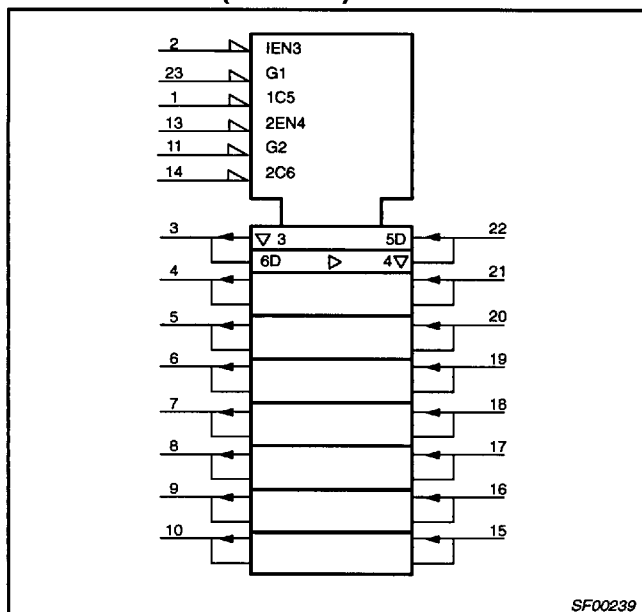
PIN CONFIGURATION – 74F543



LOGIC SYMBOL – 74F543



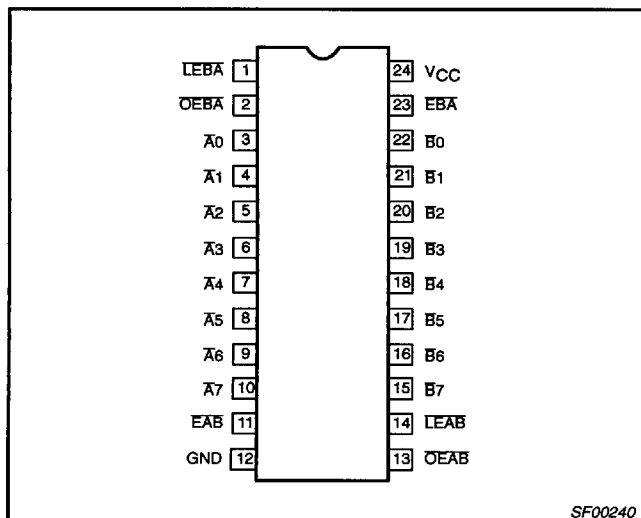
LOGIC SYMBOL (IEEE/IEC) – 74F543



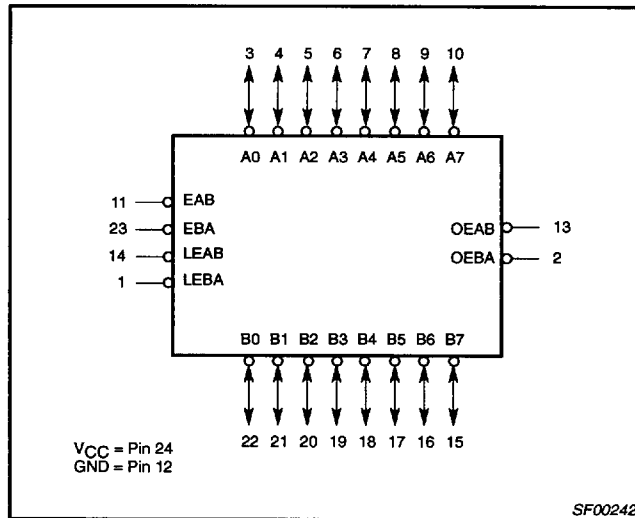
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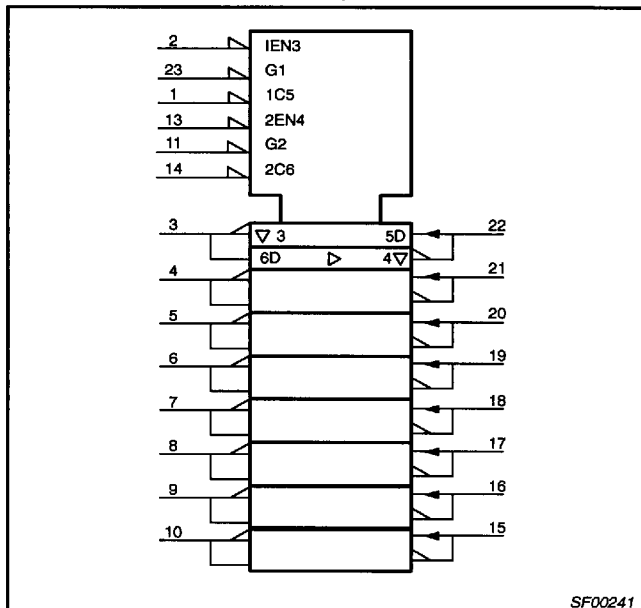
PIN CONFIGURATION – 74F544



LOGIC SYMBOL – 74F544



LOGIC SYMBOL (IEEE/IEC) – 74F544



FUNCTION TABLE for 74F543 and 74F544

INPUTS				OUTPUTS		STATUS
OE _{XX}	EX _{XX}	LE _{XX}	DATA	74F543	74F544	
H	X	X	X	Z	Z	Disabled
X	H	X	X	Z	Z	Disabled
L	↑	L	h	Z	Z	Disable + Latch
L	↑	L	l	Z	Z	Disable + Latch
L	L	↑	h	H	L	Latch + Display
L	L	↑	l	L	H	Latch + Display
L	L	L	H	H	L	Transparent
L	L	L	L	L	H	Transparent
L	L	H	X	NC	NC	Hold

H = High voltage level

L = Low voltage level

h = High state must be present one setup time before the Low-to-High transition of LE_{XX} or EX_{XX} (XX=AB or BA)l = Low state must be present one setup time before the Low-to-High transition of LE_{XX} or EX_{XX} (XX=AB or BA)↑ = Low-to-High transition of LE_{XX} or EX_{XX} XX = AB or BA

X = Don't care

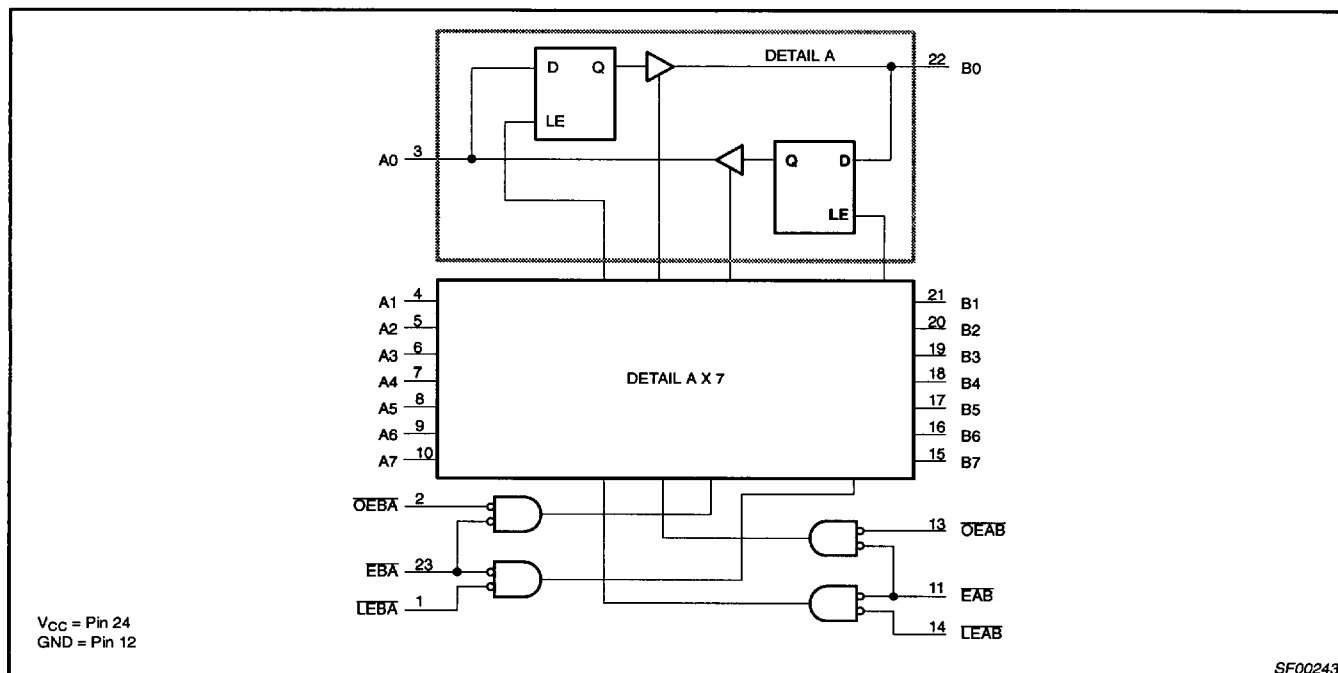
NC = No change

Z = High impedance "off" state

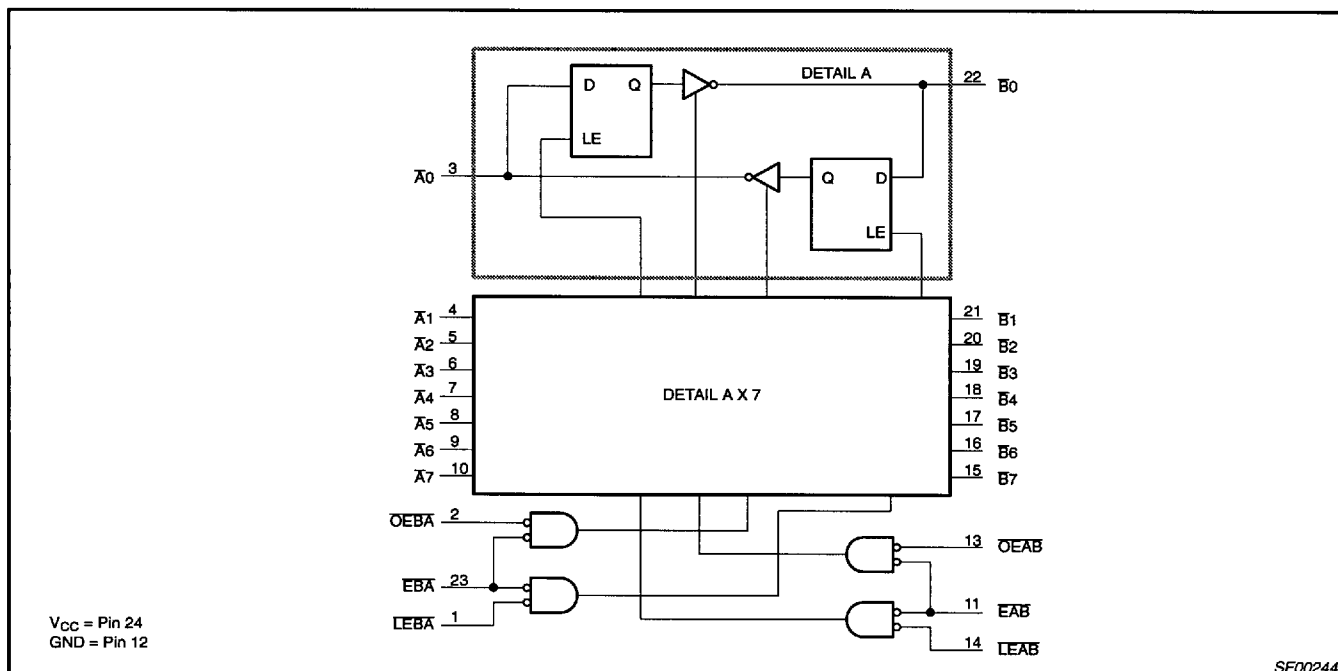
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LOGIC DIAGRAM FOR 74F543



LOGIC DIAGRAM FOR 74F544



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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V _{CC}	Supply voltage		-0.5 to +7.0	V
V _{IN}	Input voltage		-0.5 to +7.0	V
I _{IN}	Input current		-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I _{OUT}	Current applied to output in Low output state	A0 - A7, $\bar{A}0$ - $\bar{A}7$	48	mA
		B0 - B7, $\bar{B}0$ - $\bar{B}7$	128	mA
T _{amb}	Operating free-air temperature range		0 to +70	°C
T _{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5.0	5.5	V
V _{IH}	High-level input voltage		2.0			V
V _{IL}	Low-level input voltage				0.8	V
I _{IK}	Input clamp current				-18	mA
I _{OH}	High-level output current	A0 - A7, $\bar{A}0$ - $\bar{A}7$			-3	mA
		B0 - B7, $\bar{B}0$ - $\bar{B}7$			-15	mA
I _{OL}	Low-level output current	A0 - A7, $\bar{A}0$ - $\bar{A}7$			24	mA
		B0 - B7, $\bar{B}0$ - $\bar{B}7$			64	mA
T _{amb}	Operating free-air temperature range		-0		+70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			UNIT	
						MIN	TYP ²	MAX		
V _{OH}	High-level output voltage	A0 - A7, A0 - A7	V _{CC} = MIN V _{IL} = MAX V _{IH} = MIN	I _{OH} = -3mA	± 10%V _{CC}	2.4			V	
		± 5%V _{CC}			2.7	3.4		V		
		B0 - B7, B0 - B7	I _{OH} = -15mA	± 10%V _{CC}	2.0			V		
				± 5%V _{CC}	2.0			V		
V _{OL}	Low-level output voltage	A0 - A7, A0 - A7	V _{CC} = MIN V _{IL} = MAX V _{IH} = MIN	I _{OL} = 24mA	± 10%V _{CC}		0.35	0.50	V	
		± 5%V _{CC}				0.35	0.50	V		
		B0 - B7, B0 - B7	I _{OL} = 64mA	± 10%V _{CC}			0.55	V		
				± 5%V _{CC}		0.42	0.55	V		
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}				-0.73	-1.2	V	
I _I	Input current at maximum input voltage	OEAB, OEBA, EAB	V _{CC} = MAX, V _I = 7.0 V					100	μA	
		Others	V _{CC} = 5.5, V _I = 5.5V					1	mA	
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V					20	μA	
I _{IL}	Low-level input current	Others	V _{CC} = MAX, V _I = 0.5V					-0.6	mA	
		EAB, EBA						-1.2	mA	
I _{OZH} + I _{IH}	Off-state output current, high-level voltage applied		V _{CC} = MAX, V _O = 2.7V					70	μA	
I _{OZH} + I _{IL}	Off-state output current, Low-level voltage applied		V _{CC} = MAX, V _O = 0. 5V					-600	μA	
I _{OS}	Short-circuit output current ³	A0 - A7, A0 - A7	V _{CC} = MAX			-60		-150	mA	
		B0 - B7, B0 - B7				-100		-225	mA	
I _{CC}	Supply current (total)	74F543	I _{CCH}	V _{CC} = MAX				70	105	mA
			I _{CCL}					95	135	mA
			I _{CCZ}					95	135	mA
		74F544	I _{CCH}	V _{CC} = MAX				80	110	mA
			I _{CCL}					105	140	mA
			I _{CCZ}					100	135	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{\text{amb}} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS FOR 74F543

SYMBOL	PARAMETER	TEST CONDITIONS	74F543 LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = 5.0V C _L = 50pF R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = 5.0V ± 10% C _L = 50pF R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay A _n to B _n	Waveform 2	3.5 3.0	5.5 5.0	8.5 8.0	3.0 2.5	9.0 8.5	ns
t _{PLH} t _{PHL}	Propagation delay B _n to A _n	Waveform 2	2.5 2.5	4.0 4.5	7.0 7.5	2.5 2.5	7.5 8.0	ns
t _{PLH} t _{PHL}	Propagation delay LEBA to A _n	Waveform 1, 2	5.0 4.0	7.0 6.0	10.0 9.0	4.5 4.0	11.0 9.5	ns
t _{PLH} t _{PHL}	Propagation delay LEAB to B _n	Waveform 1, 2	6.0 4.5	8.5 6.5	11.5 9.5	5.5 4.0	12.5 10.0	ns
t _{PZH} t _{PZL}	Output Enable time OEBA to A _n or OEAB to B _n	Waveform 4 Waveform 5	2.0 3.5	4.0 5.0	7.5 8.5	1.5 3.0	8.0 9.0	ns
t _{PHZ} t _{PLZ}	Output Disable time OEBA to A _n or OEAB to B _n	Waveform 4 Waveform 5	1.0 1.5	3.0 4.0	6.5 7.5	1.0 1.0	7.5 8.5	ns
t _{PZH} t _{PZL}	Output Enable time EBA to A _n or EAB to B _n	Waveform 4 Waveform 5	4.5 5.0	7.0 7.0	10.5 10.5	4.0 4.5	11.5 11.0	ns
t _{PHZ} t _{PLZ}	Output Disable time EBA to A _n or EAB to B _n	Waveform 4 Waveform 5	2.5 4.5	5.0 7.0	8.5 11.0	2.0 3.0	9.5 12.0	ns

AC SETUP REQUIREMENTS FOR 74F543

SYMBOL	PARAMETER	TEST CONDITIONS	74F543 LIMITS				UNIT
			T _{amb} = +25°C V _{CC} = 5.0V C _L = 50pF R _L = 500Ω		T _{amb} = 0°C to +70°C V _{CC} = 5.0V ± 10% C _L = 50pF R _L = 500Ω		
			MIN	TYP	MIN	MAX	
t _s (H) t _s (L)	Setup time, High or Low A _n to LEAB or B _n to LEBA	Waveform 3	0.0 2.5		0.0 3.0		ns
t _h (H) t _h (L)	Hold time, High or Low A _n to LEAB or B _n to LEBA	Waveform 3	0.0 1.5		0.0 2.0		ns
t _s (H) t _s (L)	Setup time, High or Low A _n to EAB or B _n to EBA	Waveform 3	1.0 2.5		1.5 3.0		ns
t _h (H) t _h (L)	Hold time, High or Low A _n to EAB or B _n to EBA	Waveform 3	0.0 1.5		0.0 2.0		ns
t _w (L)	Latch enable pulse width, Low	Waveform 3	4.0		4.5		ns

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AC ELECTRICAL CHARACTERISTICS FOR 74F544

SYMBOL	PARAMETER	TEST CONDITIONS	74F544 LIMITS						UNIT
			T _{amb} = +25°C V _{CC} = 5.0V C _L = 50pF R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = 5.0V ± 10% C _L = 50pF R _L = 500Ω			
			MIN	TYP	MAX	MIN	MAX		
t _{PLH} t _{PHL}	Propagation delay A _n to B _n or B _n to A _n	Waveform 1	3.0 3.0	6.5 5.0	9.5 8.0	3.0 3.0	10.5 8.5	ns	
t _{PLH} t _{PHL}	Propagation delay LEBA to A _n	Waveform 1, 2	4.0 4.0	7.0 7.0	9.5 9.5	4.0 4.0	10.5 10.5	ns	
t _{PLH} t _{PHL}	Propagation delay LEAB to B _n	Waveform 1, 2	5.0 4.0	8.0 7.5	11.5 9.5	4.0 4.0	12.5 10.5	ns	
t _{PZH} t _{PZL}	Output Enable time OEBA to A _n or OEAB to B _n	Waveform 4 Waveform 5	2.0 3.5	4.0 5.5	7.0 8.5	1.5 3.0	7.5 9.0	ns	
t _{PHZ} t _{PLZ}	Output Disable time OEBA to A _n or OEAB to B _n	Waveform 4 Waveform 5	1.0 1.5	4.0 4.0	6.5 6.5	1.0 1.5	7.0 7.5	ns	
t _{PZH} t _{PZL}	Output Enable time EBA to A _n or EAB to B _n	Waveform 4 Waveform 5	4.0 4.5	7.0 8.0	9.5 11.0	3.5 4.5	10.0 12.0	ns	
t _{PHZ} t _{PLZ}	Output Disable time EBA to A _n or EAB to B _n	Waveform 4 Waveform 5	2.5 4.5	5.0 8.5	8.0 11.5	2.5 4.0	9.0 11.5	ns	

AC SETUP REQUIREMENTS FOR 74F544

SYMBOL	PARAMETER	TEST CONDITIONS	74F544 LIMITS				UNIT
			T _{amb} = +25°C V _{CC} = 5.0V C _L = 50pF R _L = 500Ω		T _{amb} = 0°C to +70°C V _{CC} = 5.0V ± 10% C _L = 50pF R _L = 500Ω		
			MIN	TYP	MIN	MAX	
t _s (H) t _s (L)	Setup time, High or Low A _n to LEAB or B _n to LEBA	Waveform 3	1.5 1.5		2.0 2.5		ns
t _h (H) t _h (L)	Hold time, High or Low A _n to LEAB or B _n to LEBA	Waveform 3	1.5 2.0		2.5 2.5		ns
t _s (H) t _s (L)	Setup time, High or Low A _n to EAB or B _n to EBA	Waveform 3	1.5 1.5		2.5 2.5		ns
t _h (H) t _h (L)	Hold time, High or Low A _n to EAB or B _n to EBA	Waveform 3	1.5 2.0		2.0 2.0		ns
t _w (L)	Latch enable pulse width, Low	Waveform 3	4.0		4.5		ns

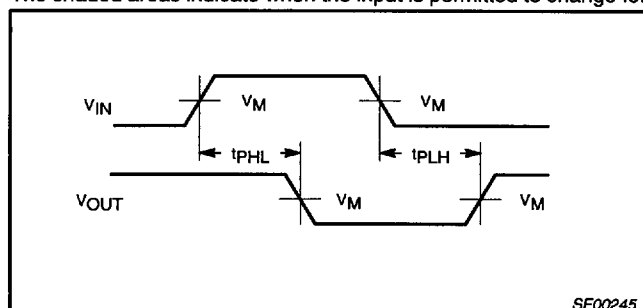
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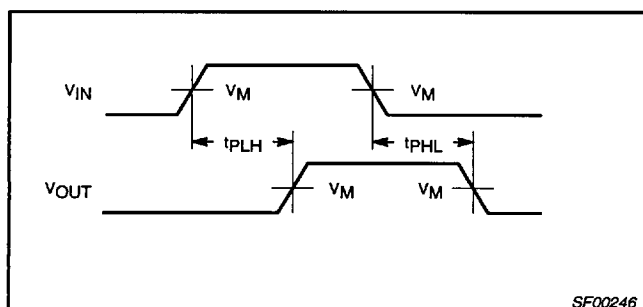
AC WAVEFORMS

 $V_M = 1.5V$

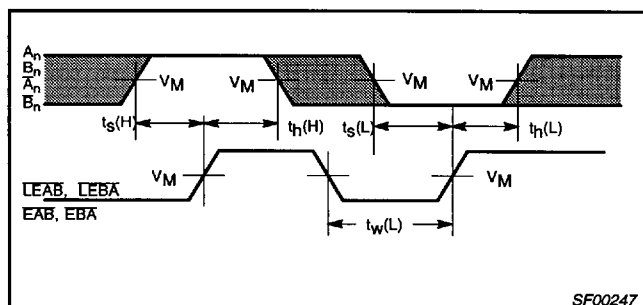
The shaded areas indicate when the input is permitted to change for predictable output performance.



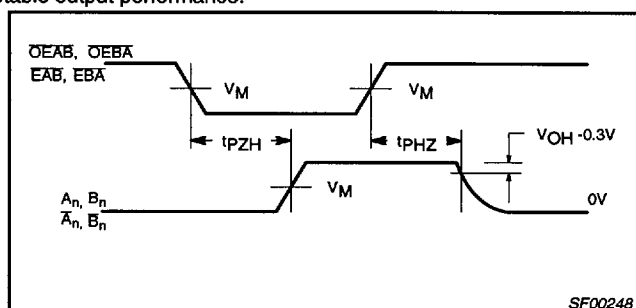
Waveform 1. Propagation Delay for Inverting Outputs



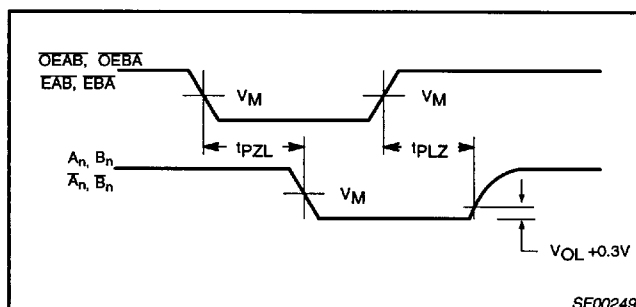
Waveform 2. Propagation Delay for Non-Inverting Outputs



Waveform 3. Data Setup Time and Hold Times, and Latch Enable Pulse Width



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

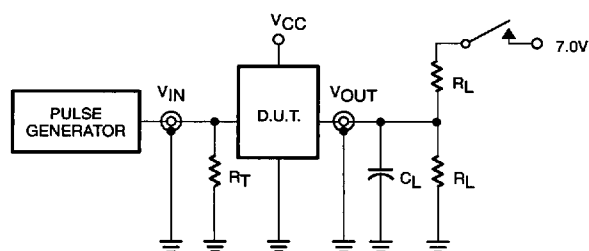


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

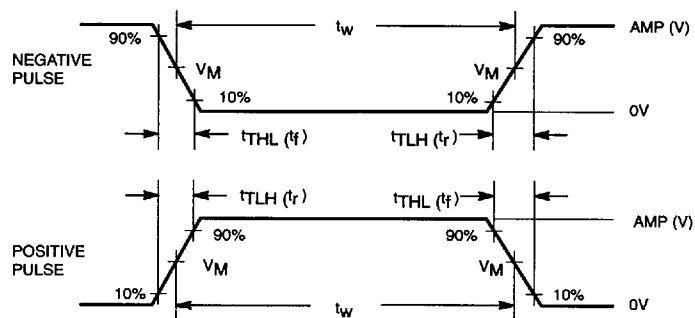
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$
Input Pulse Definition

family	INPUT PULSE REQUIREMENTS				
	amplitude	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

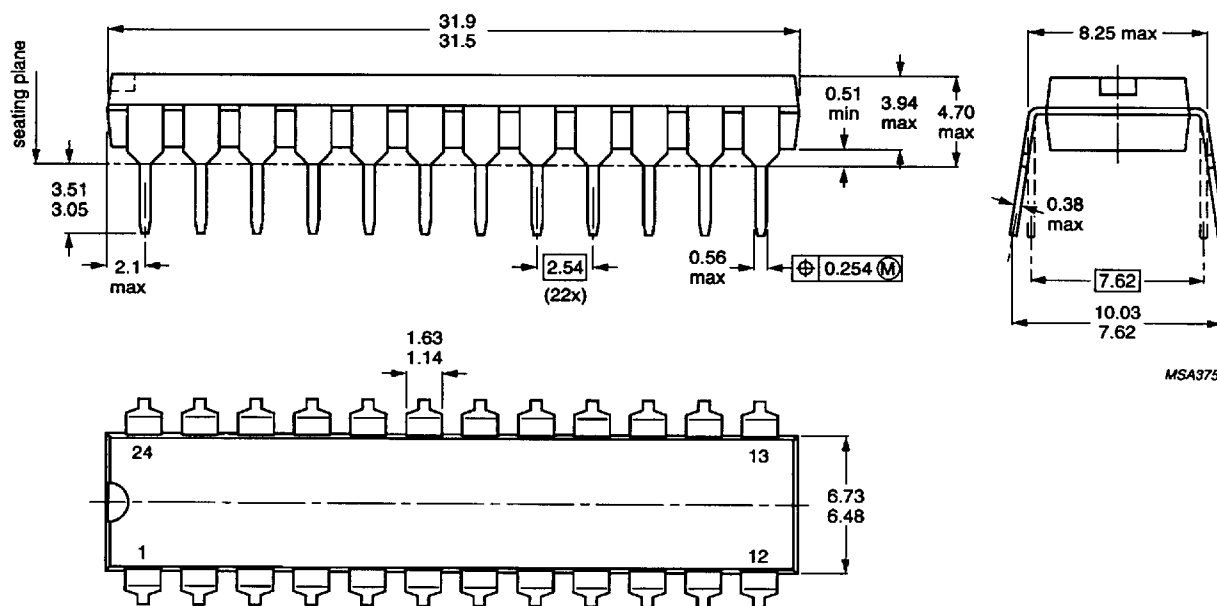
SF00333

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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222



MSA375

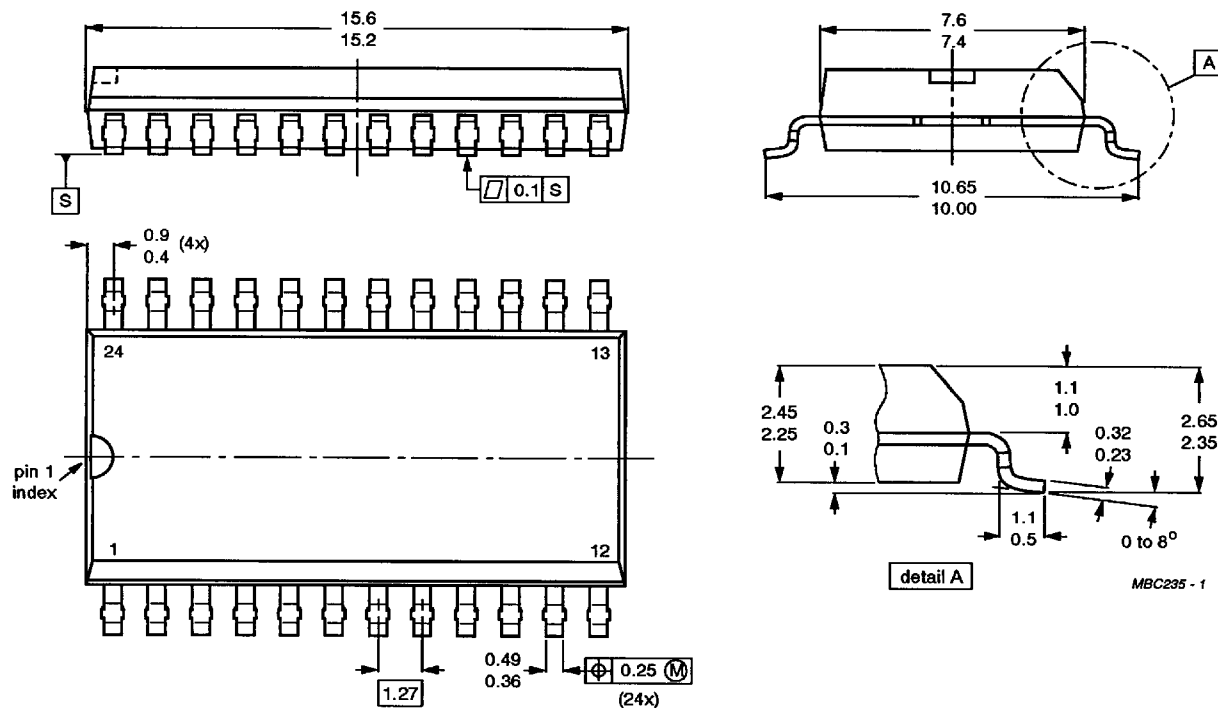
Dimensions in mm.

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SOP24: plastic small outline package; 24 leads; body width 7.5mm

SOT137-1

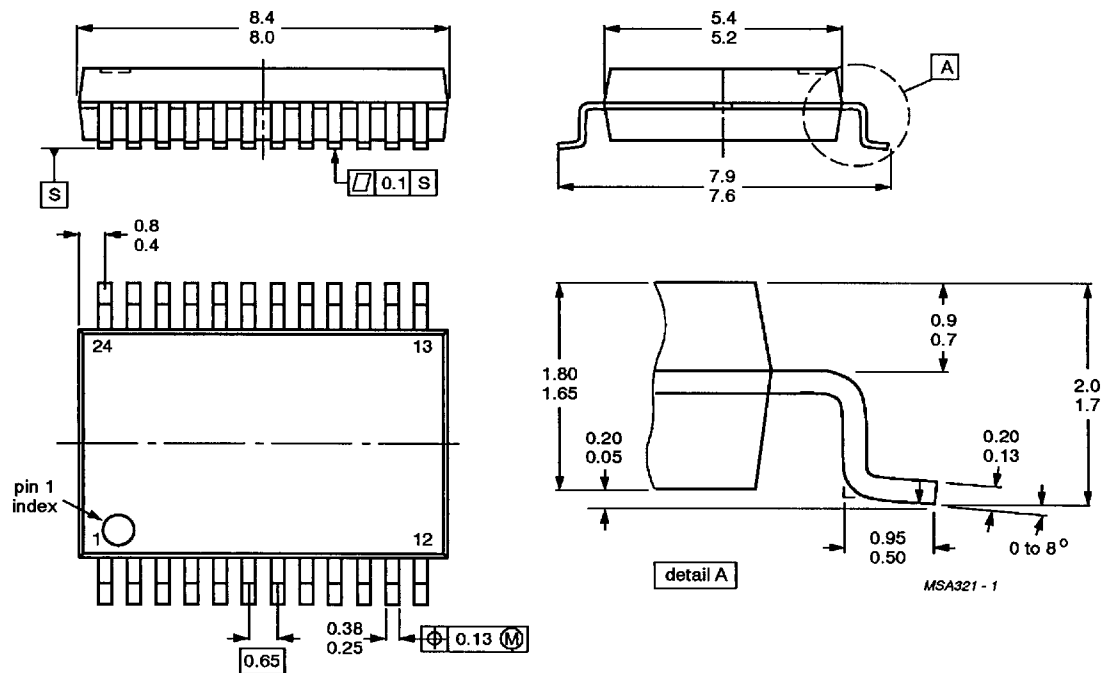


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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3mm

SOT340-1



Dimensions in mm.