115-885

HOLTEK

HT6264-70
CMOS 8K×8-Bit SRAM

Features

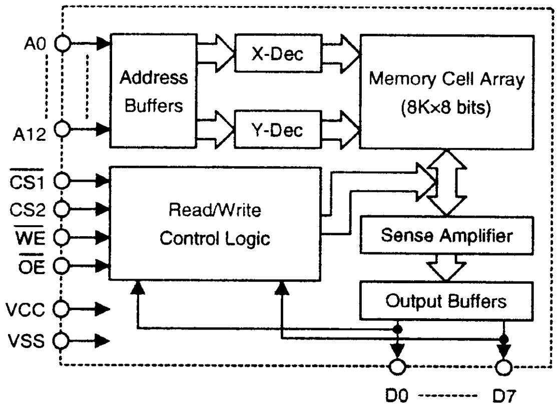
- Operating voltage: 5V
- Low power consumption
  - Operation: 200mW (typ.)
  - Standby: 5μW (typ.)
- 70ns (max.) high speed access time
- Memory expansion by pin $\overline{OE}$
- Pin-compatible with standard 8K×8 bits of EPROM/MASK ROM
- TTL compatible interface levels
- Common I/O using tristate outputs
- Fully static operation
- 28-pin DIP/SDIP/SOP package

General Description

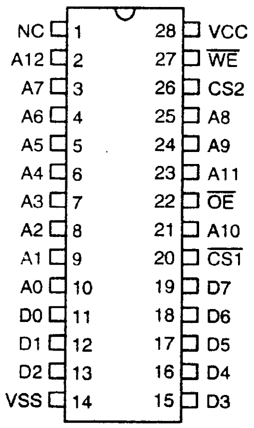
The HT6264-70 is a 65,536-bit static random access memory organized into 8192 words by 8 bits and operates from a single 5V power supply. It is built with HOLTEK's high performance CMOS 0.8μm SPDM process.

Six transistor full CMOS memory cell provides low standby current and high reliability. Inputs and tristate outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Block Diagram



Pin Assignment



HT6264-70
– 28 DIP/SDIP/SOP

Pin Description

Pin Name	I/O	Description
A0~A12	I	Address input pins
D0~D2, D3~D7	I/O	Data input and output signal pins
CS2, $\overline{\text{CS1}}$	I	Chip select signal pin
$\overline{\text{OE}}$	I	Output enable signal pin
$\overline{\text{WE}}$	I	Write enable signal pin
VCC	I	Positive power supply pin
GND	I	Negative power supply pin
NC		No connection

Absolute Maximum Ratings*

VCC to GND	–0.3V to +7.0V
IN, IN/OUT Voltage to GND, V_T	–0.3V to V_{CC}+0.5V
Operating Temperature, T_{opr}	–40°C to +85°C
Storage Temperature (Plastic), T_{stg}	–55°C to +125°C
Temperature Under Bias, T_{bias}	–10°C to +85°C
Power Dissipation, P_T	1.0W

*Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

VCC=5V±10%, GND=0V, Ta=–40°C to 85°C

Symbol	Parameter		Min.	Typ.*	Max.	Unit
V_{CC}	Operating Voltage	—	4.5	5.0	5.5	V
I_{CC1}	Operating Current	T_{CYC}=Min. Cycle, I_{OUT}=0mA	—	—	45	mA
I_{CC2}		T_{CYC}=1µs, I_{OUT}=0mA	—	—	15	mA
I_{SB1}	Standby Current	$\overline{\text{CS1}}$=V_{IH} or CS2=V_{IL}	—	—	10	mA
I_{SB2}		$\overline{\text{CS1}}$=CS2>=V_{CC}–0.2V, V_{IN}>=V_{CC}–0.2V or V_{IN}<=0.2V	—	—	50	µA
V_{OH}	Output High Voltage	I_{OH}= –1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=4mA	—	—	0.4	V

Symbol	Parameter		Min.	Typ.*	Max.	Unit
V_{IH}	Input High Voltage	—	2.2	—	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	—	-0.3	—	0.8	V
I_{LI}	Input Leakage Current	V_{CC}=5.5V, V_{IN}=GND to V_{CC}	—	—	1	μA
I_{LO}	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=GND to V_{CC}	—	—	1	μA

*V_{CC}=5V, Ta=25°C

A.C. Characteristics

Read cycle

V_{CC}=5V±10%, Ta=–40°C to 85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RC}	Read Cycle Time	70	—	—	ns
t_{AA}	Address Access Time	—	—	70	ns
t_{ACS}	Chip Selection Access Time	—	—	70	ns
t_{OE}	Output Enabled to Valid Outputs	—	—	40	ns
t_{OH}	Outputs Hold from Address Change	5	—	—	ns
t_{CLZ}	Chip select to Outputs in Low-Z	10	—	—	ns
t_{OLZ}	Output Enabled to Outputs in Low-Z	10	—	—	ns
t_{CHZ}	Chip Disabled to Outputs in High-Z	0	—	30	ns
t_{OHZ}	Output Disabled to Outputs in High-Z	0	—	30	ns

Notes: A read occurs during the overlap of a low $\overline{CS1}$, a high CS2, a low $\overline{OE}$, and a high $\overline{WE}$.

t_{CLZ} is specified from $\overline{CS1}$ or CS2 whichever occurs last.

t_{CHZ} is specified from $\overline{CS1}$ or CS2 whichever occurs first.

t_{CHZ} and t_{OHZ} are specified by the time when DATA OUT is floating

Write cycle V_{CC}=5V±10%, Ta=–40°C to 85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WC}	Write Cycle Time	70	—	—	ns
t_{CW}	Chip Select to End of Write	35	—	—	ns
t_{AW}	Address Valid to End of Write	50	—	—	ns
t_{AS}	Address Setup Time	0	—	—	ns
t_{WP}	Write Pulse Width	25	—	—	ns
t_{WR}	Write Recovery Time	0	—	—	ns
t_{DW}	Data to Write Time Overlap	20	—	—	ns
t_{DH}	Data Hold from Write Time	0	—	—	ns
t_{OW}	Outputs Active from End of Write	5	—	—	ns
t_{OHZ}	Outputs Disable to Outputs in High-Z	0	—	40	ns
t_{WHZ}	Write to Outputs in High-Z	0	—	50	ns

Notes: A write cycle occurs during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$.

$\overline{OE}$ may be both high and low in a write cycle.

t_{AS} is specified from $\overline{CS1}$, CS2, or $\overline{WE}$, whichever occurs last.

t_{WP} is an overlap time of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$.

t_{WR}, t_{DW} and t_{DH} is specified from $\overline{CS1}$, CS2, or $\overline{WE}$, whichever occurs first

t_{WHZ} is specified by the time when DATA OUT is floating, not defined by output level.

When I/O pins are data output mode, don't force inverse signals to those pins.

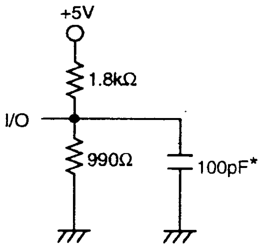
A.C. test conditions

Output load: See Figures below

Input pulse levels: 0V to 3.0V

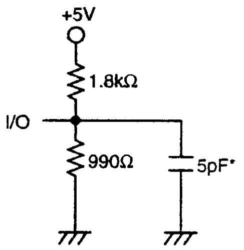
Input rise and fall time: 5ns

Input and output timing reference levels: 1.5V



*Including scope and jig

Output load



*Including scope and jig

Output load for
t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{OW}

Data retention characteristics

Ta=−40°C to 85°C

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{CS1}$=CS2≥V_{CC}−0.2V	2	5.5	V
I_{CCDR}	Data Retention Current	V_{CC}=3V, $\overline{CS1}$=CS2≥V_{CC}−0.2V V_{IN}≥V_{CC}−0.2V or V_{IN}≤0.2V	—	50	µA
t_{CDR}	Chip Disable Data Retention Time	See Retention Timing	0	—	ns
t_R	Operation Recovery Time	See Retention Timing	t_{RC}*	—	ns

*t_{RC}=Read Cycle Time

Operation Truth Table

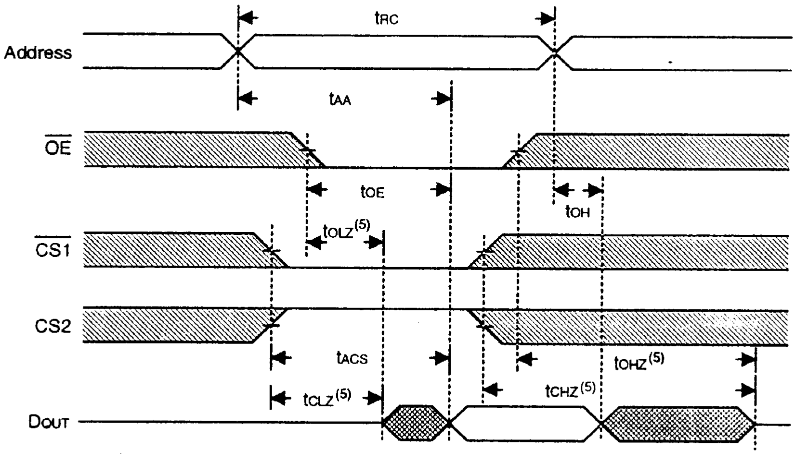
All relations between $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$ and CS2 can be described in the following truth table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	D0~D7
H	X*	X	X	Standby	High-Z
X	L	X	X		
L	H	L	H	Read	Dout
L	H	H	H	Read	High-Z
L	H	X	L	Write	Din

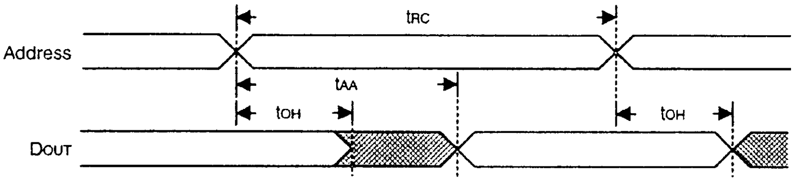
*X: Don't Care, Logical High or Low

Timing Diagrams

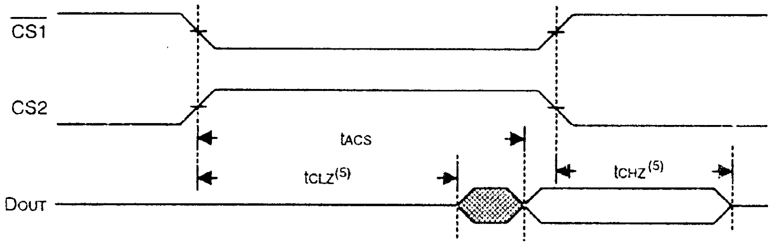
Read cycle 1$^{(1)}$



Read cycle 2[1, 2, 4]

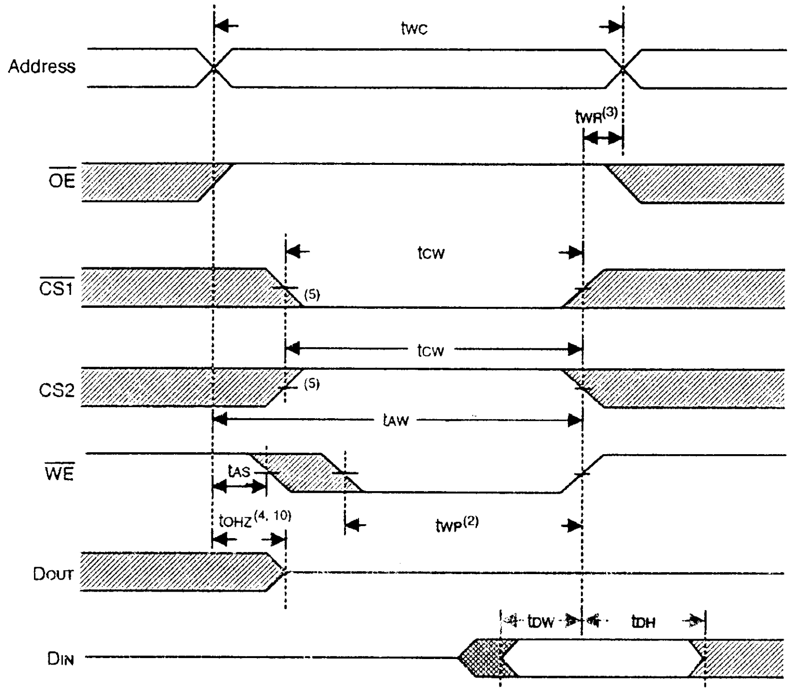


Read cycle 3[1, 3, 4]

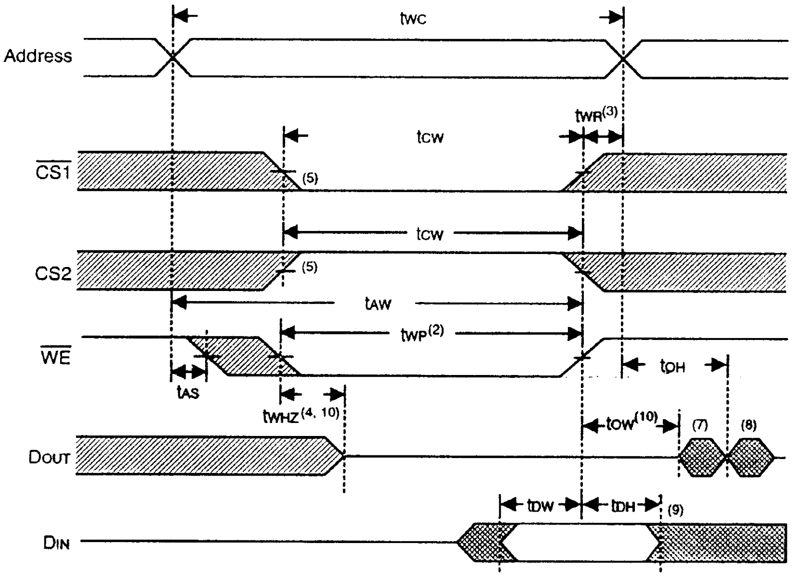


Notes:
1. $\overline{WE}$ is High for Read Cycle
2. Device is continuously enabled, $\overline{CS1}=V_{IL}$ and $CS2=V_{IH}$
3. Address valid prior to or coincident with $\overline{CS1}$ transition low and CS2 transition high
4. $\overline{OE}=V_{IL}$
5. Transition is measured ± 500mV from steady state

Write cycle 1(1)

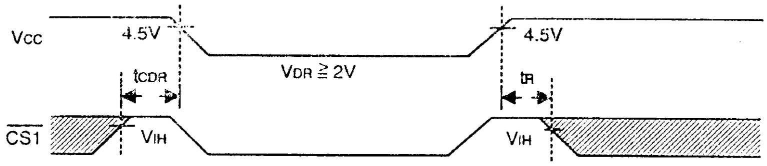


Write cycle 2(1, 6)



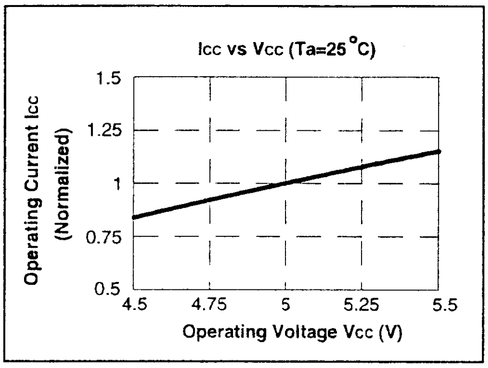
Notes:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier $\overline{CS1}$ or $\overline{WE}$ going high and CS2 going low to the end of the write cycle.
4. During this period, I/O pins are in the output state so the input signals of the opposite phase to the outputs must not be applied.
5. If the $\overline{CS1}$ low transition (or CS2 high transition) occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}=V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of the next address.
9. If $\overline{CS1}$ is low (or CS2 is high) during this period, I/O pins are in the output state. Then the data input signals of the opposite phase to the outputs must not be applied to them.
10. Transition is measured at ±500mV from steady state

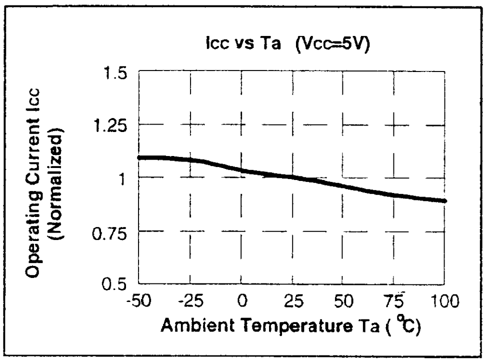
Low V_{CC} data retention timing

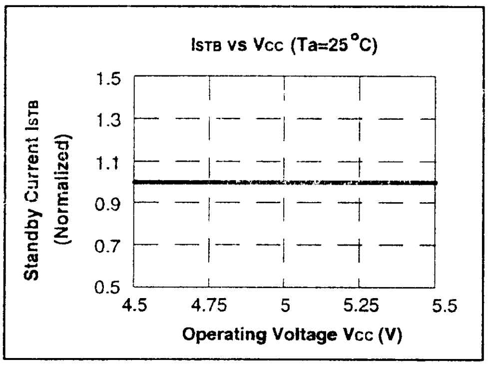


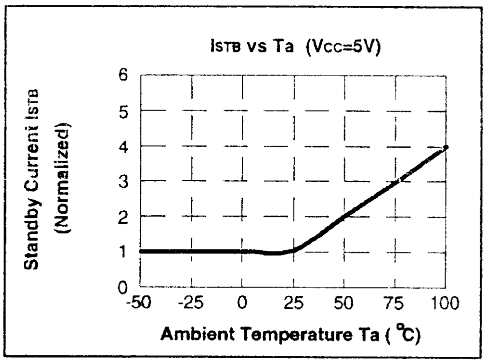
$\overline{CS1} \geq V_{DR}$-0.2V, CS2=$V_{IH}$

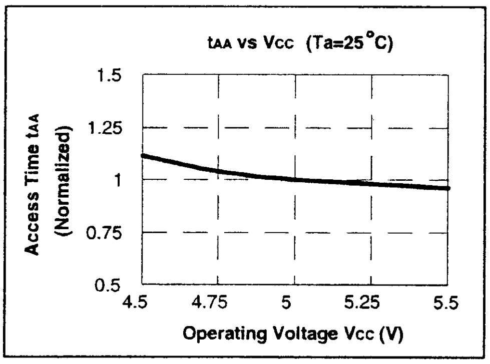
Characteristic Curves

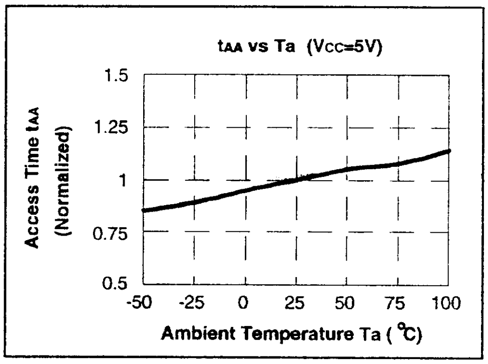


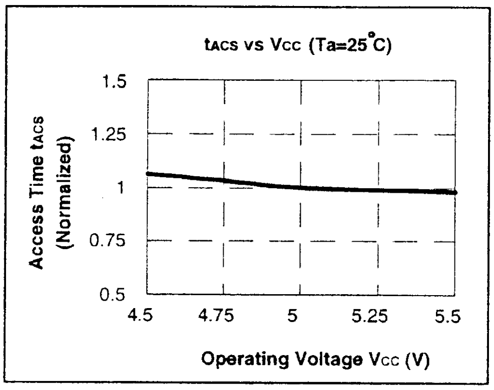


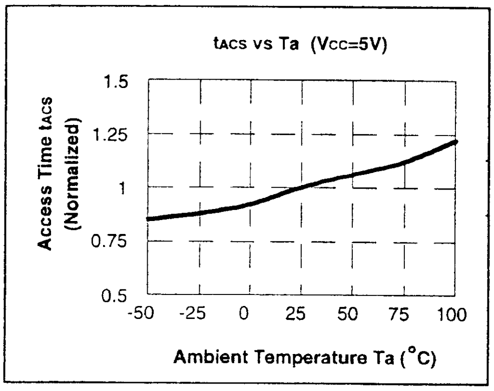


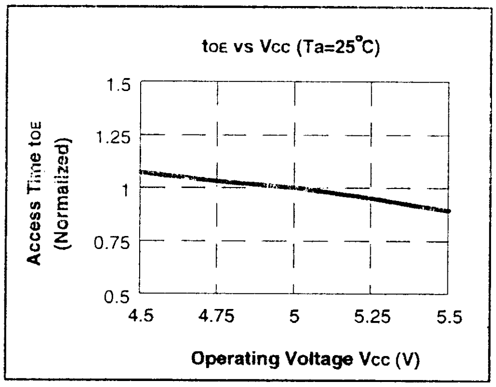


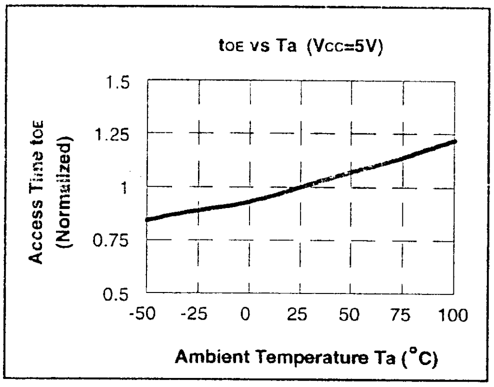





tACS vs VCC (Ta=25°C)
Access Time tACS (Normalized)
1.5
1.25
1
0.75
0.5
4.5
4.75
5
5.25
5.5
Operating Voltage VCC (V)


tACS vs Ta (VCC=5V)
Access Time tACS (Normalized)
1.5
1.25
1
0.75
0.5
-50
-25
0
25
50
75
100
Ambient Temperature Ta (°C)


tOE vs VCC (Ta=25°C)
Access Time tOE (Normalized)
1.5
1.25
1
0.75
0.5
4.5
4.75
5
5.25
5.5
Operating Voltage VCC (V)


tOE vs Ta (VCC=5V)
Access Time tOE (Normalized)
1.5
1.25
1
0.75
0.5
-50
-25
0
25
50
75
100
Ambient Temperature Ta (°C)