HARRIS SEMICONDUCTOR

# HM-6514

T-46-23-08

February 1992

## 1024 x 4 CMOS RAM

### Features

- Low Power Standby.....125µW Max.
- Low Power Operation .....35mW/MHz Max.
- Data Retention ..... @2.0V Min.
- TTL Compatible Input/Output
- Common Data Input/Output
- Three-State Output
- Standard JEDEC Pinout
- Fast Access Time.....120/200ns Max.
- 18 Pin Package for High Density
- On-Chip Address Register
- Gated Inputs - No Pull Up or Pull Down Resistors Required

### Description

The HM-6514 is a 1024 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

Gated inputs allow lower operating current and also eliminate the need for pull up or pull down resistors. The HM-6514 is a fully static RAM and may be maintained in any state for an indefinite period of time.

Data retention supply voltage and supply current are guaranteed over temperature.

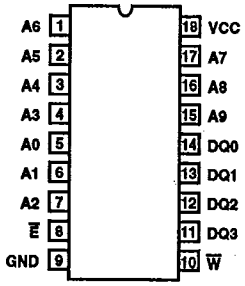
### Ordering Information

| PACKAGE | TEMPERATURE RANGE | 120ns | 200ns | 300ns |
|---|---|---|---|---|
| Plastic DIP | -40°C to +85°C | HM3-6514S-9 | HM3-6514B-9 | HM3-6514-9 |
| Ceramic DIP | -40°C to +85°C | HM1-6514S-9 | HM1-6514B-9 | HM1-6514-9 |
| */883 | -55°C to +125°C | HM1-6514S/883 | HM1-6514B/883 | HM1-6514/883 |
| JAN# | | 24502BVA | - | - |
| SMD# | | 8102402VA | 8102404VA | 8102406VA |
| LCC | -40°C to +85°C | - | HM4-6514B-9 | HM4-6514-9 |
| | -55°C to +125°C | - | HM4-6514B-8 | HM4-6514-8 |

* Respective /883 specifications are included at the end of this data sheet.

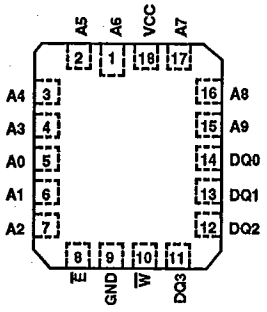
### Pinouts

18 LEAD DIP
TOP VIEW




| PIN | DESCRIPTION |
|---|---|
| A | Address Input |
| $\overline{E}$ | Chip Enable |
| $\overline{W}$ | Write Enable |
| D | Data Input |
| Q | Data Output |

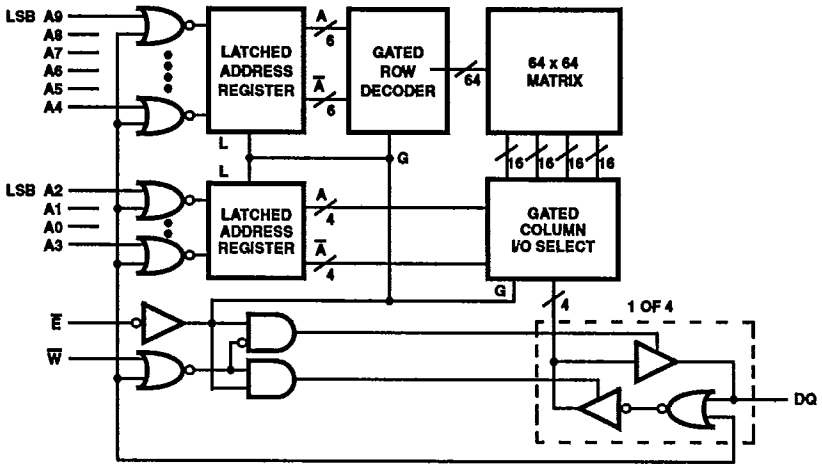
18 LEAD LCC
TOP VIEW






File Number 2995

## Functional Diagram



## Specifications HM-6514

T-46-23-08

### Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
ESD Classification ..... Class 1

### Reliability Information

| Thermal Resistance | $\theta_{ja}$ | $\theta_{jc}$ |
|---|---|---|
| Ceramic DIP Package | 66°C/W | 12°C/W |

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.75W
Gate Count ..... 6910 Gates

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V

Operating Temperature Ranges:
HM-6514S-9, HM-6514B-9, HM-6514-9 ..... -40°C to +85°C
HM-6514B-8, HM-6514-8 ..... -55°C to +125°C

### DC Electrical Specifications

VCC = 5V ± 10%; $T_A$ = -40°C to +85°C (HM-6514S-9, HM-6514B-9, HM-6514-9)
$T_A$ = -55°C to +125°C (HM-6514B-8, HM-6514-8)

| SYMBOL | PARAMETER | | LIMITS MIN | LIMITS MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| ICCSB | Standby Supply Current | HM-6514-9 | - | 25 | µA | IO = 0mA, $\overline{E}$ = VCC-0.3V, VCC = 5.5V |
| | | HM-6514-8 | - | 50 | µA | |
| ICCOP | Operating Supply Current (Note 1) | | - | 7 | mA | $\overline{E}$ = 1MHz, IO = 0mA, VI = GND, VCC = 5.5V, |
| ICCDR | Data Retention Supply Current | HM-6514-9 | - | 15 | µA | IO = 0mA, VCC = 2.0V, $\overline{E}$ = VCC |
| | | HM-6514-8 | - | 25 | µA | |
| VCCDR | Data Retention Supply Voltage | | 2.0 | - | V | |
| II | Input Leakage Current | | -1.0 | +1.0 | µA | VI = VCC or GND, VCC = 5.5V |
| IIOZ | Input/Output Leakage Current | | -1.0 | +1.0 | µA | VIO = VCC or GND, VCC = 5.5V |
| VIL | Input Low Voltage | | -0.3 | 0.8 | V | VCC = 4.5V |
| VIH | Input High Voltage | | VCC-2.0 | VCC+0.3 | V | VCC = 5.5V |
| VOL | Output Low Voltage | | - | 0.4 | V | IO = 2.0mA, VCC = 4.5V |
| VOH1 | Output High Voltage | | 2.4 | - | V | IO = -1.0mA, VCC = 4.5V |
| VOH2 | Output High Voltage (Note 2) | | VCC-0.4 | - | V | IO = -100µA, VCC = 4.5V |

### Capacitance

$T_A$ = +25°C

| SYMBOL | PARAMETER | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|
| CI | Input Capacitance (Note 2) | 8 | pF | f = 1MHz, All measurements are referenced to device GND |
| CIO | Input/Output Capacitance (Note 2) | 10 | pF | |

NOTES:

1. Typical derating 5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

**AC Electrical Specifications** VCC = 5V ± 10%; $T_A$ = -40°C to +85°C (HM-6514S-9, HM-6514B-9, HM-6514-9)
$T_A$ = -55°C to +125°C (HM-6514B-8, HM-6514-8)

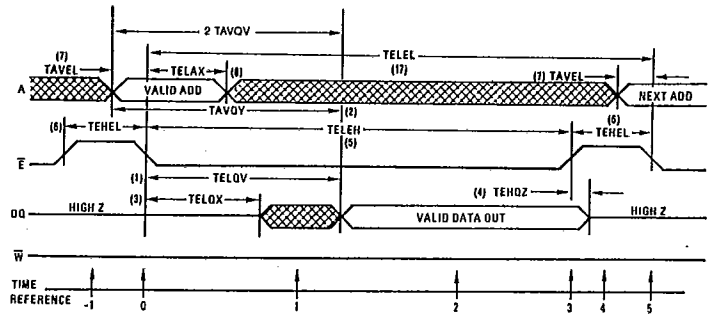
| SYMBOL | PARAMETER | LIMITS | | | | | | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | HM-6514S-9 | | HM-6514B-9 | | HM-6514-9 | | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| (1) TELQV | Chip Enable Access Time | - | 120 | - | 220 | - | 300 | ns | (Notes 1, 3) |
| (2) TAVQV | Address Access Time | - | 120 | - | 220 | - | 320 | ns | (Notes 1, 3, 4) |
| (3) TELQX | Chip Enable Output Enable Time | 5 | - | 5 | - | 5 | - | ns | (Notes 2, 3) |
| (4) TEHQZ | Chip Enable Output Disable Time | - | 50 | - | 80 | - | 100 | ns | (Notes 2, 3) |
| (5) TELEH | Chip Enable Pulse Negative Width | 120 | - | 200 | - | 300 | - | ns | (Notes 1, 3) |
| (6) TEHEL | Chip Enable Pulse Positive Width | 50 | - | 90 | - | 120 | - | ns | (Notes 1, 3) |
| (7) TAVEL | Address Setup Time | 0 | - | 20 | - | 20 | - | ns | (Notes 1, 3) |
| (8) TELAX | Address Hold Time | 40 | - | 50 | - | 50 | - | ns | (Notes 1, 3) |
| (9) TWLWH | Write Enable Pulse Width | 120 | - | 200 | - | 300 | - | ns | (Notes 1, 3) |
| (10) TWLEH | Chip Enable Write Pulse Setup Time | 120 | - | 200 | - | 300 | - | ns | (Notes 1, 3) |
| (11) TELWH | Chip Enable Write Pulse Hold Time | 120 | - | 200 | - | 300 | - | ns | (Notes 1, 3) |
| (12) TDVWH | Data Setup Time | 50 | - | 120 | - | 200 | - | ns | (Notes 1, 3) |
| (13) TWHDX | Data Hold Time | 0 | - | 0 | - | 0 | - | ns | (Notes 1, 3) |
| (14) TWLDV | Write Data Delay Time | 70 | - | 80 | - | 100 | - | ns | (Notes 1, 3) |
| (15) TWLEL | Early Output High-Z Time | 0 | - | 0 | - | 0 | - | ns | (Notes 1, 3) |
| (16) TEHWH | Late Output High-Z Time | 0 | - | 0 | - | 0 | - | ns | (Notes 1, 3) |
| (17) TELEL | Read or Write Cycle Time | 170 | - | 290 | - | 420 | - | | (Notes 1, 3) |

NOTES:

1. Input pulse levels: 0.8V to VCC - 2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. VCC = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

## Timing Waveforms

**READ CYCLE**

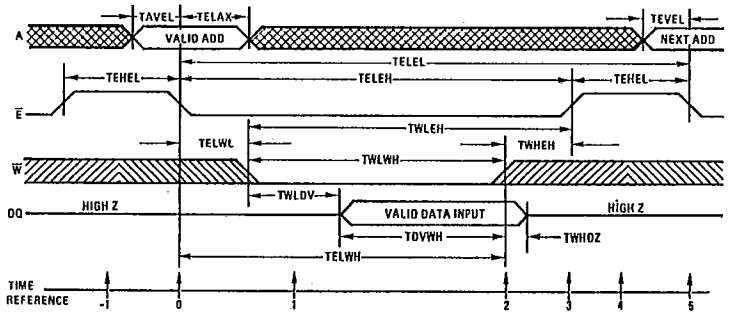



**TRUTH TABLE**

| TIME REFERENCE | INPUTS $\overline{E}$ | INPUTS $\overline{W}$ | INPUTS A | DATA I/O DQ | FUNCTION |
|---|---|---|---|---|---|
| -1 | H | X | X | Z | Memory Disabled |
| 0 | ↘ | H | V | Z | Cycle Begins, Addresses are Latched |
| 1 | L | H | X | X | Output Enabled |
| 2 | L | H | X | V | Output Valid |
| 3 | ↗ | H | X | V | Read Accomplished |
| 4 | H | X | X | Z | Prepare for Next Cycle (Same as -1) |
| 5 | ↘ | H | V | Z | Cycle Ends, Next Cycle Begins (Same as 0) |

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all inputs and ready the RAM for the next memory cycle (T = 4).

**WRITE CYCLE**




**TRUTH TABLE**

| TIME REFERENCE | INPUTS $\overline{E}$ | INPUTS $\overline{W}$ | INPUTS A | DQ | FUNCTION |
|---|---|---|---|---|---|
| -1 | H | X | X | Z | Memory Disabled |
| 0 | ↘ | X | V | Z | Cycle Begins, Addresses are Latched |
| 1 | L | L | X | Z | Write Period Begins |
| 2 | L | ↗ | X | V | Data In is Written |
| 3 | ↗ | H | X | Z | Write Completed |
| 4 | H | X | X | Z | Prepare for Next Cycle (Same as -1) |
| 5 | ↘ | X | V | Z | Cycle Ends, Next Cycle Begins (Same as 0) |

## Timing Waveforms (Continued)

**WRITE CYCLE** (Continued)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on-chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before $\overline{E}$. The RAM outputs and all inputs will three-state after $\overline{E}$ rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rising

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met, but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDX become TDVEH and TEHDX. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

| | IF | OBSERVE | IGNORE |
|---|---|---|---|
| Case 1 | $\overline{E}$ falls before $\overline{W}$ | TWLDV | TWLEL |
| Case 2 | $\overline{E}$ falls after $\overline{W}$ and $\overline{E}$ rises before $\overline{W}$ | TWLEL<br>TEHWH | TWLDV<br>TWHDX |

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

## Test Load Circuit