# PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Fast access time (10 ns) improves system cycle speeds.
   Fully compatible with standard voltage-compensated
- Fully compatible with standard voltage-compensated 10K series ECL — no board changes required.
- Enhanced output voltage level compensation providing 6X improvement in V<sub>OL</sub> and V<sub>OH</sub> stability over supply and temperature ranges.
- Internally voltage-compensated providing flat AC performance
- Emitter follower outputs easy wire-ORing
- Power dissipation decreases with increasing temperature.

## **GENERAL DESCRIPTION**

The Am10474-10, Am10474-15 and Am10474-25 are fully decoded 4096-bit ECL RAMs, organized 1024 words by 4 bits. Word selection is achieved by means of a 10-bit address, A<sub>0</sub> through A<sub>9</sub>. Easy memory expansion is provided by an active LOW chip select (CS) input and an unterminated OR-tieable emitter follower output.

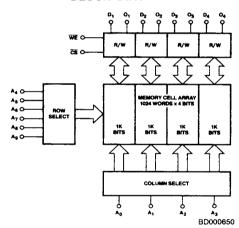
An active LOW write enable (WE) controls the write/read operation of the memory. When the chip select and write

enable lines are LOW, the data inputs ( $D_1 - D_4$ ) are written into the addressed memory word.

Reading is performed with the chip select line LOW and the write enable line HIGH. The information stored in the addressed word is read out on the noninverting outputs,  $O_1 - O_{\Delta}$ .

During the writing operation, or when the chip select line is HIGH, the output of the memory goes to a LOW state.

# **BLOCK DIAGRAM**



## MODE SELECT TABLE

	Inpu	t	Output					
CS	CS WE DIN		DOUT	Mode				
Н	х	Х	L	Not Selected				
L	L	L	L	Write ''0''				
L	L	Н	L	Write ''1''				
L	Н	X	DOUT	Read				

H = HIGH L = LOW X = Don't Care

## PRODUCT SELECTOR GUIDE

## Highlights of Key Performance Parameters (Commercial)

Part Number	Am10474-10	Am10474-15	Am10474-25
Address Access Time (t <sub>AA</sub> )	10 ns	15 ns	25 ns
Write Pulse Width (tw)	12 ns	15 ns	25 ns
Write Recovery (twn)	14 ns	17 ns	27 ns
Chip Select Access/ Recovery and Write Disable Times (t <sub>ACS</sub> , t <sub>RCS</sub> , t <sub>WS</sub> )	8 ns	8 ns	10 ns
Power Supply (IEE)	230 mA	200 mA	200 mA

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Publication # Rev. Amendment 03231 D /0

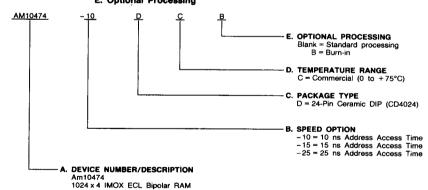
#### CONNECTION DIAGRAM LOGIC SYMBOL **Top View** VCCA [ □ vcc ص (ت \_\_\_\_ O2 23 D<sub>2</sub> D3 O4 [ 7 9 A, **□** 0₄ A<sub>2</sub> 70 A<sub>3</sub> \_ ₽2 1024 x 4 ECL RAM A<sub>5</sub> ره 🖂 11 ۸s ा टड 17 13 A7 WE 14 A8 15 15 A۵ 03 \_\_\_ As 12 CD000931 LS000251 V<sub>CCA</sub> = Pin 1 V<sub>CC</sub> = Pin 24 V<sub>EE</sub> = Pin 12 NC = Pin 10

## ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number** 

- B. Speed Option (if applicable)
- C. Package Type
- D. Temperature Range E. Optional Processing



Valid Combinations							
AM10474-10							
AM10474-15	DC, DCB						
AM10474-25							

Note: Pin 1 is marked for orientation.

### **Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature65 to +150°C
Case Temperature with
Power Applied55 to +125°C
VEE Pin Potential to GND Pin7.0 V to +0.5 V
Input Voltage (DC)VEE to +0.5 V
Output Current (DC Output HIGH)30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

# **OPERATING RANGES**

Commercial (C) Devices (Note 2)		
Temperature	0 t	o +75°C
Supply Voltage5.46	V to	-4.94 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

# DC CHARACTERISTICS (Commercial) V<sub>EE</sub> = -5.2 V, V<sub>CC</sub> = GND (Note 2)

Parameter Symbol	Parameter Description	Test Conditions (Note 2)		2)	<b>B</b> (Note 3)	Typ. (Note 1)	A (Note 3)	Units
	Output Voltage HIGH			T = 0°C	-1000		-840	
Vон				T = +25°C	-960		-810	mV
		VIN - VIHA OF VILB		T = +75°C	-900		-720	
VOL				T = 0°C	-1870		-1665	
	Output Voltage LOW			T = +25°C	-1850		-1650	mV
	, ,		Loading is	T = + 75°C	- 1830		-1625	
Vонс	Output Voltage HIGH		50 Ω to -2.0 V	T = 0°C	-1020			
				T = + 25°C	-980			mV
		VIN = VIHB OF VILA		T - + 75°C	-920	at L		
	Output Voltage LOW	] "" ""	an armay	T = 0°C	jose		-1645	
V <sub>OLC</sub>				T = + 25°C			-1630	mV
		34 5	THE ROYALK	T = +75°C			-1605	
	Input Voltage HIGH		T = 0°C	-1145		-840	m∨	
VIH		Guaranteed Input Volt for All Inputs (Note 4	T = +25°C	-1105		-810		
		TOT AIR IMPORTS (NOTO T	T = +75°C	-1045		-720		
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	14.4 (189)		T = 0°C	- 1870		- 1490	
V <sub>iL</sub>	Input Voltage LOW	Guaranteed Input Volt for All Inputs (Note 4	T = +25°C	-1850		-1475	m∨	
~		TO All Impais (Note 4	T = +75°C	-1830		-1450	1	
lн	Input Current HIGH	VIN = VIHA	T = 0 to +75°C			220	μΑ	
	Input Current LOW Chip Select (CS)	V <sub>IN</sub> = V <sub>ILB</sub>		T = 0 to +75°C	0.5		170	μA
I <sub>IL</sub>	All Other Inputs	1	1 - 0 10 + /5 C	-50			μΛ	
	Power Supply	All Inputs and	All Inputs and Am10474-10					mA
IEE	Current (Pin 12)	Outputs Open	T=0 to +75°C	-200			ША	

Notes: 1. Typical values are:

- typical values are:
   VEC = VCC = VCC = GND, TA = 25°C
   Output Load = 50 Ω and 30 pF to -2.0 V, T = TA = 0 to +75°C for DIPs. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Approximate thermal resistance values of the package are:
  - $\theta_{\rm JA}$  (Junction-to-Ambient) = 90°C/Watt (still air)  $\theta_{\rm JA}$  (Junction-to-Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
  - T = T<sub>C</sub> = 0 to +75°C for Flatpak and LCC packages
  - $\theta_{\text{JC}}$  (Junction-to-Case) = 25°C/Watt
- 3. Definition of symbols and terms used in this product specification. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
- 4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- 5. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed  $\dot{\theta} = 25^{\circ}\text{C/w}$  (approximately)

No.			Test Conditions	Am10474-10			Am10474-15			Am10474-25			
	Parameter Symbol			Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	Unite
REAL	MODE				<u> </u>								
1	tacs	Chip Select				8	ļ		8			10	ns
	1	Access Time Chip Select Recovery	Measured at 50% of input to	$\vdash$			<del>                                     </del>	-	-				
2	tRCS	Time	50% of output			8			8			10	ns
3	TAA MODE	Address Access Time	l			10	<u> </u>		15			25	ns
	E MODE	Write Pulse Width		г	r	T			1		T	T	T
4	tw	(to Guarantee Writing)	twsa = twsa (Min.)	12		<u> </u>	15			25			ns
5	twsp	Data Setup Time Prior to Write		2			2		Rate in the state of	2			ns
6	twho	Data Hold Time After Write		2			2			2			ns
	· · · · · · · · · · · · · · · · · · ·	Address Setup Time	A	<del>  </del>		<del> </del>	t .		L committee			$\vdash$	
7	twsa	Prior to Write	tw = tw (Min.)	2	E4034	L.,	·:. 2		18	- 2		<b> </b>	ns
8	twha .	Address Hold Time After Write	1,34	2	- F. G		2			2			ns
9	twee	Chip Select Setup Time		2		100	2			2			ns
	twscs	Prior to Write	Measured at			ļ	<u> </u>			<u> </u>			
10	twics .	Chip Select Hold Time After Write	50% of input to 50% of output	2			2			2			ns
11	tws	Write Disable Time				8			8			10	ns
12	twn	Write Recovery Time				14			17			27	ns
RISE	TIME AND	FALL TIME				,							
13	t <sub>r</sub>	Output Rise Time	Measured between 20%		2.5			2.5			2.5		١ "
14	tr	Output Fall Time	and 80% points		2.5			2.5			2.5		ns
CAP	ACITANCE												
15	CIN	Input Pin Capacitance	Measured with a		4			4			4		
16	Соит	Output Pin Capacitance	pulse technique on sample basis		7			7			7		pF
ADD	RESS	ADDRESS J	WITCHING \			#S (C	Jone (		DDRESS				50%
	cs —								/				50%
DATA	. OUT		-3-			-			-	<u> </u>	<b>\</b>		50%
	CHIP DESELEC	READ A HIGH TED IN ADDRESS J	READ A IN ADDR	LOW ESS K				O A HIGH ORESS L		DES	CHIP ELECTED		
												***	F0011
			Rea	d Mo	de							•••	<b>F001</b> 1

