Am100474

1024 x 4 IMOX™ ECL Bipolar RAM

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Fast access time (10 ns) — improves system cycle speeds.
- Fully compatible with 100K series ECL logic — no board changes required.
- Enhanced output voltage level compensation providing 6X (improvement in) V_{OL} and V_{OH} stability over supply and temperature ranges.
- Internally voltage-compensated providing flat AC performance.
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature.

GENERAL DESCRIPTION

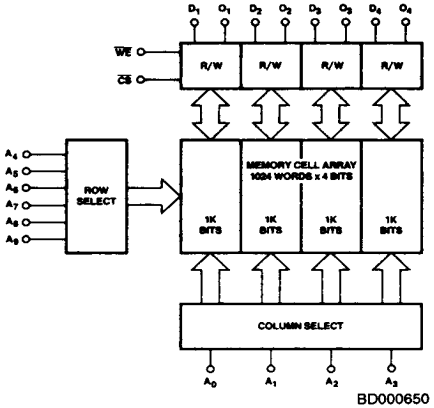
The Am100474-10, Am100474-15 and Am100474-25 are fully decoded 4096-bit ECL RAMs, organized 1024 words by 4 bits. Word selection is achieved by means of a 10-bit address, A_0 through A_9. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and unterminated OR-tieable emitter follower outputs.

An active LOW write enable ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write enable lines are LOW, the data inputs ($D_1 - D_4$) are written into the addressed memory word.

Reading is performed with the chip select line LOW and the write enable line HIGH. The information stored in the addressed word is read out on the noninverting outputs, $O_1 - O_4$.

During the writing operation, or when the chip select line is HIGH, the output of the memory goes to a LOW state.

BLOCK DIAGRAM



BD000650

MODE SELECT TABLE

Input			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH
L = LOW
X = Don't Care

PRODUCT SELECTOR GUIDE

Highlights of Key Performance Parameters (Commercial)

Part Number	Am100474-10	Am100474-15	Am100474-25
Address Access Time (t_{AA})	10 ns	15 ns	25 ns
Write Pulse Width (t_W)	12 ns	15 ns	25 ns
Write Recovery (t_{WR})	14 ns	17 ns	27 ns
Chip Select Access/ Recovery and Write Disable Times (t_{ACS}, t_{RCS}, t_{WS})	8 ns	8 ns	10 ns
Power Supply (I_{EE})	230 mA	200 mA	200 mA

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Issue Date: May 1986

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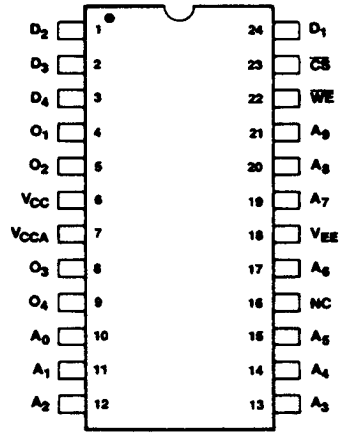
CONNECTION DIAGRAMS
Top View

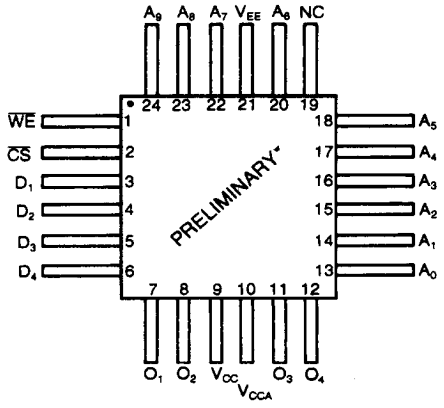
DIP



CD000940

Note: Pin 1 is marked for orientation.

Flatpak



CD006022

*Preliminary. Subject to Change.

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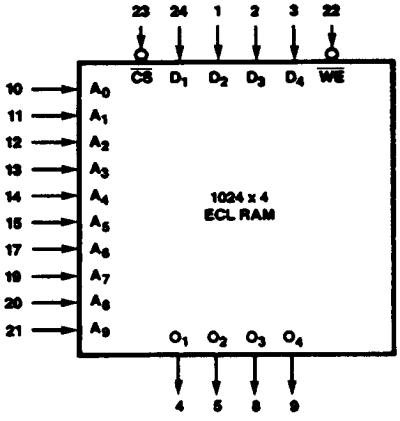
LOGIC SYMBOL*



LS000262

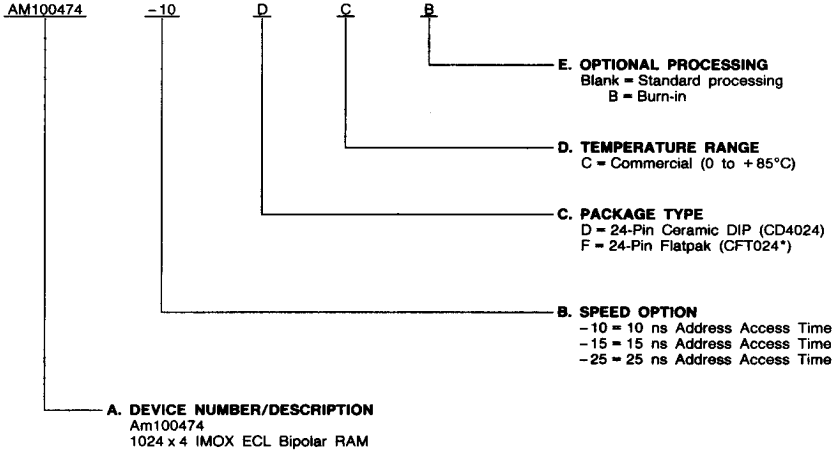
V_{CC} = Pin 6
V_{CCA} = Pin 7
V_{EE} = Pin 18
NC = Pin 16

*Pin numbers apply to DIP.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



*Preliminary. Subject to Change.

Valid Combinations	
AM100474-10	DC, DCB FC, FCB
AM100474-15	
AM100474-25	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Case Temperature with
Power Applied ..... −55 to +125°C
V_{EE} Pin Potential to
GND Pin ..... −7.0 V to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
Output Current (DC Output HIGH) .... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices (Note 2)
Temperature ..... 0 to +85°C
Supply Voltage ..... −5.7 V to −4.2 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS (V_{EE} = −4.5 V, V_{CC} = GND (Note 2))

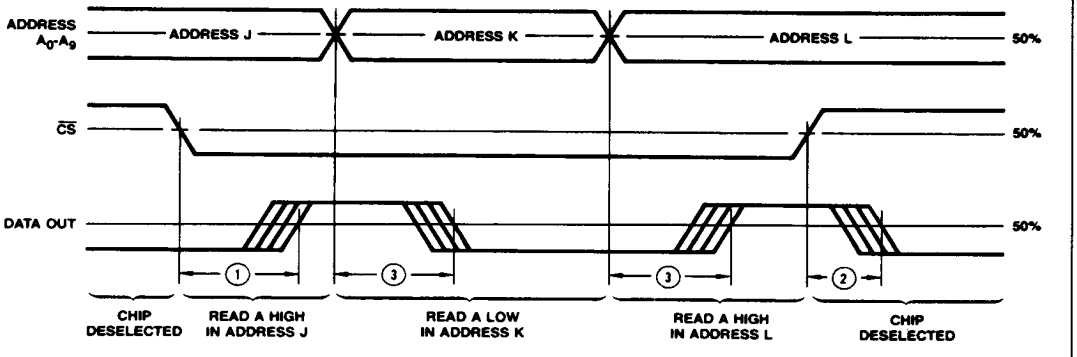
Parameter Symbol	Parameter Description	Test Conditions (Note 2)		B (Note 3)	Typ. (Note 1)	A (Note 3)	Units
V_{OH}	Output Voltage HIGH	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50 Ω to −2.0 V	−1025		−880	mV
V_{OL}	Output Voltage LOW			−1810		−1620	mV
V_{OHC}	Output Voltage HIGH	V_{IN} = V_{IHB} or V_{ILA}		−1035			mV
V_{OLC}	Output Voltage LOW					−1610	mV
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs (Note 4)		−1165		−880	mV
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 4)		−1810		−1475	mV
I_{IH}	Input Current HIGH	V_{IN} = V_{IHA}				220	µA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$)	V_{IN} = V_{ILB}		0.5		170	µA
	All Other Inputs			−50			
I_{EE}	Power Supply Current (Pin 18)	All Inputs and Outputs Open	Am100474-10	−230			mA
			Am100474-15/-25	−200			

Notes: 1. Typical values are:
V_{EE} = −4.5 V, V_{CC} = V_{CCA} = GND, T_A = 25°C
2. Output Load = 50 Ω and 30 pF to −2.0 V, T = T_A = 0 to +85°C for DIPs. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Approximate resistance values of the package are:
θ_{JA} (Junction-to-Ambient) = 90°C/Watt (still air)
θ_{JA} (Junction-to-Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
T = T_C = 0 to +85°C for Flatpak and LCC packages
θ_{JC} (Junction-to-Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

SWITCHING CHARACTERISTICS V_{EE} = −4.8 to −4.2 V, V_{CC} = GND (Note 2)

No.	Parameter Symbol	Parameter Description	Test Conditions	Am100474-10			Am100474-15			Am100474-25			Units
				Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	
READ MODE													
1	t_{ACS}	Chip Select Access Time	Measured at 50% of input to 50% of output			8			8			10	ns
2	t_{RCS}	Chip Select Recovery Time				8			8			10	ns
3	t_{AA}	Address Access Time				10			15			25	ns
WRITE MODE													
4	t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$ (Min.)	12			15			25			ns
5	t_{WSD}	Data Setup Time Prior to Write		2			2			2			ns
6	t_{WHD}	Data Hold Time After Write		2			2			2			ns
7	t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$ (Min.)	2			2			2			ns
8	t_{WHA}	Address Hold Time After Write		2			2			2			ns
9	t_{WSCS}	Chip Select Setup Time Prior to Write	Measured at 50% of input to 50% of output	2			2			2			ns
10	t_{WHCS}	Chip Select Hold Time After Write		2			2			2			ns
11	t_{WS}	Write Disable Time				8			8			10	ns
12	t_{WR}	Write Recovery Time				14			17			27	ns
RISE TIME AND FALL TIME													
13	t_r	Output Rise Time	Measured between 20% and 80% points		2.5			2.5			2.5		ns
14	t_f	Output Fall Time			2.5			2.5			2.5		
CAPACITANCE													
15	C_{IN}	Input Pin Capacitance	Measured with a pulse technique on sample basis		4			4			4		pF
16	C_{OUT}	Output Pin Capacitance			7			7			7		

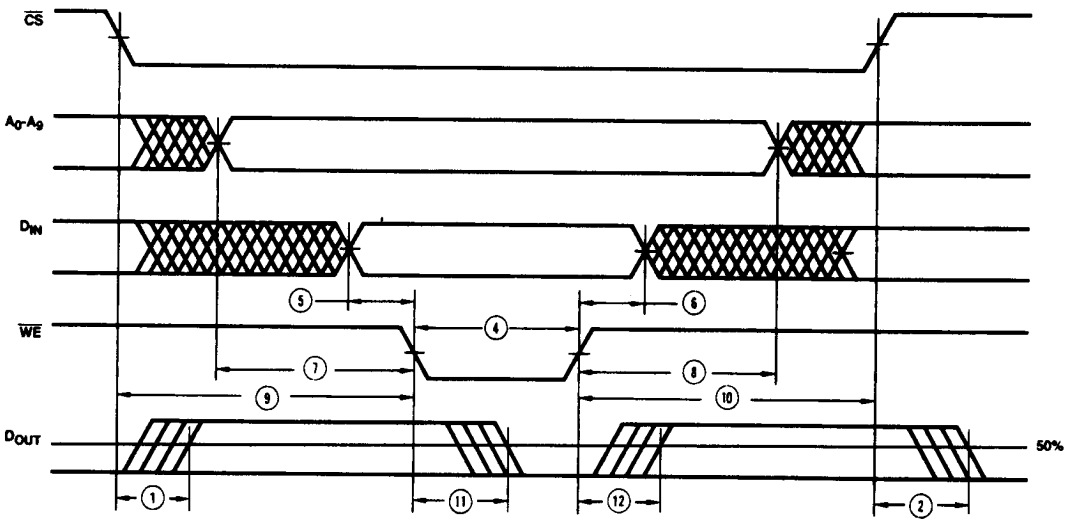
SWITCHING WAVEFORMS (Cont'd.)



WF001173

Read Mode

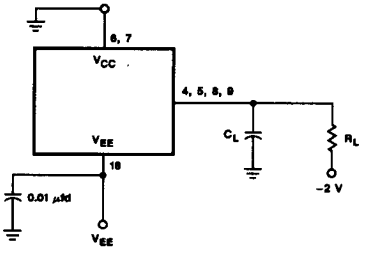
SWITCHING WAVEFORMS



WF001163

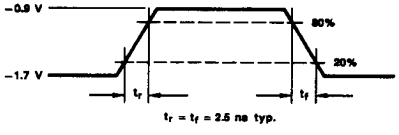
Write Mode

SWITCHING TEST CIRCUIT



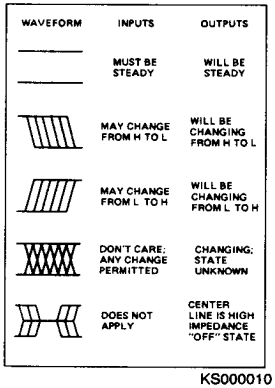
TC000225

SWITCHING TEST WAVEFORM



TW000310

KEY TO SWITCHING WAVEFORMS



KS000010

R_L = 50 Ω termination of measurement system
C_L = 30 pF (including stray jig capacitance)