NEC

MOS INTEGRATED CIRCUIT

μPD4502161

2M-bit Synchronous DRAM

Description

The μPD4502161 is a high-speed 2,097,152-bit synchronous dynamic random-access memory, organized as 65,536 × 16 × 2 (word × bit × bank), respectively.

The synchronous DRAM achieves high-speed data transfer using the pipeline architecture.

All inputs and outputs are synchronized with the positive edge of the clock.

The synchronous DRAM is compatible with Low Voltage TTL (LVTTL).

The synchronous DRAM is packaged in 50-pin TSOP (II).

Features

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Dual internal banks controlled by A9 (Bank Select)
- Programmable burst-length (1, 2, 4, 8, Full Page)
- Programmable wrap sequence (Sequential/Interleave)
- Programmable $\overline{CAS}$ latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- ×16 organization
- Single + 3.3 ±0.3 V power supply
- LVTTL compatible
- Byte control by LDQM and UDQM
- 512 refresh cycles/8 ms
- Burst termination by Burst Stop command and Precharge command

Ordering Information

Part number	Organization (word × bit × bank)	Clock frequency MHz (MAX.)	Package
μPD4502161G5-A10-7JF	64 K × 16 × 2	100	50-pin Plastic TSOP(II) (400 mil)
μPD4502161G5-A12-7JF		83	

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

Part Number

[×16]

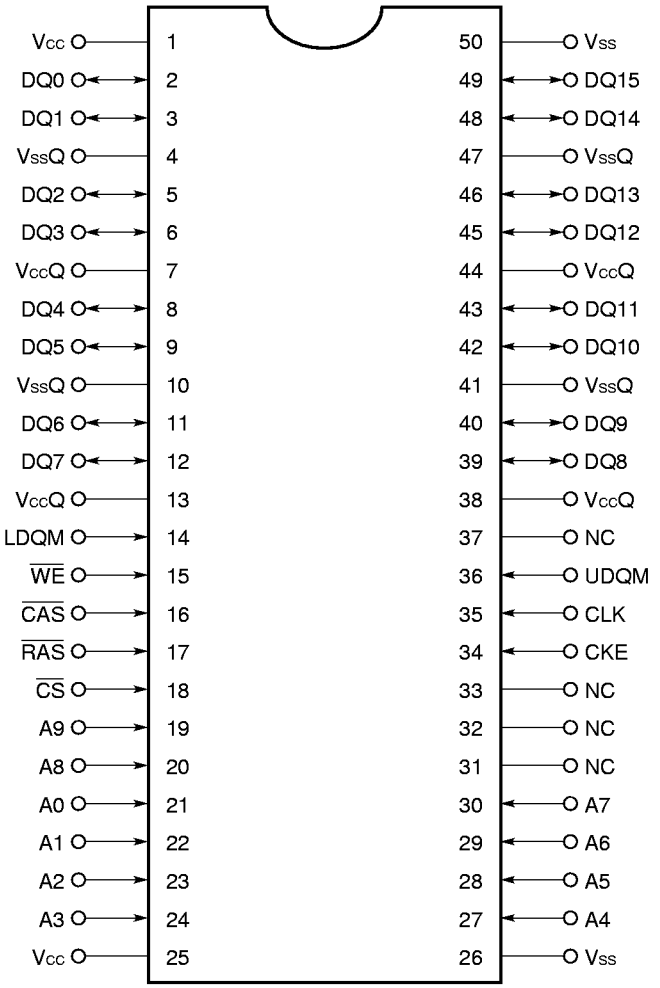
μPD4502161G5-A10

- NEC Memory
- Synchronous DRAM
- Memory Density
  02: 2M bits
- Organization
  16: ×16
- Number of banks & Interface
  1: 2 banks, LVTTL
- Package
  G5: TSOP (II)
- Low Voltage
  A: 3.3 V ± 0.3 V
- Minimum Cycle time
  10: 10 ns (100 MHz)
  12: 12 ns (83 MHz)

Pin Configuration

[μPD4502161]

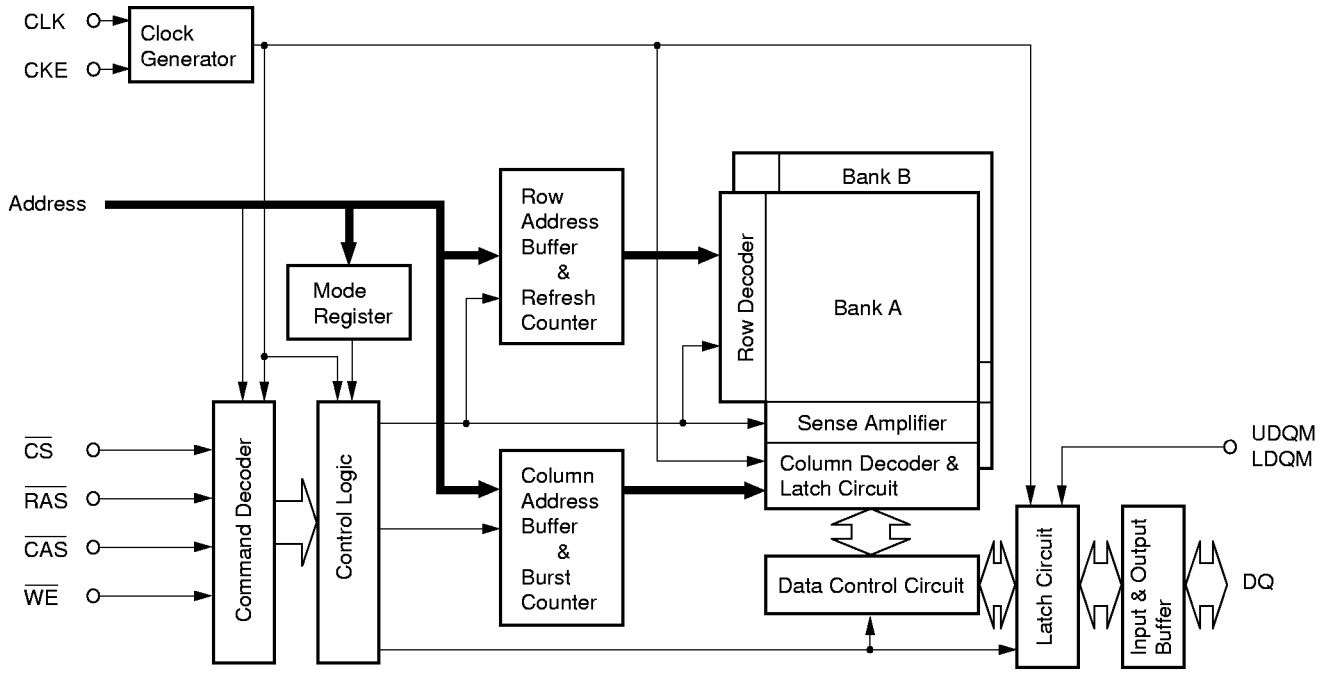
50-pin Plastic TSOP(II) (400 mil)
μPD4502161G5-7JF



A0 to A9 [Note] : Address inputs
DQ0 to DQ15 : Data inputs/outputs
CLK : System clock input
CKE : Clock enable
$\overline{CS}$: Chip select
$\overline{RAS}$: Row address strobe
$\overline{CAS}$: Column address strobe
$\overline{WE}$: Write enable
UDQM : Upper DQ mask enable
LDQM : Lower DQ mask enable
VCC : Supply voltage
VSS : Ground
VCCQ : Supply voltage for DQ
VSSQ : Ground for DQ
NC : No connection

Note A0 to A6, A8 : Row address inputs
A0 to A7 : Column address inputs
A9 : Bank select

Block Diagram

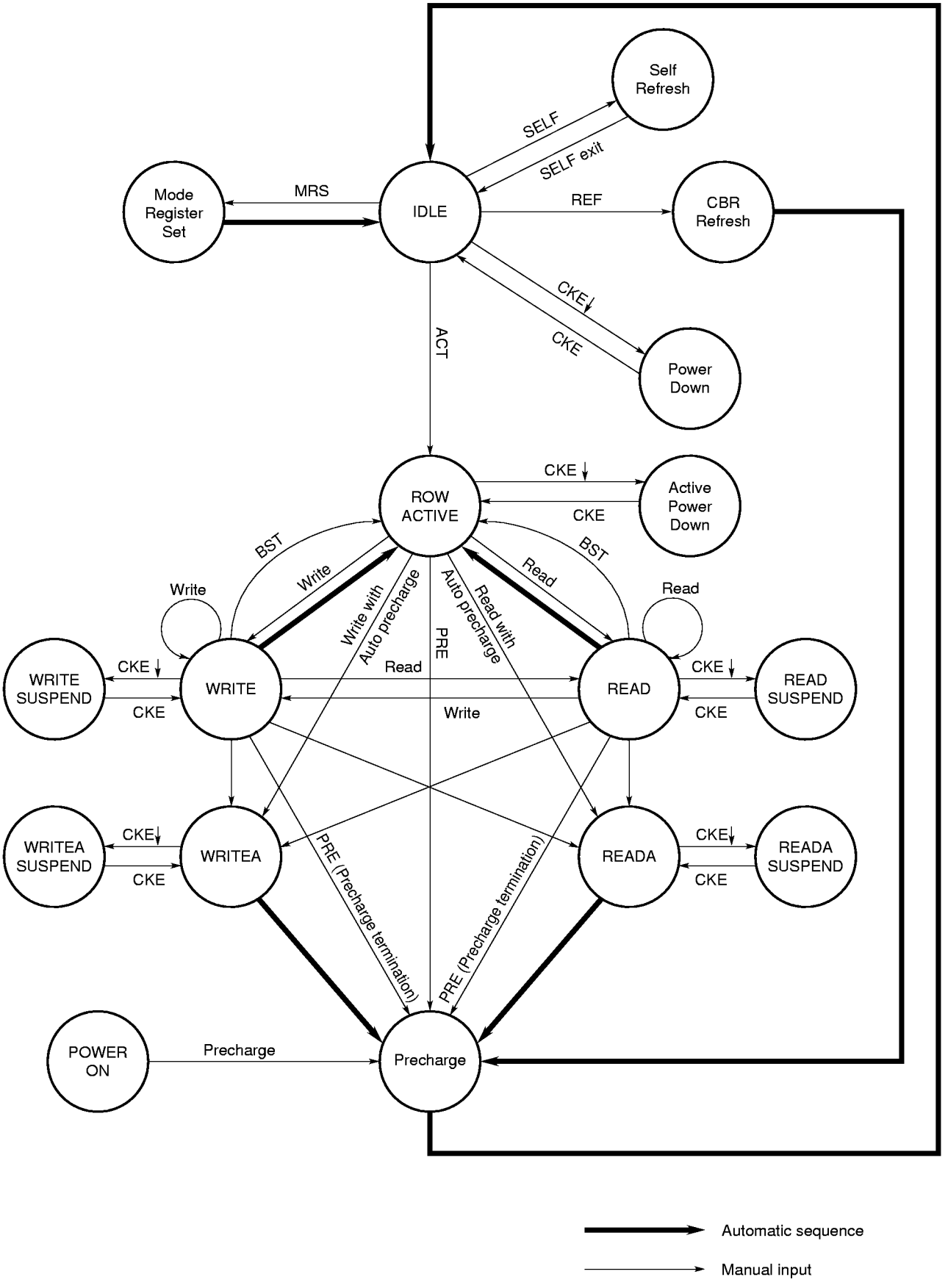


CONTENTS

1. Input/Output Pin Function

Pin name	Input/Output	Function
CLK	Input	CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.
CKE	Input	CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not issued and the μPD4502161 suspends operation. When the μPD4502161 is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.
$\overline{CS}$	Input	$\overline{CS}$ low starts the command input cycle. When $\overline{CS}$ is high, commands are ignored but operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ have the same symbols on conventional DRAM but different functions. For details, refer to the command table.
A0 - A9	Input	Row Address is determined by A0 - A6, A8 at the CLK (clock) rising edge in the activate command cycle. It does not depend on the bit organization. Column Address is determined by A0 - A7 at the CLK rising edge in the read or write command cycle. A9 is the bank select signal (BS). In command cycle, A9 low selects bank A and A9 high selects bank B. A8 defines the precharge mode. When A8 is high in the precharge command cycle, both banks are precharged; when A8 is low, only the bank selected by A9 is precharged. When A8 high in read or write command cycle, the precharge start automatically after the burst access.
DQM (UDQM, LDQM)	Input	UDQM and LDQM control upper byte and lower byte I/O buffers, respectively. In read mode, DQM controls the output buffers like a conventional $\overline{OE}$ pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
DQ0 - DQ15	Input/Output	DQ pins have the same function as I/O pins on a conventional DRAM.
V_{CC} V_{SS} $V_{CC}Q$ $V_{SS}Q$	(Power supply)	V_{CC} and V_{SS} are power supply pins for internal circuits. $V_{CC}Q$ and $V_{SS}Q$ are power supply pins for the output buffers.

2. Simplified State Diagram



3. Truth Table

3.1 Command Truth Table

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A7-A0
		n-1	n							
Device deselect	DESL	H	×	H	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×
Burst stop	BST	H	×	L	H	H	L	×	×	×
Read	READ	H	×	L	H	L	H	V	L	V
Read with auto precharge	READA	H	×	L	H	L	H	V	H	V
Write	WRIT	H	×	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	×	L	H	L	L	V	H	V
Bank activate	ACT	H	×	L	L	H	H	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	L	×
Precharge all banks	PALL	H	×	L	L	H	L	×	H	×
Mode register set	MRS	H	×	L	L	L	L	L	L	V

3.2 DQM Truth Table

Function	Symbol	CKE		DQM	
		n-1	n	U	L
Data write/output enable	ENB	H	×	L	
Data mask/output disable	MASK	H	×	H	
Upper byte write enable/output enable	ENBU	H	×	L	×
Lower byte write enable/output enable	ENBL	H	×	×	L
Upper byte write inhibit/output disable	MASKU	H	×	H	×
Lower byte write inhibit/output disable	MASKL	H	×	×	H

3.3 CKE Truth Table

Current state	Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add-ress
			n-1	n					
Activating	Clock suspend mode entry		H	L	×	×	×	×	×
Any	Clock suspend		L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit		L	H	×	×	×	×	×
Idle	CBR refresh command	REF	H	H	L	L	L	H	×
Idle	Self refresh entry	SELF	H	L	L	L	L	H	×
Self refresh	Self refresh exit		L	H	L	H	H	H	×
			L	H	H	×	×	×	×
Idle	Power down entry		H	L	×	×	×	×	×
Power down	Power down exit		L	H	×	×	×	×	×

H: High level, L: Low level

×: High or Low level (Don't care), V: Valid Data input

3.4 Operative Command Table[Notes1, 2]

(1/3)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Idle	H	×	×	×	×	DESL	Nop or Power down	**3**
	L	H	H	×	×	NOP or BST	Nop or Power down	**3**
	L	H	L	H	BA, CA, A8	READ/READA	ILLEGAL	**4**
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	**4**
	L	L	H	H	BA, RA	ACT	Row activating	
	L	L	H	L	BA, A8	PRE/PALL	Nop	
	L	L	L	H	×	REF/SELF	Refresh or Self refresh	**5**
	L	L	L	L	Op-Code	MRS	Mode register accessing	
Row active	H	×	×	×	×	DESL	Nop	
	L	H	H	×	×	NOP or BST	Nop	
	L	H	L	H	BA, CA, A8	READ/READA	Begin read:Determine AP	**6**
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Begin write:Determine AP	**6**
	L	L	H	H	BA, RA	ACT	ILLEGAL	**4**
	L	L	H	L	BA, A8	PRE/PALL	Precharge	**7**
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	H	×	×	×	×	DESL	Continue burst to end → Row active	
	L	H	H	H	×	NOP	Continue burst to end → Row active	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A8	READ/READA	Term burst, new read:Determine AP	**8**
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Term burst, start write:Determine AP	**8, 9**
	L	L	H	H	BA, RA	ACT	ILLEGAL	**4**
	L	L	H	L	BA, A8	PRE/PALL	Term burst, precharging	
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	H	×	×	×	×	DESL	Continue burst to end → Write recovering	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A8	READ/READA	Term burst, start read:Determine AP	**8, 9**
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Term burst, new write:Determine AP	**8**
	L	L	H	H	BA, RA	ACT	ILLEGAL	**4**
	L	L	H	L	BA, A8	PRE/PALL	Term burst, precharging	**10**
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(2/3)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Read with auto precharge	H	×	×	×	×	DESL	Continue burst to end → Precharging	
	L	H	H	H	×	NOP	Continue burst to end → Precharging	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A8	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	**4**
	L	L	H	L	BA, A8	PRE/PALL	ILLEGAL	**4**
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write with auto precharge	H	×	×	×	×	DESL	Continue burst to end → Write recovering with auto precharge	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering with auto precharge	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A8	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	**4**
	L	L	H	L	BA, A8	PRE/PALL	ILLEGAL	**4**
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Precharging	H	×	×	×	×	DESL	Nop → Enter idle after t_{RP}	
	L	H	H	H	×	NOP	Nop → Enter idle after t_{RP}	
	L	H	H	L	×	BST	Nop → Enter idle after t_{RP}	
	L	H	L	H	BA, CA, A8	READ/READA	ILLEGAL	**4**
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	**4**
	L	L	H	H	BA, RA	ACT	ILLEGAL	**4**
	L	L	H	L	BA, A8	PRE/PALL	Nop → Enter idle after t_{RP}	
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Row activating	H	×	×	×	×	DESL	Nop → Enter row active after t_{RCD}	
	L	H	H	H	×	NOP	Nop → Enter row active after t_{RCD}	
	L	H	H	L	×	BST	Nop → Enter row active after t_{RCD}	
	L	H	L	H	BA, CA, A8	READ/READA	ILLEGAL	**4**
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	**4**
	L	L	H	H	BA, RA	ACT	ILLEGAL	**4, 11**
	L	L	H	L	BA, A8	PRE/PALL	ILLEGAL	**4**
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(3/3)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Write recovering	H	×	×	×	×	DESL	Nop → Enter row active after t_{DPL}	
	L	H	H	H	×	NOP	Nop → Enter row active after t_{DPL}	
	L	H	H	L	×	BST	Nop → Enter row active after t_{DPL}	
	L	H	L	H	BA, CA, A8	READ/READA	Start read, Determine AP	**9**
	L	H	L	L	BA, CA, A8	WRIT/WRITA	New write, Determine AP	
	L	L	H	H	BA, RA	ACT	ILLEGAL	**4**
	L	L	H	L	BA, A8	PRE/PALL	ILLEGAL	**4**
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write recovering with auto precharge	H	×	×	×	×	DESL	Nop → Enter precharge after t_{DPL}	
	L	H	H	H	×	NOP	Nop → Enter precharge after t_{DPL}	
	L	H	H	L	×	BST	Nop → Enter precharge after t_{DPL}	
	L	H	L	H	BA, CA, A8	READ/READA	ILLEGAL	**4, 9**
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	**4**
	L	L	H	H	BA, RA	ACT	ILLEGAL	**4**
	L	L	H	L	BA, A8	PRE/PALL	ILLEGAL	**4**
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Refreshing	H	×	×	×	×	DESL	Nop → Enter idle after t_{RC}	
	L	H	H	×	×	NOP/BST	Nop → Enter idle after t_{RC}	
	L	H	L	×	×	READ/WRIT	ILLEGAL	
	L	L	H	×	×	ACT/PRE/PALL	ILLEGAL	
	L	L	L	×	×	REF/SELF/MRS	ILLEGAL	
Mode register accessing	H	×	×	×	×	DESL	Nop → Enter idle after t_{RSC}	
	L	H	H	H	×	NOP	Nop → Enter idle after t_{RSC}	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	×	×	READ/WRITE	ILLEGAL	
	L	L	×	×	×	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL	

Notes 1. H: High level, L: Low level, ×: High or Low level (Don't care), V: Valid data input

2. All entries assume that CKE was active (High level) during the preceding clock cycle.

3. If both banks are idle, and CKE is inactive (Low level), μPD4502161 will enter Power down mode. All input buffers except CKE will be disabled.

4. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

5. If both banks are idle, and CKE is inactive (Low level), μPD4502161 will enter Self refresh mode. All input buffers except CKE will be disabled.

6. Illegal if t_{RCD} is not satisfied.

7. Illegal if t_{RAS} is not satisfied.

8. Must satisfy burst interrupt condition.

9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.

10. Must mask preceding data which don't satisfy t_{DPL}.

11. Illegal if t_{RRD} is not satisfied.

3.5 Command Truth Table for CKE[Note 1]

Current state	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Notes
Self refresh (S.R.)	H	×	×	×	×	×	×	INVALID, CLK(n-1) would exit S.R.	
	L	H	H	×	×	×	×	S.R. Recovery	
	L	H	L	H	H	×	×	S.R. Recovery	
	L	H	L	H	L	×	×	ILLEGAL	
	L	H	L	L	×	×	×	ILLEGAL	
	L	L	×	×	×	×	×	Maintain S.R.	
Self refresh recovery	H	H	H	×	×	×	×	Idle after t_{RC}	
	H	H	L	H	H	×	×	Idle after t_{RC}	
	H	H	L	H	L	×	×	ILLEGAL	
	H	H	L	L	×	×	×	ILLEGAL	
	H	L	H	×	×	×	×	ILLEGAL	
	H	L	L	H	H	×	×	ILLEGAL	
	H	L	L	H	L	×	×	ILLEGAL	
	H	L	L	L	×	×	×	ILLEGAL	
Power down (P.D.)	H	×	×	×	×	×		INVALID, CLK(n-1) would exit P.D.	
	L	H	×	×	×	×	×	EXIT P.D. → Idle	
	L	L	×	×	×	×	×	Maintain power down mode	
Both banks idle	H	H	H	×	×	×		Refer to operations in Operative Command Table	
	H	H	L	H	×	×		Refer to operations in Operative Command Table	
	H	H	L	L	H	×		Refer to operations in Operative Command Table	
	H	H	L	L	L	H	×	Refresh	
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	H	L	H	×	×	×		Refer to operations in Operative Command Table	
	H	L	L	H	×	×		Refer to operations in Operative Command Table	
	H	L	L	L	H	×		Refer to operations in Operative Command Table	
	H	L	L	L	L	H	×	Self refresh	2
	H	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	L	×	×	×	×	×	×	Power down	2
Row active	H	×	×	×	×	×		Refer to operations in Operative Command Table	
	L	×	×	×	×	×		Power down	3
Any state other than listed above	H	H	×	×	×	×	×	Refer to operations in Operative Command Table	
	H	L	×	×	×	×	×	Begin clock suspend next cycle	3
	L	H	×	×	×	×	×	Exit clock suspend next cycle	
	L	L	×	×	×	×	×	Maintain clock suspend	

Notes 1. H: High level, L: Low level, X: High or low level (Don't care)

2. Self refresh can be entered only from the both banks idle state. Power down can be entered from the both banks idle state or row active state.

3. Must be legal command as defined in Operative Command Table.

3.6 Command Truth Table for Two Banks Operation [Notes 1, 2]

$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A8	A7 - A0	Action	"FROM" State [Note 3]	"TO" State [Note 4]
H	×	×	×	×	×	×	NOP	Any	Any
L	H	H	H	×	×	×	NOP	Any	Any
L	H	H	L	×	×	×	BST	(R/W/A)0(I/A)1	A0(I/A)1
								I0(I/A)1	I0(I/A)1
								(R/W/A)1(I/A)0	A1(I/A)0
								I1(I/A)0	I1(I/A)0
L	H	L	H	H	H	CA	Read	(R/W/A)1(I/A)0	RP1(I/A)0
				H	H	CA		A1(R/W)0	RP1A0
				H	L	CA		(R/W/A)1(I/A)0	R1(I/A)0
				H	L	CA		A1(R/W)0	R1A0
				L	H	CA		(R/W/A)0(I/A)1	RP0(I/A)1
				L	H	CA		A0(R/W)1	RP0A1
				L	L	CA		(R/W/A)0(I/A)1	R0(I/A)1
				L	L	CA		A0(R/W)1	R0A1
L	H	L	L	H	H	CA	Write	(R/W/A)1(I/A)0	WP1(I/A)0
				H	H	CA		A1(R/W)0	WP1A0
				H	L	CA		(R/W/A)1(I/A)0	W1(I/A)0
				H	L	CA		A1(R/W)0	W1A0
				L	H	CA		(R/W/A)0(I/A)1	WP0(I/A)1
				L	H	CA		A0(R/W)1	WP0A1
				L	L	CA		(R/W/A)0(I/A)1	W0(I/A)1
				L	L	CA		A0(R/W)1	W0A1
L	L	H	H	H	RA		Activate Row	I1Any0	A1Any0
				L	RA			I0Any1	A0Any1
L	L	H	L	×	H	×	Precharge	(R/W/A/I)0(I/A)1	I0I1
				×	H	×		(R/W/A/I)1(I/A)0	I1I0
				H	L	×		(R/W/A/I)1(I/A)0	I1(I/A)0
				H	L	×		(I/A)1(R/W/A/I)0	I1(R/W/A/I)0
				L	L	×		(R/W/A/I)0(I/A)1	I0(I/A)1
				L	L	×		(I/A)0(R/W/A/I)1	I0(R/W/A/I)1
L	L	L	H	×	×	×	Refresh	I0I1	I0I1
L	L	L	L	Op-Code			Mode Register Access	I0I1	I0I1

Notes 1. Logic level abbreviations

H: High level, L: Low level, ×: High or low level (Don't care)

Pin name abbreviation

BA: Bank address (A9)

2. State abbreviations

I = Idle
A = Row active
R = Read with No precharge (No precharge is posted)
W = Write with No precharge (No precharge is posted)
RP = Read with auto precharge (Precharge is posted)
WP = Write with auto precharge (Precharge is posted)
Any = Any State
X0Y1 = Y1X0 = Bank A is in state "X", Bank B is in state "Y"
(X/Y)0Z1 = Z1(X/Y)0 = Bank A is in state "X" or "Y", Bank B is in state "Z"

3. If the μPD4502161 is in a state other than above listed in the "From State" column, the command is illegal.
4. The states listed under "To" might not be entered on the next clock cycle.
Timing restrictions apply.

4. Initialization

The synchronous DRAM is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, when power is applied, a 100-μs or longer pause must precede any signal toggling.

(2) After the pause, both banks must be precharged using the Precharge command (The Precharge all banks command is convenient).

(3) Once the precharge is completed and the minimum t_{RP} is satisfied, the mode register can be programmed. After the mode register set cycle, t_{RSC} (2CLK minimum) pause must be satisfied as well.

(4) Two or more CBR (Auto) refresh must be performed.

Remarks 1. The sequence of Mode register programming and Refresh above may be transposed.
2. CKE and DQM must be held high until the Precharge command is issued to ensure data bus Hi-Z.

5. Programming the Mode Register

The mode register is programmed by the Mode register set command using address bits A9 through A0 as data inputs. The register retains data until it is reprogrammed or the device loses power.

The mode register has four fields;

Options : A9 through A7
$\overline{\text{CAS}}$ latency : A6 through A4
Wrap type : A3
Burst length : A2 through A0

Following mode register programming, no command can be issued before at least 2CLK have elapsed.

$\overline{\text{CAS}}$ Latency

$\overline{\text{CAS}}$ latency is the most critical of the parameters being set. It tells the device how many clocks must elapse before the data will be available.

The value is determined by the frequency of the clock and the speed grade of the device. The table in 1**2.3 Relationship between Frequency and Latency** shows the relationship of $\overline{\text{CAS}}$ latency to the clock period and the speed grade of the device.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become Hi-Z.

The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either “Sequential” or “Interleave”. The method chosen will depend on the type of CPU in the system.

Some microprocessor cache system are optimized for sequential addressing and others for interleaved addressing. The table in **6.1 Burst length and Sequence** shows the addressing sequence for each burst length using them. Both sequences support bursts of 1, 2, 4 and 8. Additionally, sequential sequence supports the full page length.

6. Mode Register

9	8	7	6	5	4	3	2	1	0	
0	0	1								JEDEC Standard Test Set (refresh counter test)
1	0	0	LTMODE			WT	BL			Burst Read and Single Write (for Write Through Cache)
×	1	0								Use in future
×	1	1	V	V	V	V	V	V	V	Vender Specific
0	0	0	LTMODE			WT	BL			Mode Register Set

V = Valid
× = Don't care

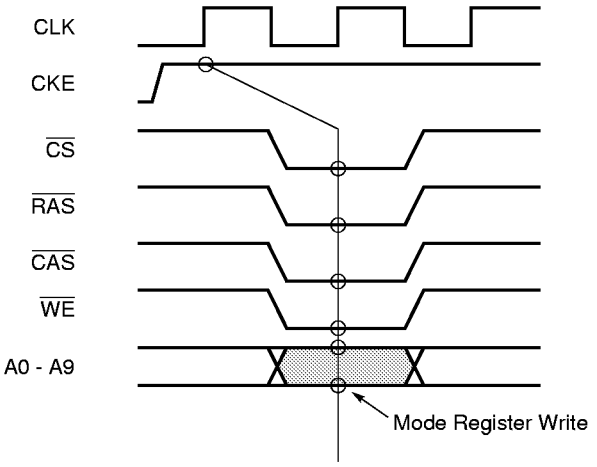
Burst length	Bits2-0	WT = 0	WT = 1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type		
	0	Sequential
	1	Interleave

Latency mode	Bits6-4	$\overline{CAS}$ latency
	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R: Reserved

Mode Register Write Timing



6.1 Burst Length and Sequence

[Burst of Two]

Starting Address (column address A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

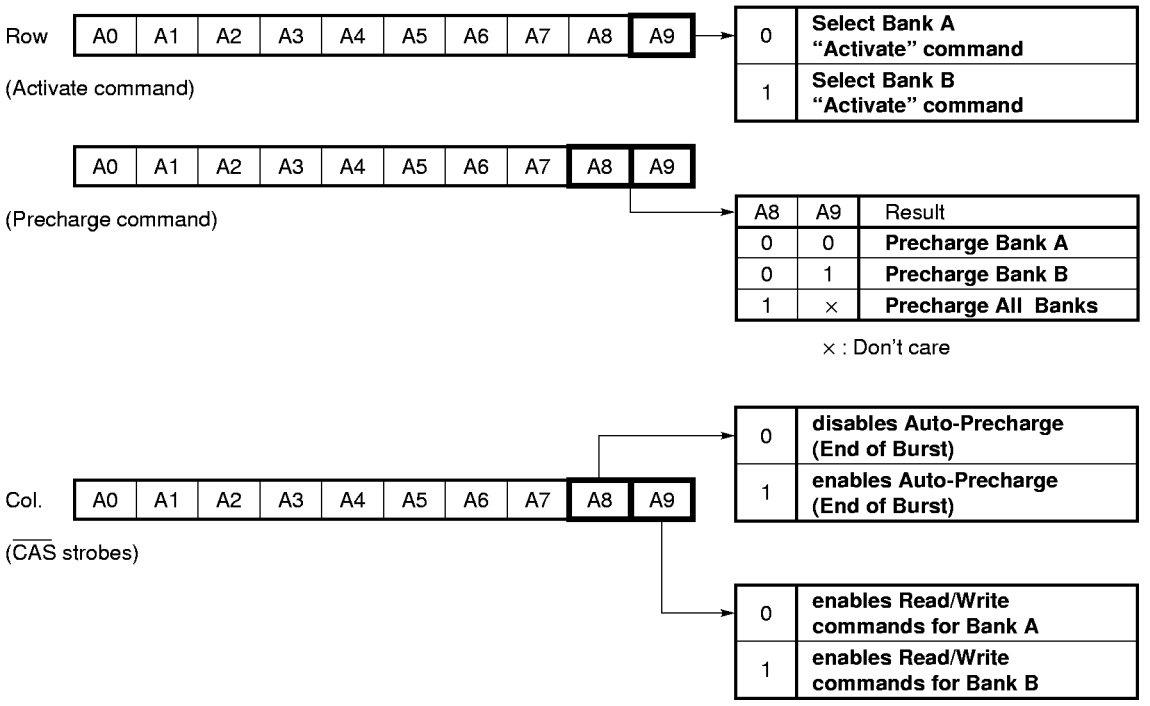
Starting Address (column address A1 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

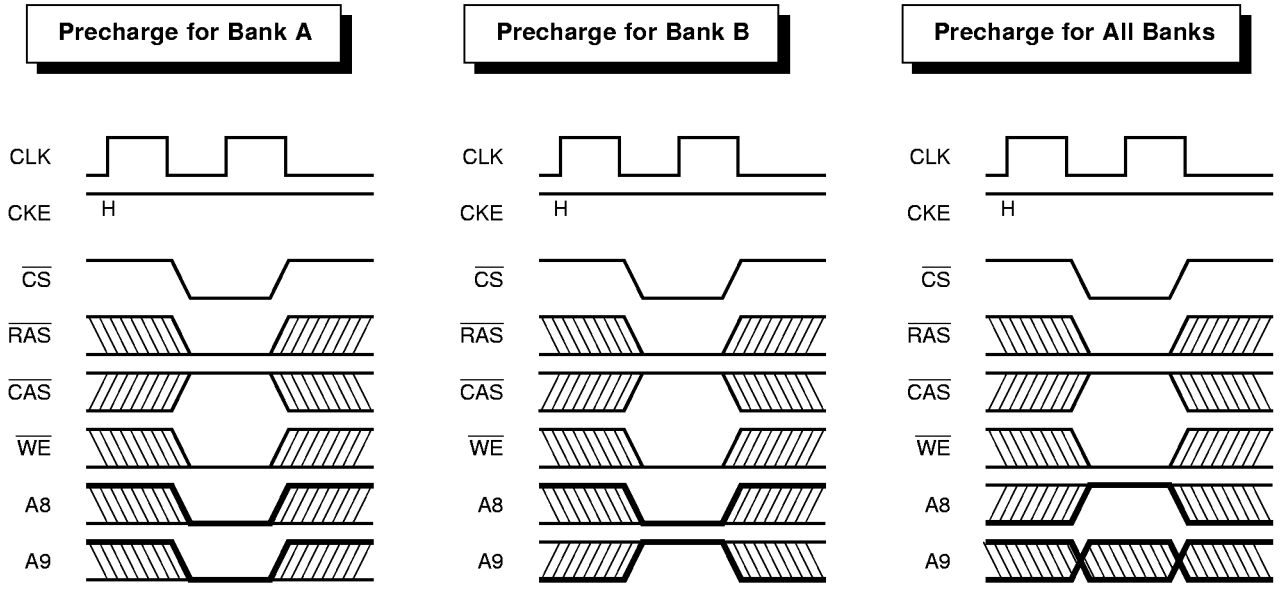
[Burst of Eight]

Starting Address (column address A2 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page burst is an extension of the above tables of Sequential Addressing, with the length being 256.

7. Address Bits of Bank-Select and Precharge





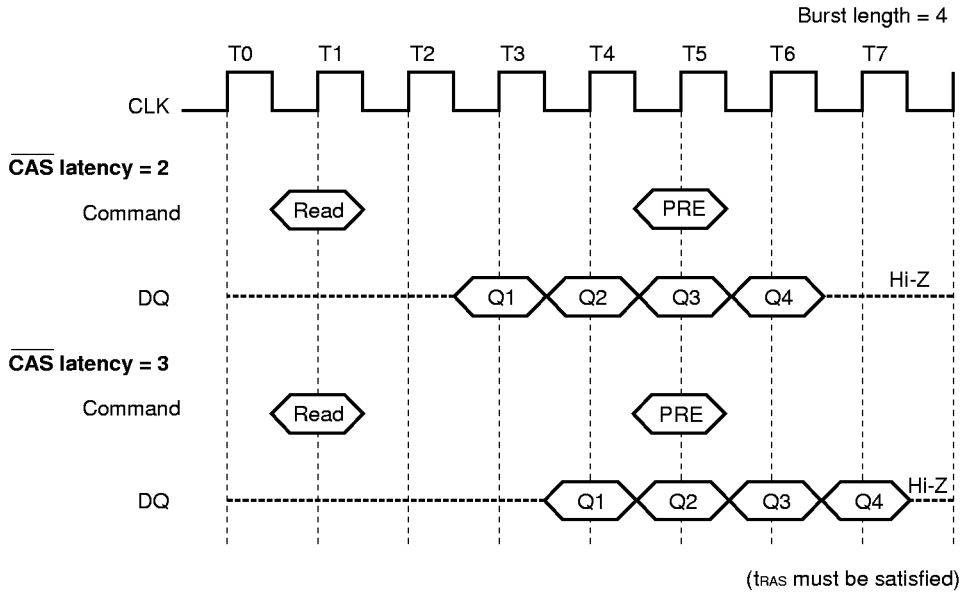
8. Precharge

The precharge command can be issued anytime after $t_{RAS(MIN.)}$ is satisfied.

Soon after the precharge command is issued, precharge operation performed and the synchronous DRAM enters the idle state after t_{RP} is satisfied. The parameter t_{RP} is the time required to perform the precharge.

The earliest timing in a read cycle that a precharge command can be issued without losing any data in the burst is as follows.

$\overline{CAS}$ latency = 2 : One clock earlier than the last read data.
$\overline{CAS}$ latency = 3 : Two clocks earlier than the last read data.



In order to write all data to the memory cell correctly, the asynchronous parameter "t_{DPL}" must be satisfied. The $t_{DPL(MIN.)}$ specification defines the earliest time that a precharge command can be issued. Minimum number of clocks are calculated by dividing $t_{DPL\ (MIN.)}$ with clock cycle time.

In summary, the precharge command can be issued relative to reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

$\overline{CAS}$ latency	Read	Write
2	–1	$+t_{DPL\ (MIN.)}$
3	–2	$+t_{DPL\ (MIN.)}$

9. Auto Precharge

During a read or write command cycle, A8 controls whether auto precharge is selected. A8 high in the Read or Write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and precharge begins automatically.

The t_{RAS} must be satisfied with a read with auto precharge or a write with auto precharge operation. In addition, the next activate command to the bank being precharged cannot be executed until the precharge cycle ends.

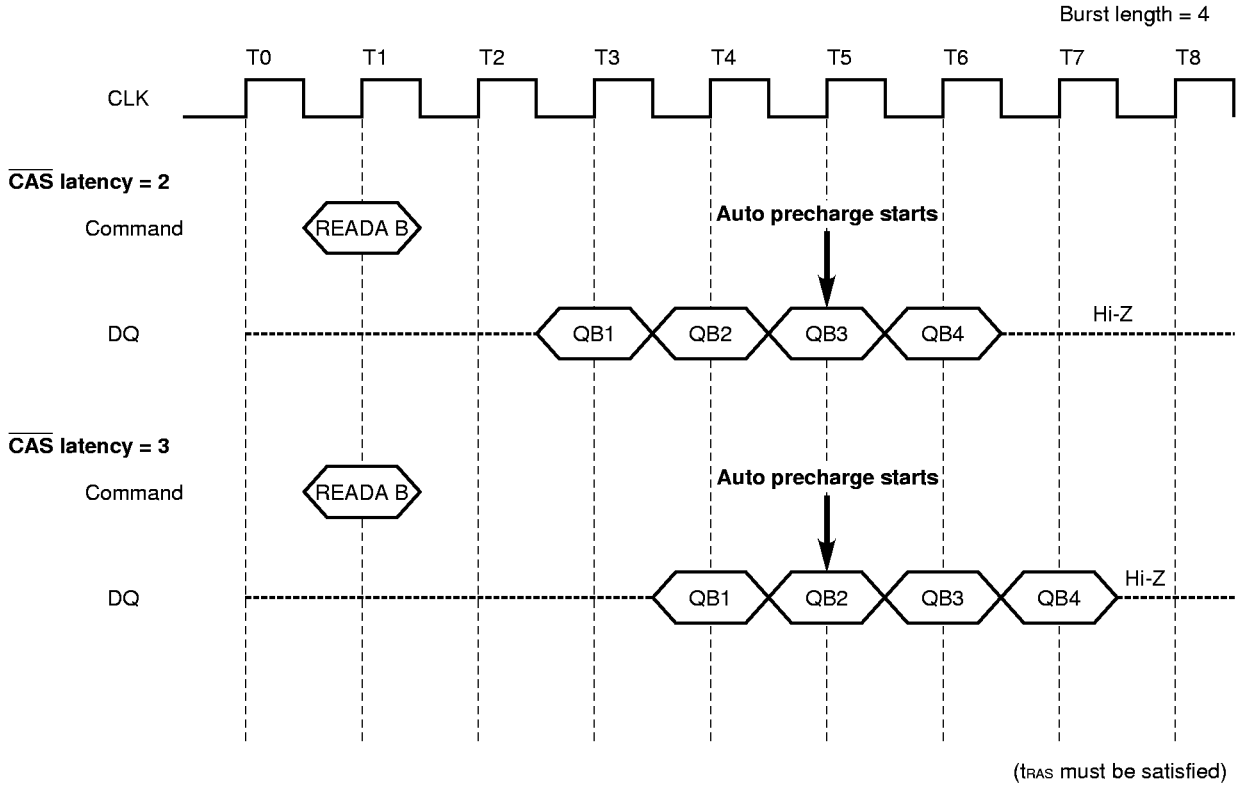
In read cycle, once auto precharge has started, an activate command to the bank can be issued after t_{RP} has been satisfied.

In write cycle, the t_{DAL} must be satisfied to issue the next activate command to the bank being precharged.

The timing that begins the auto precharge cycle depends on both the $\overline{CAS}$ latency programmed into the mode register and whether read or write cycle.

9.1 Read with Auto Precharge

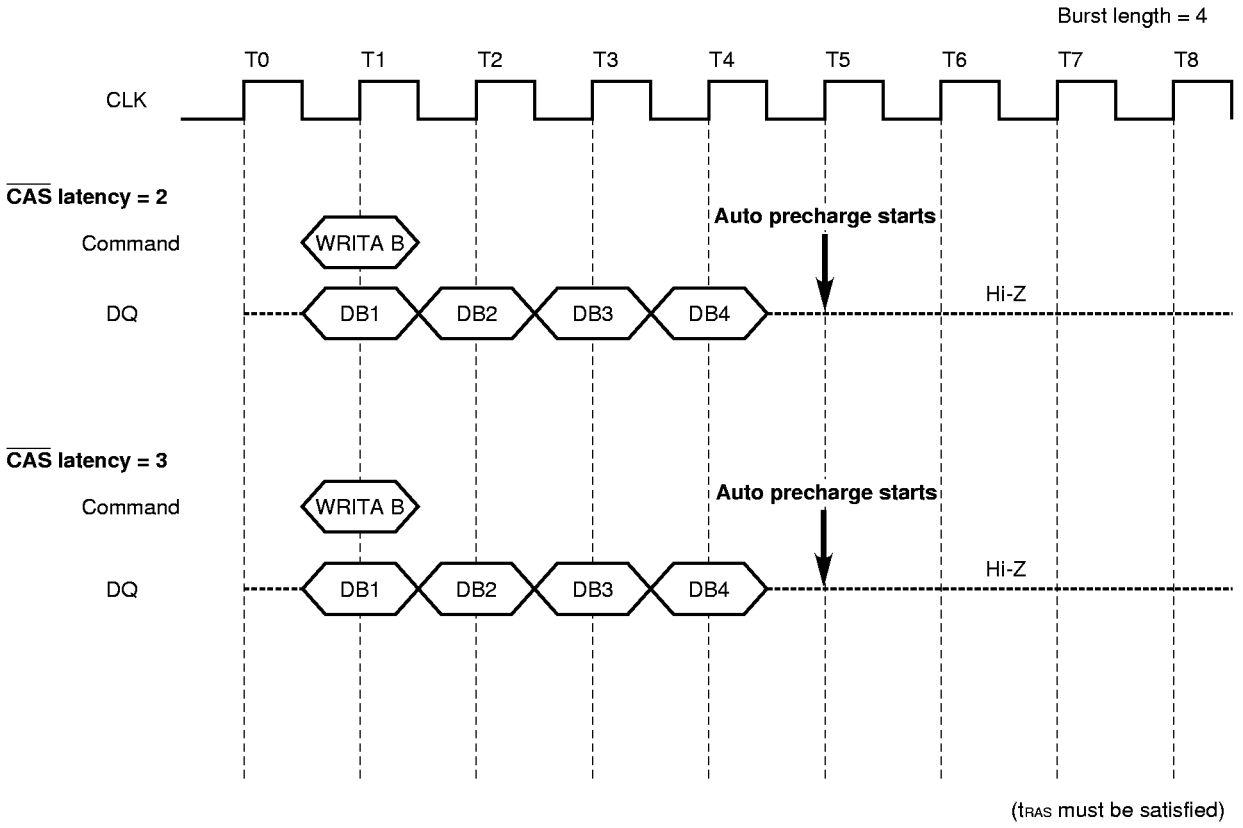
During a read cycle, the auto precharge begins one clock earlier ($\overline{CAS}$ latency of 2) or two clocks earlier ($\overline{CAS}$ latency of 3) the last data word output.



Remark READA means Read with Auto precharge

9.2 Write with Auto Precharge

During a write cycle, the auto precharge begins one clock after the last data word input to the device ($\overline{CAS}$ latency of 2 or 3).



Remark WRITA means Write with Auto precharge

In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid. In the table below, minus means clocks before the reference; plus means clocks after the reference.

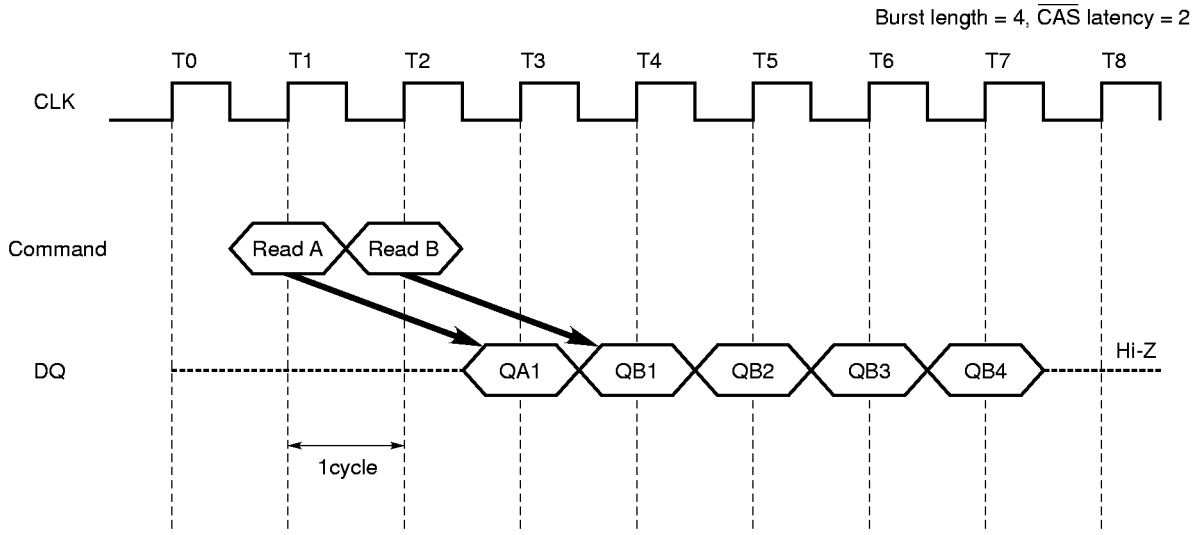
$\overline{CAS}$ latency	Read	Write
2	–1	+1
3	–2	+1

10. Read/Write Command Interval

10.1 Read to Read Command Interval

During a read cycle, when new Read command is issued, it will be effective after $\overline{CAS}$ latency, even if the previous READ operation does not completed. READ will be interrupted by another READ.

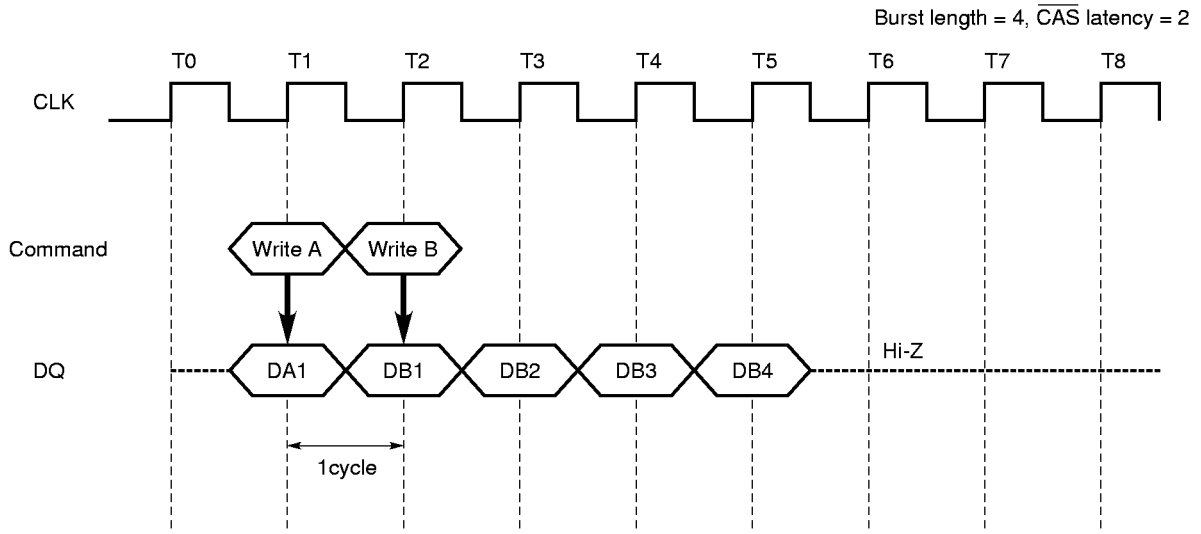
The interval between the commands is 1 cycle minimum. Each Read command can be issued in every clock without any restriction.



10.2 Write to Write Command Interval

During a write cycle, when new Write command is issued, the previous burst will terminate and the new burst will begin with a new Write commnad. WRITE will be interrupted by another WRITE.

The interval between the commands is minimum 1. Each Write command can be issued in every clock without any restriction.

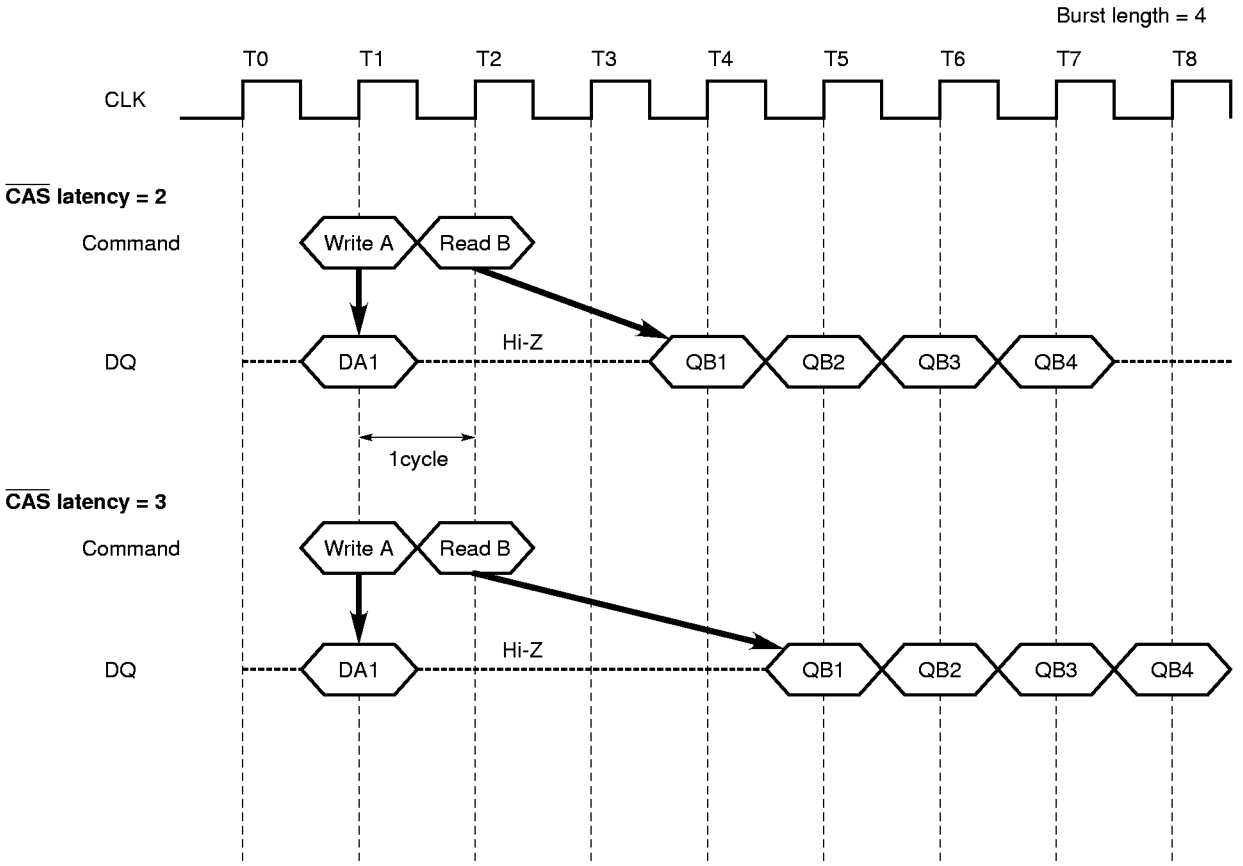


10.3 Write to Read Command Interval

Write command and Read command interval is also 1 cycle.

Only the write data before Read command will be written.

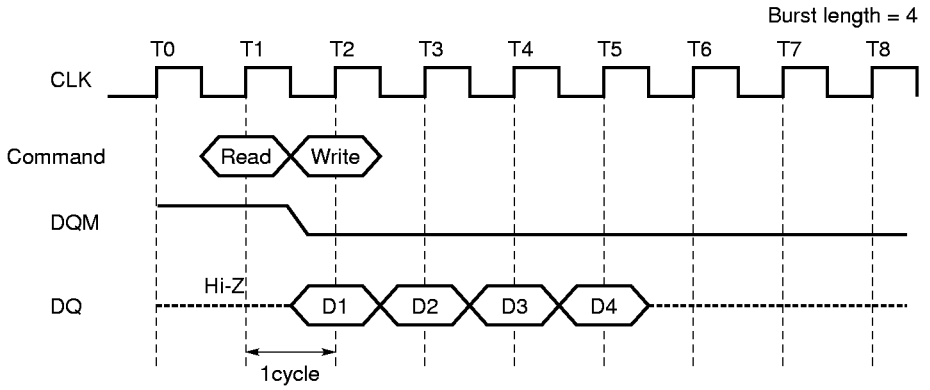
The data bus must be Hi-Z at least one cycle prior to the first DOUT.



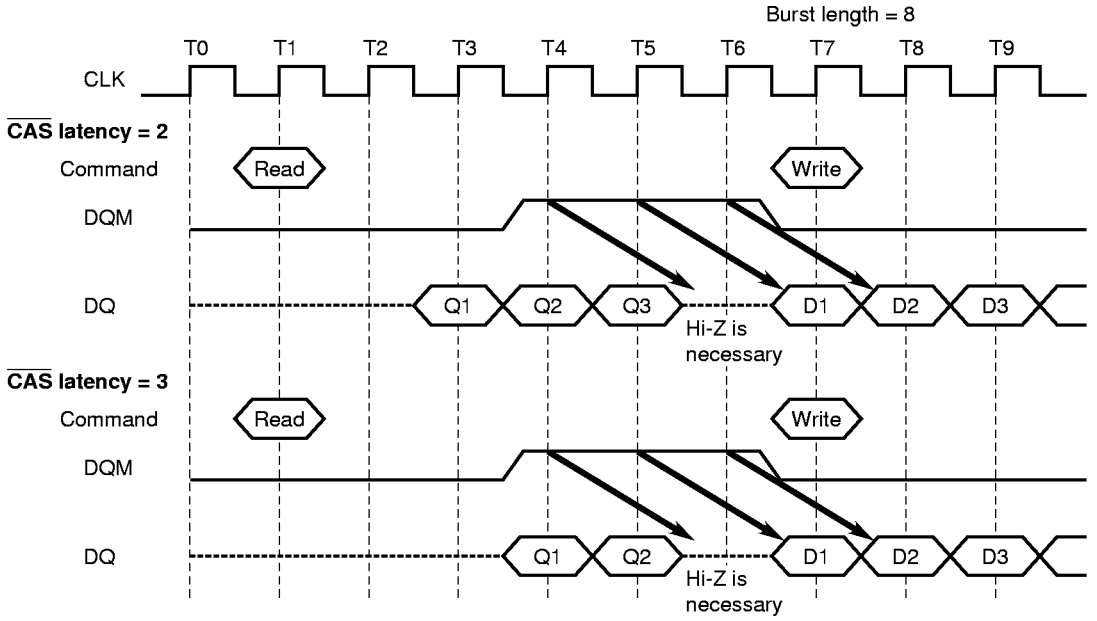
10.4 Read to Write Command Interval

During a read cycle, READ can be interrupted by WRITE.

The Read and Write command interval is 1 cycle minimum. There is a restriction to avoid data conflict. The data bus must be Hi-Z using DQM before WRITE.



READ can be interrupted by WRITE. DQM must be High at least 3 clocks prior to the Write command.

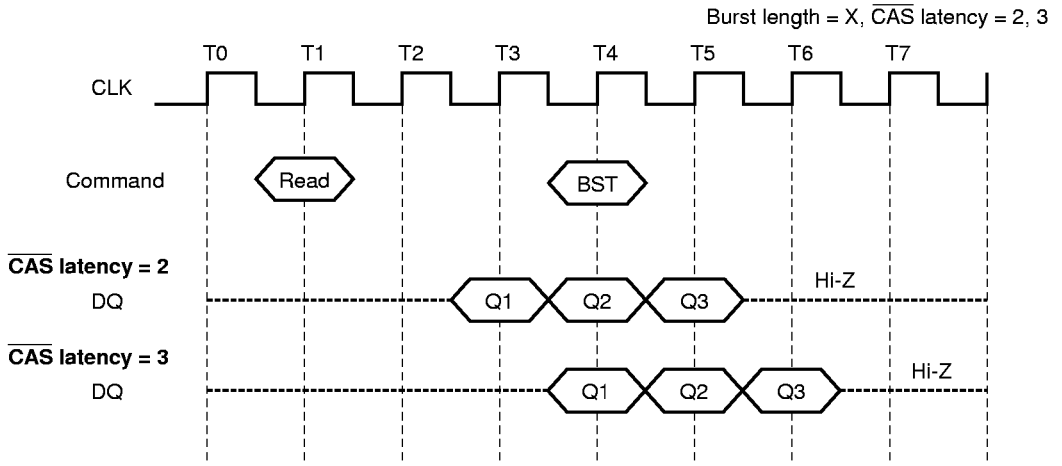


11. Burst Termination

There are two methods to terminate a burst operation other than using a Read or a Write command.
One is the burst stop command and the other is the precharge command.

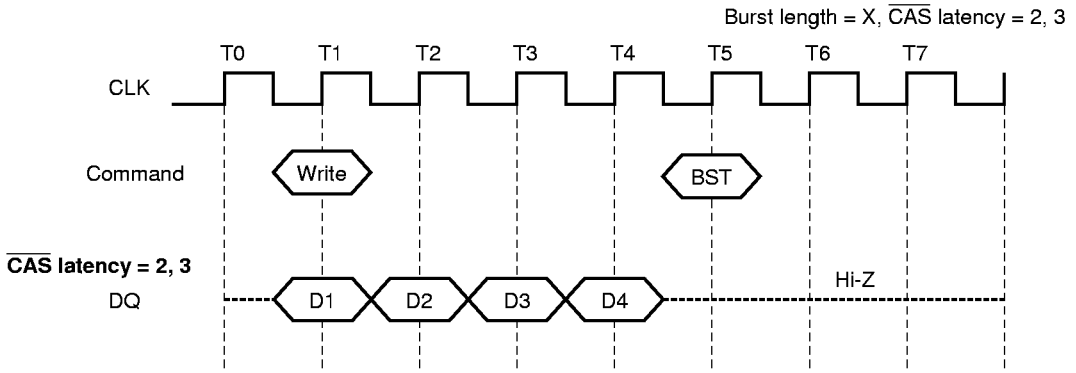
11.1 Burst Stop Command

During a read cycle, when the burst stop command is issued, the burst read data are terminated and the data bus goes to Hi-Z after the $\overline{CAS}$ latency from the burst stop command.



Remark BST: Burst stop command

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to Hi-Z at the same clock with the burst stop command.



Remark BST: Burst stop command

11.2 Precharge Termination

11.2.1 Precharge Termination in READ Cycle

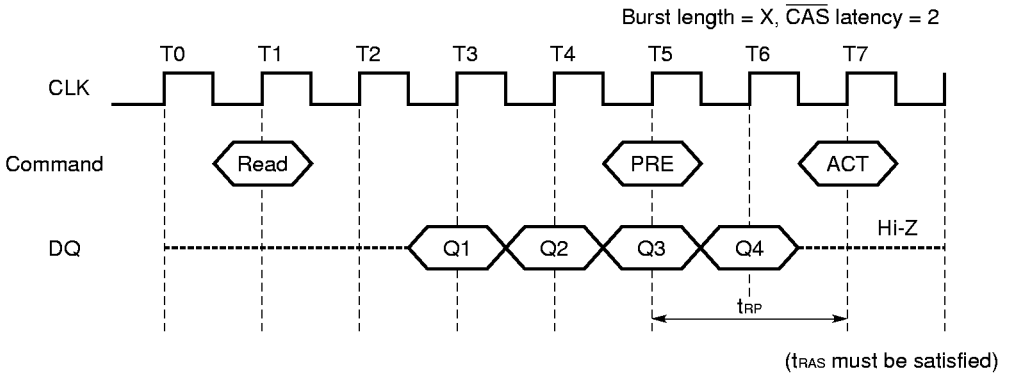
During a read cycle, the burst read operation is terminated by a precharge command.

When the precharge command is issued, the burst read operation is terminated and precharge starts.

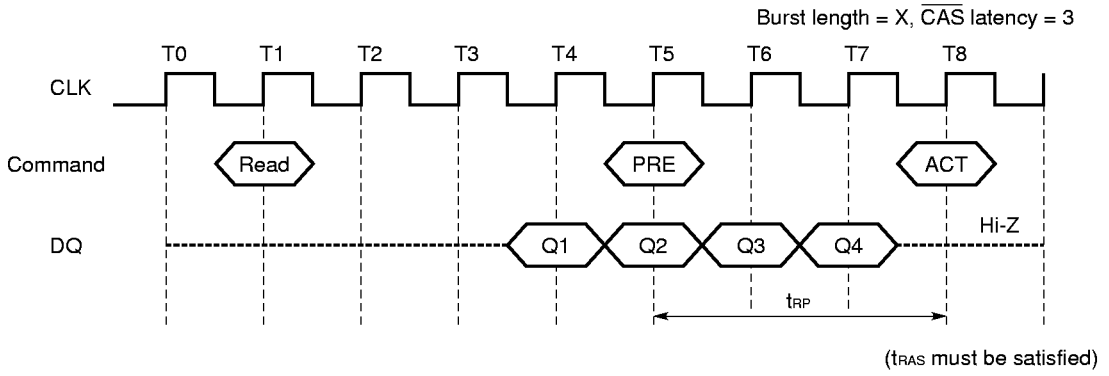
The same bank can be activated again after t_{RP} from the precharge command.

To issue a precharge command, t_{RAS} must be satisfied.

When $\overline{CAS}$ latency is 2, the read data will remain valid until one clock after the precharge command.



When $\overline{CAS}$ latency is 3, the read data will remain valid until two clocks after the precharge command.



11.2.2 Precharge Termination in WRITE Cycle

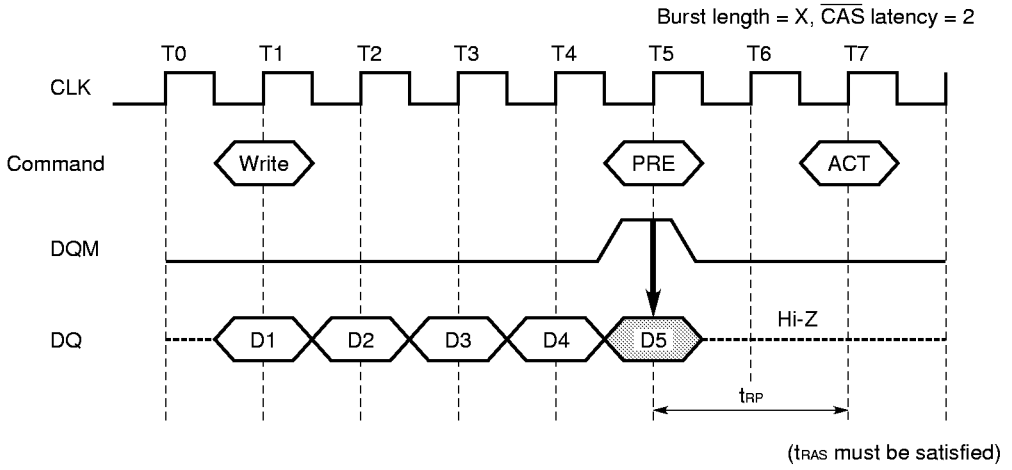
During a write cycle, the burst write operation is terminated by a precharge command.

When the precharge command is issued, the burst write operation is terminated and precharge starts.

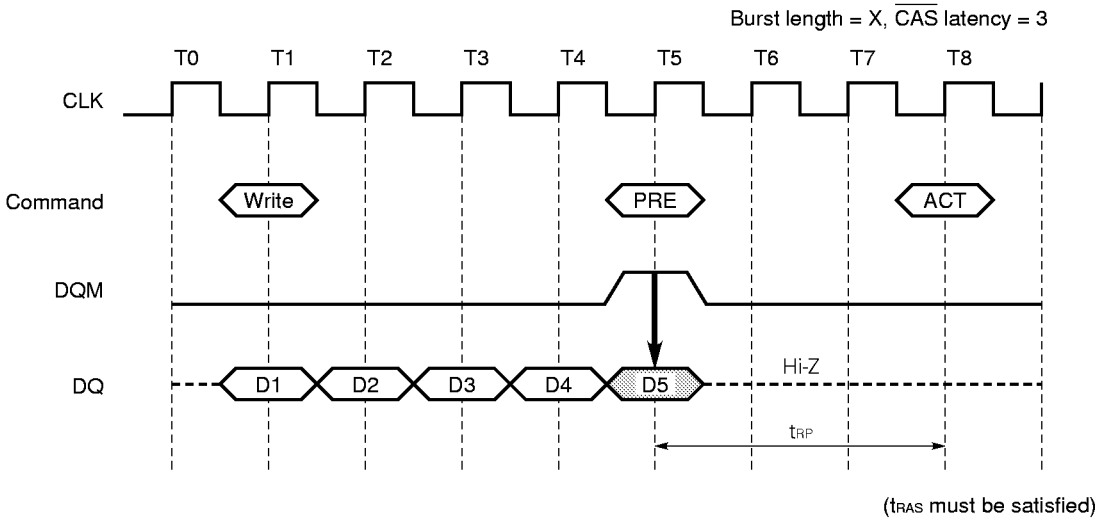
The same bank can be activated again after t_{RP} from the precharge command.

To issue a precharge command, t_{RAS} must be satisfied.

When $\overline{CAS}$ latency is 2, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



When $\overline{CAS}$ latency is 3, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



12. Electrical Specifications

- All voltage are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute **Power on sequence and Auto Refresh** before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}, $V_{CC}Q$		–1.0 to +4.6	V
Voltage on input pin relative to GND	V_T		–1.0 to +5.5	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		5.5	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A9	2		4	pF
	C_{I2}	CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, UDQM, LDQM	2		4	pF
Data input/output capacitance	$C_{I/O}$	DQ0 to DQ15	2		6	pF

DC Characteristics 1 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	$\overline{CAS}$ latency	Grade	Maximum	Unit	Notes
Operating current	I_{CC1}	Burst length=1 $t_{RC} \geq t_{RC\ (MIN.)}$ I_O = 0 mA One bank active	CL = 2	–10	90	mA	1
				–12	90		
			CL = 3	–10	90		
				–12	90		
Precharge standby current in Power down mode	I_{CC2P}	CKE ≤ $V_{IL\ (MAX.)}$ t_{CK} = 15 ns			3	mA	
	I_{CC2PS}	CKE ≤ $V_{IL\ (MAX.)}$ t_{CK} = ∞			2		
Precharge standby current in Non power down mode	I_{CC2N}	CKE ≥ $V_{IH\ (MIN.)}$ t_{CK} = 15 ns $\overline{CS}$ ≥ $V_{IH\ (MIN.)}$ Input signals are changed one time during 30 ns.			25	mA	
	I_{CC2NS}	CKE ≥ $V_{IH\ (MIN.)}$ t_{CK} = ∞ Input signals are stable.			6		
Active standby current in Power down mode	I_{CC3P}	CKE ≤ $V_{IL\ (MAX.)}$ t_{CK} = 15 ns			3	mA	
	I_{CC3PS}	CKE ≤ $V_{IL\ (MAX.)}$ t_{CK} = ∞			2		
Active standby current in Non power down mode	I_{CC3N}	CKE ≥ $V_{IH\ (MIN.)}$ t_{CK} = 15 ns $\overline{CS}$ ≥ $V_{IH\ (MIN.)}$ Input signals are changed one time during 30 ns.			30	mA	
	I_{CC3NS}	CKE ≥ $V_{IH\ (MIN.)}$ t_{CK} = ∞ Input signals are stable.			10		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN.)}$ I_O = 0 mA All banks active	CL = 2	–10	100	mA	2
				–12	100		
			CL = 3	–10	140		
				–12	120		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN.)}$	CL = 2	–10	85	mA	3
				–12	85		
			CL = 3	–10	85		
				–12	85		
Self refresh Current	I_{CC6}	CKE ≤ 0.2V			2	mA	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

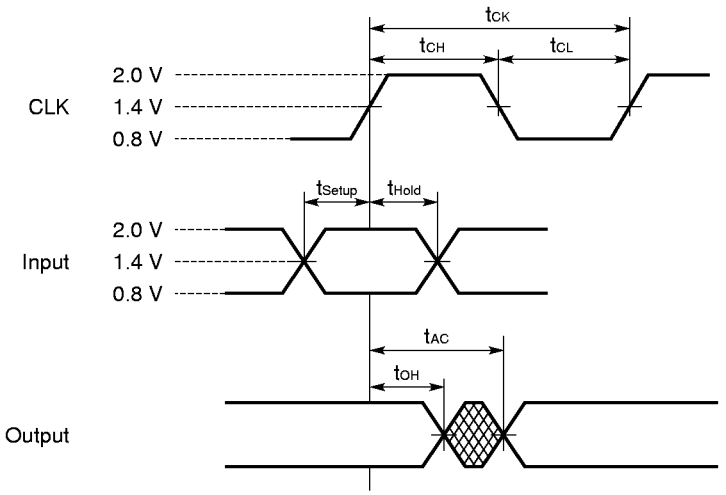
DC Characteristics 2 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V, all other pins not under test = 0 V	–5.0		+5.0	μA
Output leakage current	$I_{O(L)}$	D_{OUT} is disabled, V_O = 0 to 3.6 V	–5.0		+5.0	μA
High level output voltage	V_{OH}	I_O = –2 mA	2.4			V
Low level output voltage	V_{OL}	I_O = +2 mA			0.4	V

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

Test Conditions

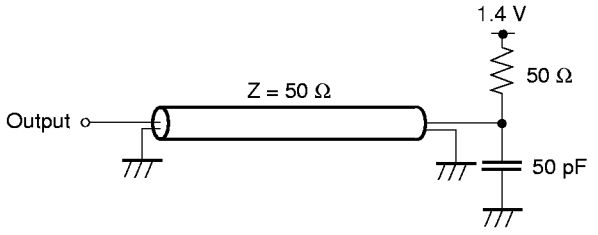
- AC measurements assume t_T = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH\ (MIN.)}$ and $V_{IL\ (MAX.)}$.
- An access time is measured at 1.4 V.



Synchronous Characteristics

Parameter		Symbol	–10		–12		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
Clock cycle time	$\overline{CAS}$ latency = 3	t_{CK3}	10	(100 MHz)	12	(83 MHz)	ns	
	$\overline{CAS}$ latency = 2	t_{CK2}	15	(67 MHz)	15	(67 MHz)	ns	
Access time from CLK	$\overline{CAS}$ latency = 3	t_{AC3}		8		9	ns	**1**
	$\overline{CAS}$ latency = 2	t_{AC2}		10		11	ns	**1**
CLK high level width		t_{CH}	3.5		4		ns	
CLK low level width		t_{CL}	3.5		4		ns	
Data-out hold time		t_{OH}	3		3		ns	**1**
Data-out low-impedance time		t_{LZ}	0		0		ns	
Data-out high-impedance time	$\overline{CAS}$ latency = 3	t_{HZ3}	3	8	3	9	ns	
	$\overline{CAS}$ latency = 2	t_{HZ2}	3	10	3	11	ns	
Data-in setup time		t_{DS}	2.5		3.0		ns	
Data-in hold time		t_{DH}	1.0		1.5		ns	
Address setup time		t_{AS}	2.5		3.0		ns	
Address hold time		t_{AH}	1.0		1.5		ns	
CKE setup time		t_{CKS}	2.5		3.0		ns	
CKE hold time		t_{CKH}	1.0		1.5		ns	
CKE setup time (Power down exit)		t_{CKSP}	2.5		3.0		ns	
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, UDQM, LDQM) setup time		t_{CMS}	2.5		3.0		ns	
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, UDQM, LDQM) hold time		t_{CMH}	1.0		1.5		ns	

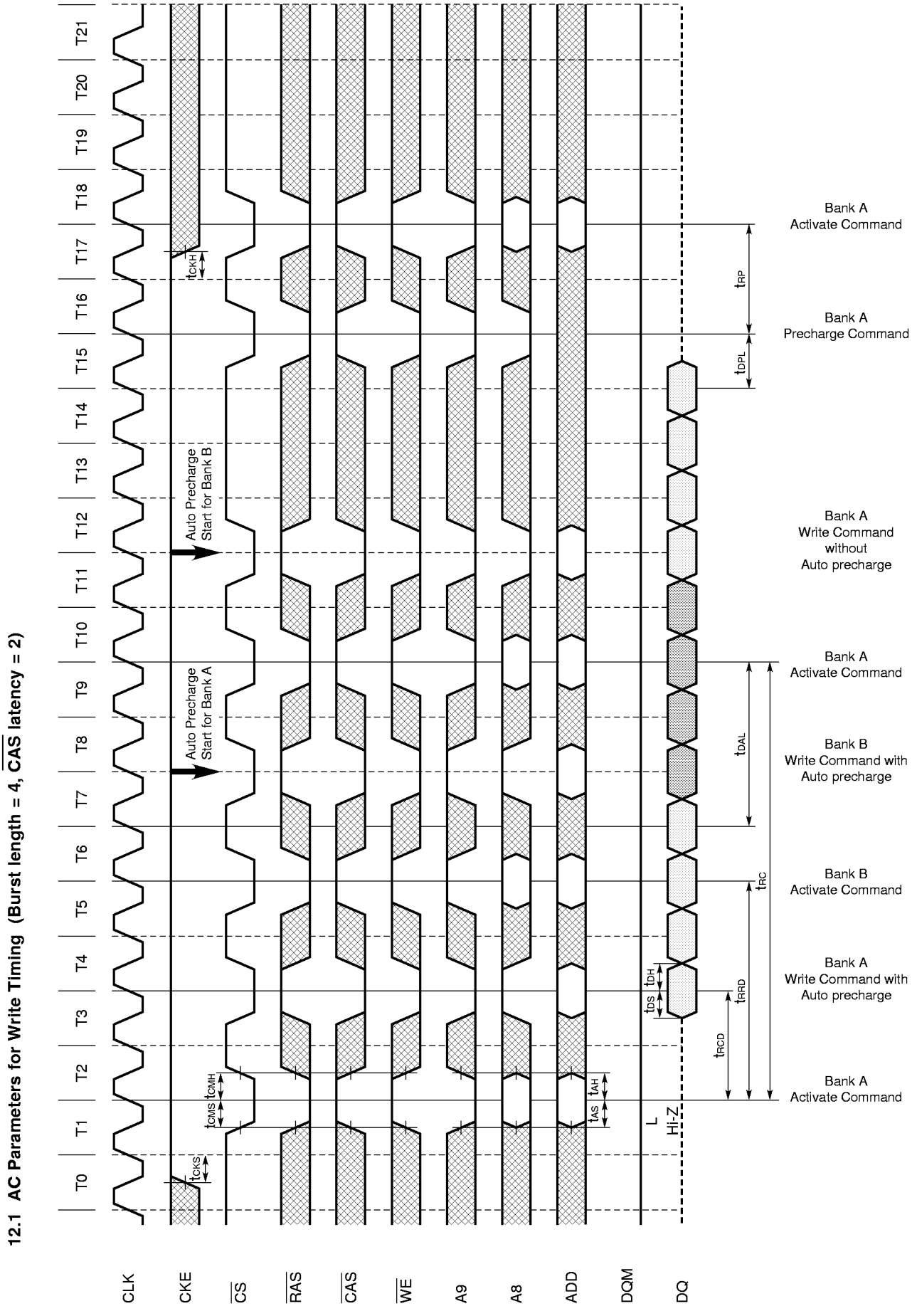
Note 1. Output load



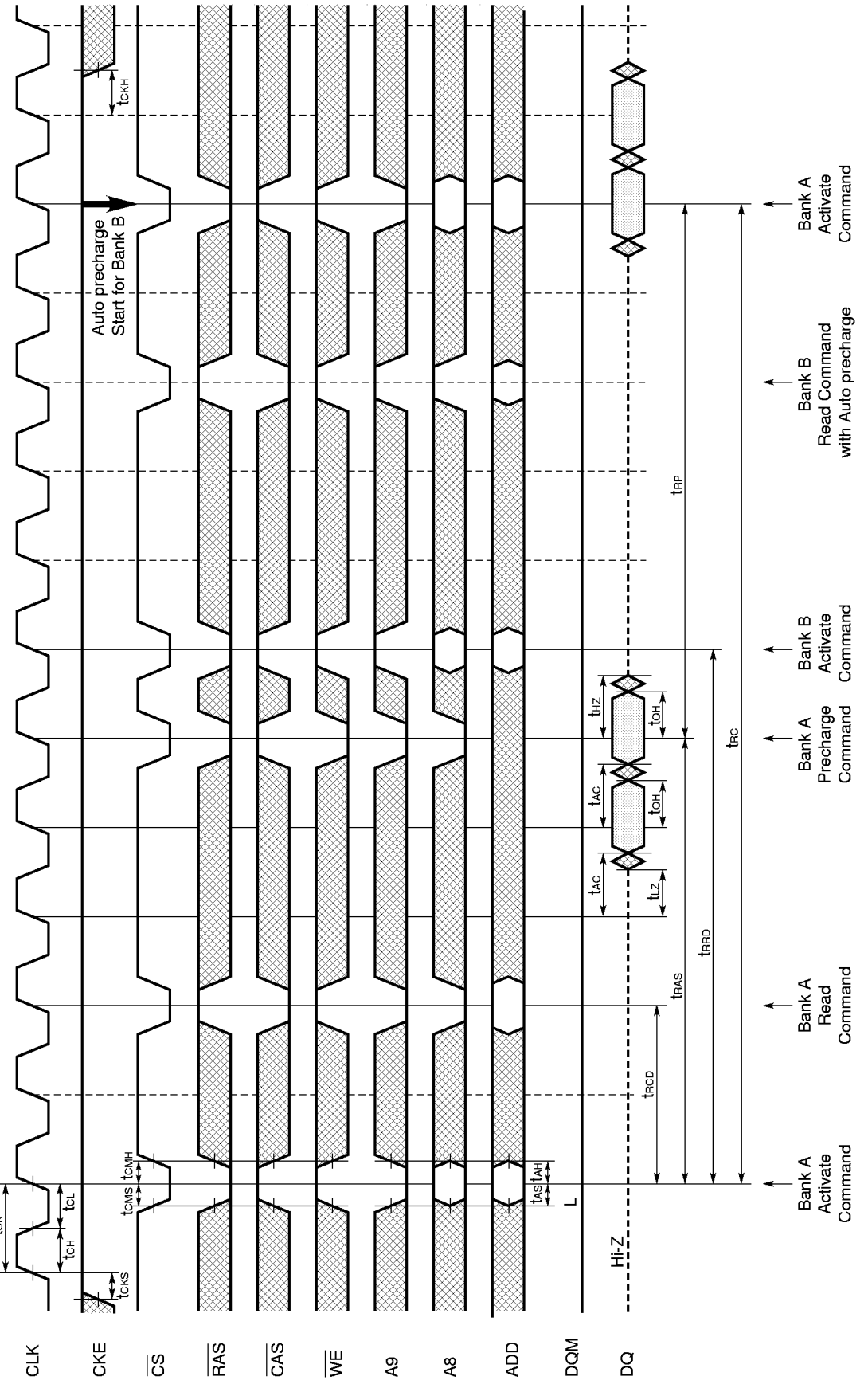
Asynchronous Characteristics

Parameter		Symbol	–10		–12		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
REF to REF/ACT Command period		t_{RC}	100		100		ns	
ACT to PRE Command period		t_{RAS}	60	120,000	70	120,000	ns	
PRE to ACT Command period		t_{RP}	30		30		ns	
Delay time ACT to READ/WRITE Command		t_{RCD}	30		30		ns	
ACT(0) to ACT(1) Command period		t_{RRD}	20		24		ns	
Data-in to PRE Command period		t_{DPL}	10		12		ns	
Data-in to ACT (REF) Command (Auto precharge) period	$\overline{CAS}$ latency = 3	t_{DAL3}	1CLK + 30		1CLK + 30		ns	
	$\overline{CAS}$ latency = 2	t_{DAL2}	1CLK + 30		1CLK + 30		ns	
Mode register set cycle time		t_{RSC}	2		2		CLK	
Transition time		t_T	1	30	1	30	ns	
Refresh time		t_{REF}		8		8	ms	

12.1 AC Parameters for Write Timing (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)



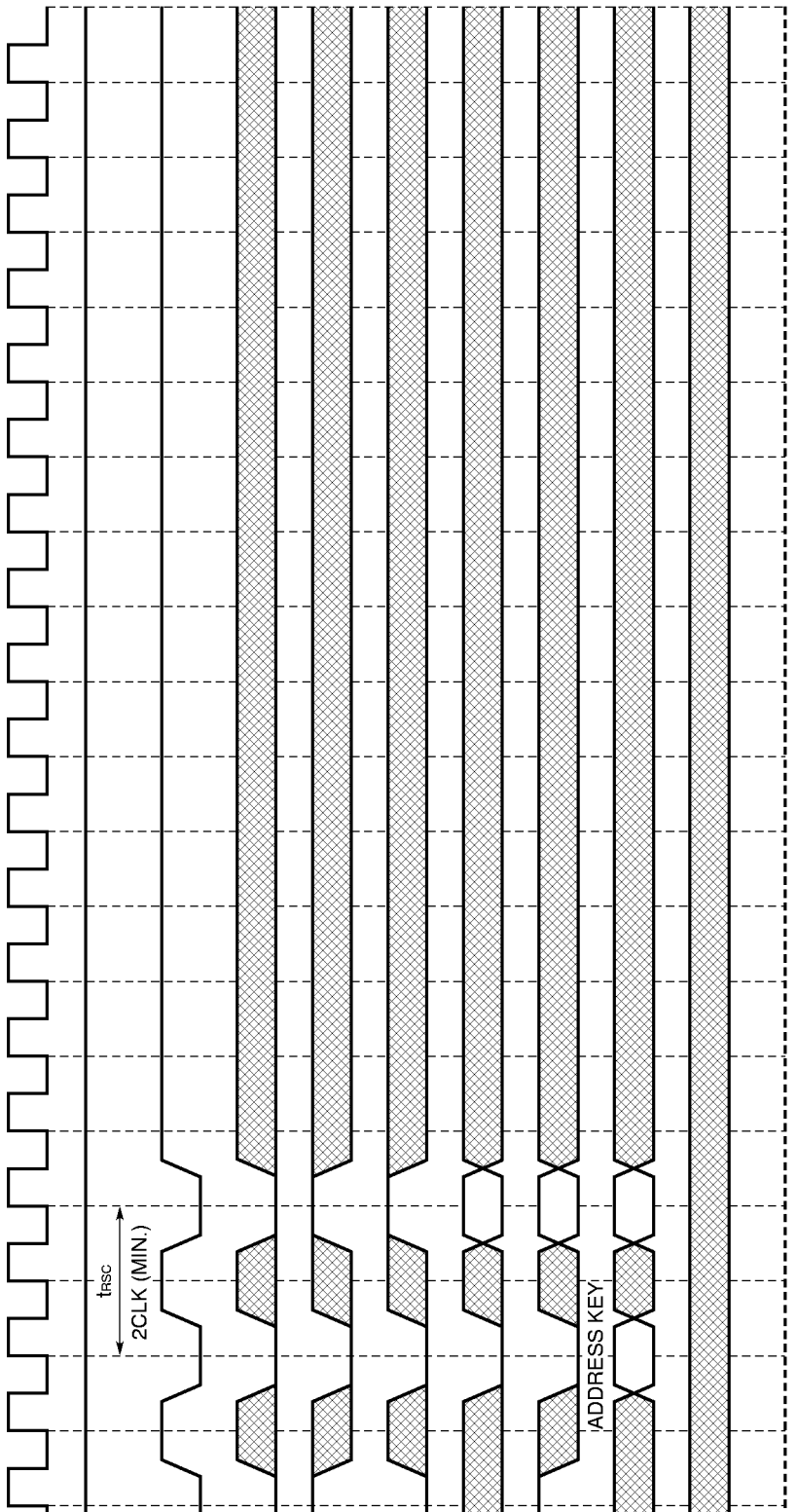
12.2 AC Parameters for Read Timing (Burst length = 2, $\overline{CAS}$ latency = 2)



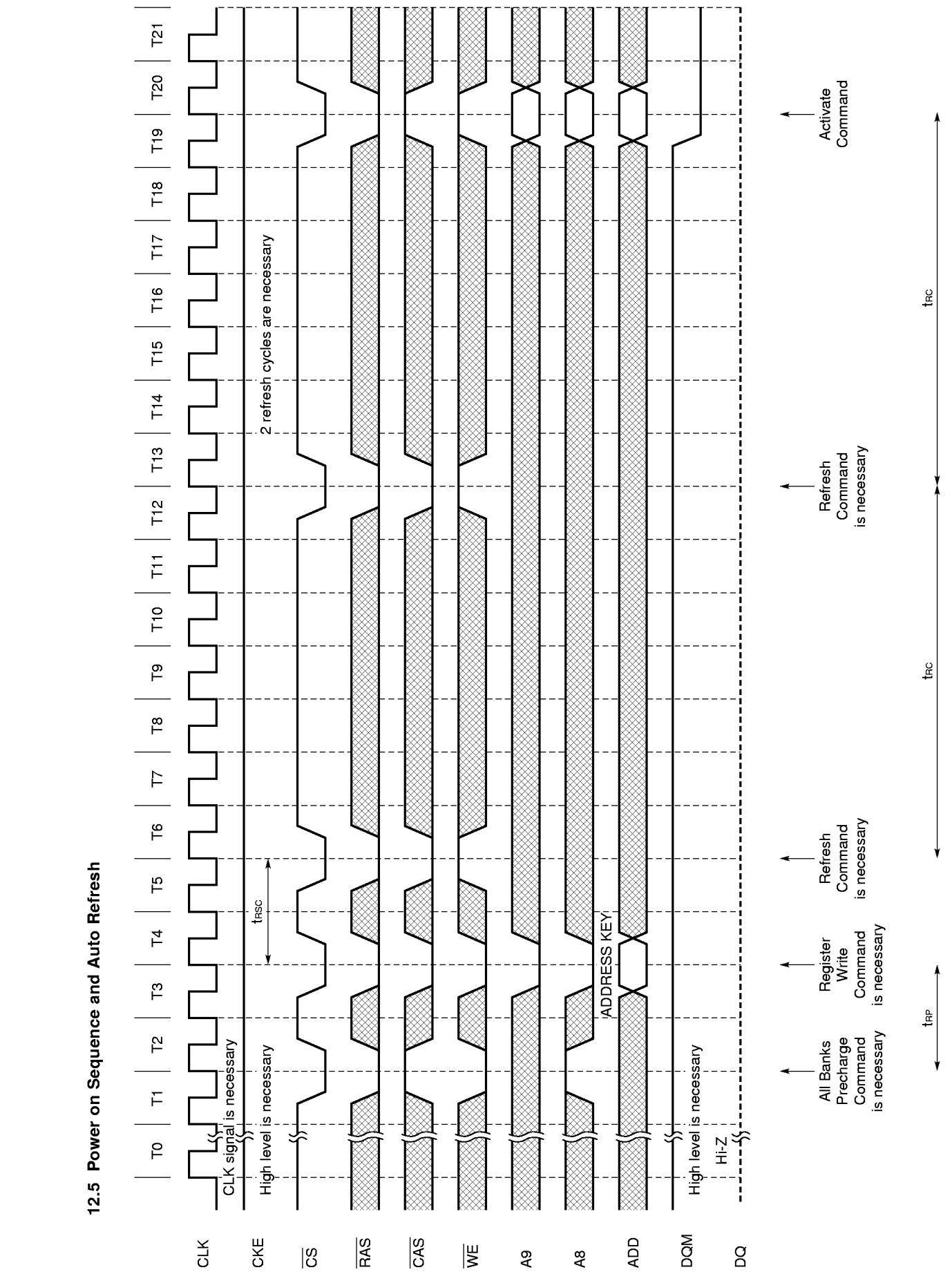
12.3 Relationship between Frequency and Latency

Speed version	–10		–12	
Clock cycle time [ns]	10	15	12	15
Frequency [MHz]	100	67	83	67
$\overline{\text{CAS}}$ latency	3	2	3	2
[t_{RCD}]	3	2	3	2
$\overline{\text{RAS}}$ latency ($\overline{\text{CAS}}$ latency + [t_{RCD}])	6	4	6	4
[t_{RC}]	10	7	9	7
[t_{RAS}]	6	4	6	5
[t_{RRD}]	2	2	2	2
[t_{RP}]	3	2	3	2
[t_{DPL}]	1	1	1	1
[t_{DAL}]	4	3	4	3
[t_{RSC}]	2	2	2	2

12.4 Mode Register Write (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)

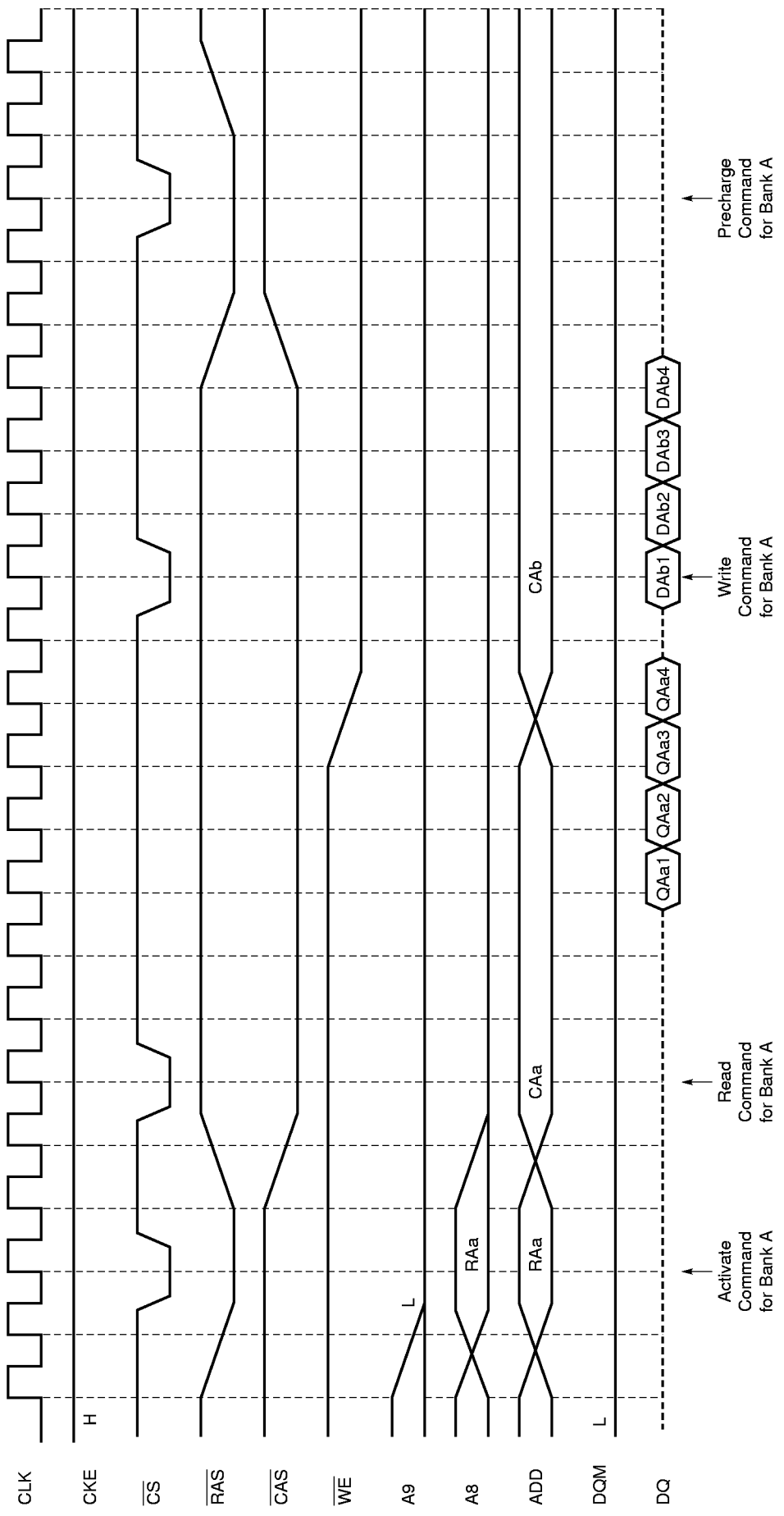


12.5 Power on Sequence and Auto Refresh

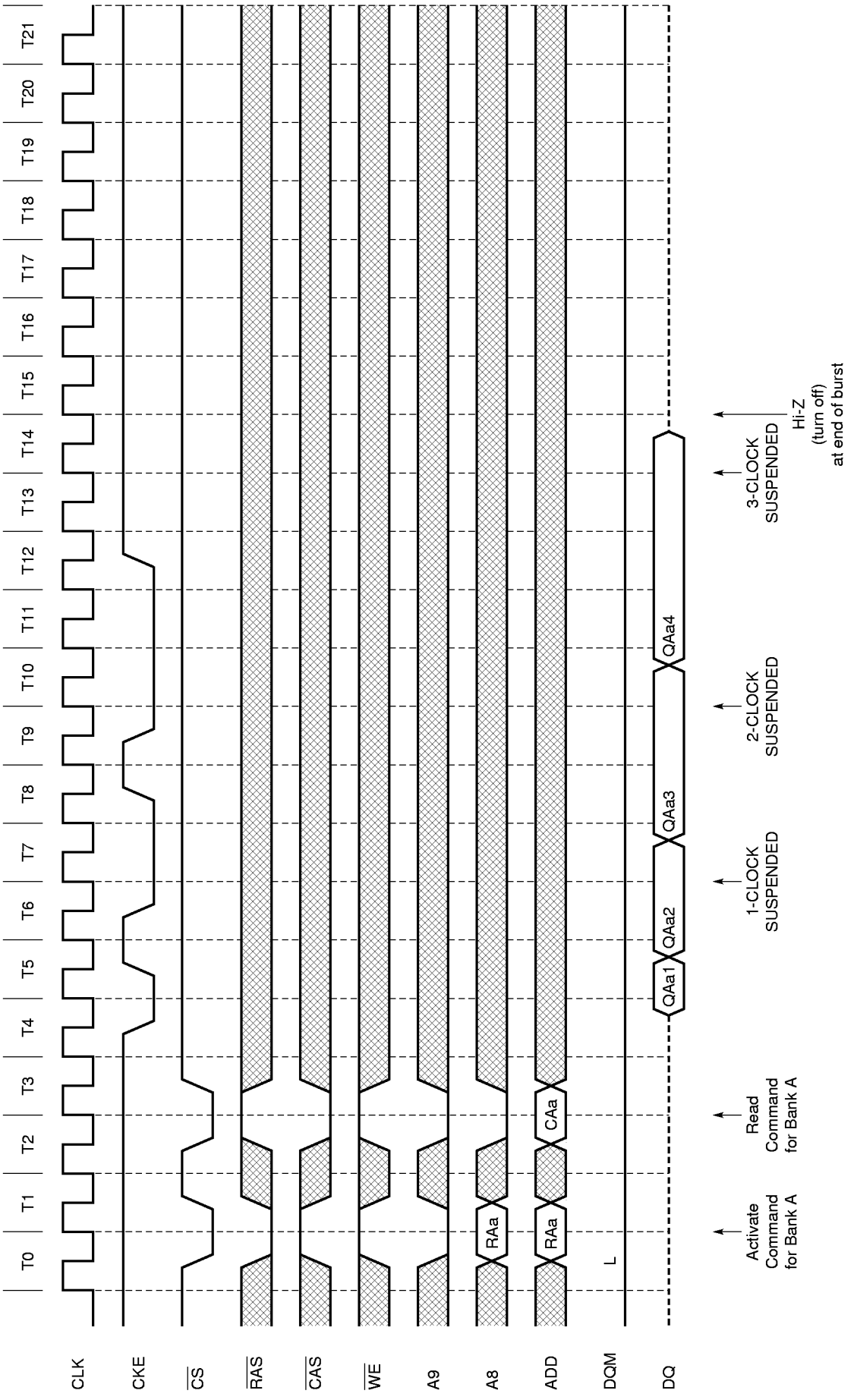


12.6 $\overline{CS}$ Function (at 100 MHz, Burst length = 4, $\overline{CAS}$ latency = 3)

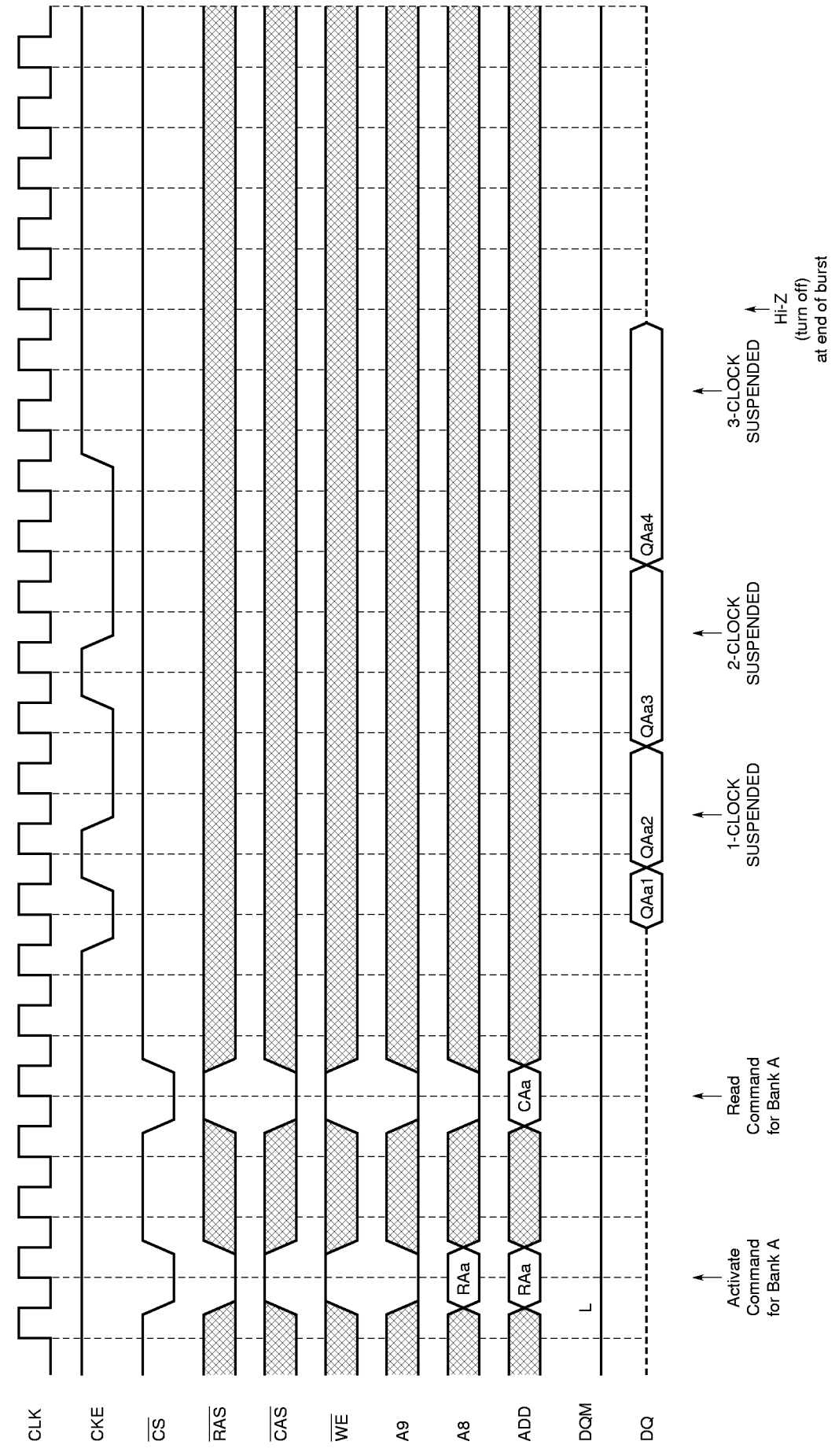
Only $\overline{CS}$ signal needs to be issued at minimum rate



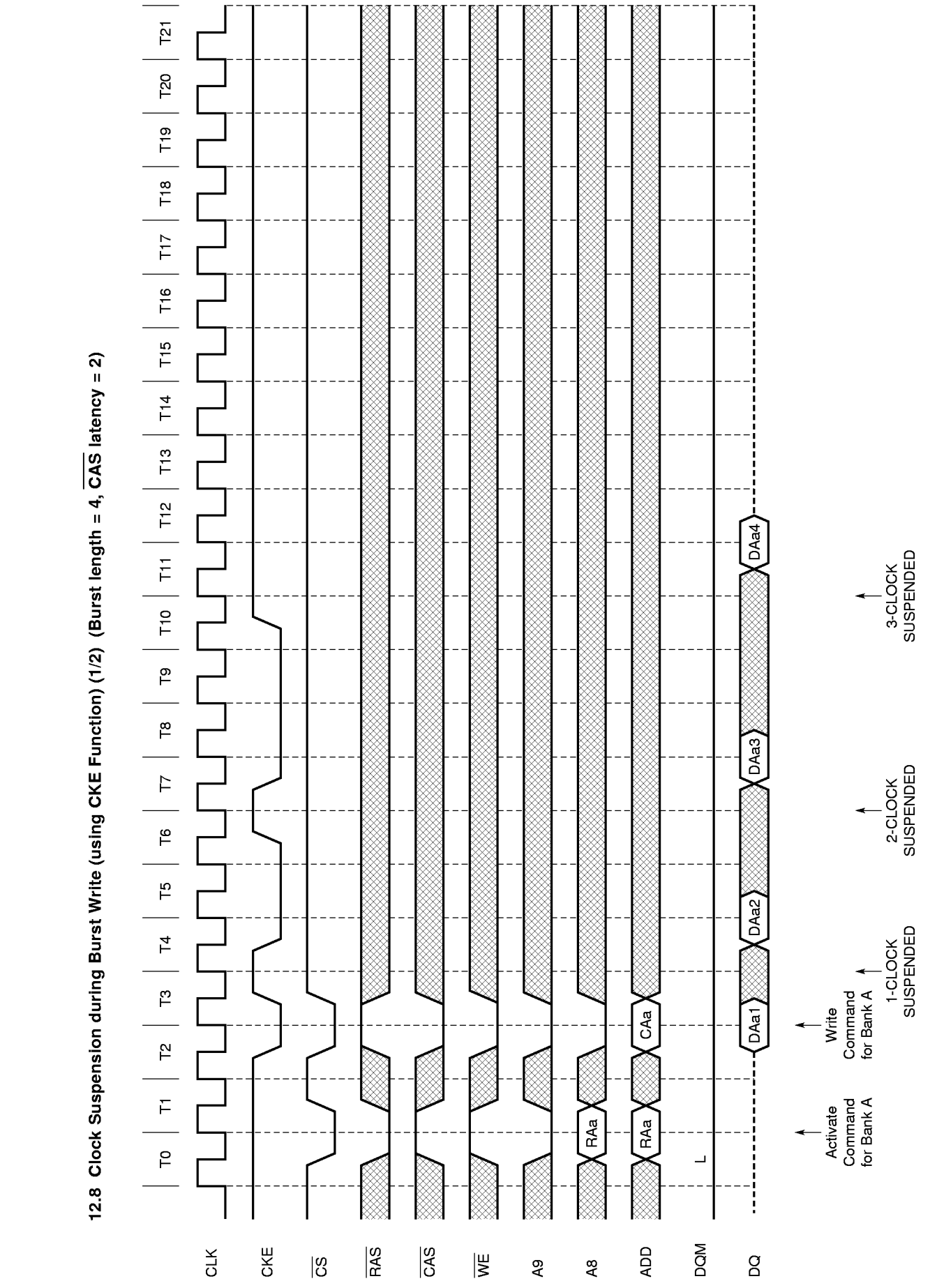
12.7 Clock Suspension during Burst Read (using CKE Function) (1/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)



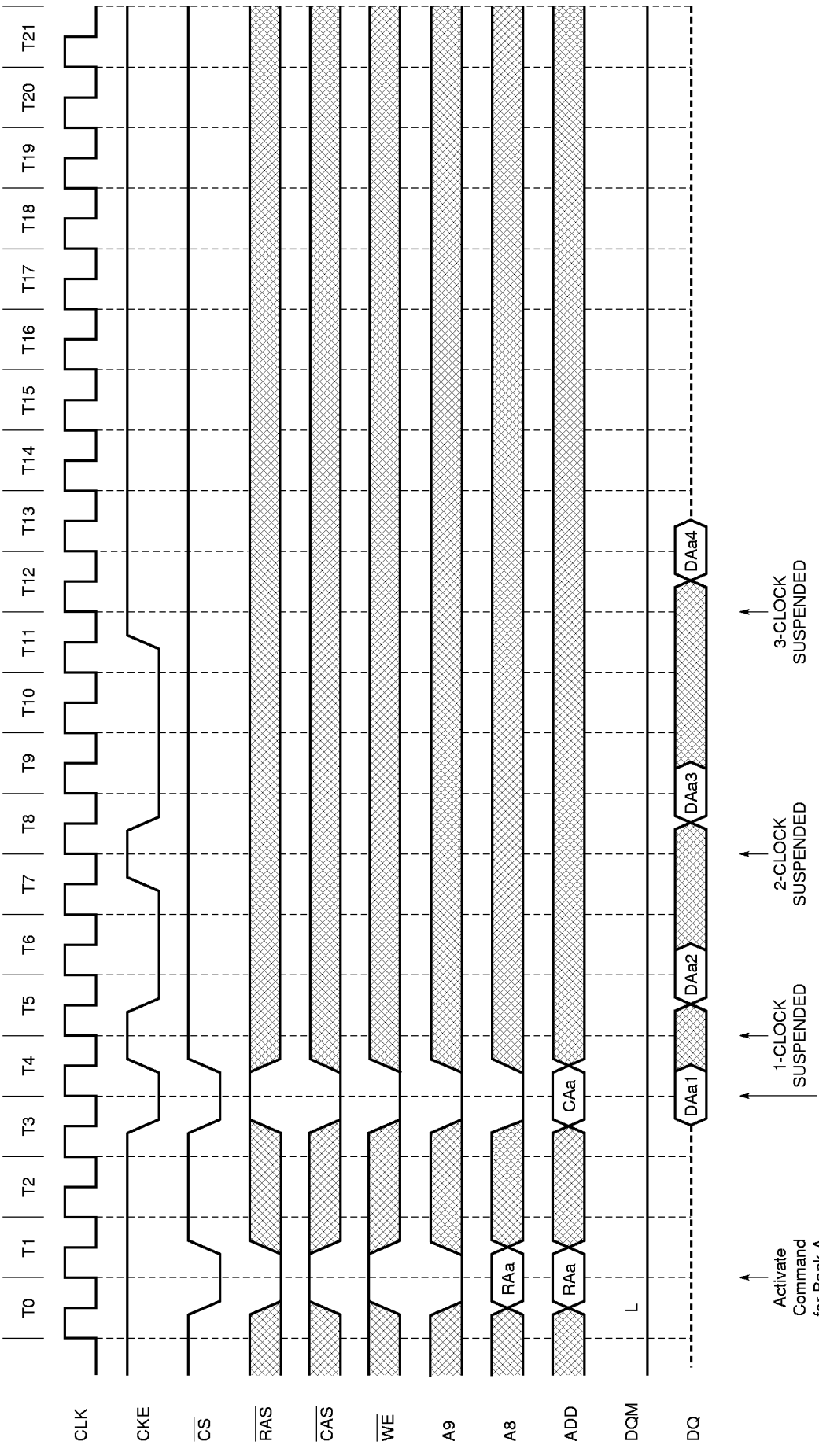
Clock Suspension during Burst Read (using CKE Function) (2/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 3)



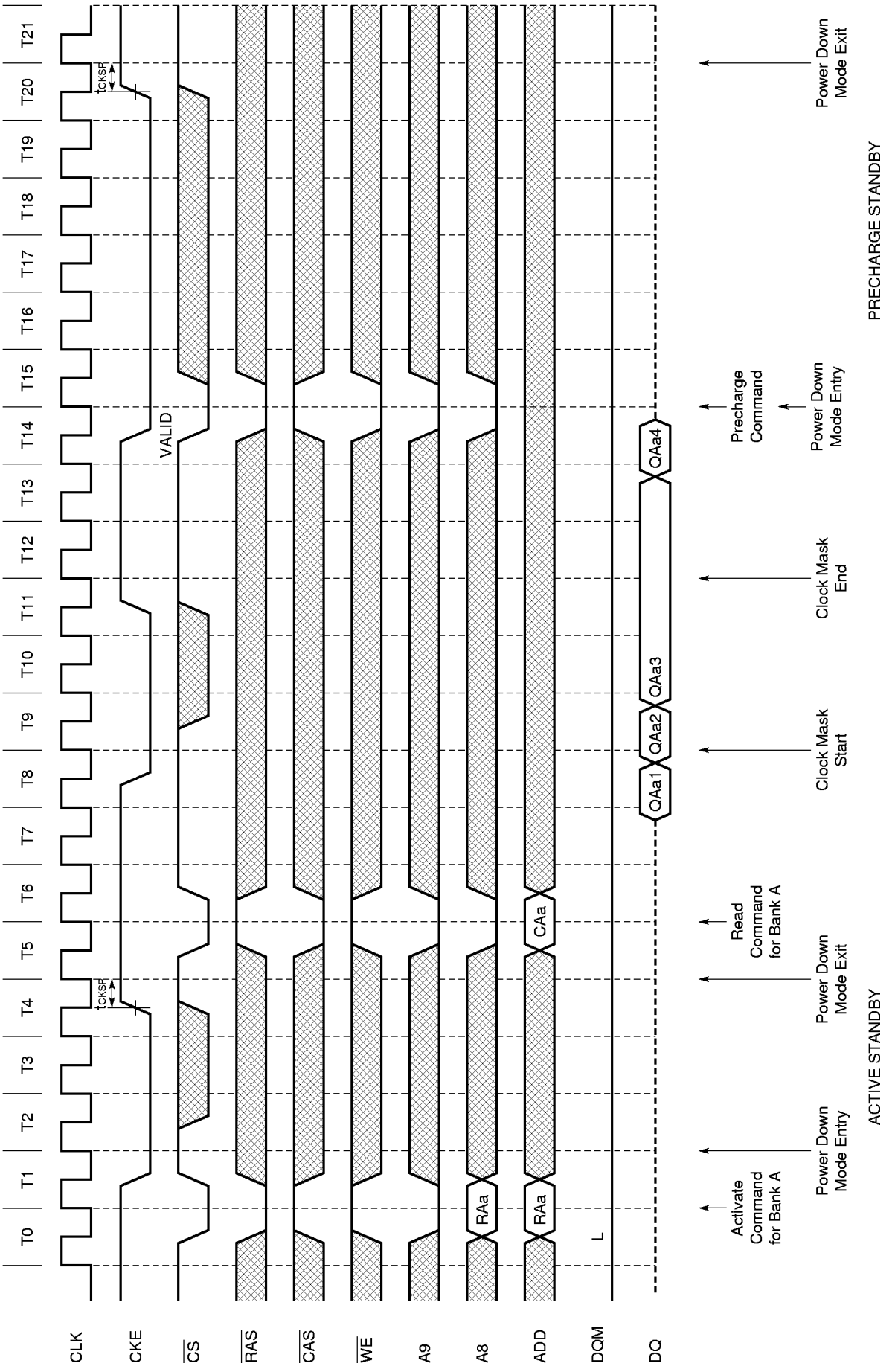
12.8 Clock Suspension during Burst Write (using CKE Function) (1/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)



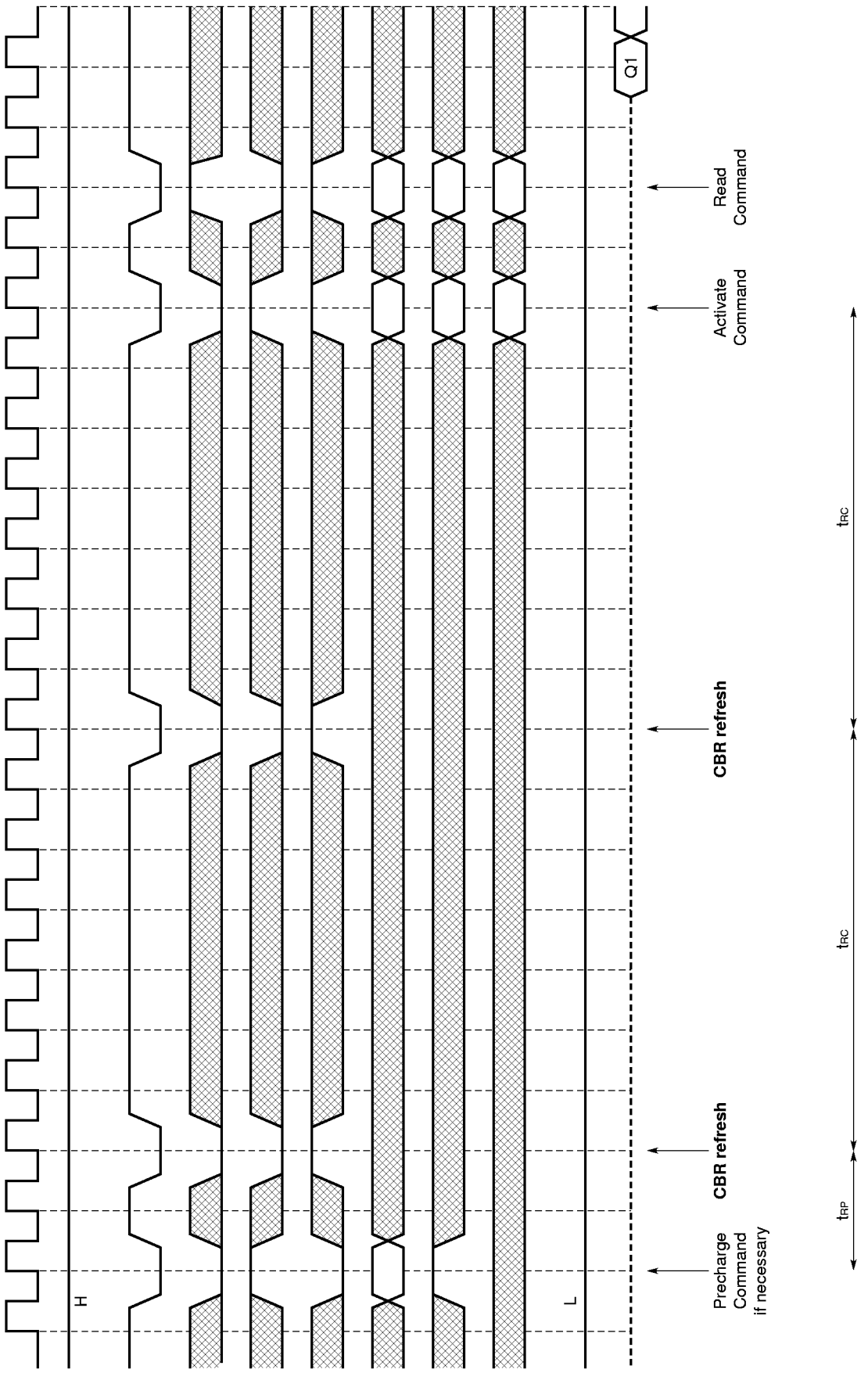
Clock Suspension during Burst Write (using CKE Function) (2/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 3)



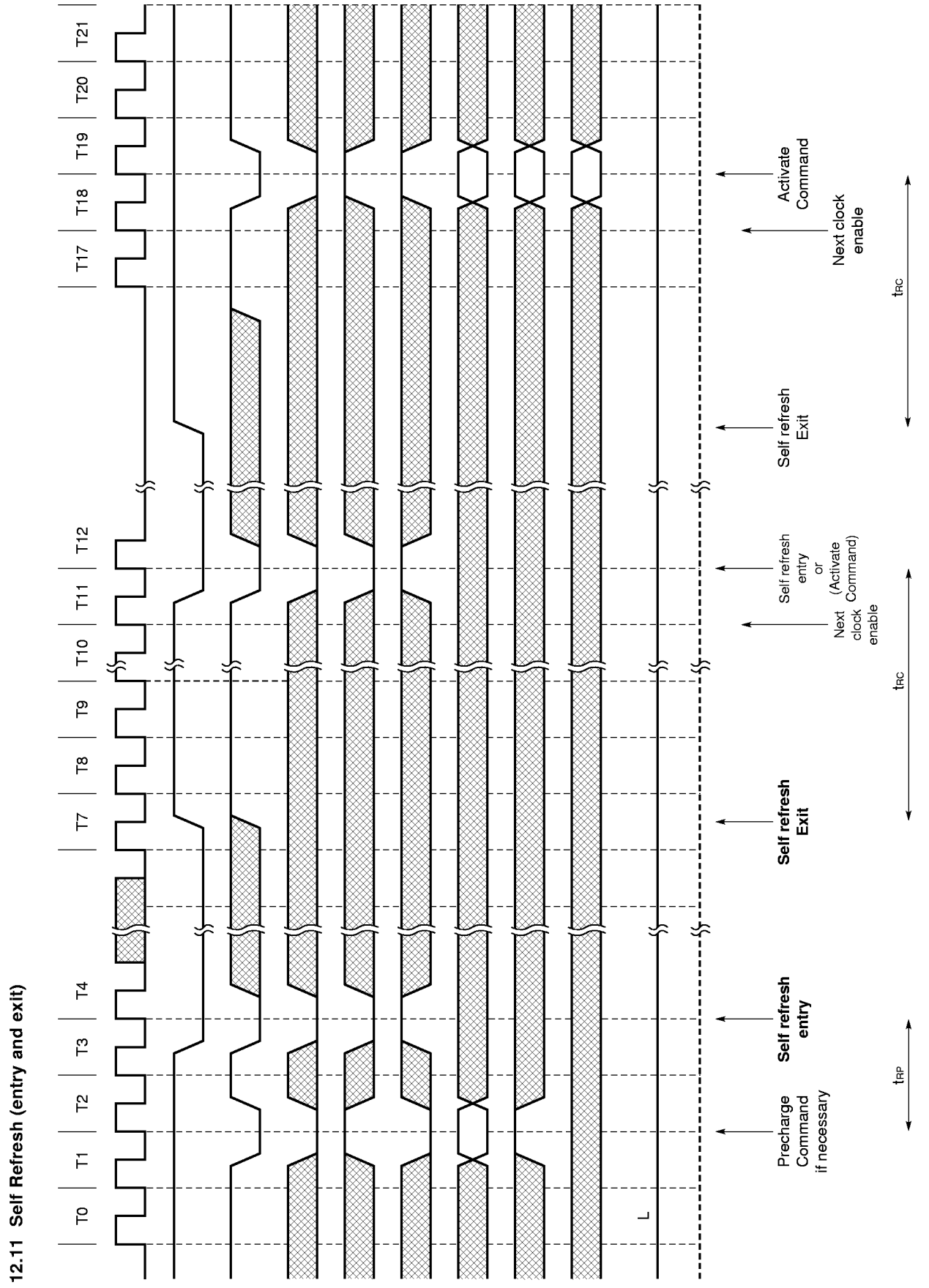
12.9 Power Down Mode and Clock Mask (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)



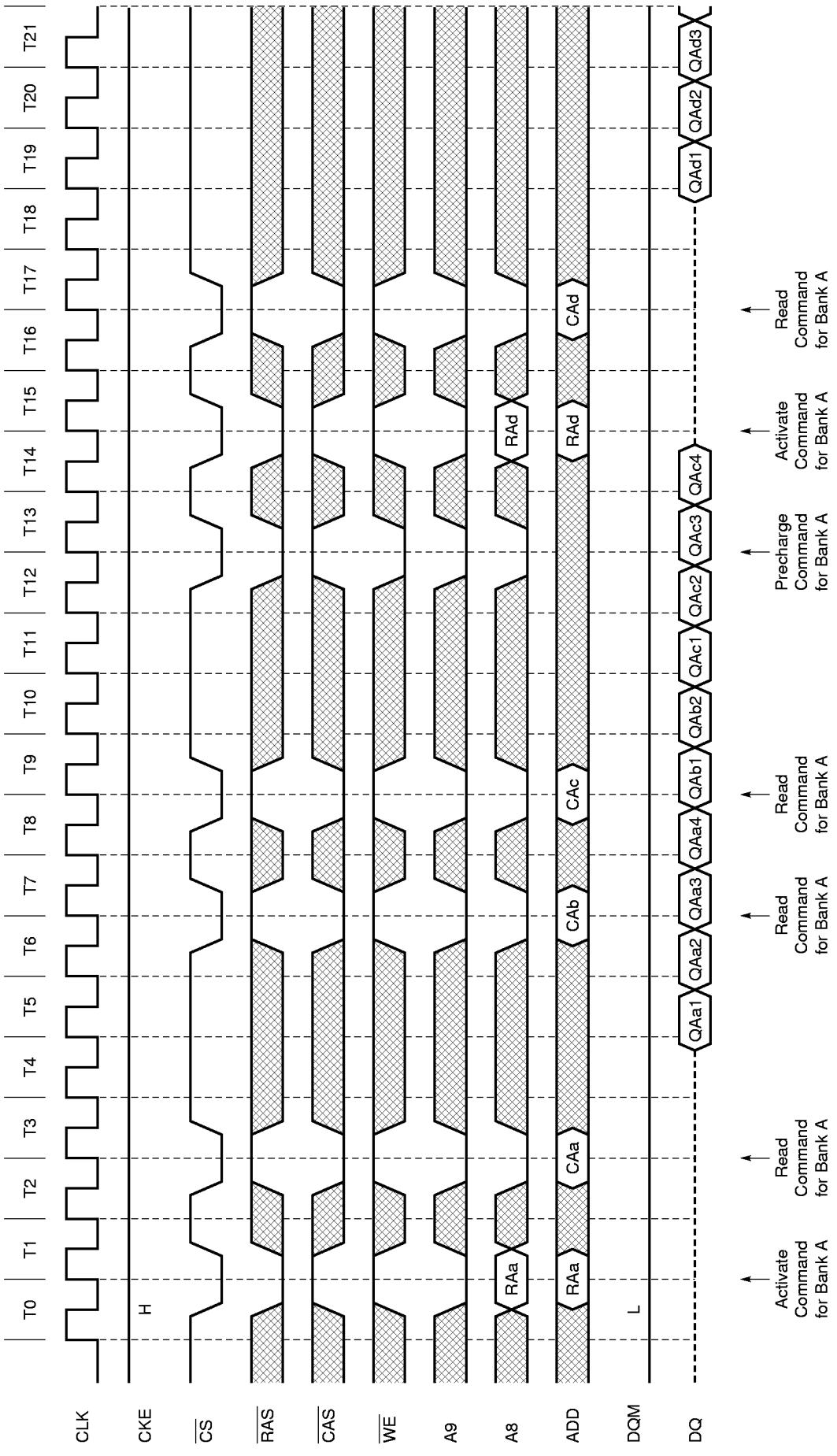
12.10 CBR Refresh



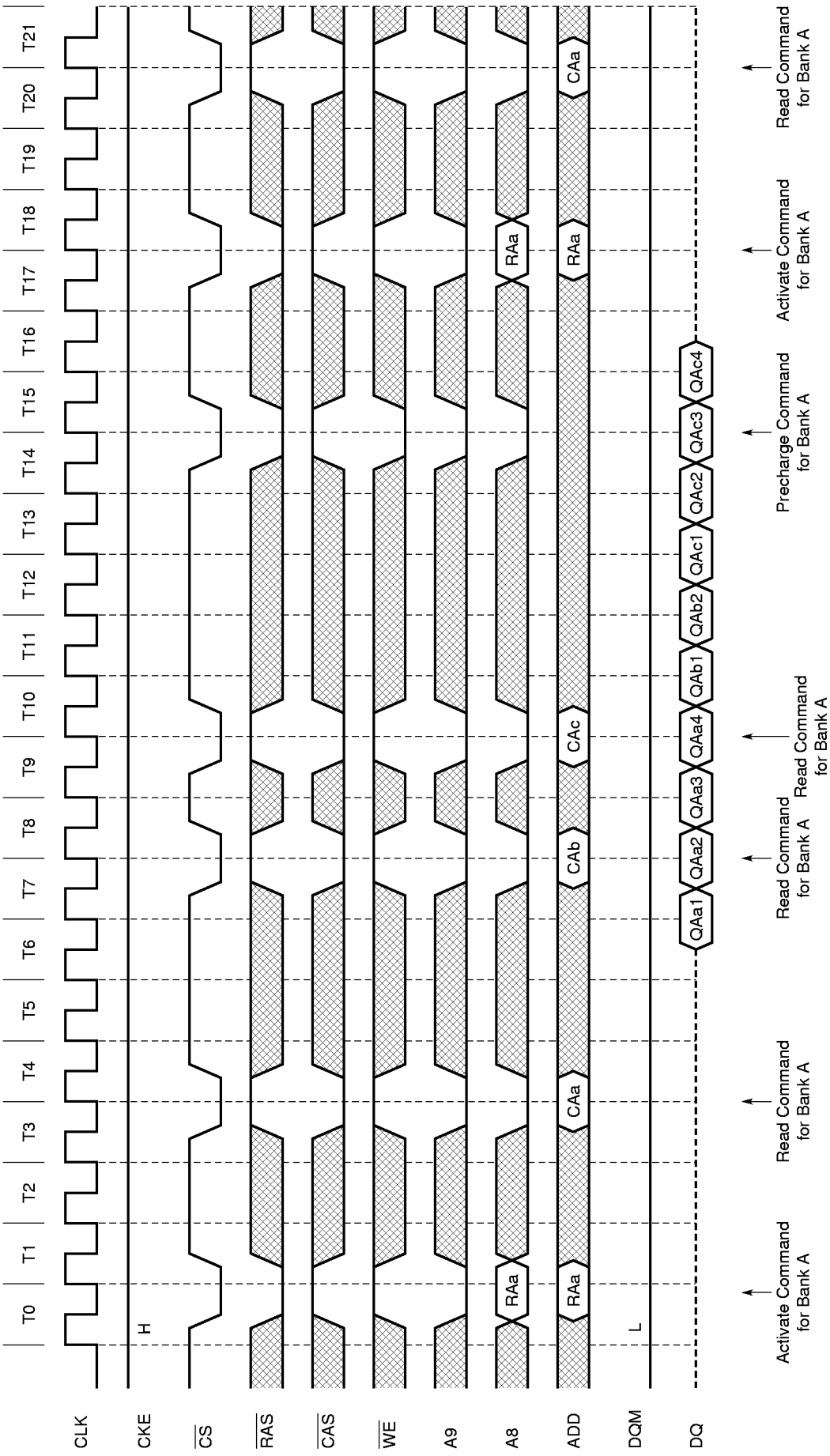
12.11 Self Refresh (entry and exit)



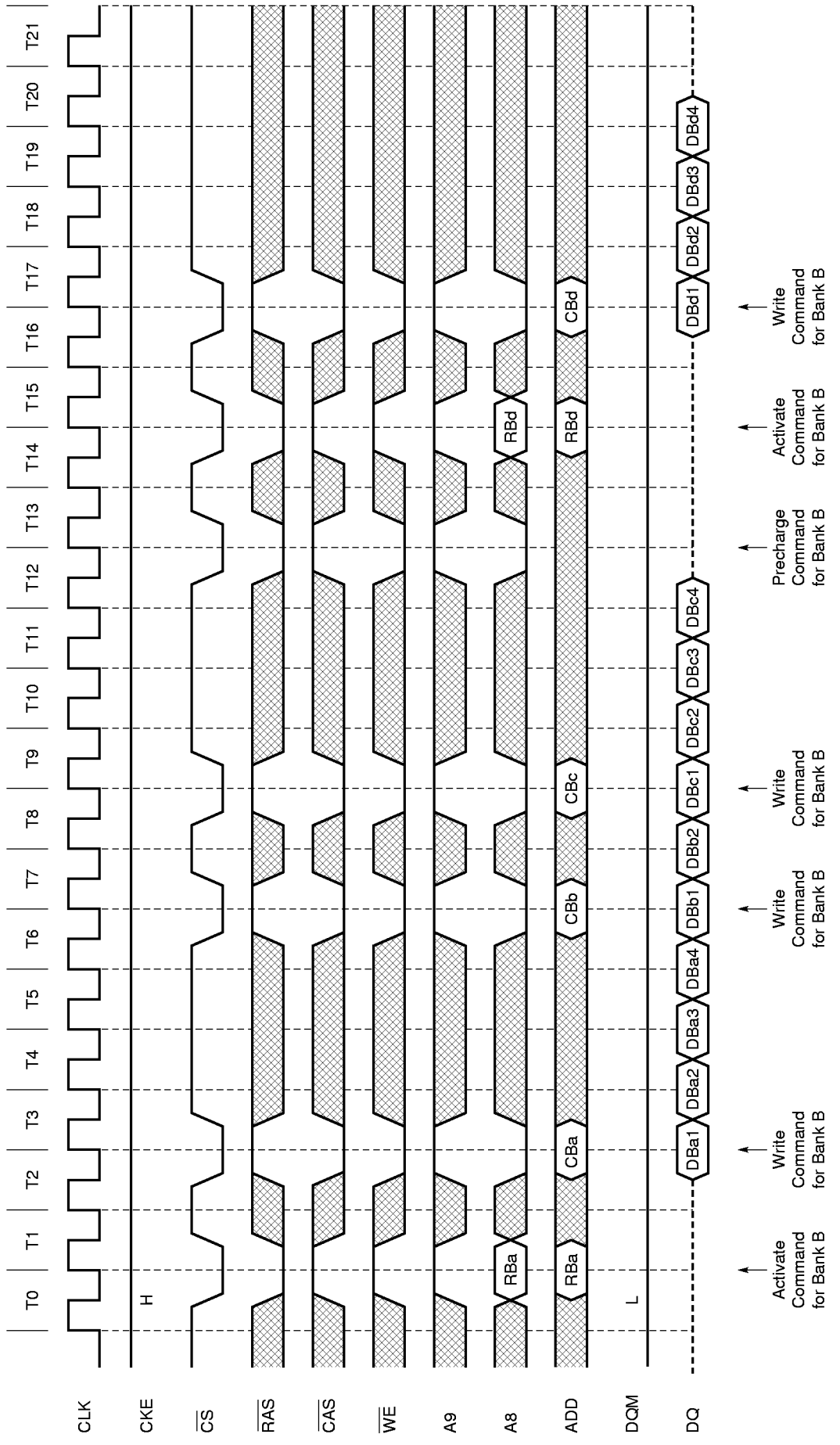
12.12 Random Column Read (Page with same bank) (1/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)



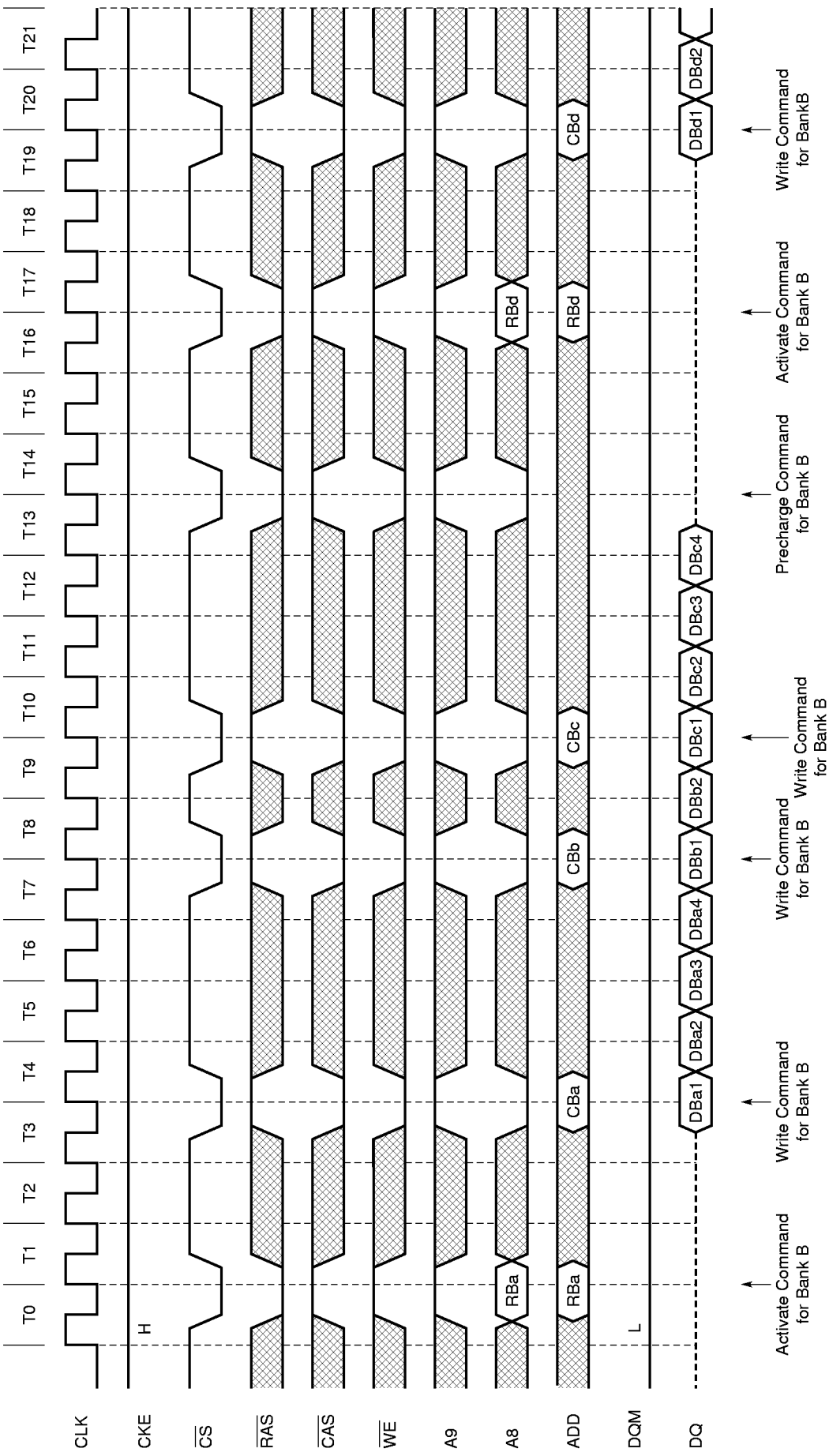
Random Column Read (Page with same bank) (2/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 3)



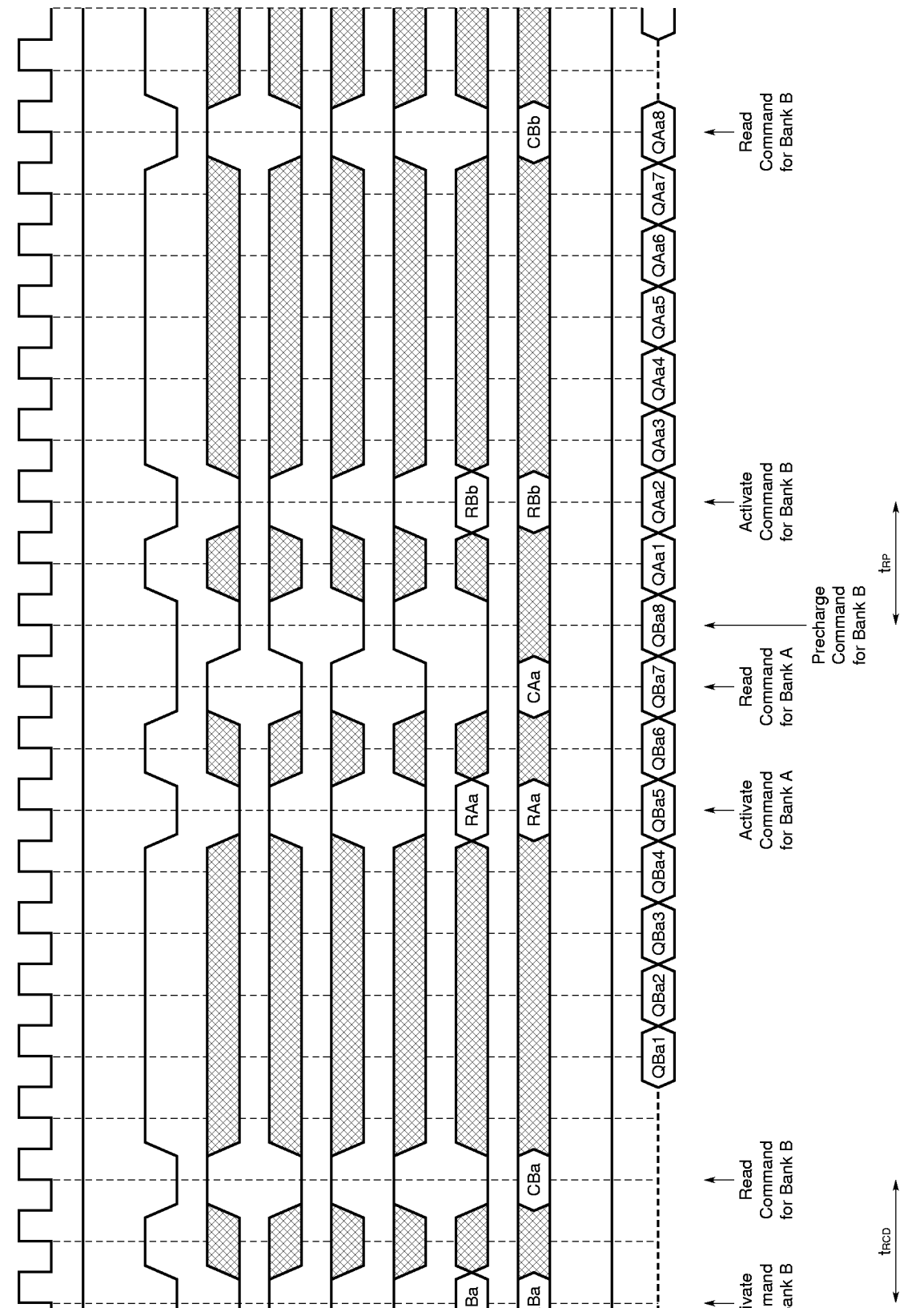
12.13 Random Column Write (Page with same bank) (1/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)



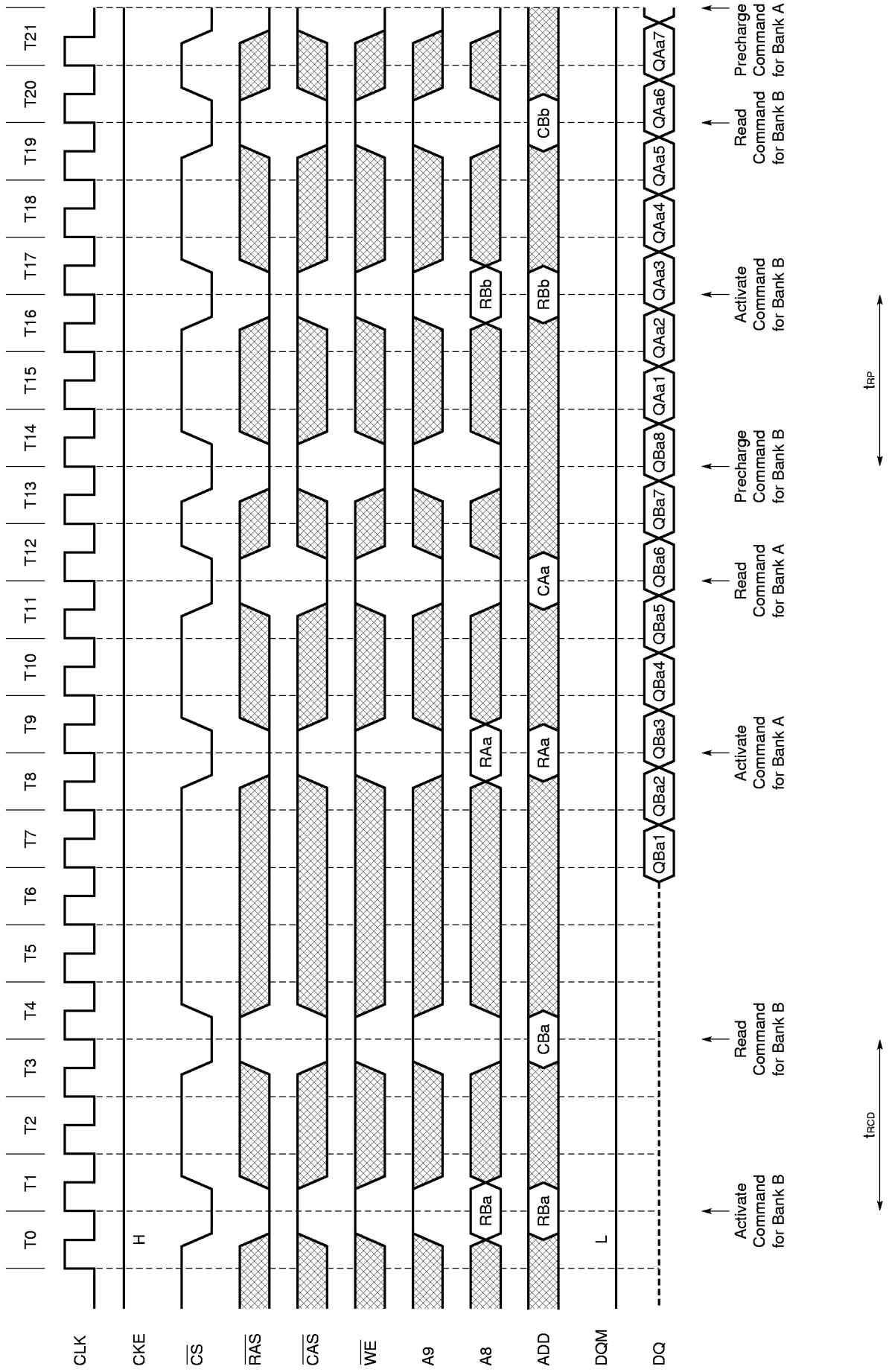
Random Column Write (Page with same bank) (2/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 3)



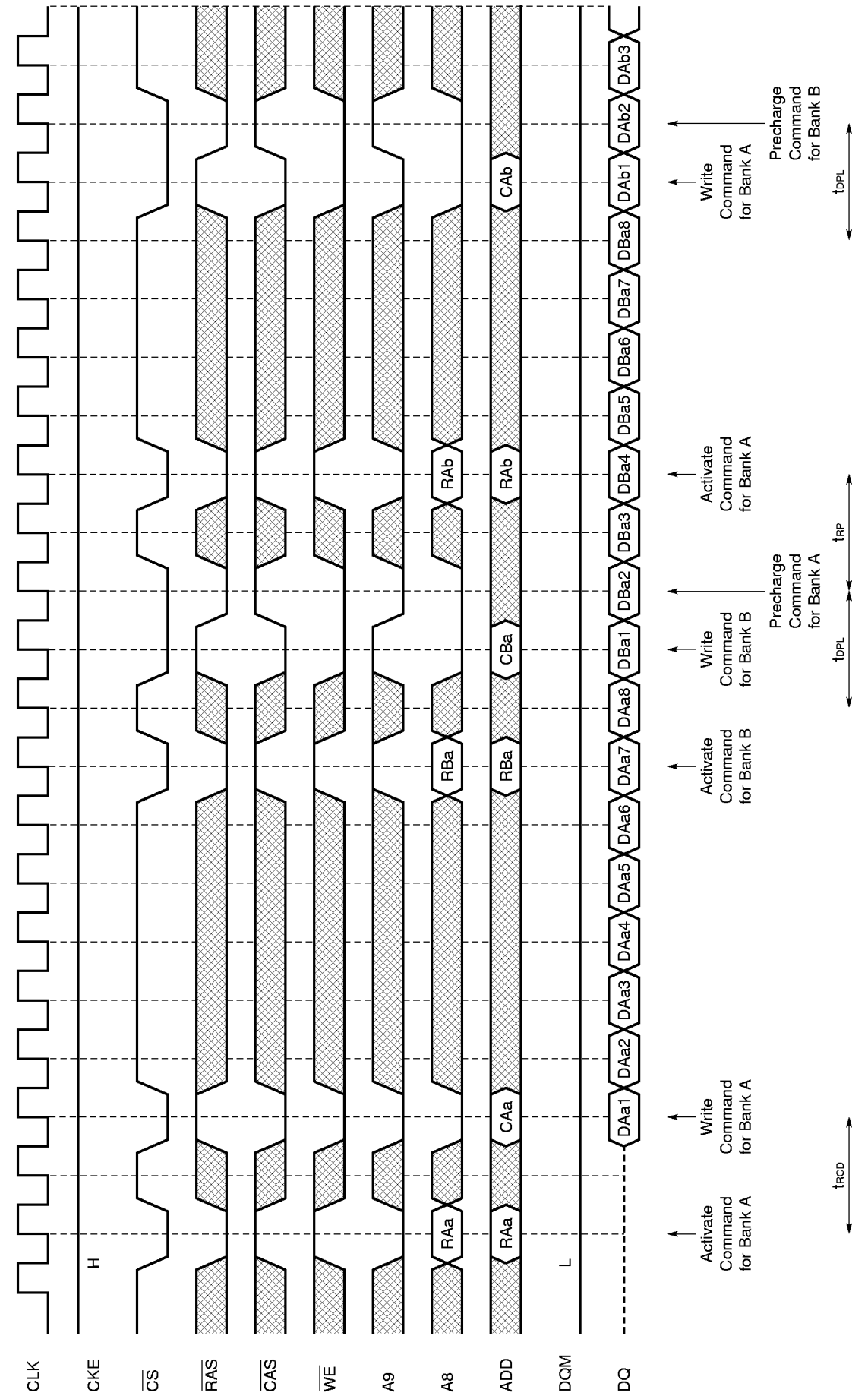
12.14 Random Row READ (Pingpong banks) (1/2) (Burst length = 8, $\overline{\text{CAS}}$ latency = 2)



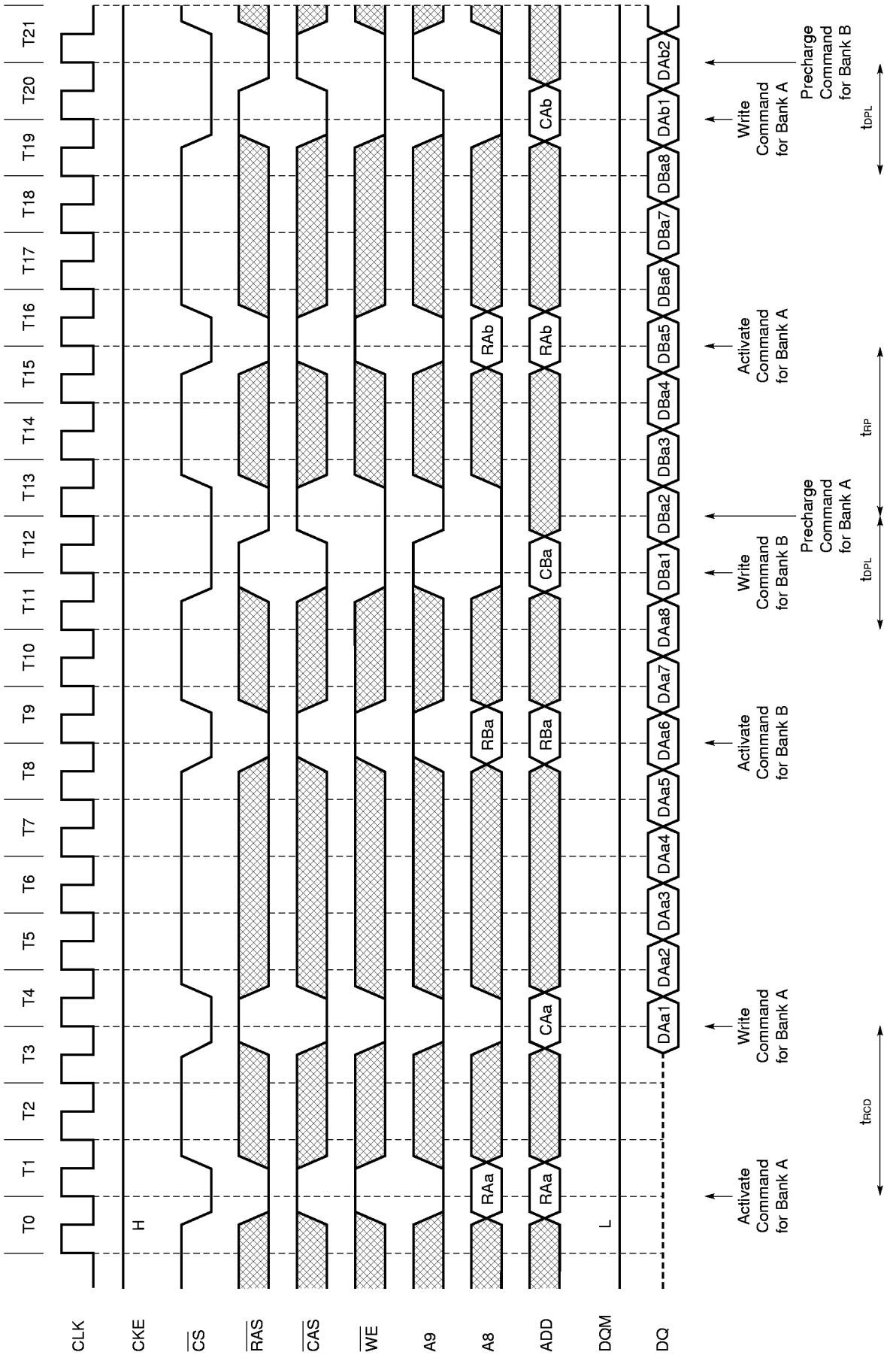
Random Row READ (Pingpong banks) (2/2) (Burst length = 8, $\overline{\text{CAS}}$ latency = 3)



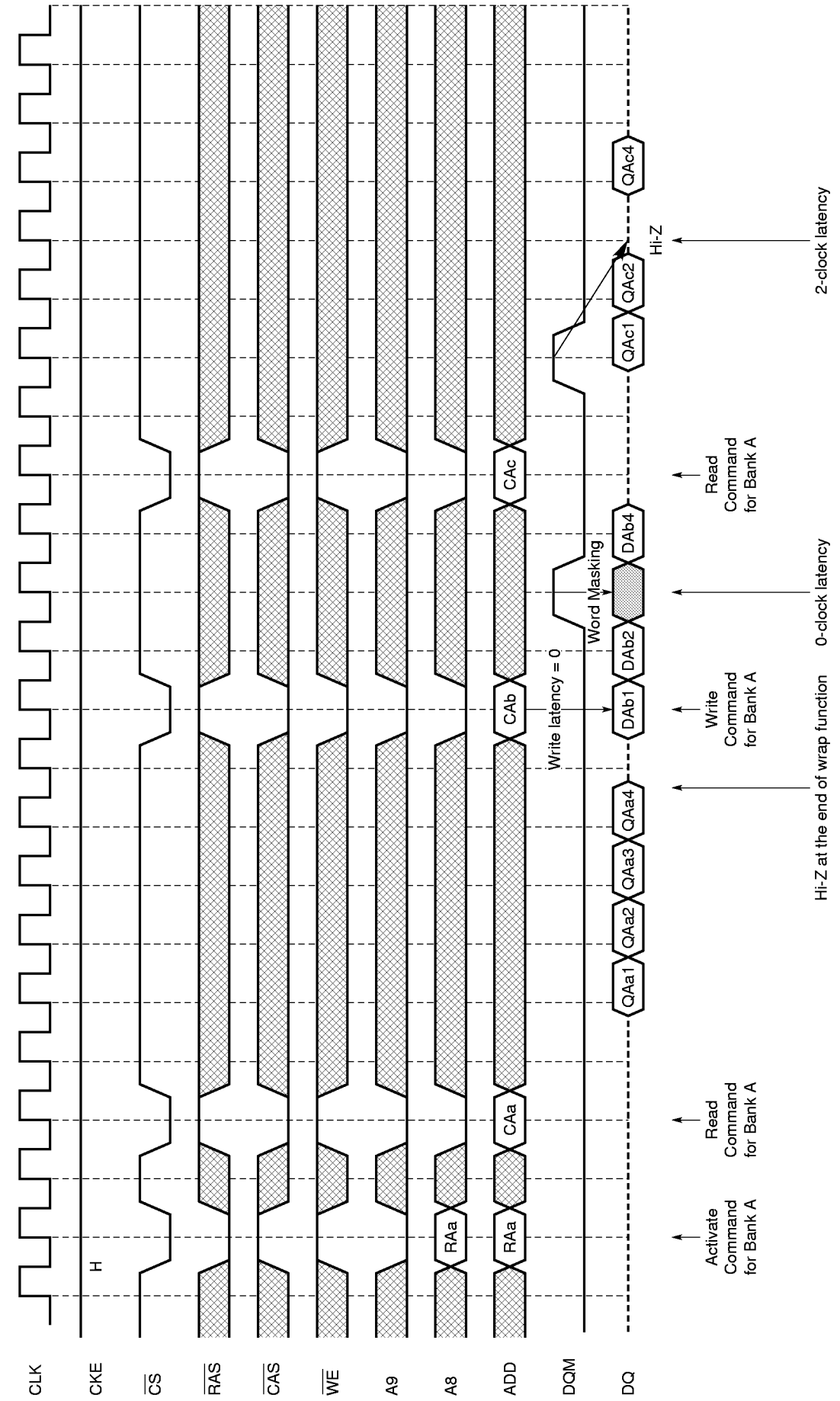
12.15 Random Row Write (Pingpong banks) (1/2) (Burst length = 8, $\overline{\text{CAS}}$ latency = 2)



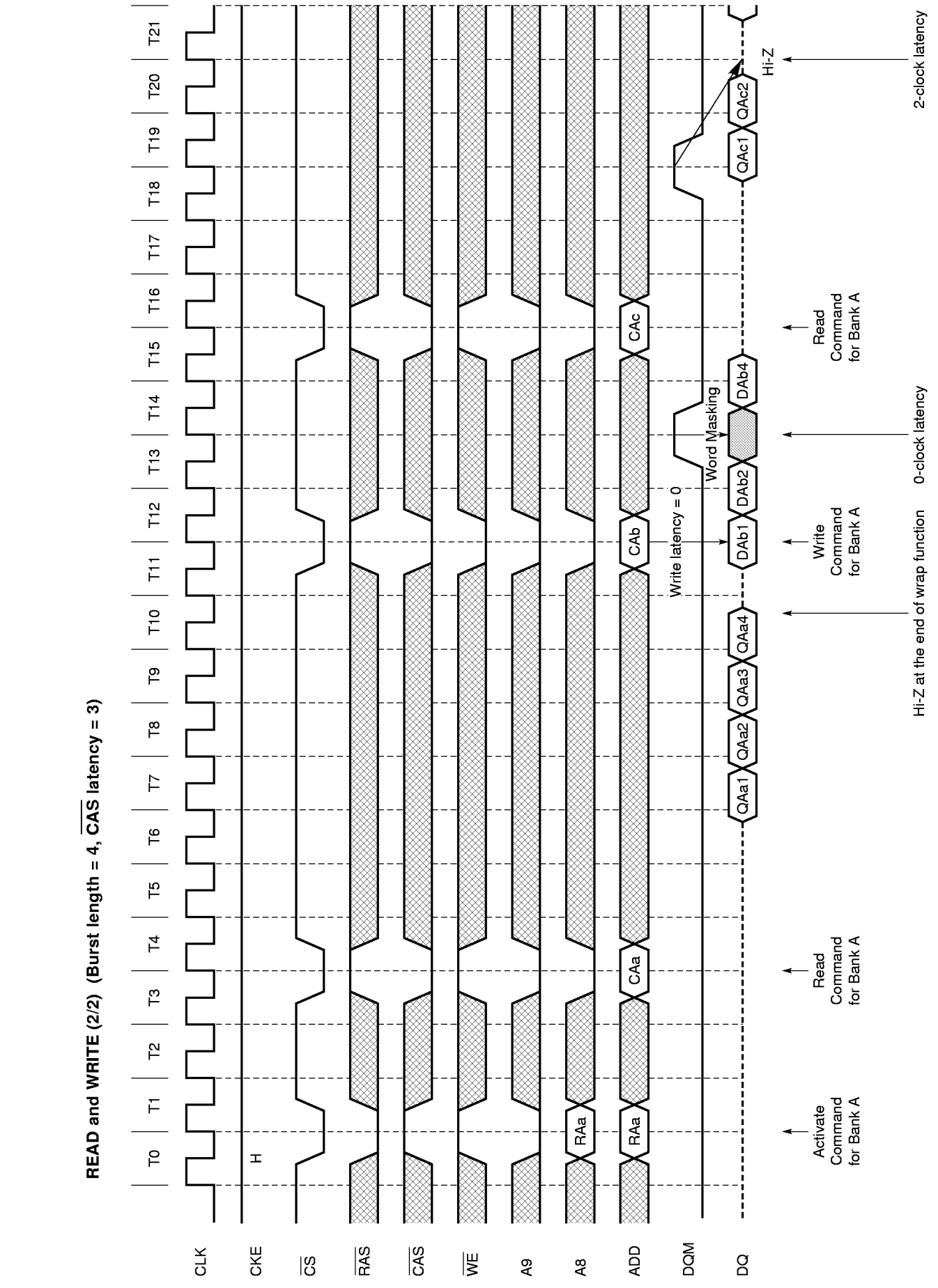
Random Row Write (Pingpong banks) (2/2) (Burst length = 8, $\overline{\text{CAS}}$ latency = 3)



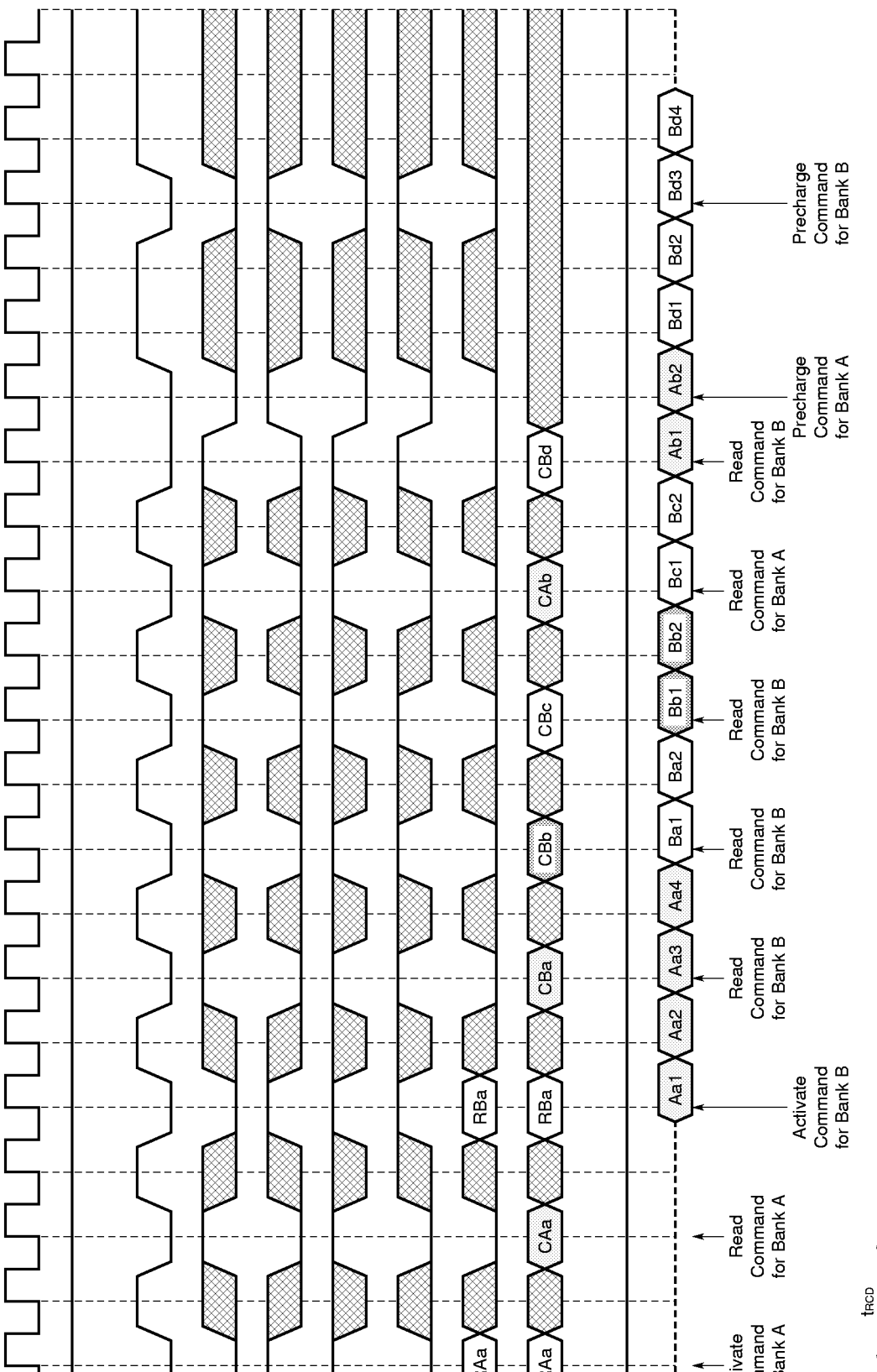
12.16 READ and WRITE (1/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)



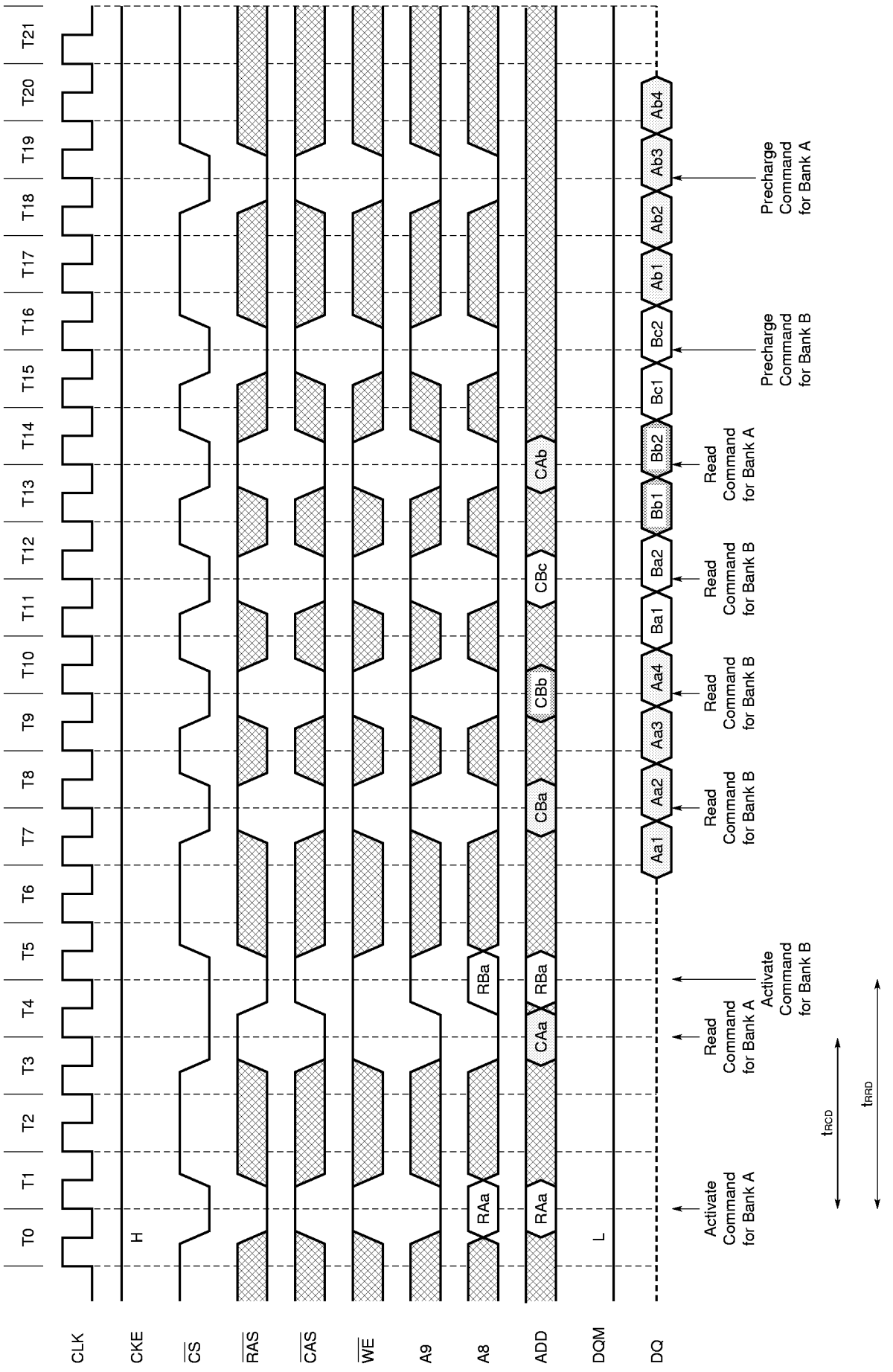
READ and WRITE (2/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 3)



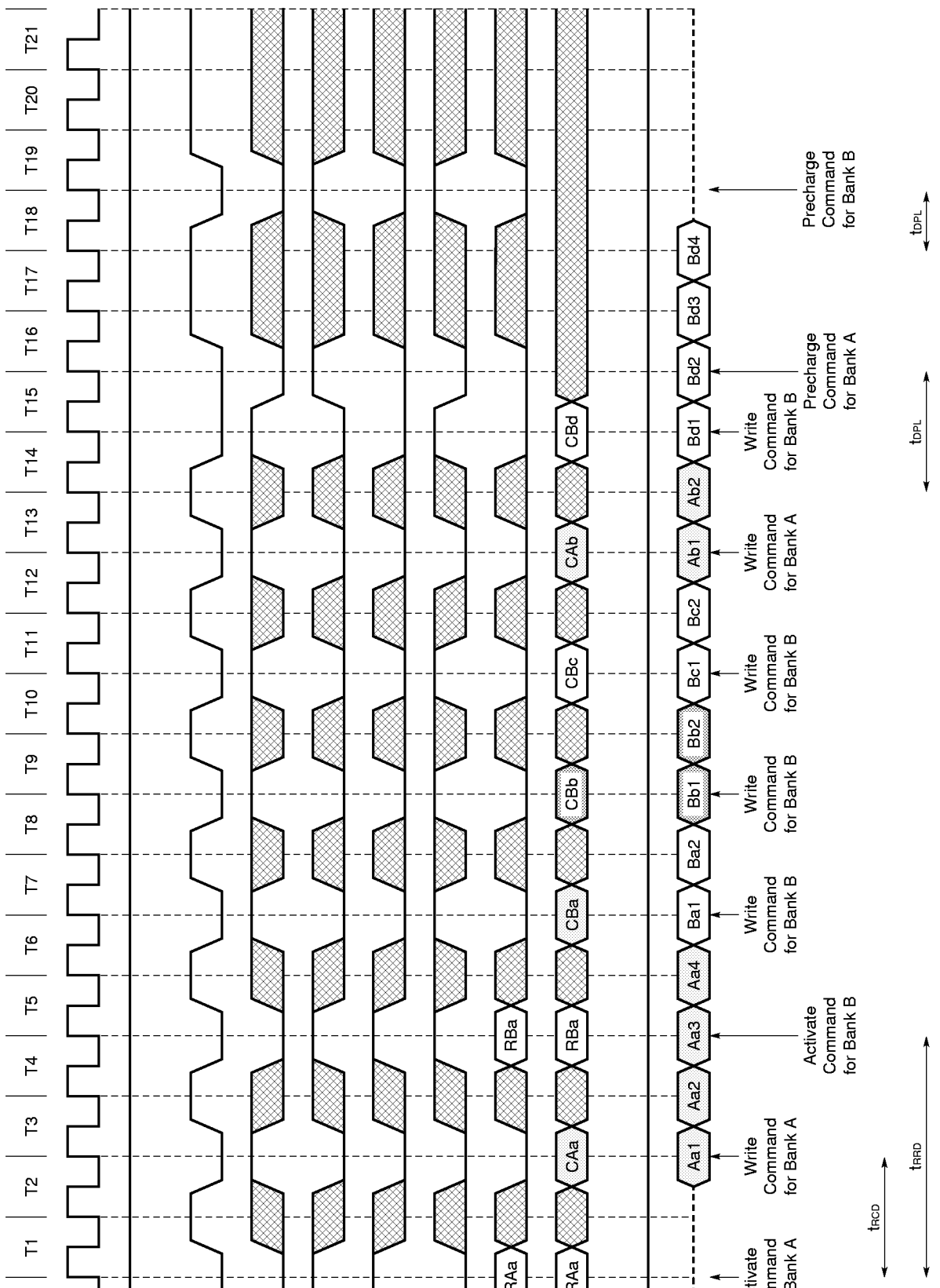
12.17 Interleaved Column READ Cycle (1/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)



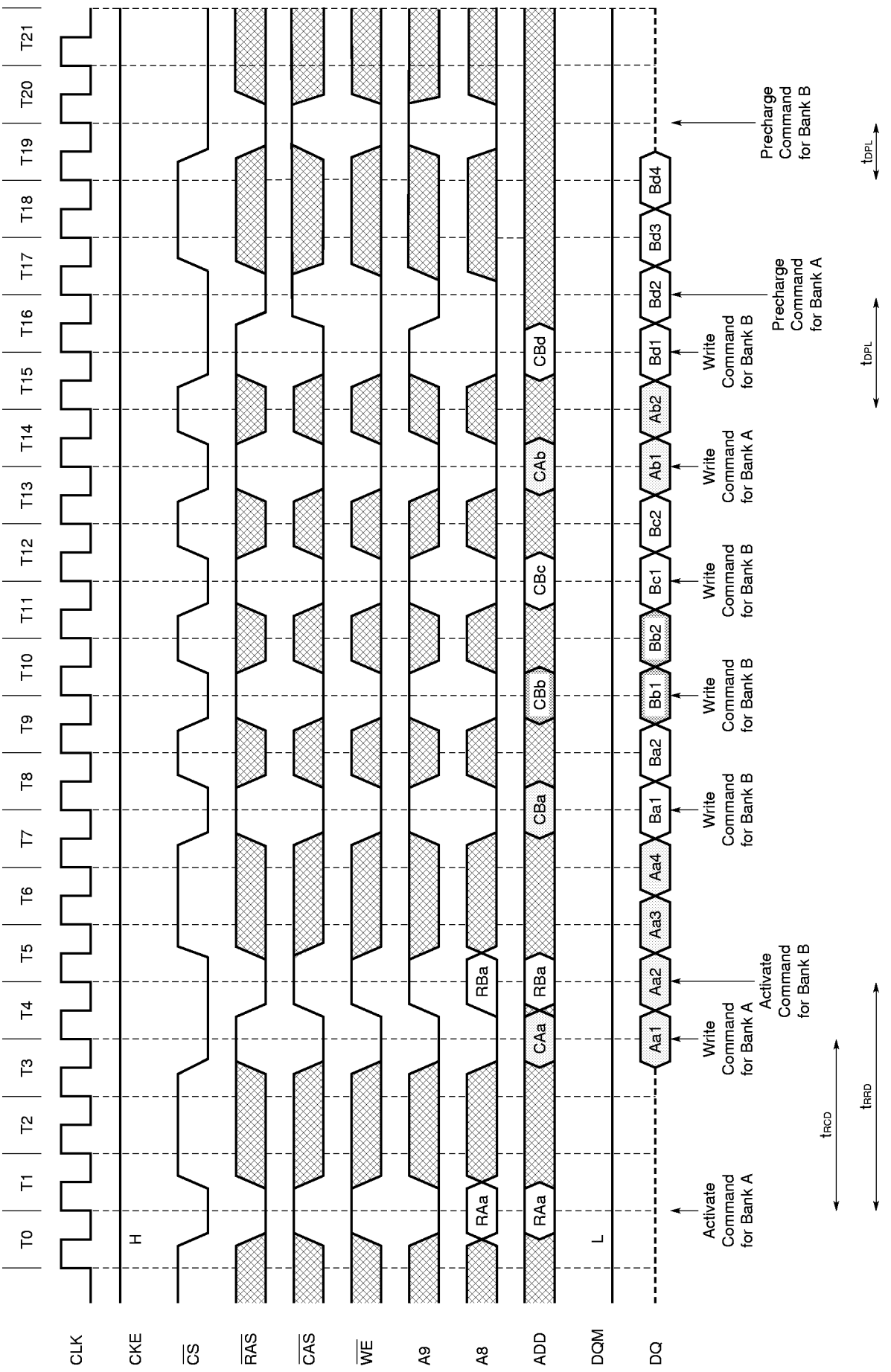
Interleaved Column READ Cycle (2/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 3)



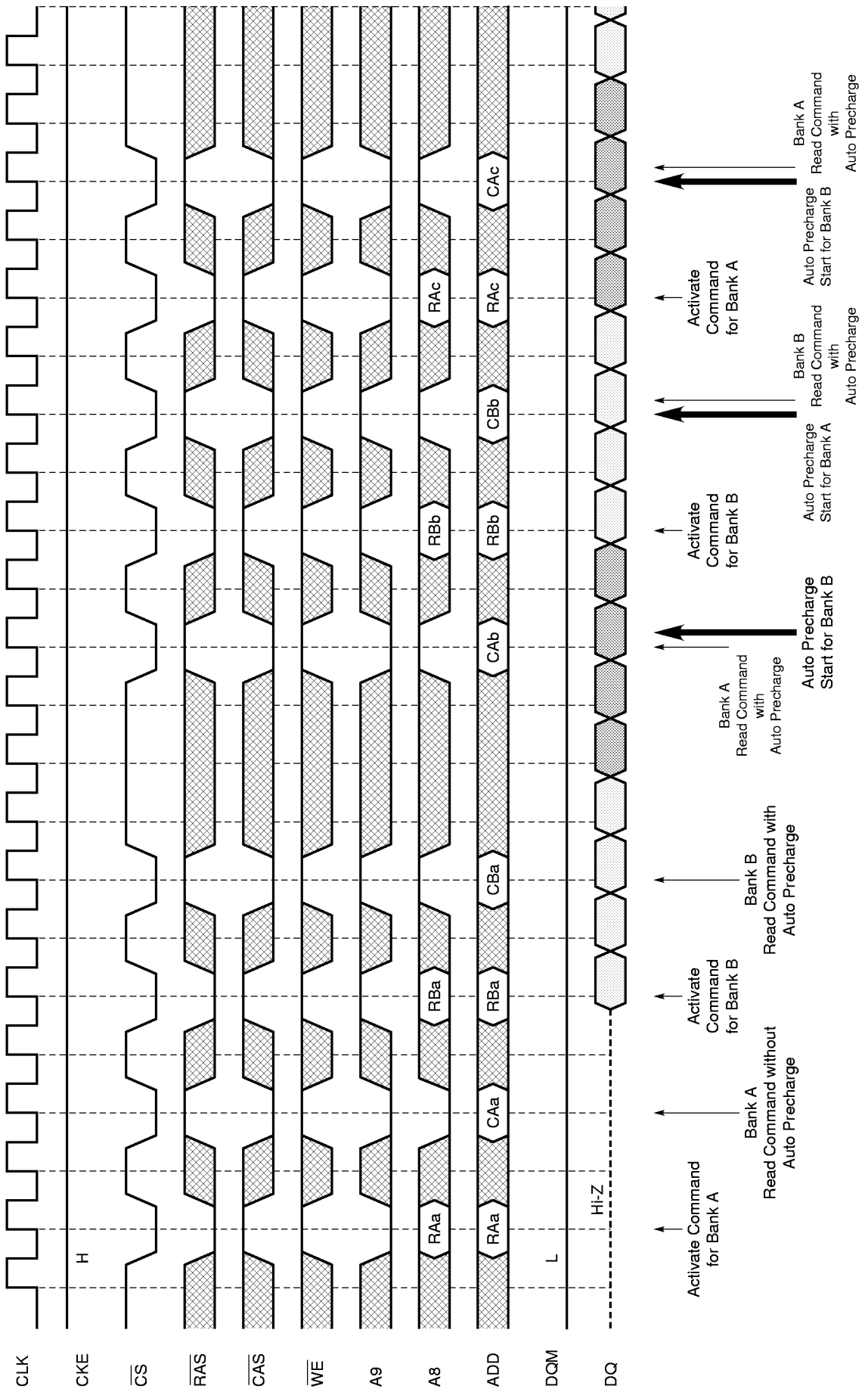
12.18 Interleaved Column WRITE Cycle (1/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)



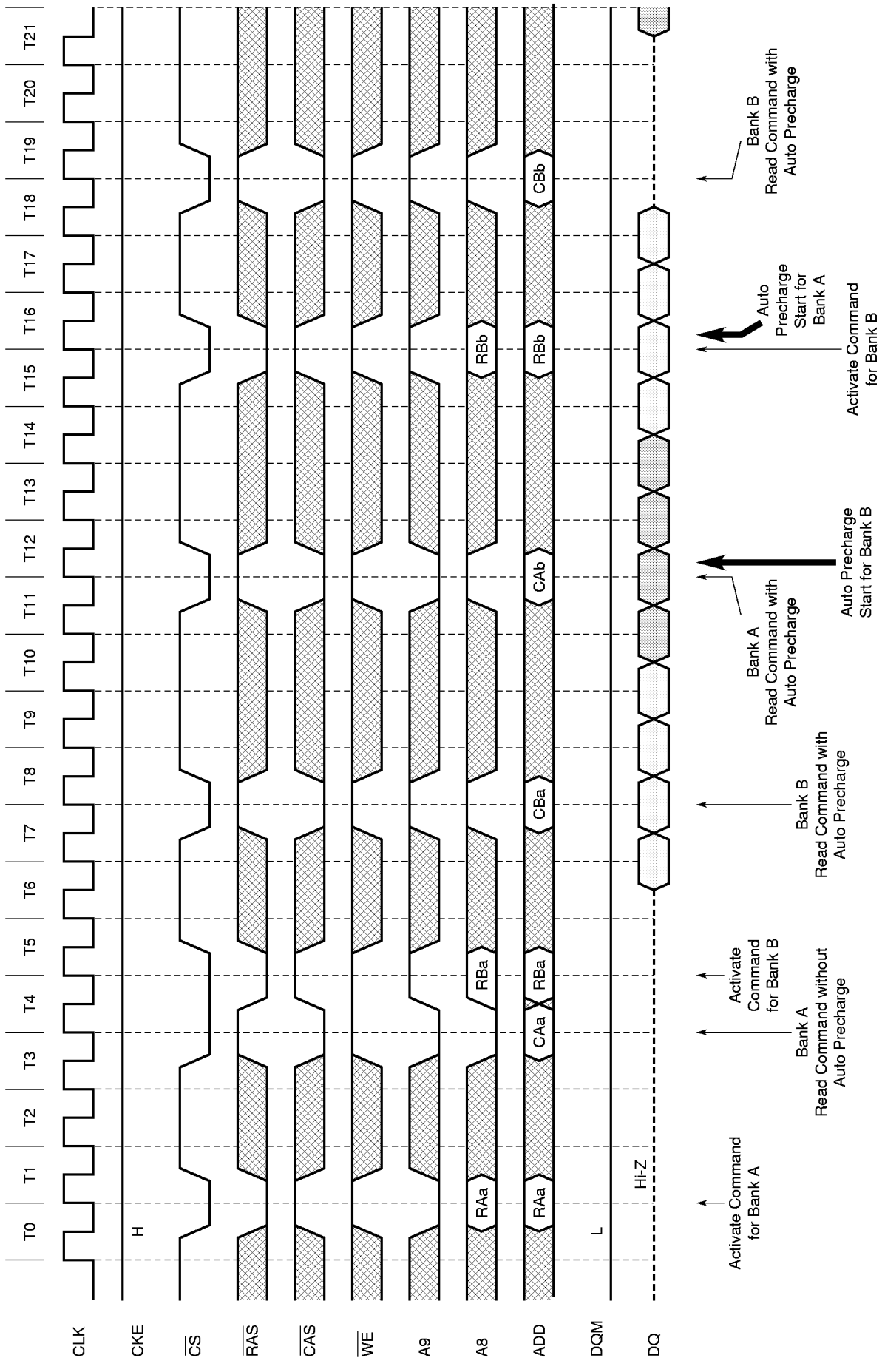
Interleaved Column WRITE Cycle (2/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 3)



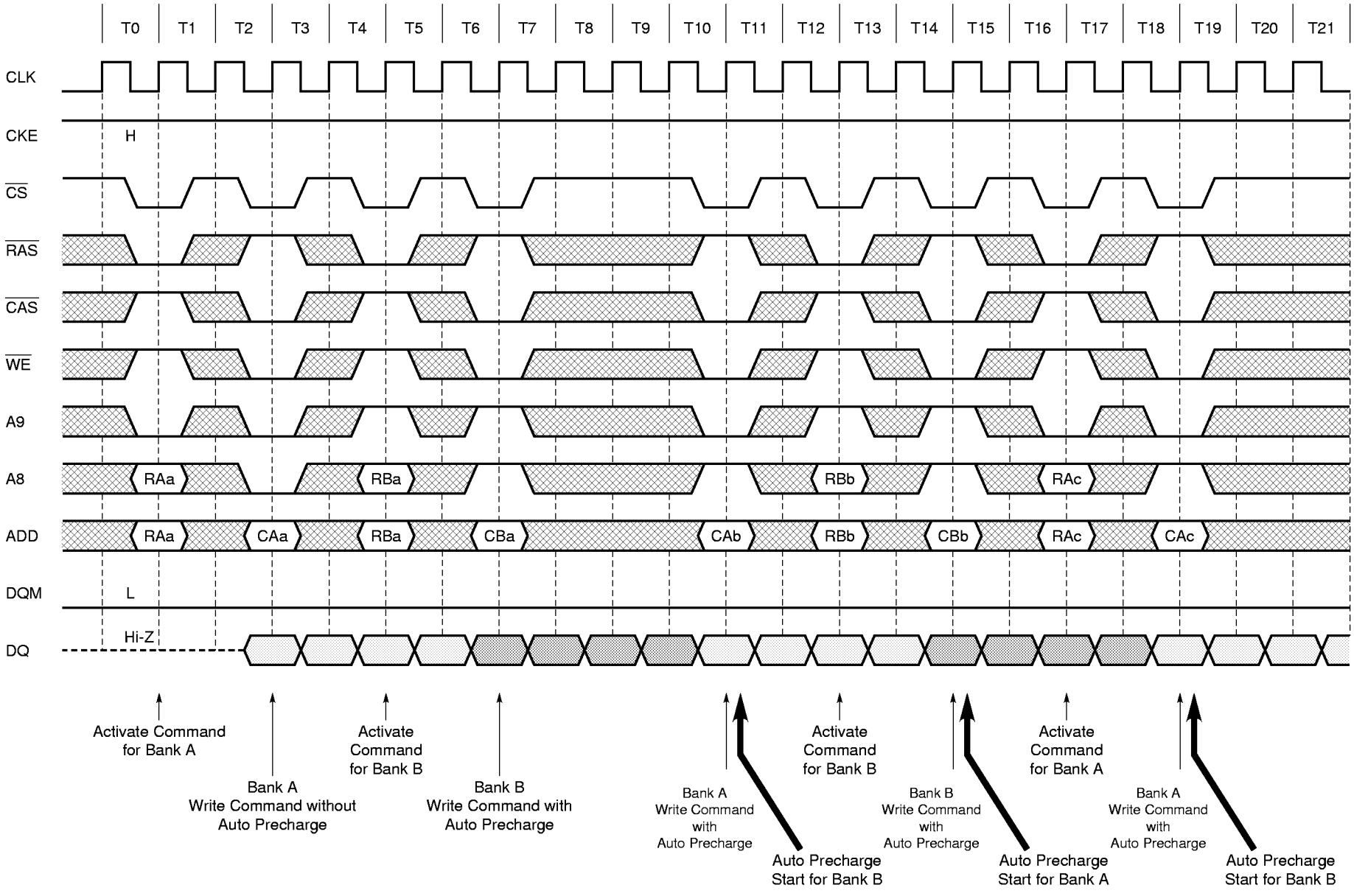
12.19 Auto Precharge after Read Burst (1/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)



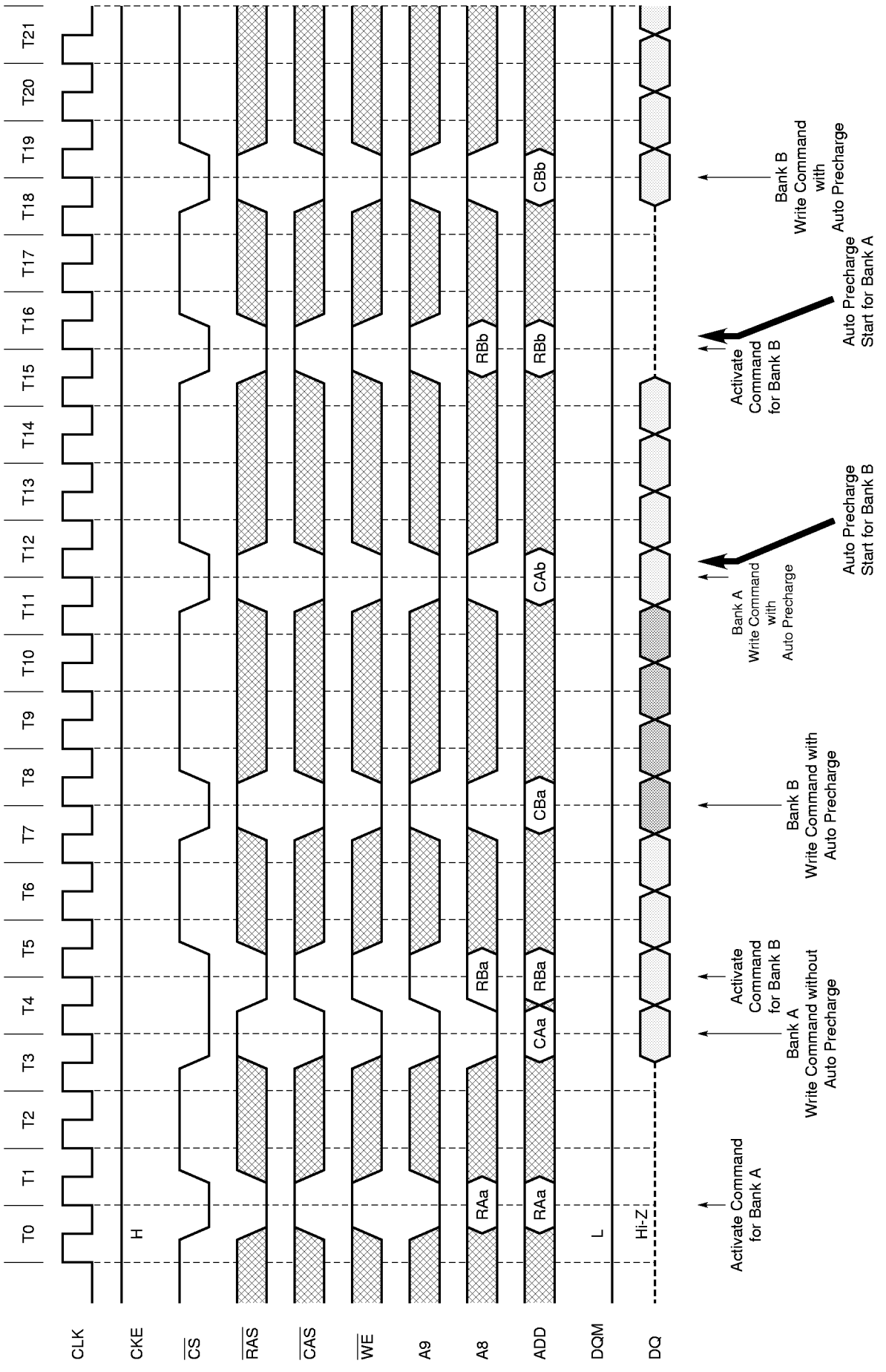
Auto Precharge after Read Burst (2/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 3)



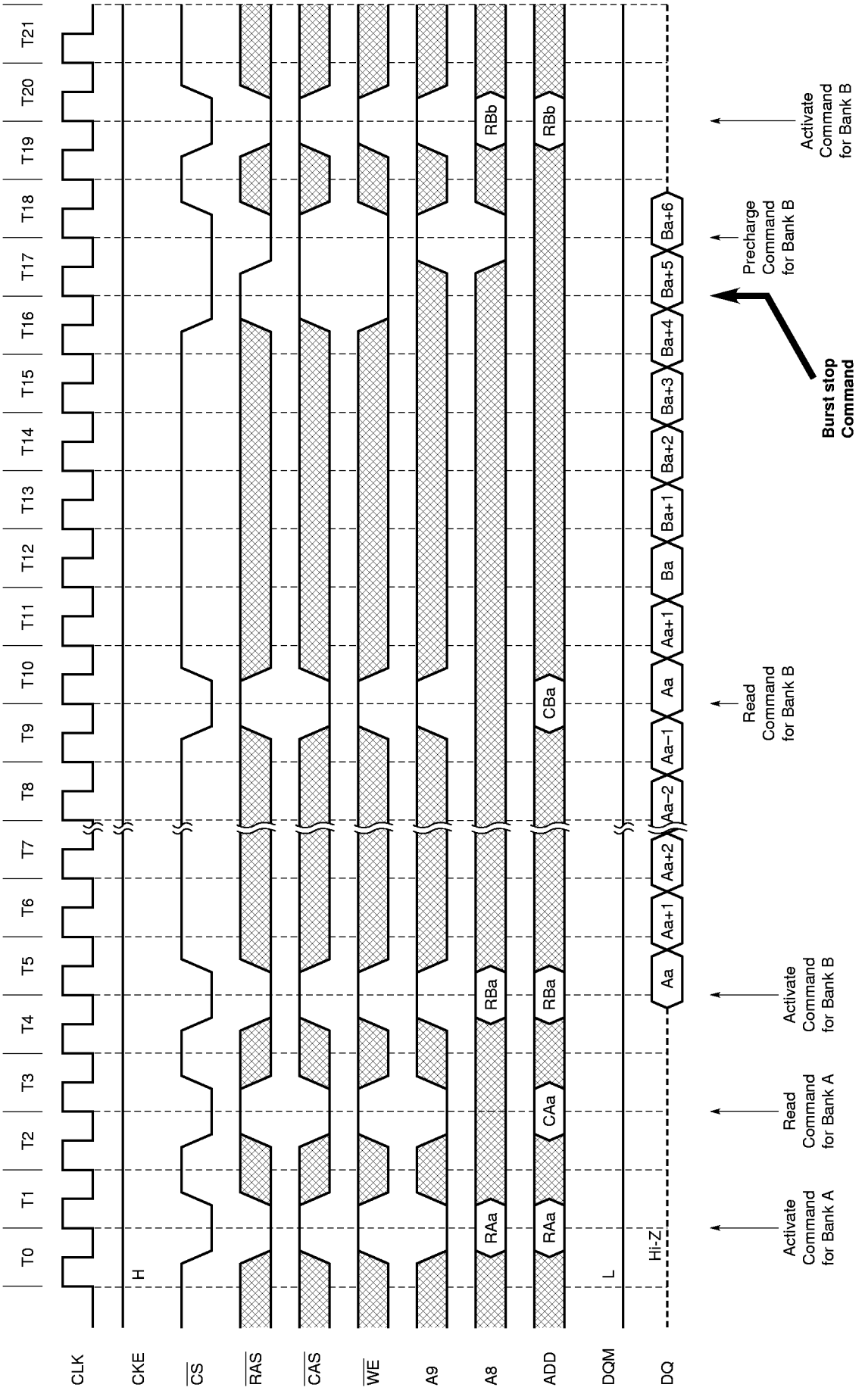
12.20 Auto Precharge after Write Burst (1/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)



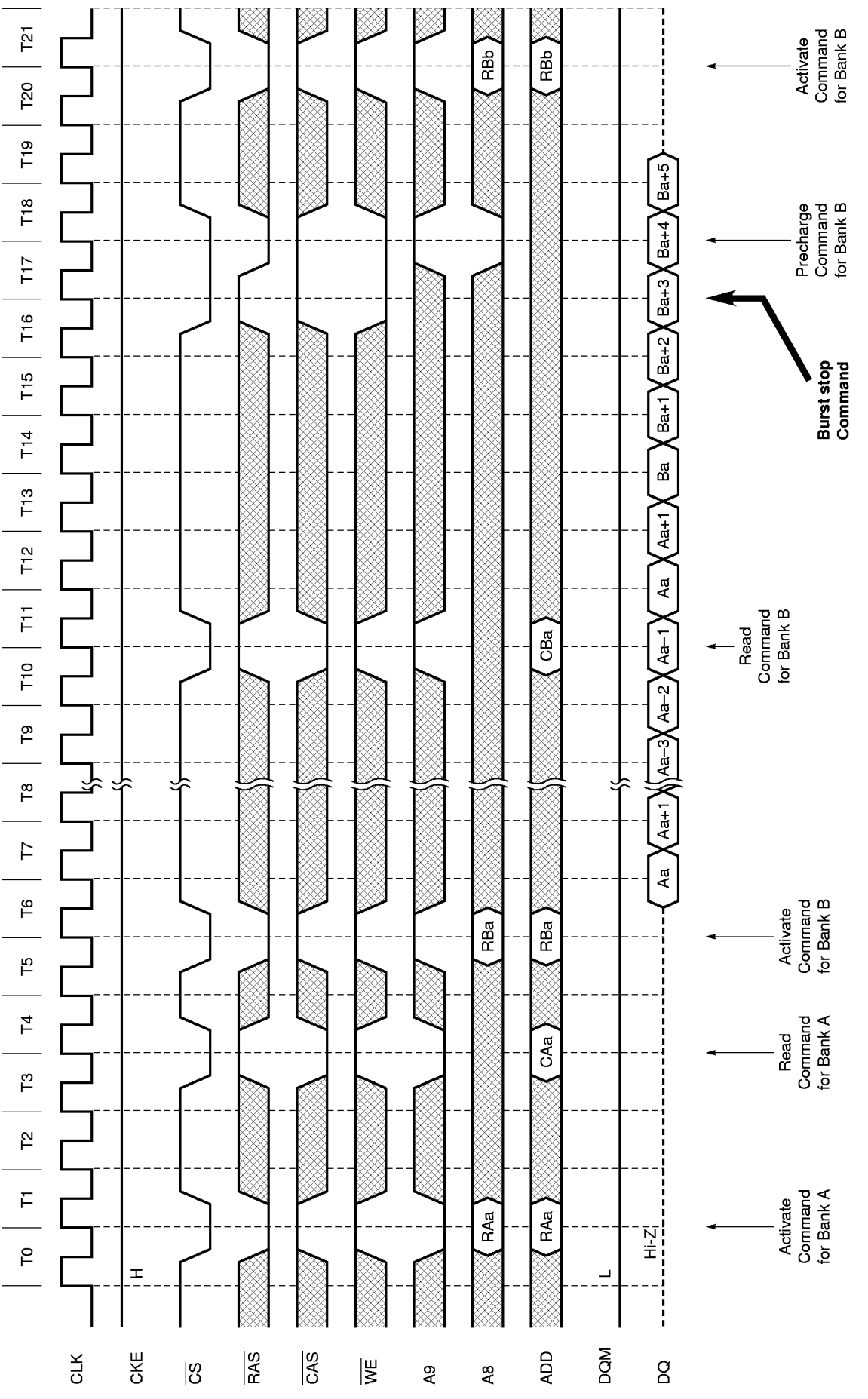
Auto Precharge after Write Burst (2/2) (Burst length = 4, $\overline{\text{CAS}}$ latency = 3)



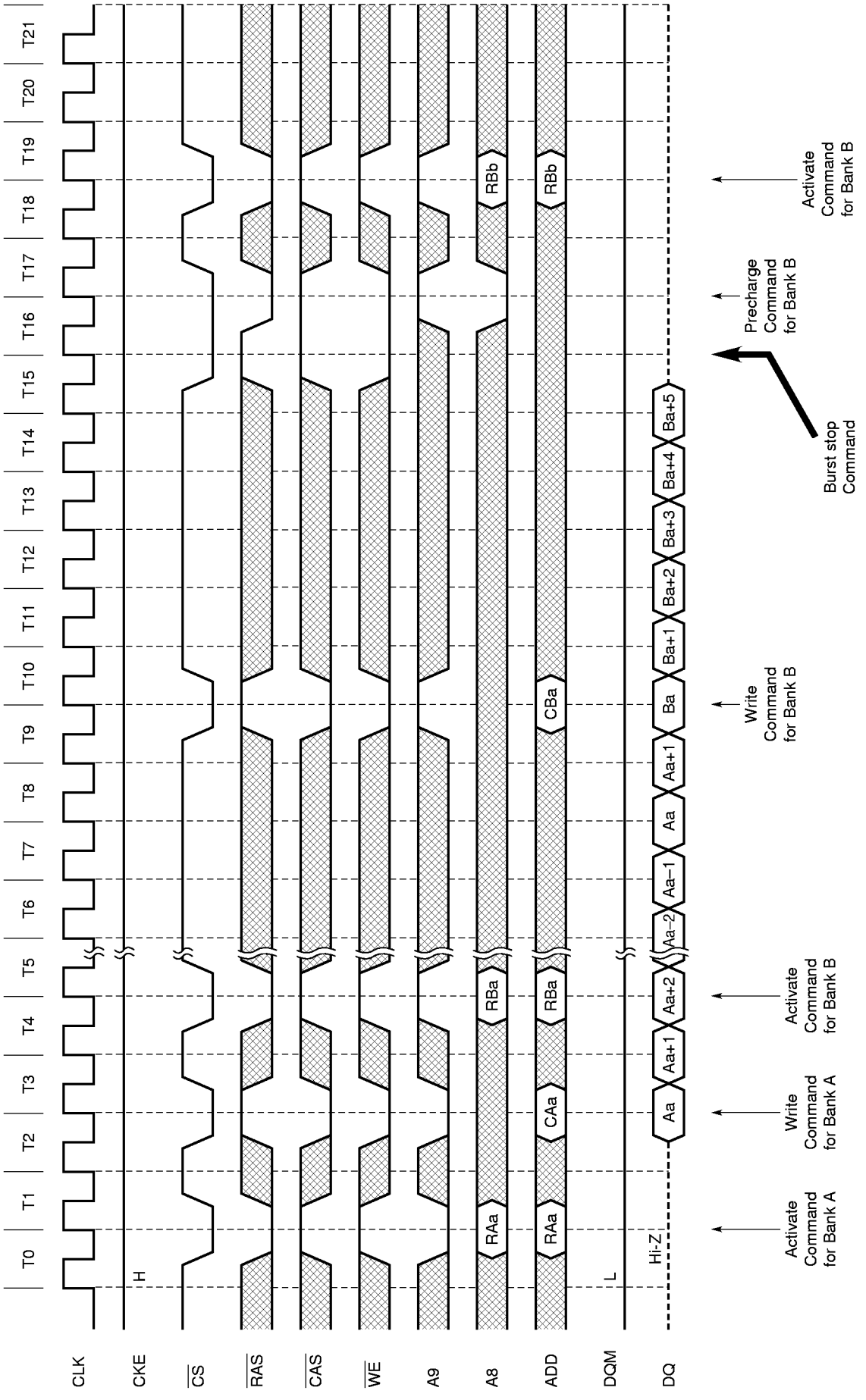
12.21 Full Page READ Cycle (1/2) ($\overline{\text{CAS}}$ latency = 2)



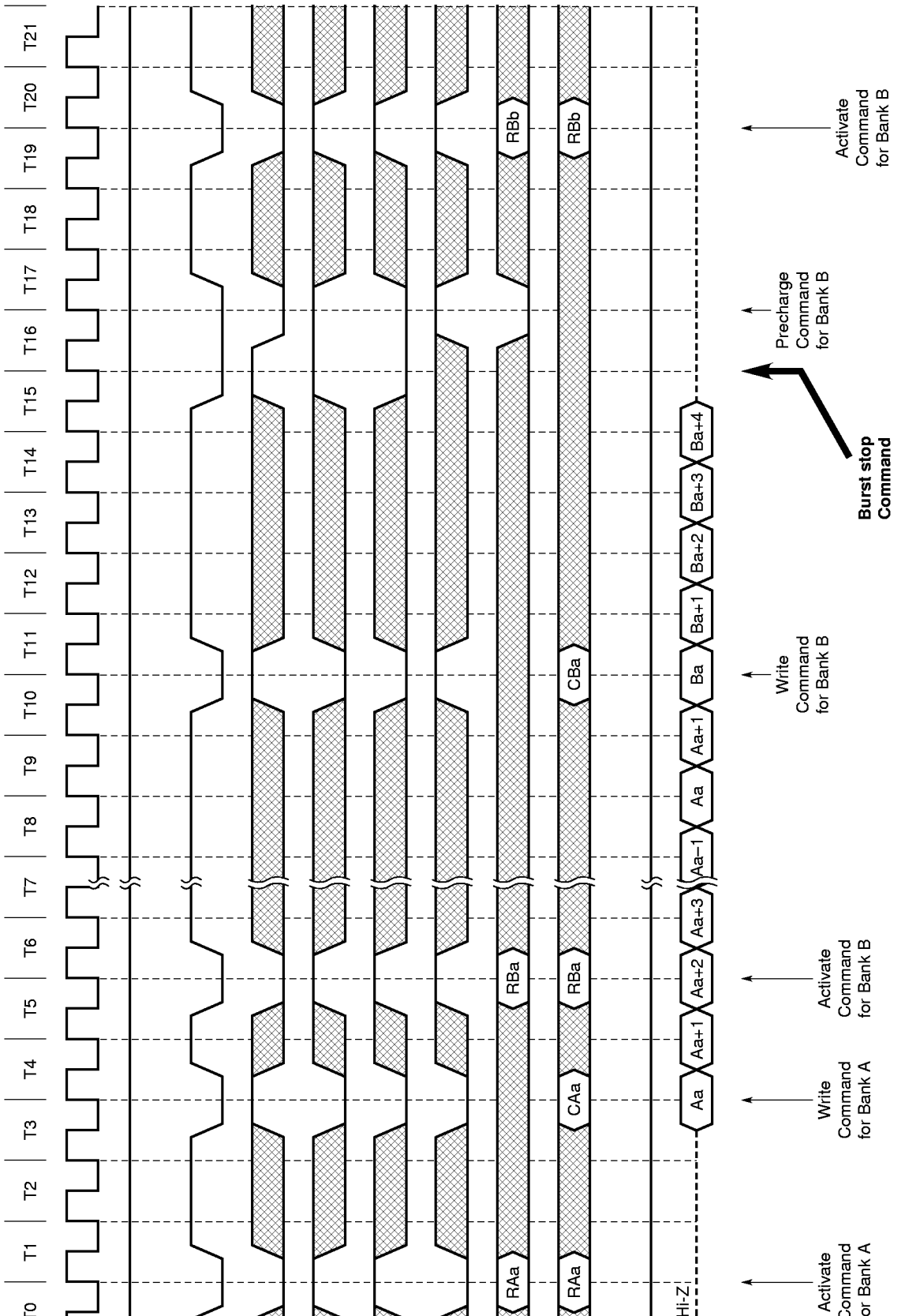
Full Page READ Cycle (2/2) ($\overline{CAS}$ latency = 3)



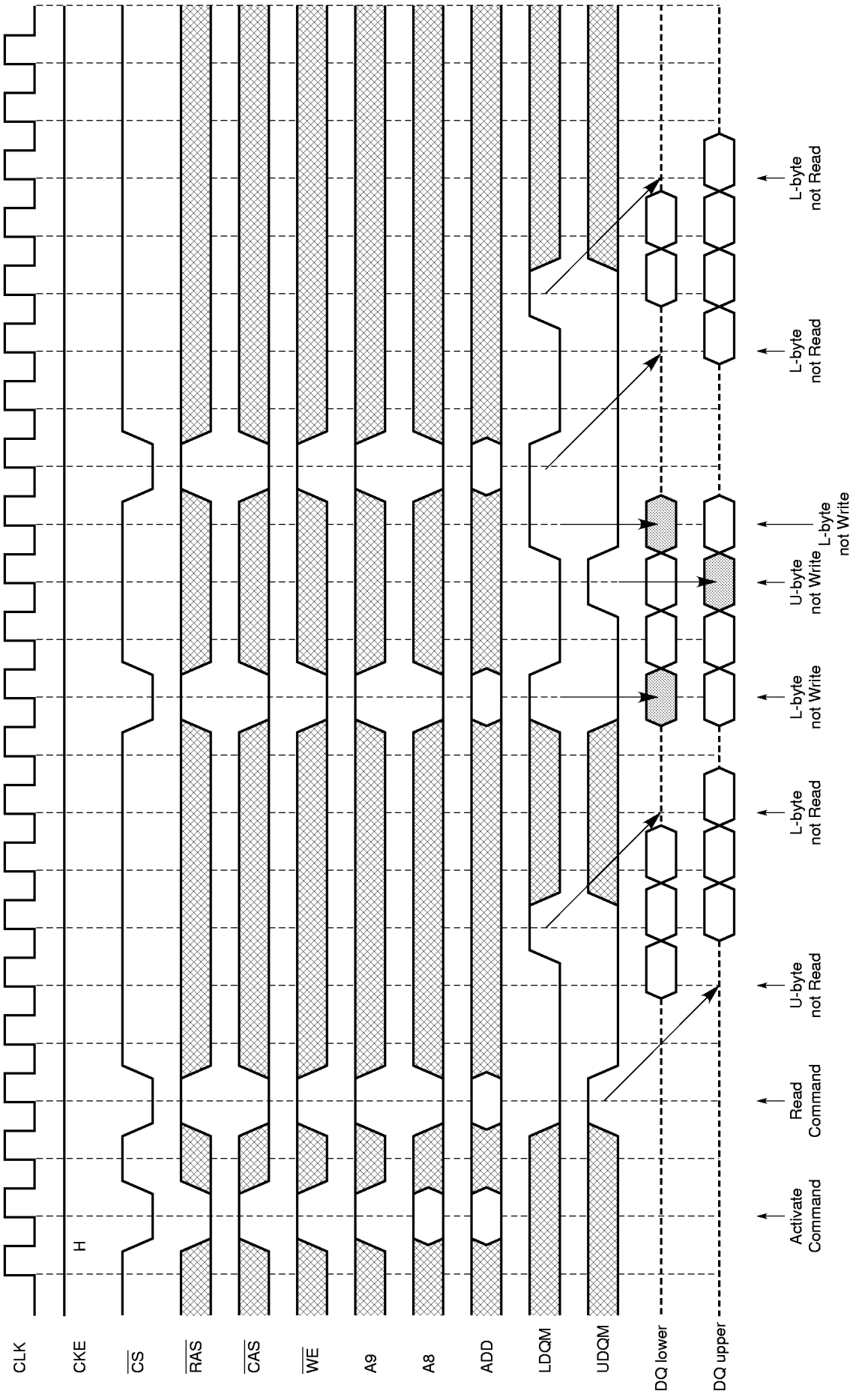
12.22 Full Page WRITE Cycle (1/2) ($\overline{CAS}$ latency = 2)



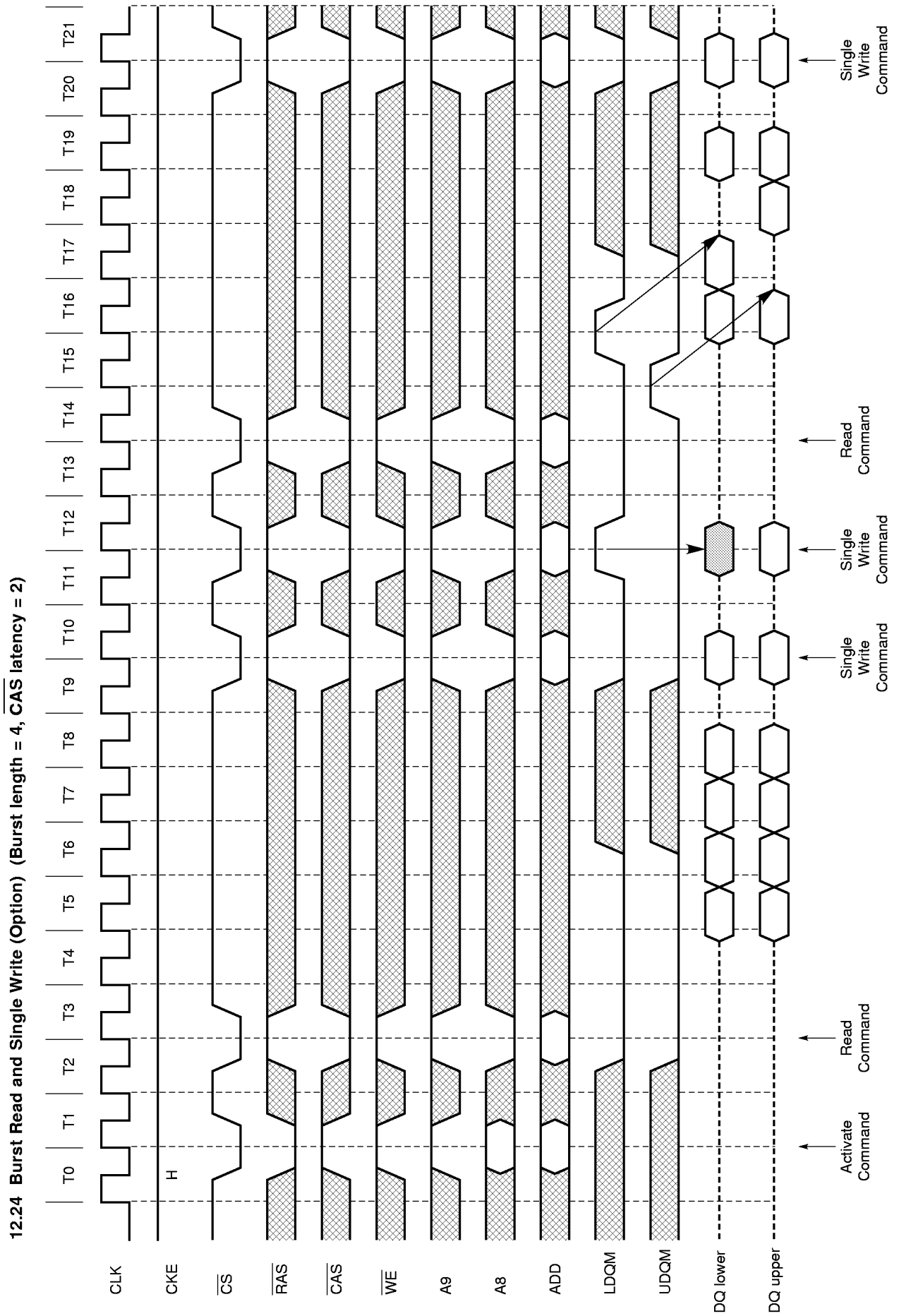
Full Page WRITE Cycle (2/2) ($\overline{CAS}$ latency = 3)



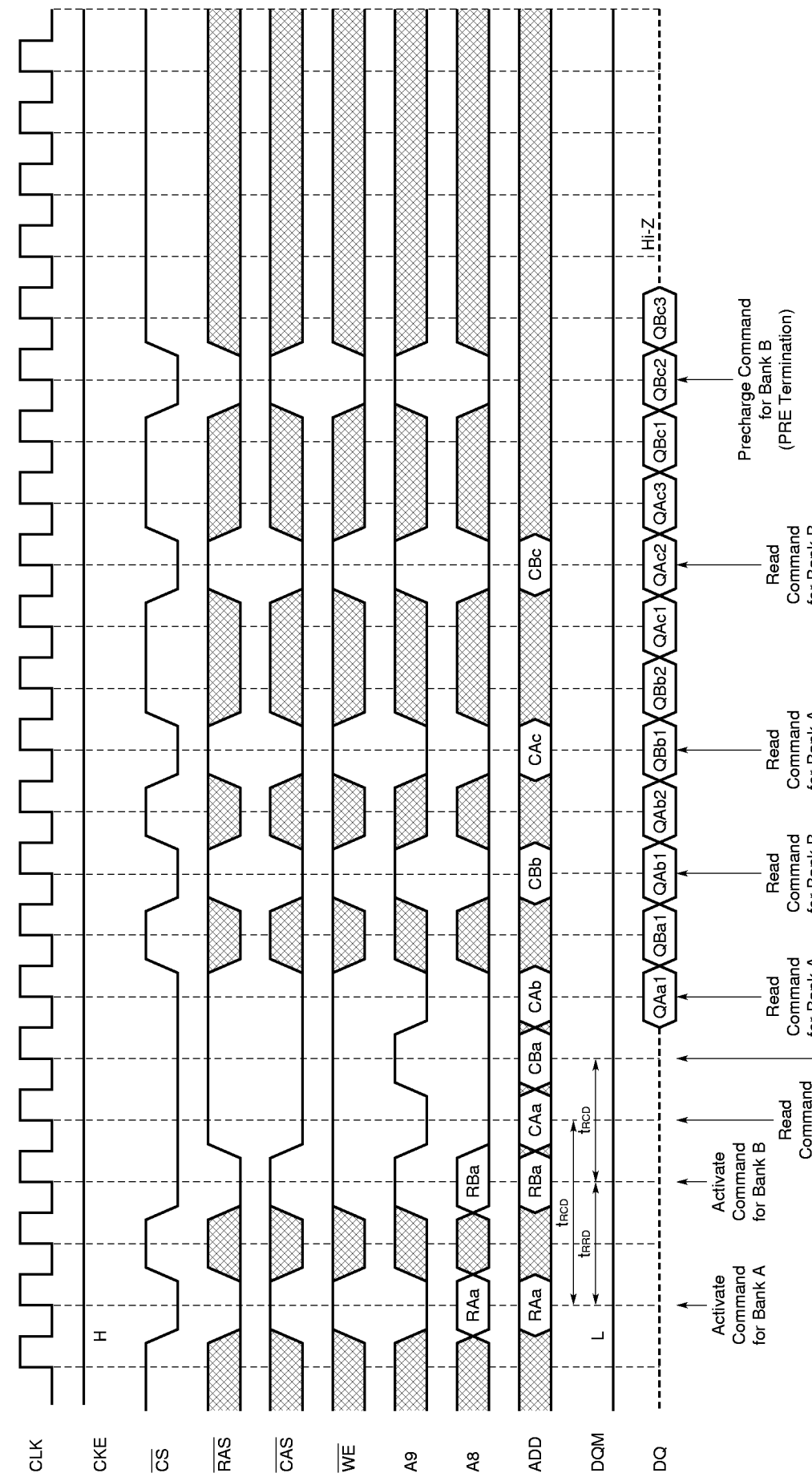
12.23 Byte Write Operation (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)



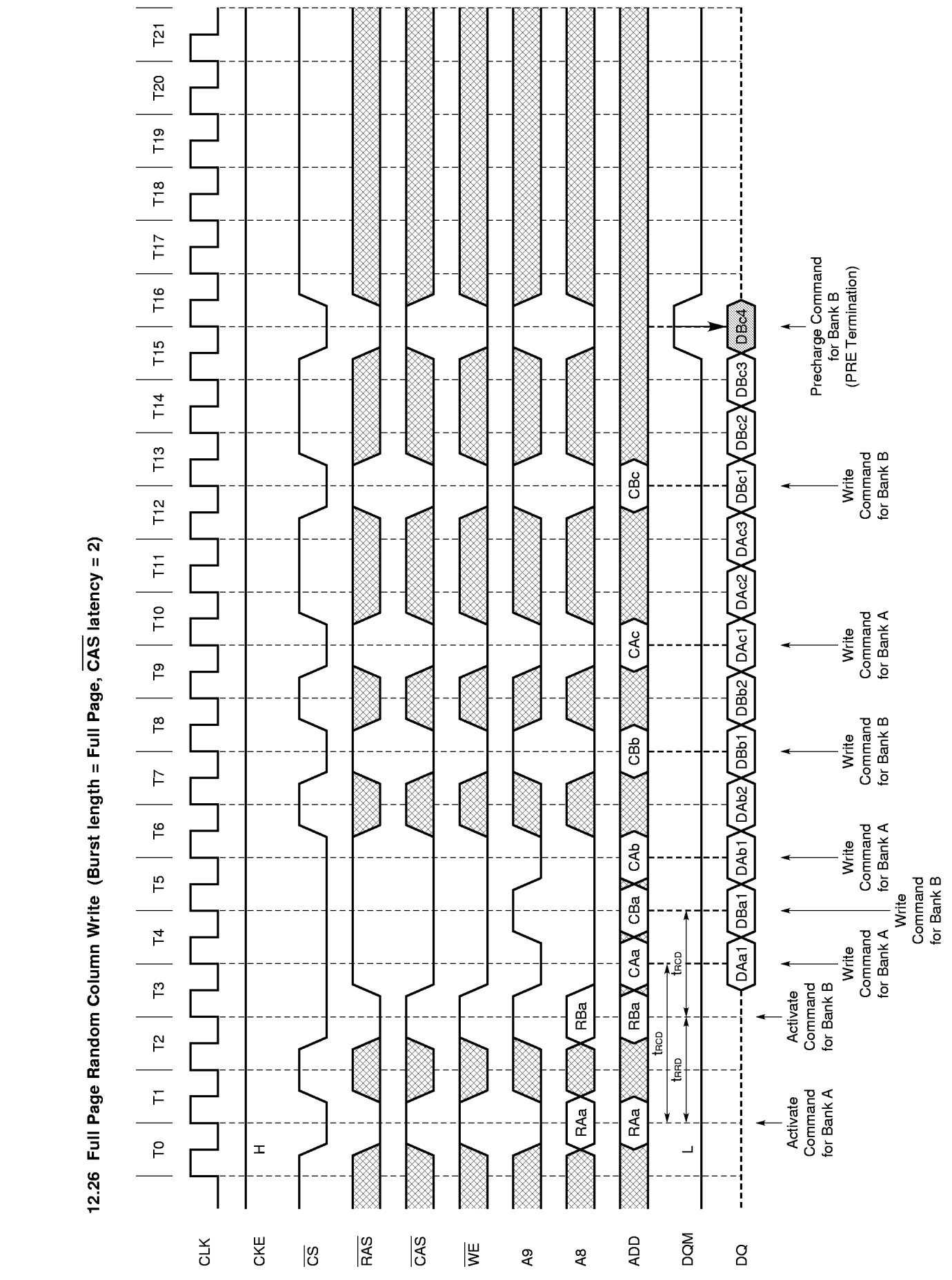
12.24 Burst Read and Single Write (Option) (Burst length = 4, $\overline{\text{CAS}}$ latency = 2)



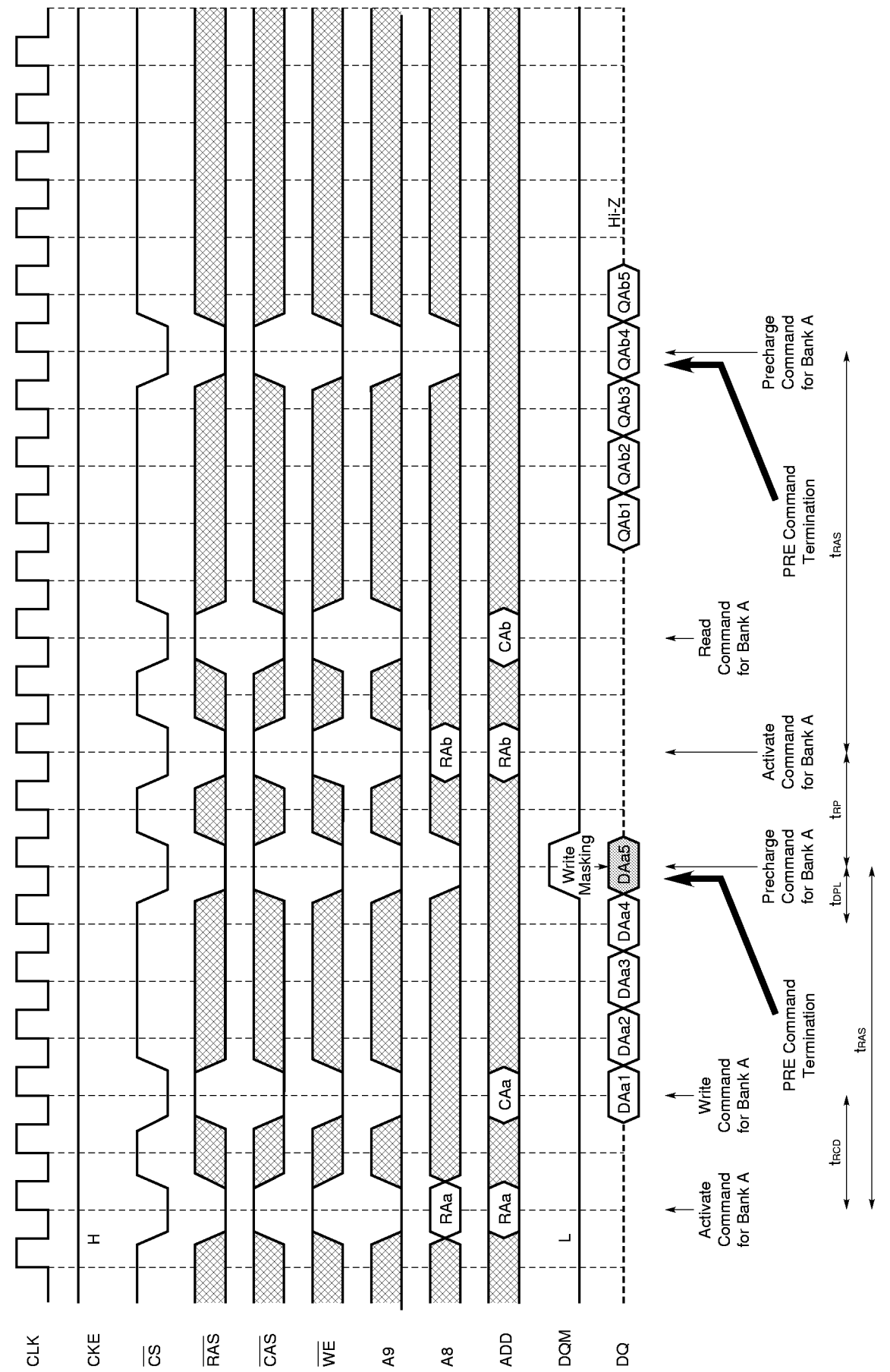
12.25 Full Page Random Column Read (Burst length = Full Page, $\overline{\text{CAS}}$ latency = 2)



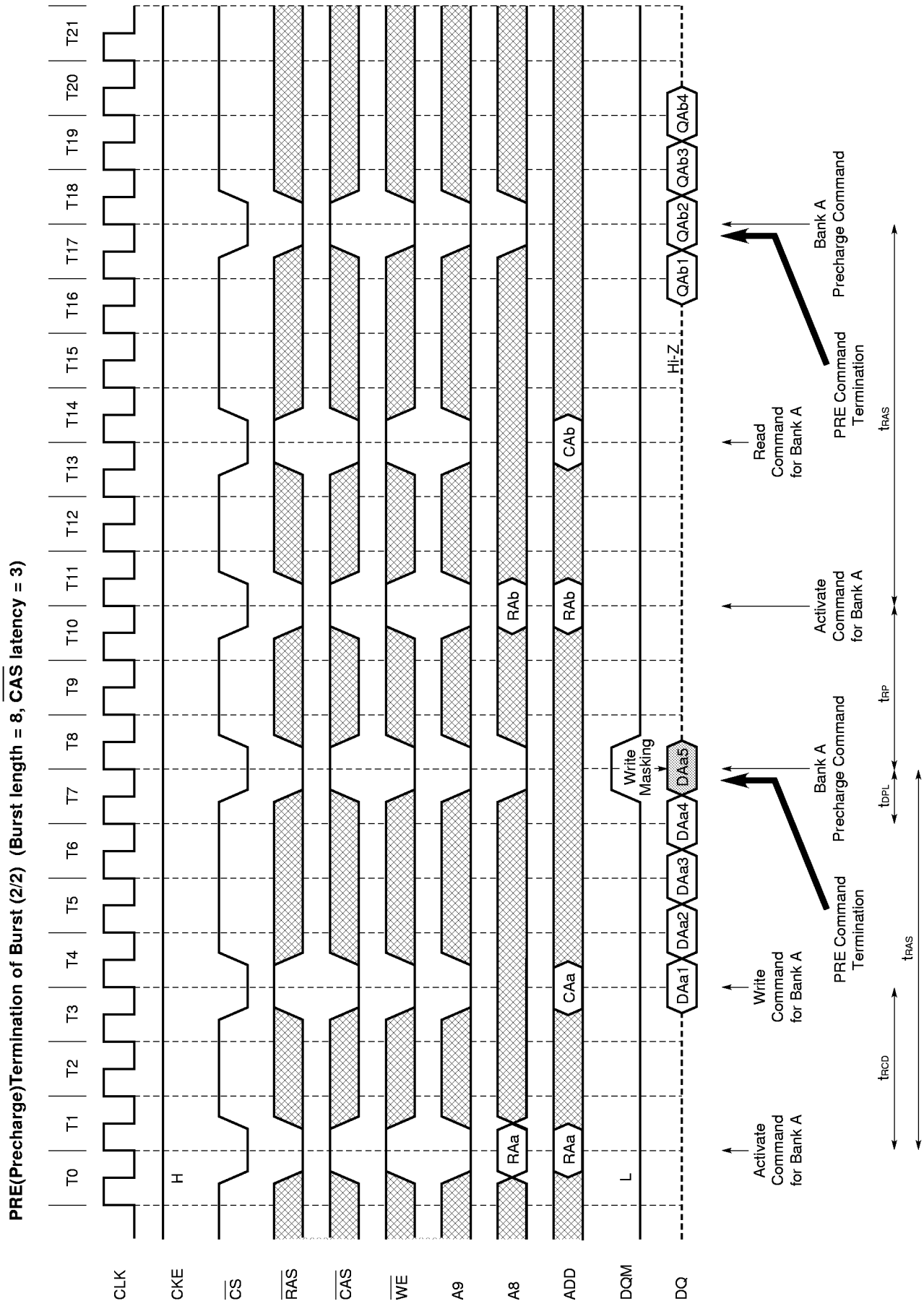
12.26 Full Page Random Column Write (Burst length = Full Page, $\overline{CAS}$ latency = 2)



12.27 PRE(Precharge)Termination of Burst (1/2) (Burst length = 8, $\overline{\text{CAS}}$ latency = 2)

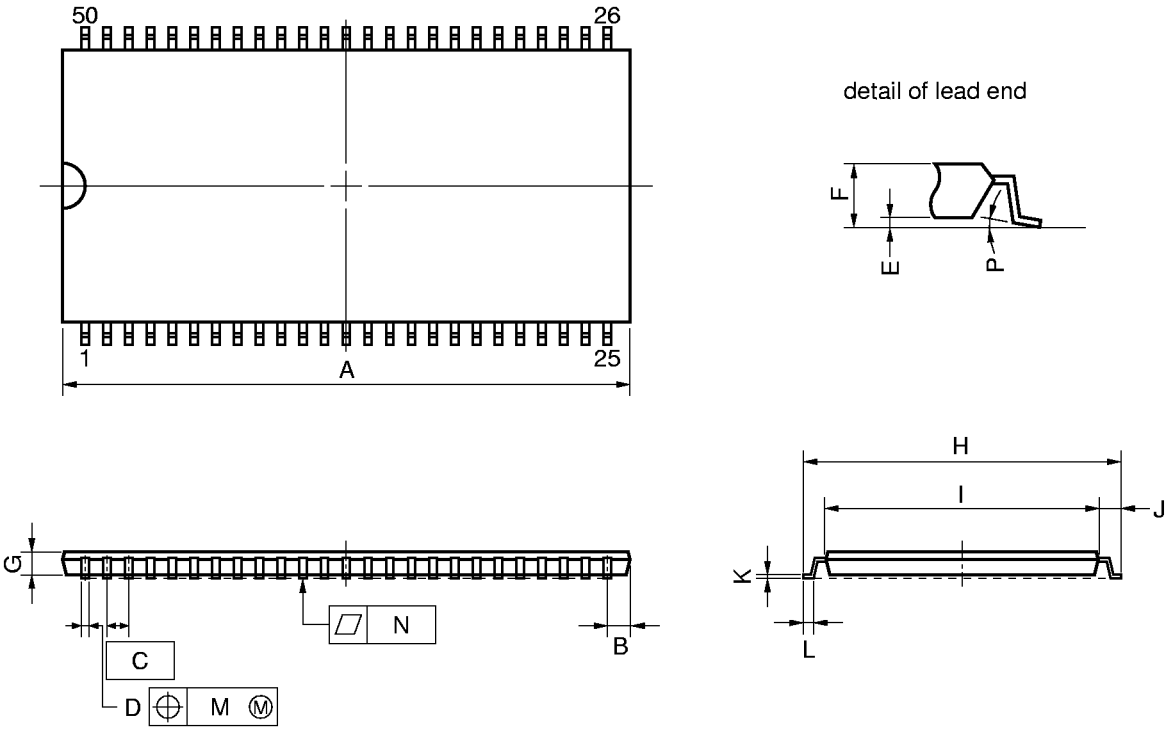


PRE(Precharge)Termination of Burst (2/2) (Burst length = 8, $\overline{\text{CAS}}$ latency = 3)



13. Package Drawing

50PIN PLASTIC TSOP(II) (400 mil)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S50G5-80-7JF3

14. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD4502161.

Type of Surface Mount Device

μPD4502161G5-7JF: 50-pin plastic TSOP (II) (400 mil)