NEC

MOS INTEGRATED CIRCUIT

μPD78P083(A)

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78P083(A) is a member of the μPD78083 Subseries of the 78K/0 Series products. Comparing with the μPD78P083 (standard), more strict quality assurance programs are applied to this product (called Special of the quality grade in NEC). The μPD78P083(A) uses one-time PROM instead of internal ROMs of the μPD78081(A) and μPD78082(A).

Because this device can be programmed by users, it is ideally suited for applications involving the evaluation of systems in development stages, small-scale production of many different products, and rapid development and time-to-market of a new product.

The details of functions are described in the user's manuals. Be sure to read the following manuals before designing.

μPD78083 Subseries User's Manual	: U12176E
78K/0 Series User's Manual — Instructions	: IEU-1372

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Internal PROM: 24 Kbytes **Note**
  - μPD78P083CU(A), μPD78P083GB(A): One-time programmable (ideally suited for small-scale production)
- Internal high-speed RAM: 512 bytes **Note**
- Can be operated in the same supply voltage as the mask ROM version (V_{DD} = 1.8 to 5.5 V)
- Corresponding to QTOP™ Microcontrollers (under planning)

Note The internal PROM and internal high-speed RAM capacities can be changed by setting the internal memory size switching register (IMS).

Remarks 1. QTOP microcontroller is a general term for microcontrollers which incorporate one-time PROM and are totally supported by NEC's programming service (from programming to marking, screening and verification).

2. For the differences between PROM and Mask ROM versions, refer to **Chapter 1. DIFFERENCES BETWEEN THE μPD78P083(A) AND MASK ROM VERSIONS**.

The information in this document is subject to change without notice.

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78P083CU(A)	42-pin plastic shrink DIP (600 mil)	One-Time PROM
μPD78P083GB(A)-3B4	44-pin plastic QFP (10 × 10 mm)	One-Time PROM
μPD78P083GB(A)-3BS-MTX**Note**	44-pin plastic QFP (10 × 10 mm)	One-Time PROM

Note   Under planning

Caution μPD78P083GB(A) has two types of packages. (Refer to Chapter 7. PACKAGE DRAWINGS). Consult an NEC's sales representative for suppliable packages.

QUALITY GRADE

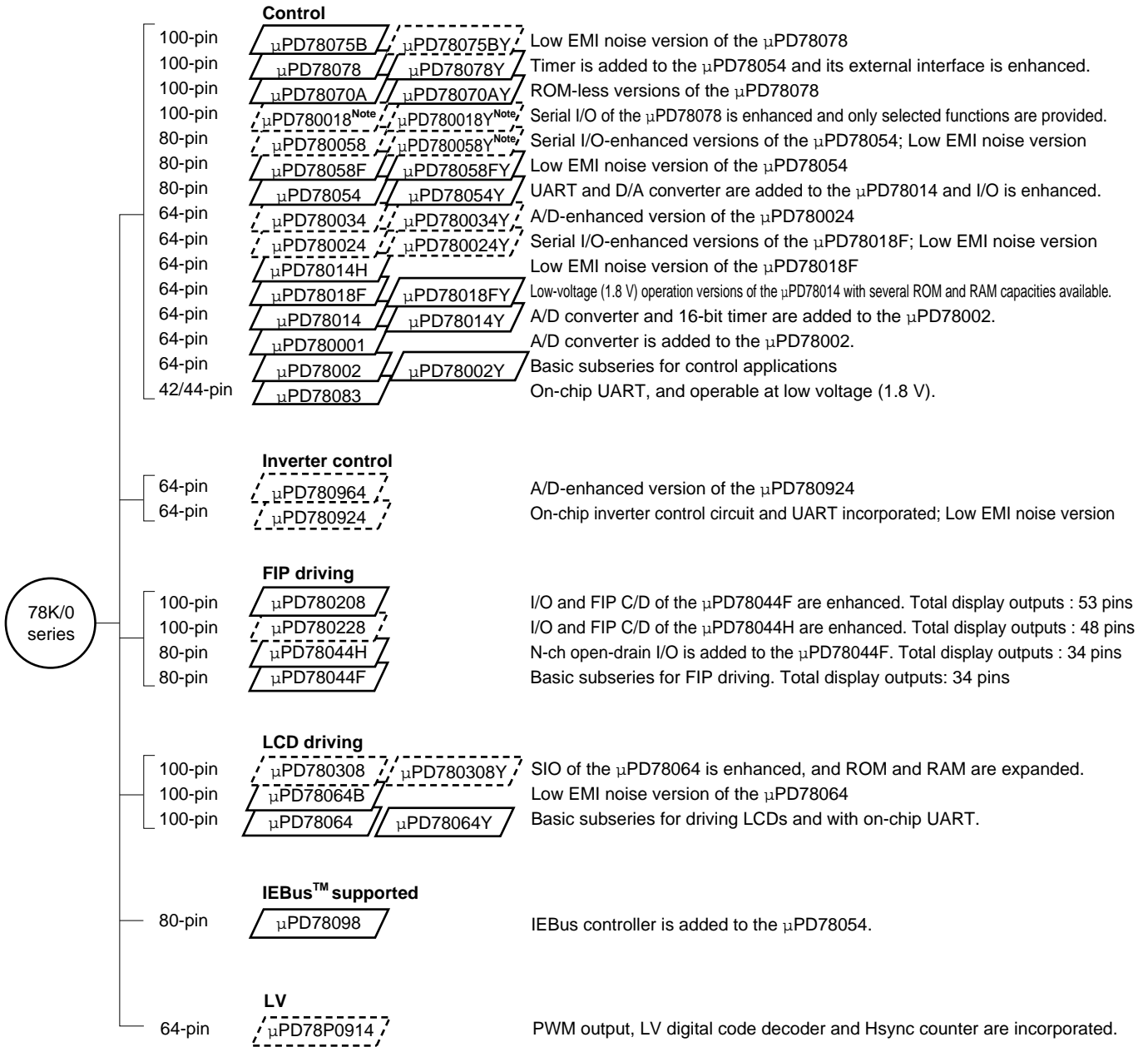| Part Number	Package	Quality Grades
μPD78P083CU(A)	42-pin plastic shrink DIP (600 mil)	Special
μPD78P083GB(A)-3B4	44-pin plastic QFP (10 × 10 mm)	Special
μPD78P083GB(A)-3BS-MTX**Note**	44-pin plastic QFP (10 × 10 mm)	Special

Note   Under planning

   Please refer to "Quality grades on NEC Semiconductor Devices" (Document number C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Deferences between μPD78P083(A) and μPD78P083

Product Item	μPD78P083(A)	μPD78P083
Quality Grade	Special	Standard
Package	42-pin plastic shrink DIP (600 mil) 44-pin plastic QFP (10 × 10 mm)	42-pin plastic shrink DIP (600 mil) 44-pin plastic QFP (10 × 10 mm) 42-pin ceramic shrink DIP (with window) (600 mil)

78K/0 SERIES DEVELOPMENT

The following shows the 78K/0 Series products development. Subseries names are shown inside frames.

Mass-produced products

Products under development

Y Subseries supports the I^{2}C bus specifications.

Control

Pins			Description
100-pin	μPD78075B	μPD78075BY	Low EMI noise version of the μPD78078
100-pin	μPD78078	μPD78078Y	Timer is added to the μPD78054 and its external interface is enhanced.
100-pin	μPD78070A	μPD78070AY	ROM-less versions of the μPD78078
100-pin	μPD780018**Note**	μPD780018Y**Note**	Serial I/O of the μPD78078 is enhanced and only selected functions are provided.
80-pin	μPD780058	μPD780058Y**Note**	Serial I/O-enhanced versions of the μPD78054; Low EMI noise version
80-pin	μPD78058F	μPD78058FY	Low EMI noise version of the μPD78054
80-pin	μPD78054	μPD78054Y	UART and D/A converter are added to the μPD78014 and I/O is enhanced.
64-pin	μPD780034	μPD780034Y	A/D-enhanced version of the μPD780024
64-pin	μPD780024	μPD780024Y	Serial I/O-enhanced versions of the μPD78018F; Low EMI noise version
64-pin	μPD78014H		Low EMI noise version of the μPD78018F
64-pin	μPD78018F	μPD78018FY	Low-voltage (1.8 V) operation versions of the μPD78014 with several ROM and RAM capacities available.
64-pin	μPD78014	μPD78014Y	A/D converter and 16-bit timer are added to the μPD78002.
64-pin	μPD780001		A/D converter is added to the μPD78002.
64-pin	μPD78002	μPD78002Y	Basic subseries for control applications
42/44-pin	μPD78083		On-chip UART, and operable at low voltage (1.8 V).

Inverter control

Pins		Description
64-pin	μPD780964	A/D-enhanced version of the μPD780924
64-pin	μPD780924	On-chip inverter control circuit and UART incorporated; Low EMI noise version

FIP driving

Pins		Description
100-pin	μPD780208	I/O and FIP C/D of the μPD78044F are enhanced. Total display outputs : 53 pins
100-pin	μPD780228	I/O and FIP C/D of the μPD78044H are enhanced. Total display outputs : 48 pins
80-pin	μPD78044H	N-ch open-drain I/O is added to the μPD78044F. Total display outputs : 34 pins
80-pin	μPD78044F	Basic subseries for FIP driving. Total display outputs: 34 pins

LCD driving

Pins			Description
100-pin	μPD780308	μPD780308Y	SIO of the μPD78064 is enhanced, and ROM and RAM are expanded.
100-pin	μPD78064B		Low EMI noise version of the μPD78064
100-pin	μPD78064	μPD78064Y	Basic subseries for driving LCDs and with on-chip UART.

IEBus™ supported

Pins		Description
80-pin	μPD78098	IEBus controller is added to the μPD78054.

LV

Pins		Description
64-pin	μPD78P0914	PWM output, LV digital code decoder and Hsync counter are incorporated.

78K/0 series

Note Under planning

The following table shows the differences among subseries functions.

Function	Subseries name	ROM capacity	Timer 8-bit	16-bit	Watch	WDT	8-bit A/D	10-bit A/D	8-bit D/A	Serial interface	I/O	V_DD MIN. value	External expansion
Control	μPD78075B	32K to 40K	4 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	88	1.8 V	Available
	μPD78078	48K to 60K											
	μPD78070A	—									61	2.7 V	
	μPD780018	48K to 60K							—	2 ch (Time division 3-wire: 1 ch)	88		
	μPD780058	24K to 60K	2 ch						2 ch	3 ch (Time division UART: 1 ch)	68	1.8 V	
	μPD78058F	48K to 60K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16K to 60K										2.0 V	
	μPD780034	8K to 32K					—	8 ch	—	3 ch (UART: 1 ch, Time division 3-wire: 1 ch)	51	1.8 V	
	μPD780024	8K to 32K					8 ch	—					
	μPD78014H	8K to 32K								2 ch	53		
	μPD78018F	8K to 60K											
	μPD78014	8K to 32K										2.7 V	
	μPD780001	8K		—	—					1 ch	39		—
	μPD78002	8K to 16K		1 ch			—				53		Available
	μPD78083	—			—		8 ch			1 ch (UART: 1 ch)	33	1.8 V	—
Inverter control	μPD780964	8K to 32K	3 ch	**Note**	—	1 ch	—	8 ch	—	2 ch (UART: 2 ch)	47	2.7 V	Available
	μPD780924						8 ch	—					
FIP driving	μPD780208	32K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	2 ch	74	2.7 V	—
	μPD780228	48K to 60K	3 ch	—	—					1 ch	72	4.5 V	
	μPD78044H	32K to 48K	2 ch	1 ch	1 ch						68	2.7 V	
	μPD78044F	16K to 40K								2 ch			
LCD driving	μPD780308	48K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	3 ch (Time division UART: 1 ch)	57	2.0 V	—
	μPD78064B	32K								2 ch (UART: 1 ch)			
	μPD78064	16K to 32K											
IEBus supported	μPD78098	32K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	69	2.7 V	Available
LV	μPD78P0914	32K	6 ch	—	—	1 ch	8 ch	—	—	2 ch	54	4.5 V	Available

Note 10 bits timer: 1 channel

FUNCTION DESCRIPTION

Item		Function
Internal memory		• PROM: 24 Kbytes **Note** • RAM High-speed RAM: 512 bytes **Note**
Memory space		64 Kbytes
General register		8 bits x 32 registers (8 bits x 8 registers x 4 banks)
Instruction cycles		Instruction execution time variable function is integrated. 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@5.0-MHz operation with main system clock)
Instruction set		• 16-bit operation • Multiply/divide (8 bits x 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total　　　　　　 : 33 • CMOS input　　　: 1 • CMOS input/output : 32
A/D converter		• 8-bit resolution x 8 channels
Serial interface		• 3-wired serial I/O/UART mode selectable: 1 channel
Timer		• 8-bit timer/event counter: 2 channels • Watchdog timer: 1 channel
Timer output		2 pins (8-bit PWM output enable)
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (@ 5.0-MHz operation with main system clock)
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, and 9.8 kHz (@ 5.0-MHz operation with main system clock)
Vectored-interrupt source	Maskable	Internal : 8　external : 3
	Non-maskable	Internal : 1
	Software	Internal : 1
Power supply voltage		V_{DD} = 1.8 to 5.5 V
Operating ambient temperature		T_A = −40 to +85°C
Packages		• 42-pin plastic shrink DIP (600 mil) • 44-pin plastic QFP (10 × 10 mm)

Note Internal PROM and high-speed RAM capacities can be changed by setting the memory size switching register (IMS).

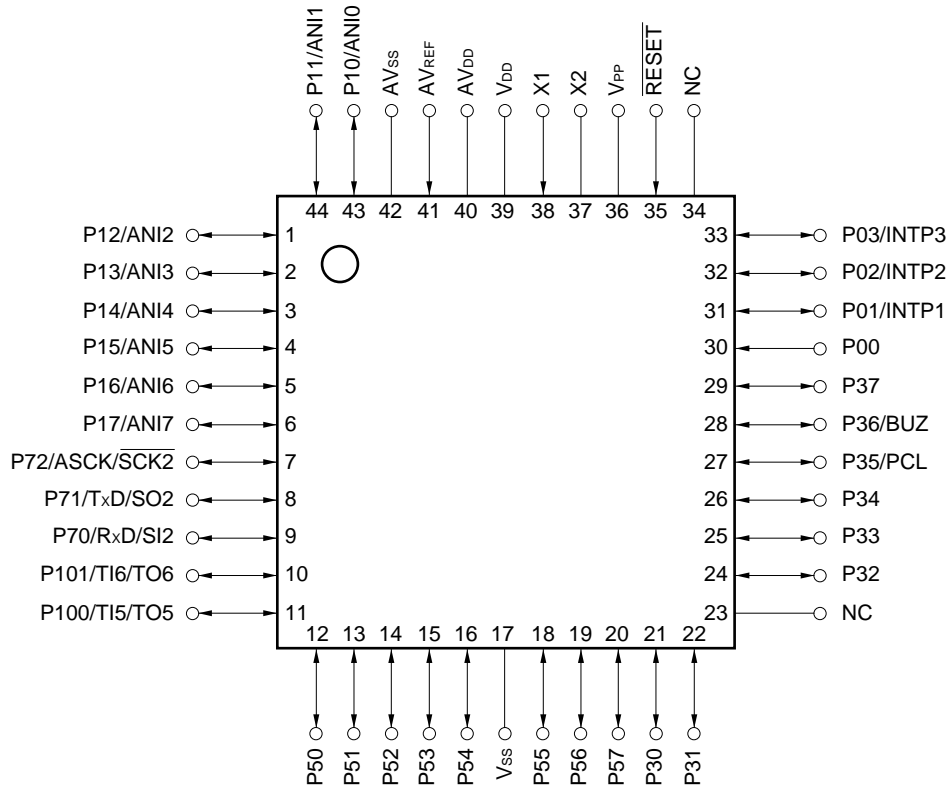PIN CONFIGURATIONS (Top View)

(1) Normal operating mode

- 42-pin plastic shrink DIP (600 mil)
  µPD78P083CU(A)
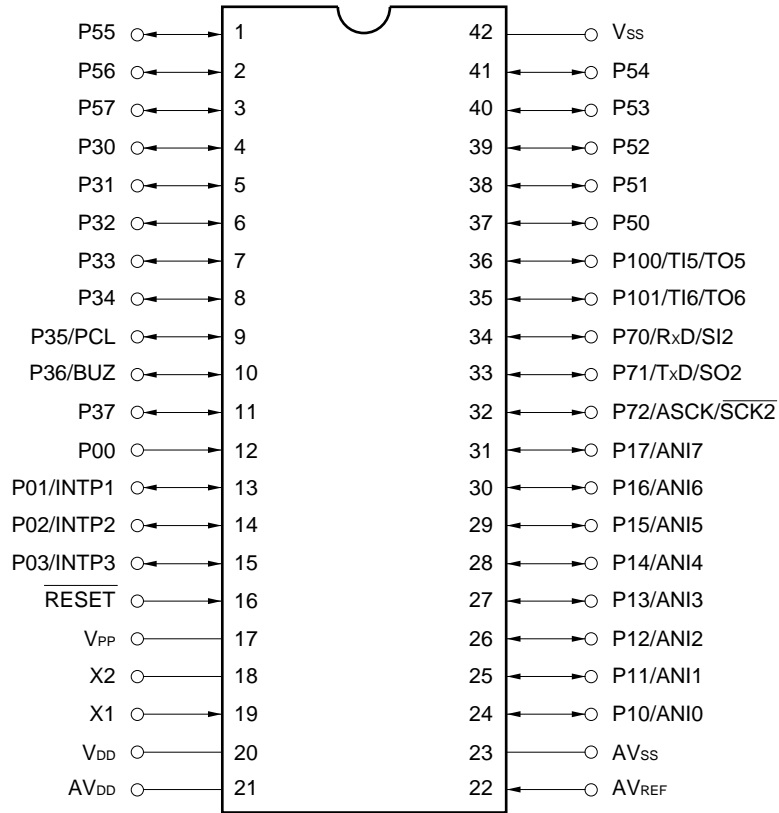
P55	1	42	Vss
P56	2	41	P54
P57	3	40	P53
P30	4	39	P52
P31	5	38	P51
P32	6	37	P50
P33	7	36	P100/TI5/TO5
P34	8	35	P101/TI6/TO6
P35/PCL	9	34	P70/RxD/SI2
P36/BUZ	10	33	P71/TxD/SO2
P37	11	32	P72/ASCK/$\overline{SCK2}$
P00	12	31	P17/ANI7
P01/INTP1	13	30	P16/ANI6
P02/INTP2	14	29	P15/ANI5
P03/INTP3	15	28	P14/ANI4
$\overline{RESET}$	16	27	P13/ANI3
VPP	17	26	P12/ANI2
X2	18	25	P11/ANI1
X1	19	24	P10/ANI0
VDD	20	23	AVss
AVDD	21	22	AVREF

Cautions 1. Connect VPP pin directly to Vss.
2. Connect AVDD pin to VDD.
3. Connect AVss pin to Vss.

• 44-pin plastic QFP (10 x 10 mm)

  μPD78P083GB(A)-3B4, μPD78P083GB(A)-3BS-MTX**Note**

Note Under planning

Pin layout (top view):

Top pins (left to right, 44–34): P11/ANI1, P10/ANI0, AV$_{SS}$, AV$_{REF}$, AV$_{DD}$, V$_{DD}$, X1, X2, V$_{PP}$, $\overline{\text{RESET}}$, NC

Left side (pins 1–11):
- 1: P12/ANI2
- 2: P13/ANI3
- 3: P14/ANI4
- 4: P15/ANI5
- 5: P16/ANI6
- 6: P17/ANI7
- 7: P72/ASCK/$\overline{\text{SCK2}}$
- 8: P71/T$_X$D/SO2
- 9: P70/R$_X$D/SI2
- 10: P101/TI6/TO6
- 11: P100/TI5/TO5

Right side (pins 33–23):
- 33: P03/INTP3
- 32: P02/INTP2
- 31: P01/INTP1
- 30: P00
- 29: P37
- 28: P36/BUZ
- 27: P35/PCL
- 26: P34
- 25: P33
- 24: P32
- 23: NC

Bottom pins (12–22): P50, P51, P52, P53, P54, V$_{SS}$, P55, P56, P57, P30, P31

Cautions 1. Connect V$_{PP}$ pin directly to V$_{SS}$.

2. Connect AV$_{DD}$ pin to V$_{DD}$.

3. Connect AV$_{SS}$ pin to V$_{SS}$.

4. Connect NC pin to V$_{SS}$ for noise protection (It can be left open).

ANI0 to ANI7	:	Analog Input	PCL	:	Programmable Clock
ASCK	:	Asynchronous Serial Clock	$\overline{\text{RESET}}$	:	Reset
AV$_{DD}$	:	Analog Power Supply	R$_X$D	:	Receive Data
AV$_{REF}$	:	Analog Reference Voltage	$\overline{\text{SCK2}}$	:	Serial Clock
AV$_{SS}$	:	Analog Ground	SI2	:	Serial Input
BUZ	:	Buzzer Clock	SO2	:	Serial Output
INTP1 to INTP3	:	Interrupt from Peripherals	TI5, TI6	:	Timer Input
NC	:	Non-connection	TO5, TO6	:	Timer Output
P00 to P03	:	Port 0	T$_X$D	:	Transmit Data
P10 to P17	:	Port 1	V$_{DD}$	:	Power Supply
P30 to P37	:	Port 3	V$_{PP}$	:	Programming Power Supply
P50 to P57	:	Port 5	V$_{SS}$	:	Ground
P70 to P72	:	Port 7	X1, X2	:	Crystal (Main System Clock)
P100, P101	:	Port 10			

(2) PROM programming mode

- 42-pin plastic shrink DIP (600 mil)
  μPD78P083CU(A)
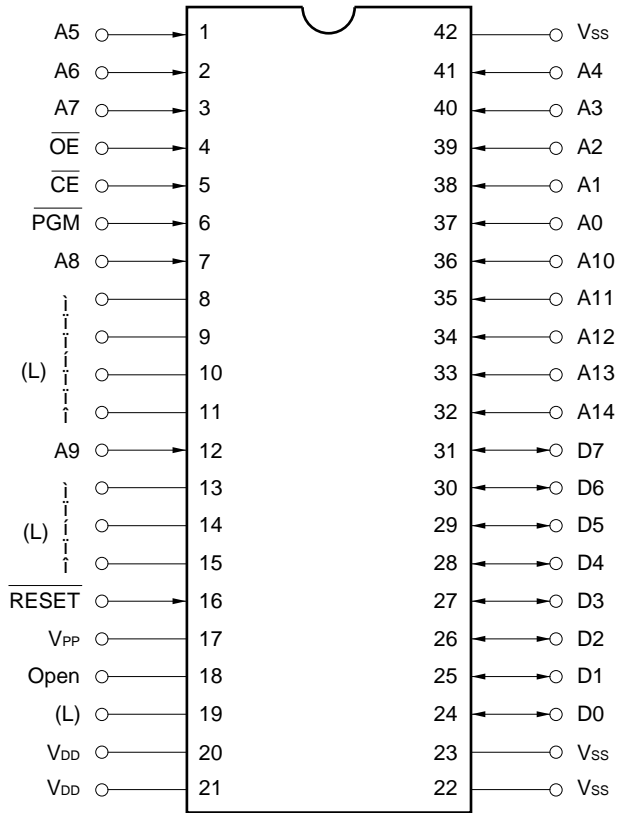
A5	1		42	Vss
A6	2		41	A4
A7	3		40	A3
$\overline{\text{OE}}$	4		39	A2
$\overline{\text{CE}}$	5		38	A1
$\overline{\text{PGM}}$	6		37	A0
A8	7		36	A10
	8		35	A11
	9		34	A12
(L)	10		33	A13
	11		32	A14
A9	12		31	D7
	13		30	D6
(L)	14		29	D5
	15		28	D4
$\overline{\text{RESET}}$	16		27	D3
VPP	17		26	D2
Open	18		25	D1
(L)	19		24	D0
VDD	20		23	Vss
VDD	21		22	Vss

Cautions 1. (L):   **Individually connect to Vss via a pull-down resistor.**
         2. Vss: **Connect to GND.**
         3. $\overline{\text{RESET}}$:   **Set to low level.**
         4. Open: **Leave open.**

- 44-pin plastic QFP (10 x 10 mm)
  µPD78P083GB(A)-3B4, µPD78P083GB(A)-3BS-MTX**Note**

  Note Under planning

Top pins (left to right): D1, D0, Vss, Vss, VDD, VDD, (L), Open, VPP, RESET, (L)
Pin numbers top: 44 43 42 41 40 39 38 37 36 35 34

Left side pins:
D2 — 1
D3 — 2
D4 — 3
D5 — 4
D6 — 5
D7 — 6
A14 — 7
A13 — 8
A12 — 9
A11 — 10
A10 — 11

Right side pins:
33 — (L)
32 — (L)
31 — (L)
30 — A9
29 — (L)
28 — (L)
27 — (L)
26 — (L)
25 — A8
24 — PGM
23 — (L)

Bottom pin numbers: 12 13 14 15 16 17 18 19 20 21 22
Bottom pins (left to right): A0, A1, A2, A3, A4, Vss, A5, A6, A7, OE, CE
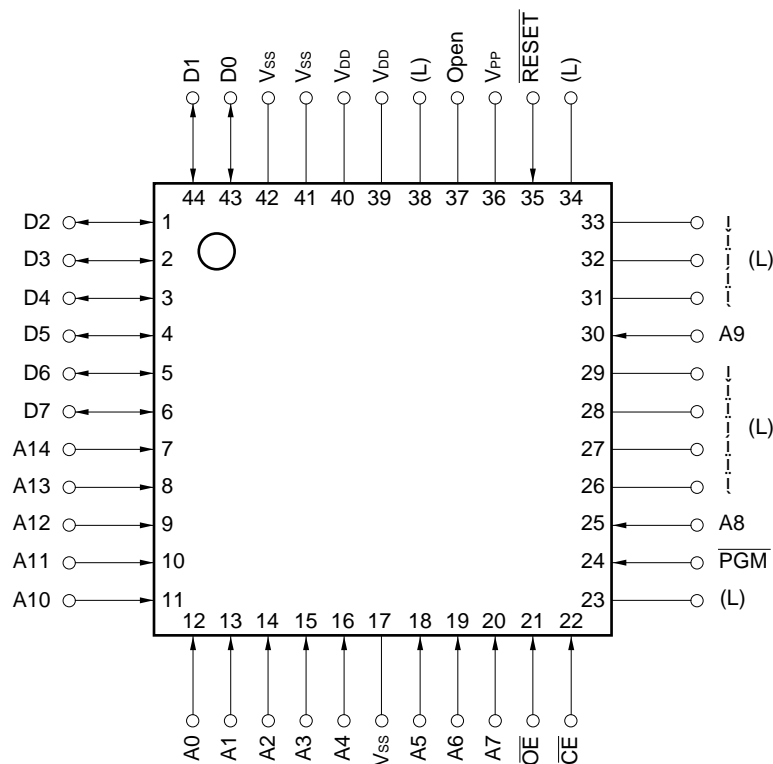
Cautions 1. (L): Individually connect to V_{SS} via a pull-down resistor.
2. V_{SS}: Connect to GND.
3. RESET: Set to low level.
4. Open: Leave open.

A0 to A14	: Address Bus	RESET	: Reset
CE	: Chip Enable	V_{DD}	: Power Supply
D0 to D7	: Data Bus	V_{PP}	: Programming Power Supply
OE	: Output Enable	V_{SS}	: Ground
PGM	: Program		

BLOCK DIAGRAM

P100/TI5/TO5 — 8-bit TIMER/ EVENT COUNTER 5

P101/TI6/TO6 — 8-bit TIMER/ EVENT COUNTER 6

WATCHDOG TIMER

SI2/R$_X$D/P70 — SERIAL INTERFACE 2
SO2/T$_X$D/P71
$\overline{SCK2}$/ASCK/P72

ANI0/P10- ANI7/P17 — A/D CONVERTER
AV$_{DD}$
AV$_{SS}$
AV$_{REF}$

INTP1/P01- INTP3/P03 — INTERRUPT CONTROL

BUZ/P36 — BUZZER OUTPUT

PCL/P35 — CLOCK OUTPUT CONTROL

78K/0 CPU CORE

PROM (24 KBytes)

DATA MEMORY (512 Bytes)

V$_{DD}$ V$_{SS}$ V$_{PP}$

PORT 0 — P00 / P01-P03

PORT 1 — P10-P17

PORT 3 — P30-P37

PORT 5 — P50-P57

PORT 7 — P70-P72

PORT 10 — P100, P101

SYSTEM CONTROL — $\overline{RESET}$ / X1 / X2

CONTENTS

1. DIFFERENCES BETWEEN THE μPD78P083(A) AND MASK ROM VERSIONS

The μPD78P083(A) is a single-chip microcontroller with an on-chip one-time PROM.

Setting the memory size switching register (IMS) makes the functions except the PROM specification identical to the mask ROM versions.

Table 1-1 shows differences between the PROM version (μPD78P083(A)) and mask ROM versions (μPD78081(A) and μPD78082(A)).

Table 1-1. Differences between the μPD78P083(A) and Mask ROM Versions

Parameter	µPD78P083(A)	Mask ROM Versions
Internal ROM type	One-time PROM/EPROM	Mask ROM
Internal ROM capacity	24 Kbytes	µPD78081(A) : 8 Kbytes
		µPD78082(A) : 16 Kbytes
Internal high-speed RAM capacity	512 bytes	µPD78081(A) : 256 bytes
		µPD78082(A) : 384 bytes
Internal ROM and internal high-speed RAM capacity change by memory size switching register (IMS)	Enable **Note**	Disable
IC pin	No	Yes
V$_{PP}$ pin	Yes	No
Electrical specifications	Refer to a data sheet of each product	

Note   The internal PROM becomes 24 Kbytes and the internal high-speed RAM becomes 512 bytes by the $\overline{\text{RESET}}$ input.

2. PIN FUNCTIONS

2.1 Pins in Normal Operating Mode

(1) Port pins

Pin Name	Input/Output	Function		After Reset	Alternate Function
P00	Input	Port 0	Input only	Input	—
P01	Input/output	4-bit input/output port	Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	INTP1
P02					INTP2
P03					INTP3
P10 to P17	Input/output	Port 1 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software. **Note**		Input	ANI0 to ANI7
P30-P34	Input/output	Port 3 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	—
P35					PCL
P36					BUZ
P37					—
P50 to P57	Input/output	Port 5 8-bit input/output port Can drive up to seven LEDs directly. Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	—
P70	Input/output	Port 7 3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{\text{SCK2}}$/ASCK
P100	Input/output	Port 10 2-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	TI5/TO5
P101					TI6/TO6

Note When P10/ANI0-P17/ANI7 pins are used as the analog inputs for the A/D converter, set the port 1 to the input mode. The on-chip pull-up resistor is automatically disabled.

(2) Non-port pins

Pin Name	Input/Output	Function	After Reset	Alternate Function
INTP1	Input	External interrupt input by which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P01
INTP2				P02
INTP3				P03
SI2	Input	Serial interface serial data input.	Input	P70/RxD
SO2	Output	Serial interface serial data output.	Input	P71/TxD
$\overline{SCK2}$	Input/Output	Serial interface serial clock input/output.	Input	P72/ASCK
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/$\overline{SCK2}$
TI5	Input	External count clock input to 8-bit timer (TM5).	Input	P100/TO5
TI6		External count clock input to 8-bit timer (TM6).		P101/TO6
TO5	Output	8-bit timer output.	Input	P100/TI5
TO6				P101/TI6
PCL	Output	Clock output. (for main system clock trimming)	Input	P35
BUZ	Output	Buzzer output.	Input	P36
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AV$_{REF}$	Input	A/D converter reference voltage input.	–	–
AV$_{DD}$	–	A/D converter analog power supply. Connected to V$_{DD}$.	–	–
$\overline{AV_{SS}}$	–	A/D converter ground potential. Connected to V$_{SS}$.	–	–
$\overline{RESET}$	Input	System reset input.	–	–
X1	Input	Main system clock oscillation crystal connection.	–	–
X2	–		–	–
V$_{DD}$	–	Positive power supply.	–	–
V$_{PP}$	–	High-voltage applied during program write/verification. Connected directly to V$_{SS}$ in normal operating mode.	–	–
V$_{SS}$	–	Ground potential.	–	–
NC	–	Does not internally connected. Connect to V$_{SS}$. (It can be left open)	–	–

2.2 Pins in PROM Programming Mode

Pin Name	Input/Output	Function
$\overline{RESET}$	Input	PROM programming mode setting
		When +5 V or +12.5 V is applied to the V$_{PP}$ pin and a low-level signal is applied to the $\overline{RESET}$ pin, this chip is set in the PROM programming mode.
V$_{PP}$	Input	PROM programming mode setting and high-voltage applied during program write/verification.
A0 to A14	Input	Address bus
D0-D7	Input/output	Data bus
$\overline{CE}$	Input	PROM enable input/program pulse input
$\overline{OE}$	Input	Read strobe input to PROM
$\overline{PGM}$	Input	Program/program inhibit input in PROM programming mode.
V$_{DD}$	—	Positive power supply
V$_{SS}$	—	Ground potential

2.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins

Types of input/output circuits of the pins and recommeded connection of unused pins are shown in Table 2-1.
For the configuration of each type of input/output circuit, see Figure 2-1.

Table 2-1. Type of Input/Output Circuit of Each Pin

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection for Unused Pins
P00	2	Input	Connect to V$_{SS}$.
P01/INTP1	8-A	Input/Output	Independently connect to V$_{SS}$ via a resistor.
P02/INTP2			
P03/INTP3			
P10/ANI0 to P17/ANI7	11	Input/Output	Independently connect to V$_{DD}$ or V$_{SS}$ via a resistor.
P30 to P32	5-A		
P33, P34	8-A		
P35/PCL	5-A		
P36/BUZ			
P37			
P50 to P57	5-A		
P70/SI2/RxD	8-A		
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P100/TI5/TO5	8-A		
P101/TI6/TO6			
$\overline{RESET}$	2	Input	–
AV$_{REF}$	–	–	Connect to V$_{SS}$.
AV$_{DD}$			Connect to V$_{DD}$.
AV$_{SS}$			Connect to V$_{SS}$.
V$_{PP}$			Connect directly to V$_{SS}$.
NC			Connect to V$_{SS}$ (can leave open)

Figure 2-1. Types of Pin Input/Output Circuits

Type 2

IN ◯────▷────→

Schmitt-triggered input with hysteresis characteristics

Type 8-A

pull-up enable
data
output disable
IN/OUT

Type 5-A

pull-up enable
data
output disable
input enable
IN/OUT

Type 11

pull-up enable
data
output disable
Comparator
V_REF (threshold voltage)
input enable
IN/OUT
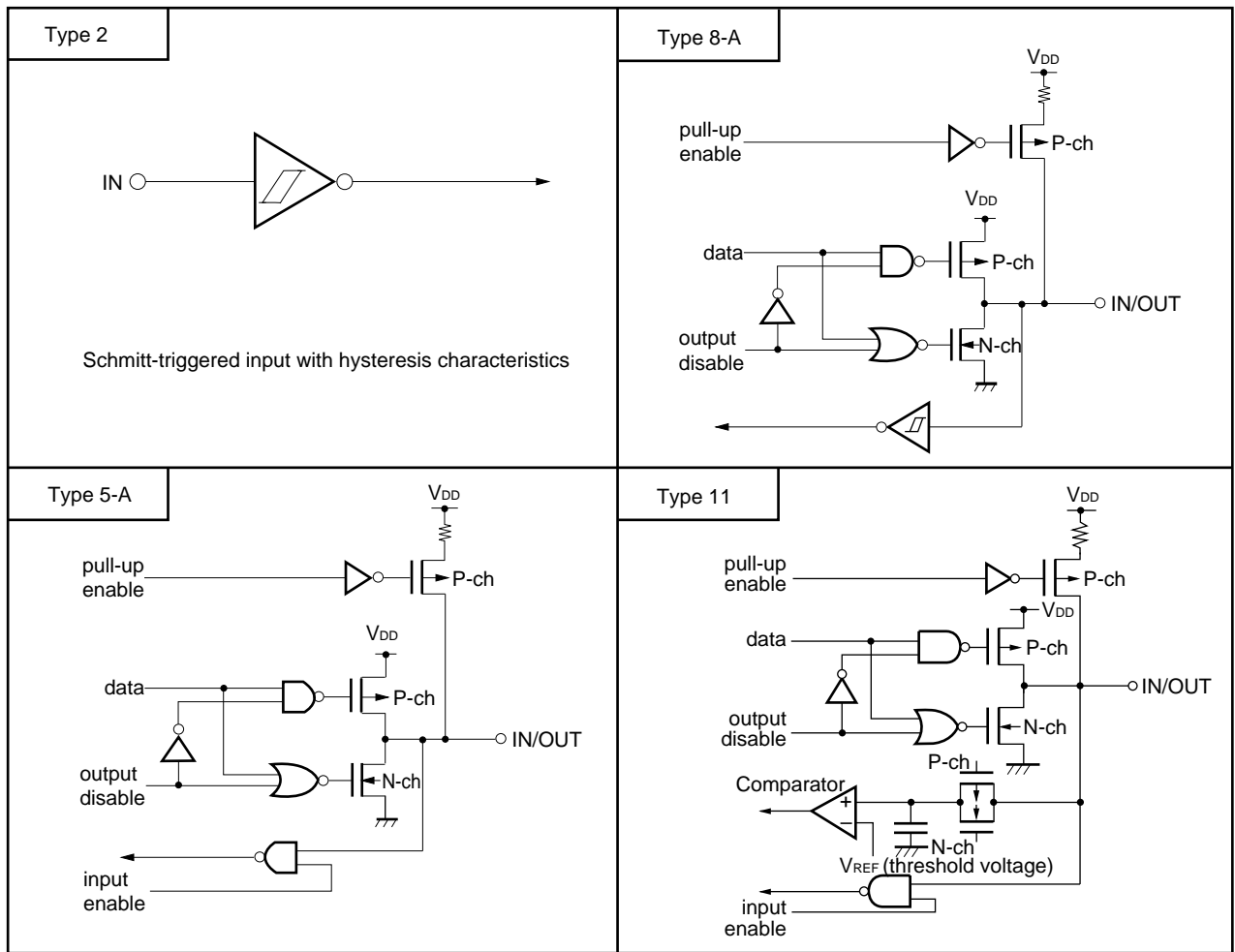
3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this memory size switching register (IMS), it is possible to get the same memory mapping as that of the mask ROM versions with a different internal memory (ROM, RAM).

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to 46H.

Figure 3-1. Internal Memory Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	46H	R/W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	0	1	0	8 Kbytes
0	1	0	0	16 Kbytes
0	1	1	0	24 Kbytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-Speed RAM Capacity
0	1	0	512 bytes
0	1	1	384 bytes
1	0	0	256 bytes
Other than above			Setting prohibited

Table 3-1 shows the setting values of IMS which make the memory mapping the same as that of the mask ROM version.

Table 3-1. Internal Memory Size Switching Register Setting Values

Target Mask ROM Versions	IMS Setting Value
µPD78081(A)	82H
µPD78082(A)	64H

4. PROM PROGRAMMING

The µPD78P083(A) has an internal 24-Kbyte PROM as a program memory. For programming, set the PROM programming mode with the VPP and $\overline{\text{RESET}}$ pins. For the connection of unused pins, refer to **"PIN CONFIGURA-TIONS (TOP VIEW) (2) PROM programming mode."**

Caution   Programs must be written in addresses 0000H to 5FFFH (The last address 5FFFH must be specified). They cannot be written by a PROM programmer which cannot specify the write address.

4.1 Operating Modes

When +5 V or +12.5 V is applied to the VPP pin and a low-level signal is applied to the $\overline{\text{RESET}}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 4-1 when the $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{PGM}}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 4-1. Operating Modes of PROM Programming

Pin / Operating Mode	$\overline{\text{RESET}}$	VPP	VDD	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				x	H	H	High-impedance
				x	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	x	High-impedance
Standby				H	x	x	High-impedance

x : L or H

(1) Read mode

Read mode is set if $\overline{CE}$ = L, $\overline{OE}$ = L is set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE}$ = H is set.

Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD78P083(A)s are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE}$ = H is set.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

If programming is not performed by a one-time program pulse, X times (X - 10) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1-ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed if OE = L is set.

If programming is not performed by a one-time program pulse, X times (X - 10) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L are set.

In this mode, check if a write operation is performed correctly after the write.

(8) Program inhibit mode

Program inhibit mode is used when the $\overline{OE}$ pin, V$_{PP}$ pin, and D0-D7 pins of multiple μPD78P083(A)s are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

4.2   PROM Write Procedure

Figure 4-1. Page Program Mode Flow Chart


```
                          ┌─────────────────┐
                          │      Start      │
                          └─────────────────┘
                          ┌─────────────────┐
                          │   Address = G   │
                          └─────────────────┘
                          ┌───────────────────────────┐
                          │ VDD = +6.5 V, VPP = +12.5 V│
                          └───────────────────────────┘
                          ┌─────────────────┐
                          │      X = 0      │
                          └─────────────────┘
                          ┌─────────────────┐
                          │      Latch      │
                          └─────────────────┘
                          ┌─────────────────┐
                          │ Address = Address + 1 │
                          └─────────────────┘
                          ┌─────────────────┐
                          │      Latch      │
                          └─────────────────┘
                          ┌─────────────────┐
                          │ Address = Address + 1 │
                          └─────────────────┘
                          ┌─────────────────┐
                          │      Latch      │
                          └─────────────────┘
                          ┌─────────────────┐
                          │ Address = Address + 1 │
                          └─────────────────┘
                          ┌─────────────────┐
                          │      Latch      │
                          └─────────────────┘
   ┌──────────────────┐   ┌─────────────────┐         No
   │ Address = Address + 1 │   │    X = X + 1    │◄──────────────┐
   └──────────────────┘   └─────────────────┘       ◇ X = 10 ?  │ Yes
                          ┌─────────────────┐         └────┘
                          │ 0.1-ms program pulse │
                          └─────────────────┘
                              ◇ Verify 4 bytes  ── Fail ──┘
                                   │ Pass
          No ──── ◇ Address = N ?
                                   │ Yes
                          │ VDD = 4.5 to 5.5 V, VPP = VDD │
            Pass ──── ◇ Verify all bytes ── Fail ──►
                                   │ All Pass
              ┌─────────────┐           ┌──────────────────┐
              │  Write end  │           │ Defective product │
              └─────────────┘           └──────────────────┘
```
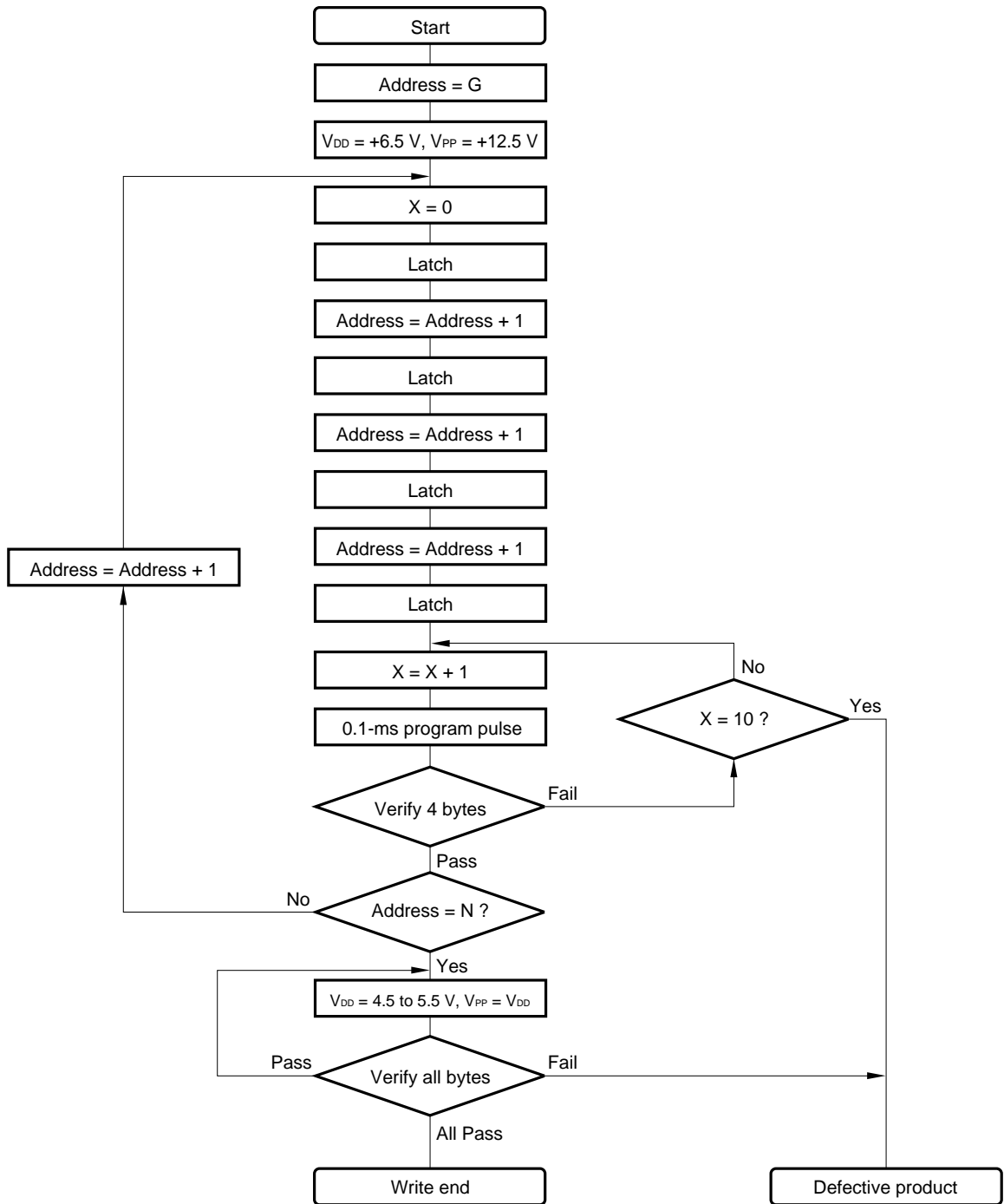
G = Start address

N = Program last address

Figure 4-2. Page Program Mode Timing
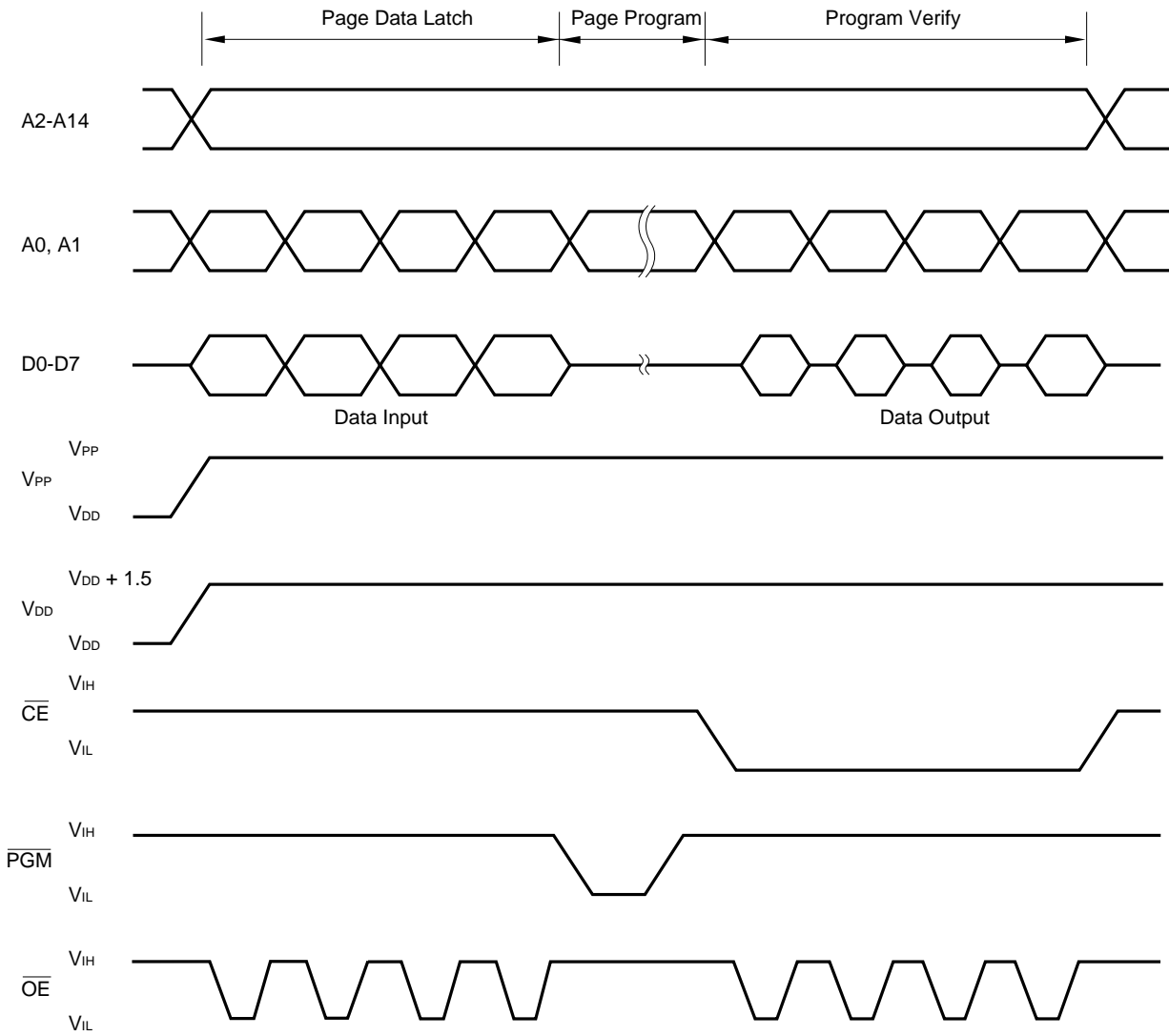
Figure 4-3. Byte Program Mode Flow Chart

```
                          ┌─────────────┐
                          │    Start    │
                          └─────────────┘
                          ┌─────────────┐
                          │ Address = G │
                          └─────────────┘
                          ┌───────────────────────────┐
                          │ VDD = +6.5 V, VPP = +12.5 V│
                          └───────────────────────────┘
                          ┌─────────────┐
                          │    X = 0    │
                          └─────────────┘
                          ┌─────────────┐                           No
                          │  X = X + 1  │
                          └─────────────┘              ╱╲
    ┌──────────────────┐  ┌──────────────────┐        ╱    ╲        Yes
    │Address = Address+1│  │0.1-ms program pulse│     ╱ X = 10?╲ ──────
    └──────────────────┘  └──────────────────┘       ╲        ╱
                               ╱╲              Fail    ╲    ╱
                              ╱    ╲  ──────────────────  ╲╱
                             ╱Verify ╲
                             ╲        ╱
                              ╲    ╱  Pass
                               ╲╱
              No             ╱╲
         ──────────────────╱    ╲
                          ╱Address╲
                          ╲ = N ? ╱
                           ╲    ╱
                            ╲╱  Yes
                          ┌──────────────────────────┐
                          │VDD = 4.5 to 5.5 V, VPP = VDD│
          Pass            └──────────────────────────┘  Fail
       ──────────────       ╱╲  ──────────────────────────────
                           ╱    ╲
                          ╱Verify  ╲
                          ╲all bytes╱
                           ╲     ╱
                            ╲ ╱  All Pass
                   ┌─────────────┐              ┌──────────────────┐
                   │  Write end  │              │ Defective product│
                   └─────────────┘              └──────────────────┘
```
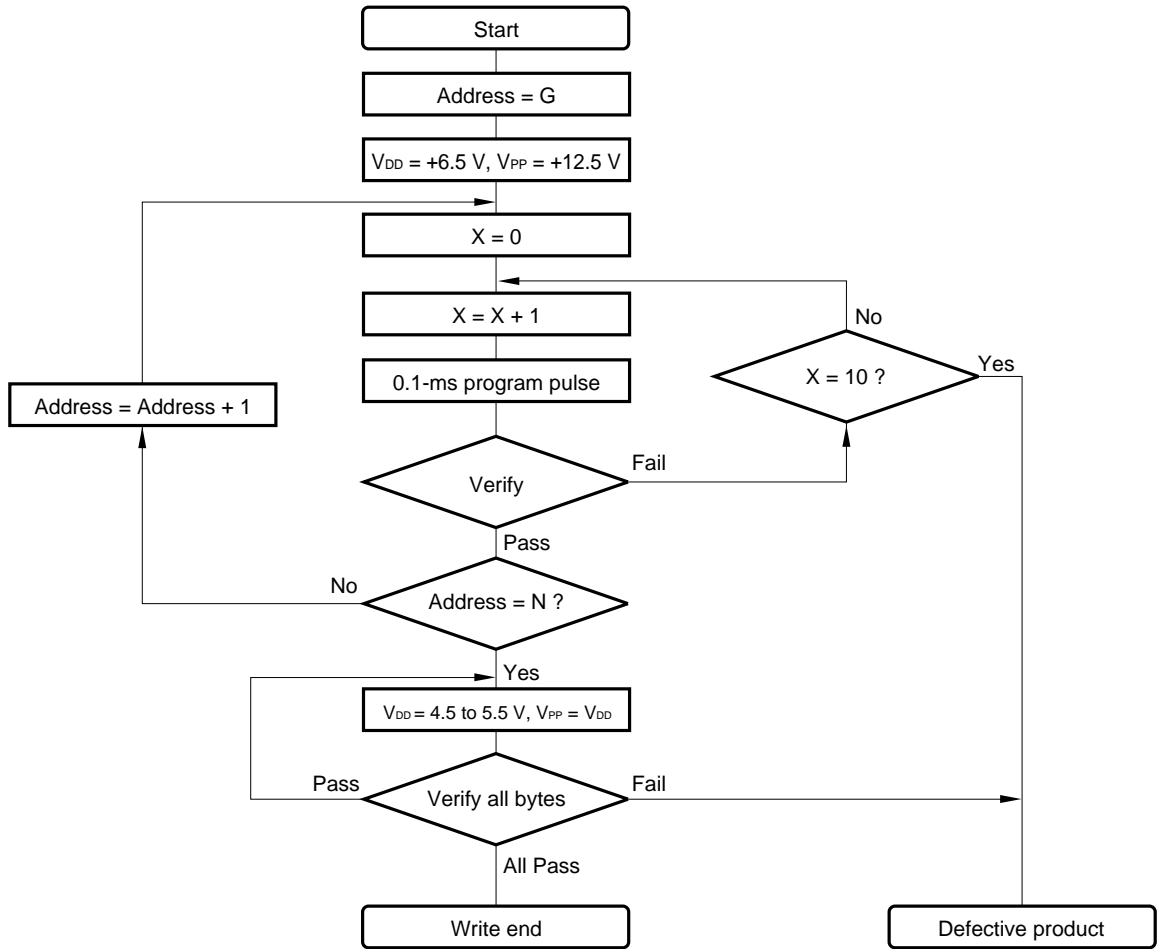
G = Start address

N = Program last address

Figure 4-4. Byte Program Mode Timing
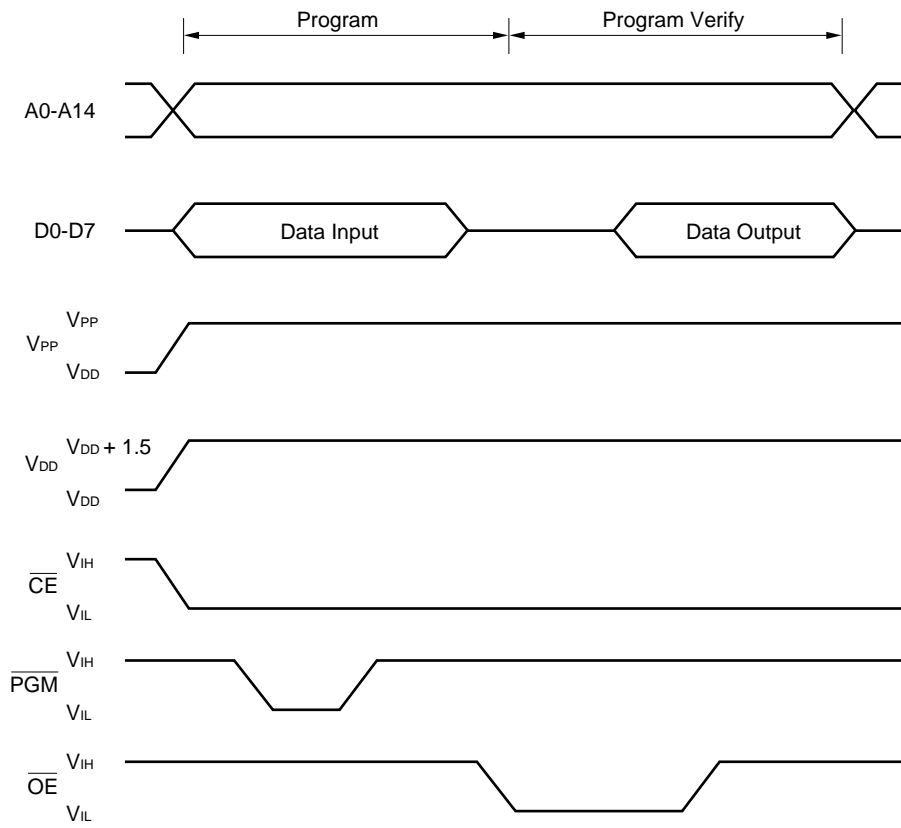
Cautions 1. V_{DD} should be applied before V_{PP} and removed after V_{PP}.

2. V_{PP} must not exceed +13.5 V including overshoot.

3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

4.3 PROM Read Procedure

The contents of PROM are readable to the external data bus (D0-D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the VPP pin, and connect all other unused pins as shown in **"PIN CONFIGURATIONS (TOP VIEW) (2) PROM programming mode".**

(2) Supply +5 V to the VDD and VPP pins.

(3) Input address of read data into the A0 to A14 pins.

(4) Read mode

(5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 4-5.

Figure 4-5. PROM Read Timings
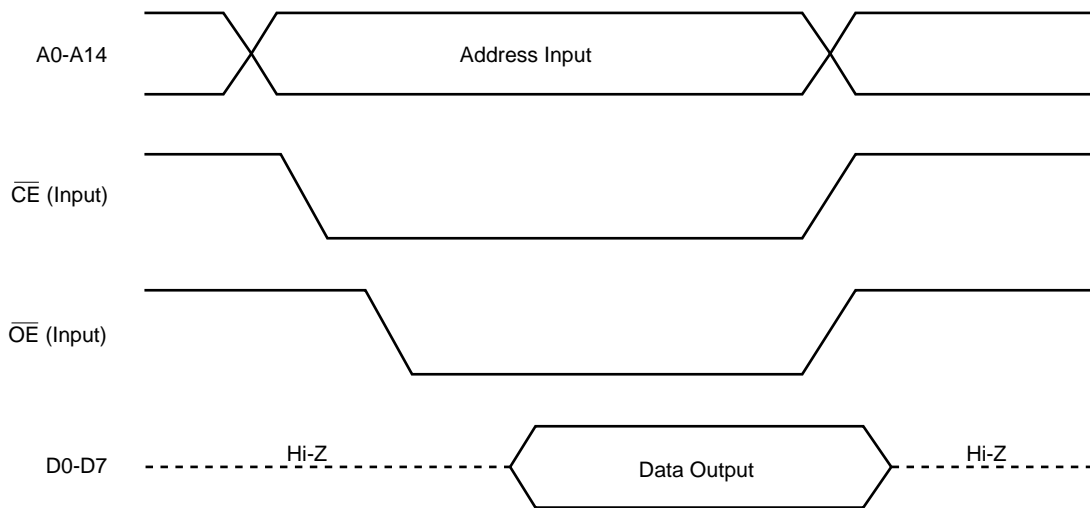
5. ONE-TIME PROM VERSION SCREENING

The one-time PROM version (μPD78P083CU(A), 78P083GB(A)-3B4, 78P083GB(A)-3BS-MTX**Note**) cannot be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Note   Under planning

Storage Temperature	Storage Time
125°C	24 hours

NEC offers for an additional fee one-time PROM writing to marking, screening, and verify for products designated as QTOP Microcontroller. A fee-charged service for the μPD78P083(A) is under planning. Consult an NEC sales representative for details.

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ($T_A = 25°C$)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			−0.3 to +7.0	V
	V_{PP}			−0.3 to +13.5	V
	AV_{DD}			−0.3 to V_{DD} + 0.3	V
	AV_{REF}			−0.3 to V_{DD} + 0.3	V
	AV_{SS}			−0.3 to +0.3	V
Input voltage	V_{I1}			−0.3 to V_{DD} + 0.3	
	V_{I2}	A9	PROM programming mode	−0.3 to +13.5	V
Output voltage	V_O			−0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pins	AV_{SS} − 0.3 to AV_{REF} + 0.3	V
Output current, high	I_{OH}	Per pin		−10	mA
		Total for P10 to P17, P50 to P54, P70 to P72, P100, P101		−15	mA
		Total for P01 to P03, P30 to P37, P55 to P57		−15	mA
Output current, low	I_{OL} **Note**	Per pin	Peak value	30	mA
			r.m.s. value	15	mA
		Total for P50 to P54	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P55 to P57	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P10 to P17, P70 to P72, P100, P101	Peak value	50	mA
			r.m.s. value	20	mA
		Total for P01 to P03, P30 to P37	Peak value	50	mA
			r.m.s. value	20	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Note The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] $\times \sqrt{\text{Duty}}$

Caution If the absolute maximum rating of even one of the above parameters is exceeded, the quality of the product may be degraded. The absolute maximum ratings are therefore the rated values that may, if exceeded, physically damage the product. Be sure to use the product with all the absolute maximum ratings observed.
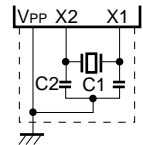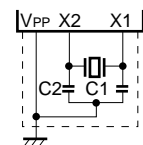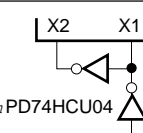
Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz, Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz, Unmeasured pins returned to 0 V.	P01 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101			15	pF

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

Main System Clock Oscillator Characteristics (T_A = −40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator	V_{PP} X2 X1, C2 C1	Oscillation frequency (fX) Note 1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time Note 2	After V_{DD} came to MIN. of oscillation voltage range			4	ms
Crystal resonator	V_{PP} X2 X1, C2 C1	Oscillation frequency (fX) Note 1		1.0		5.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock	X2 X1, μPD74HCU04	X1 input frequency (fX) Note 1		1.0		5.0	MHz
		X1 input high- and low-level widths (t_{XH}, t_{XL})		85		500	ns

Notes 1. Only the oscillator characteristics are shown. For the instruction execution time, refer to **AC Characteristics**.
    2. Time required for oscillation to stabilize after a reset or the STOP mode has been released.

Caution **When using the oscillation circuit of the main system clock, wire the portion enclosed in broken lines in the figures as follows to avoid adverse influences on the wiring capacitance:**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}.**
- **Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

DC Characteristics (T$_A$ = −40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P10 to P17, P30 to P32, P35 to P37, P50 to P57, P71	V$_{DD}$ = 2.7 to 5.5 V	0.7V$_{DD}$		V$_{DD}$	V
				0.8V$_{DD}$		V$_{DD}$	V
	V$_{IH2}$	P00 to P03, P33, P34, P70, P72, P100, P101, $\overline{RESET}$	V$_{DD}$ = 2.7 to 5.5 V	0.8V$_{DD}$		V$_{DD}$	V
				0.85V$_{DD}$		V$_{DD}$	V
	V$_{IH3}$	X1, X2	V$_{DD}$ = 2.7 to 5.5 V	V$_{DD}$ − 0.5		V$_{DD}$	V
				V$_{DD}$ − 0.2		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P10 to P17, P30 to P32, P35 to P37, P50 to P57, P71	V$_{DD}$ = 2.7 to 5.5 V	0		0.3V$_{DD}$	V
				0		0.2V$_{DD}$	V
	V$_{IL2}$	P00 to P03, P33, P34, P70, P72, P100, P101, $\overline{RESET}$	V$_{DD}$ = 2.7 to 5.5 V	0		0.2V$_{DD}$	V
				0		0.15V$_{DD}$	V
	V$_{IL3}$	X1, X2	V$_{DD}$ = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
Output voltage, high	V$_{OH}$	V$_{DD}$ = 4.5 to 5.5 V, I$_{OH}$ = −1 mA		V$_{DD}$ − 1.0			V
		I$_{OH}$ = −100 μA		V$_{DD}$ − 0.5			V
Output voltage, low	V$_{OL}$	P50 to P57	V$_{DD}$ = 2.0 to 4.5 V, I$_{OL}$ = 10 mA			0.8	V
			V$_{DD}$ = 4.5 to 5.5 V, I$_{OL}$ = 15 mA		0.4	2.0	V
		P01 to P03, P10 to P17, P30 to P37, P70 to P72, P100, P101	V$_{DD}$ = 4.5 to 5.5 V, I$_{OL}$ = 1.6 mA			0.4	V
			I$_{OL}$ = 400 μA			0.5	V
Input-leak current, high	I$_{LIH1}$	V$_{IN}$ = V$_{DD}$	P00 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101, $\overline{RESET}$			3	μA
	I$_{LIH2}$		X1, X2			20	μA
Input-leak current, low	I$_{LIL1}$	V$_{IN}$ = 0 V	P00 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101, $\overline{RESET}$			−3	μA
	I$_{LIL2}$		X1, X2			−20	μA
Output leak current, high	I$_{LOH}$	V$_{OUT}$ = V$_{DD}$				3	μA
Output leak current, low	I$_{LOL}$	V$_{OUT}$ = 0 V				−3	μA
Software pull-up resistor	R	V$_{IN}$ = 0 V	P01 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101	15	40	90	kΩ

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current [1]	I_{DD1}	5.0-MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz) [2]	V_{DD} = 5.0 V ± 10% [4]		5.4	16.2	mA
			V_{DD} = 3.0 V ± 10% [5]		0.8	2.4	mA
			V_{DD} = 2.0 V ± 10% [5]		0.45	1.35	mA
		5.0-MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz) [3]	V_{DD} = 5.0 V ± 10% [4]		9.5	28.5	mA
			V_{DD} = 3.0 V ± 10% [5]		1.0	3.0	mA
	I_{DD2}	5.0-MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz) [2]	V_{DD} = 5.0 V ± 10%		1.4	4.2	mA
			V_{DD} = 3.0 V ± 10%		0.5	1.5	mA
			V_{DD} = 2.0 V ± 10%		280	840	μA
		5.0-MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz) [3]	V_{DD} = 5.0 V ± 10%		1.6	4.8	mA
			V_{DD} = 3.0 V ± 10%		0.65	1.95	mA
	I_{DD3}	STOP mode	V_{DD} = 5.0 V ± 10%		0.1	30	μA
			V_{DD} = 3.0 V ± 10%		0.05	10	μA
			V_{DD} = 2.0 V ± 10%		0.05	10	μA

Notes 1. Not including AV_{REF}, AV_{DD} currents or port currents (including current flowing into internal pull-up resistors).

2. f_{XX} = f_X/2 operation (when oscillation mode selection register (OSMS) is set to 00H).

3. f_{XX} = f_X operation (when oscillation mode selection register (OSMS) is set to 01H).

4. High-speed mode operation (when processor clock control register (PCC) is set to 00H).

5. Low-speed mode operation (when processor clock control register (PCC) is set to 04H).

Remark f_{XX}: Main system clock frequency (f_X or f_X/2)

f_X: Main system clock oscillation frequency

AC Characteristics

(1) Basic Operation (T$_A$ = −40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T$_{CY}$	f$_{XX}$ = f$_X$/2 **Note1**	V$_{DD}$ = 2.7 to 5.5 V	0.8		64	μs
				2.0		64	μs
		f$_{XX}$ = f$_X$/ **Note2**	3.5 V - V$_{DD}$ - 5.5 V	0.4		32	μs
			2.7 V - V$_{DD}$ < 3.5 V	0.8		32	μs
TI5, TI6 input frequency	f$_{TI}$	V$_{DD}$ = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI5, TI6 input high-/ low-level widths	t$_{TIH}$, t$_{TIL}$	V$_{DD}$ = 4.5 to 5.5 V		100			ns
				1.8			μs
Interrupt input high-/ low-level widths	t$_{INTH}$, t$_{INTL}$	V$_{DD}$ = 2.7 to 5.5 V		10			μs
				20			μs
$\overline{RESET}$ low-level width	t$_{RSL}$	V$_{DD}$ = 2.7 to 5.5 V		10			μs
				20			μs

Notes 1. When oscillation mode selection register (OSMS) is set to 00H.
　　　　2. When OSMS is set to 01H.

Remark f$_{XX}$: Main system clock frequency (f$_X$ or f$_X$/2)
　　　　f$_X$: Main system clock oscillation frequency

T$_{CY}$ vs V$_{DD}$
(Main System Clock f$_{XX}$ = f$_X$/2 Operation)
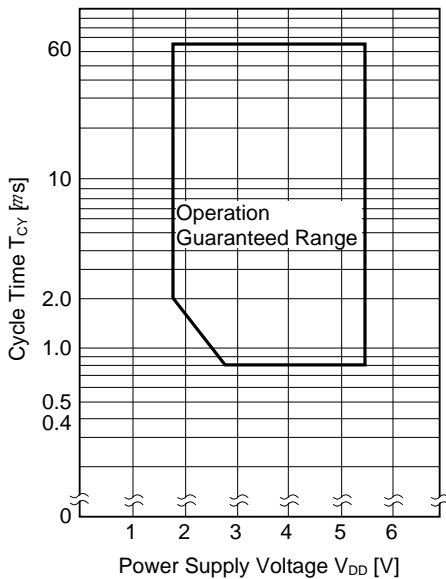
T$_{CY}$ vs V$_{DD}$
(Main System Clock f$_{XX}$ = f$_X$ Operation)
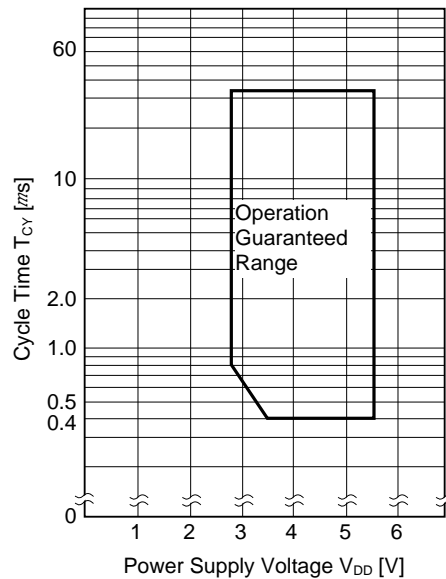
(2) Serial Interface (T_A = −40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wired serial I/O mode ($\overline{SCK2}$ ··· internal clock output)

| Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY1}	4.5 V - V_{DD} - 5.5 V	800			ns
		2.7 V - V_{DD} < 4.5 V	1600			ns
		2.0 V - V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK2}$ high-/low-level width	t_{KH1},	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2–50			ns
	t_{KL1}		t_{KCY1}/2–100			ns
SI2 setup time (to $\overline{SCK2}$ ↑)	t_{SIK1}	4.5 V - V_{DD} - 5.5 V	100			ns
		2.7 V - V_{DD} < 4.5 V	150			ns
		2.0 V - V_{DD} < 2.7 V	300			ns
			400			ns
SI2 hold time (from $\overline{SCK2}$ ↑)	t_{KSI1}		400			ns
$\overline{SCK2}$ ↓ → SO2 output delay time	t_{KSO1}	C = 100 pF**Note**			300	ns

Note C is the $\overline{SCK2}$, SO2 output line load capacitance.

(b) 3-wired serial I/O mode ($\overline{SCK2}$ ··· external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY2}	4.5 V - V_{DD} - 5.5 V		800			ns
		2.7 V - V_{DD} < 4.5 V		1600			ns
		2.0 V - V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK2}$ high-/low-level width	t_{KH2},	4.5 V - V_{DD} - 5.5 V		400			ns
	t_{KL2}	2.7 V - V_{DD} < 4.5 V		800			ns
		2.0 V - V_{DD} < 2.7 V		1600			ns
				2400			ns
SI2 setup time (to $\overline{SCK2}$ ↑)	t_{SIK2}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI2 hold time (from $\overline{SCK2}$ ↑)	t_{KSI2}			400			ns
$\overline{SCK2}$ ↓ → SO2 output delay time	t_{KSO2}	C = 100 pF**Note**	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK2}$ rise, fall time	t_{R2}, t_{F2}					1000	ns

Note C is the SO2 output line load capacitance.

(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V - V_{DD} - 5.5 V			78125	bps
		2.7 V - V_{DD} < 4.5 V			39063	bps
		2.0 V - V_{DD} < 2.7 V			19531	bps
					9766	bps

(d) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	4.5 V - V_{DD} - 5.5 V	800			ns
		2.7 V - V_{DD} < 4.5 V	1600			ns
		2.0 V - V_{DD} < 2.7 V	3200			ns
			4800			ns
ASCK high-/low-level width	t_{KH3}, t_{KL3}	4.5 V - V_{DD} - 5.5 V	400			ns
		2.7 V - V_{DD} < 4.5 V	800			ns
		2.0 V - V_{DD} < 2.7 V	1600			ns
			2400			ns
Transfer rate		4.5 V - V_{DD} - 5.5 V			39063	bps
		2.7 V - V_{DD} < 4.5 V			19531	bps
		2.0 V - V_{DD} < 2.7 V			9766	bps
					6510	bps
ASCK rise, fall time	t_{R3}, t_{F3}				1000	ns

AC Timing Test Point (Excluding X1 Input)

$$0.8\ V_{DD}$$
$$0.2\ V_{DD}$$
Test Points
$$0.8\ V_{DD}$$
$$0.2\ V_{DD}$$

Clock Timing

$1/f_x$

t_{XL} t_{XH}

X1 Input

V_{IH3} (MIN.)
V_{IL3} (MAX.)

TI Timing

$1/f_{TI}$

t_{TIL} t_{TIH}

TI5, TI6
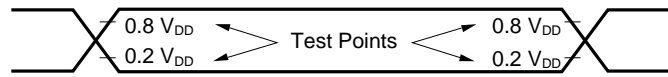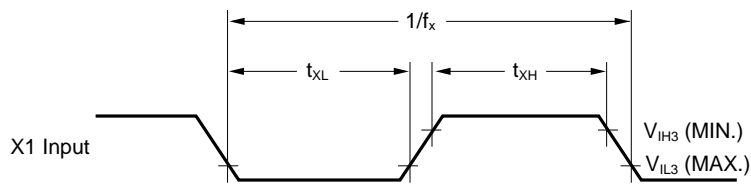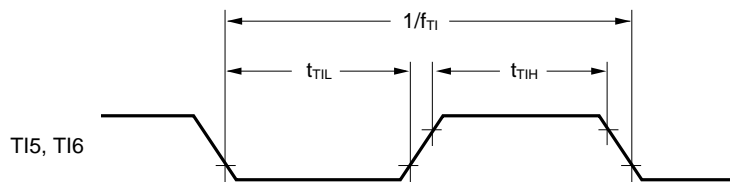
Serial Transfer Timing

3-wired serial I/O mode:
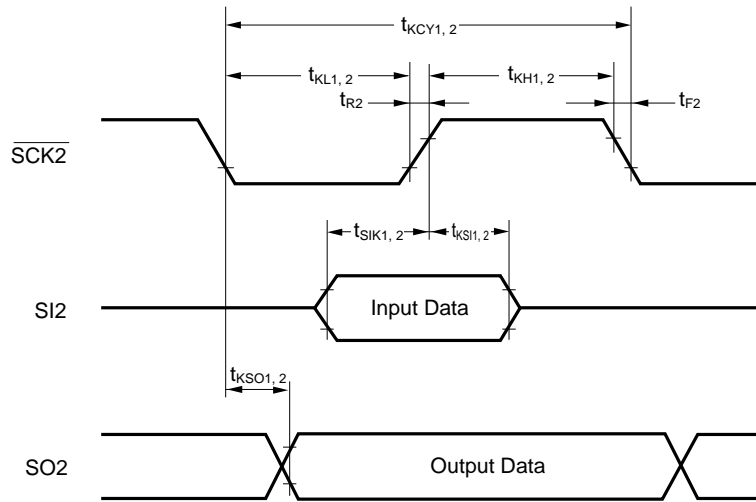
UART mode (external clock input):
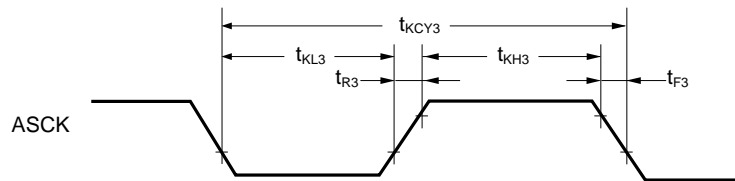
A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error **Note**		2.7 V - AV_{REF} - AV_{DD}			1.4	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		$12/f_{XX}$			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		2.7		AV_{DD}	V
AV_{REF}-AV_{SS} resistance	R_{AIREF}		4	14		kΩ

Note Excluding quantization error (±1/2 LSB). Shown as a percentage of the full scale value.

Remark f_{XX}: Main system clock frequency (f_X or $f_X/2$)
     f_X: Main system clock oscillation frequency

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = −40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt		**Note**		ms

Note $2^{12}/f_{XX}$ or $2^{14}/f_{XX}$ to $2^{17}/f_{XX}$ can be selected by bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time selection register (OSTS).

Remark f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency

Data Retention Timing (STOP mode released by $\overline{RESET}$)
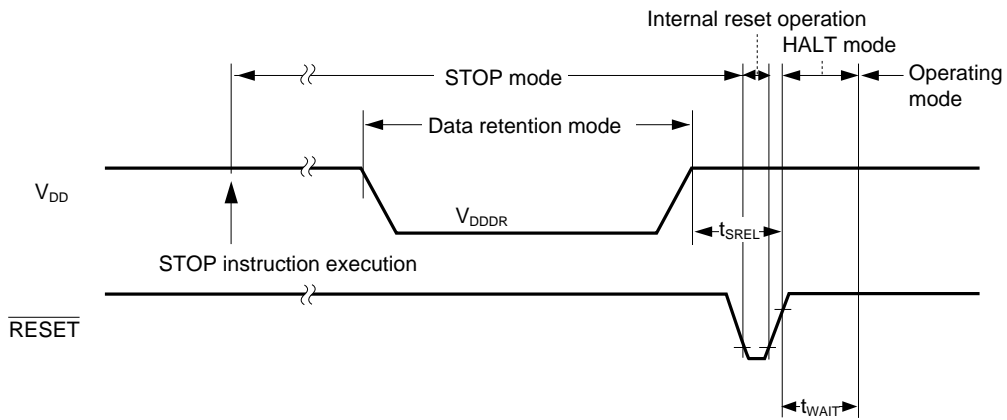
Data Retention Timing (Standby release signal: STOP mode released by interrupt request signal)
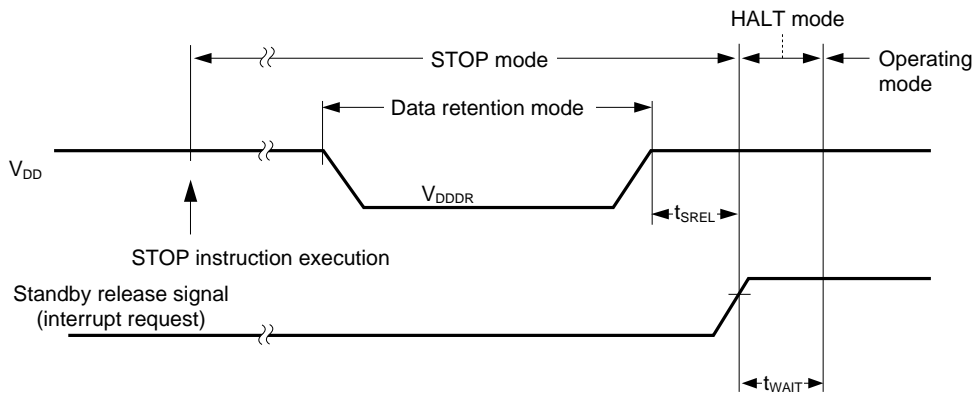
Interrupt Input Timing

INTP1-INTP3

t_{INTL} t_{INTH}
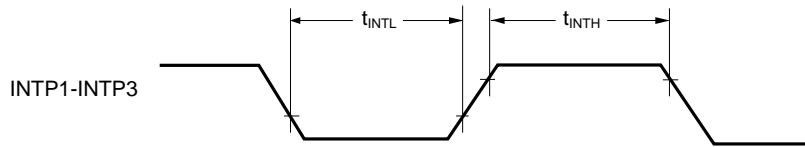
RESET Input Timing

$\overline{RESET}$

t_{RSL}
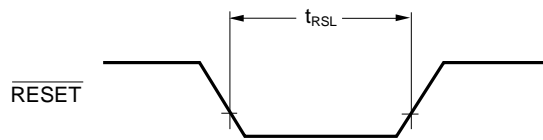
PROM Programming Characteristics

DC Characteristics

(**1**) **PROM Write Mode** (T$_A$ = 25 ±5½C, V$_{DD}$ = 6.5 ±0.25 V, V$_{PP}$ = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH}$	V$_{IH}$		0.7V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL}$	V$_{IL}$		0		0.3V$_{DD}$	V
Output voltage, high	V$_{OH}$	V$_{OH}$	I$_{OH}$ = −1 mA	V$_{DD}$ − 1.0			V
Output voltage, low	V$_{OL}$	V$_{OL}$	I$_{OL}$ = 1.6 mA			0.4	V
Input leakage current	I$_{LI}$	I$_{LI}$	0 - V$_{IN}$ - V$_{DD}$	−10		+10	μA
V$_{PP}$ supply voltage	V$_{PP}$	V$_{PP}$		12.2	12.5	12.8	V
V$_{DD}$ supply voltage	V$_{DD}$	V$_{CC}$		6.25	6.5	6.75	V
V$_{PP}$ supply current	I$_{PP}$	I$_{PP}$	$\overline{PGM}$ = V$_{IL}$			50	mA
V$_{DD}$ supply current	I$_{DD}$	I$_{CC}$				50	mA

(**2**) **PROM Read Mode** (T$_A$ = 25 ±5½C, V$_{DD}$ = 5.0 ±0.5 V, V$_{PP}$ = V$_{DD}$ ±0.6 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH}$	V$_{IH}$		0.7V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL}$	V$_{IL}$		0		0.3V$_{DD}$	V
Output voltage, high	V$_{OH1}$	V$_{OH1}$	I$_{OH}$ = −1 mA	V$_{DD}$ − 1.0			V
	V$_{OH2}$	V$_{OH2}$	I$_{OH}$ = −100 μA	V$_{DD}$ − 0.5			V
Output voltage, low	V$_{OL}$	V$_{OL}$	I$_{OL}$ = 1.6 mA			0.4	V
Input leakage current	I$_{LI}$	I$_{LI}$	0 - V$_{IN}$ - V$_{DD}$	−10		+10	μA
Output leakage current	I$_{LO}$	I$_{LO}$	0 - V$_{OUT}$ - V$_{DD}$, $\overline{OE}$ = V$_{IH}$	−10		+10	μA
V$_{PP}$ supply voltage	V$_{PP}$	V$_{PP}$		V$_{DD}$ − 0.6	V$_{DD}$	V$_{DD}$ + 0.6	V
V$_{DD}$ supply voltage	V$_{DD}$	V$_{CC}$		4.5	5.0	5.5	V
V$_{PP}$ supply current	I$_{PP}$	I$_{PP}$	V$_{PP}$ = V$_{DD}$			100	μA
V$_{DD}$ supply current	I$_{DD}$	I$_{CCA1}$	$\overline{CE}$ = V$_{IL}$, V$_{IN}$ = V$_{IH}$			50	mA

Note Corresponding μPD27C1001A symbol.

AC Characteristics

(1) PROM Write Mode

(a) Page program mode (T_A = 25 ±5½C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{OE}$ ↓)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{OE}$ ↓)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{OE}$ ↓)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}$ ↑)	t_{AH}	t_{AH}		2			μs
	t_{AHL}	t_{AHL}		2			μs
	t_{AHV}	t_{AHV}		0			μs
Input data hold time (from $\overline{OE}$ ↑)	t_{DH}	t_{DH}		2			μs
$\overline{OE}$ ↑ → Data output float delay time	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{OE}$ ↓)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{OE}$ ↓)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ ↓ → Valid data delay time	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ pulse width during data latching	t_{LW}	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}	t_{OEH}		2			μs

(b) Byte program mode (T_A = 25 ±5½C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{PGM}$ ↓)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{PGM}$ ↓)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{PGM}$ ↓)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}$ ↑)	t_{AH}	t_{AH}		2			μs
Input data hold time (from $\overline{PGM}$ ↑)	t_{DH}	t_{DH}		2			μs
$\overline{OE}$ ↑ → Data output float delay time	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{PGM}$ ↓)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{PGM}$ ↓)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ ↓ → Valid data delay time	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ hold time	t_{OEH}	—		2			μs

Note Corresponding μPD27C1001A symbol.

(2) PROM Read Mode (T$_A$ = 25 ±5½C, V$_{DD}$ = 5.0 ±0.5 V, V$_{PP}$ = V$_{DD}$ ±0.6 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Address ↑ → Data output float delay time	t$_{ACC}$	t$_{ACC}$	$\overline{CE}$ = $\overline{OE}$ = V$_{IL}$			800	ns
$\overline{CE}$ ↓ → Valid output delay time	t$_{CE}$	t$_{CE}$	$\overline{OE}$ = V$_{IL}$			800	ns
$\overline{OE}$ ↓ → Valid output delay time	t$_{OE}$	t$_{OE}$	$\overline{CE}$ = V$_{IL}$			200	ns
$\overline{OE}$ ↓ → Data output float delay time	t$_{DF}$	t$_{DF}$	$\overline{CE}$ = V$_{IL}$	0		60	ns
Address → Data hold time	t$_{OH}$	t$_{OH}$	$\overline{CE}$ = $\overline{OE}$ = V$_{IL}$	0			ns

Note Corresponding µPD27C1001A symbol.

(3) PROM Programming Mode (T$_A$ = 25½C, V$_{SS}$ = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	tSMA		10			µs

PROM Write Mode Timing (page program mode)
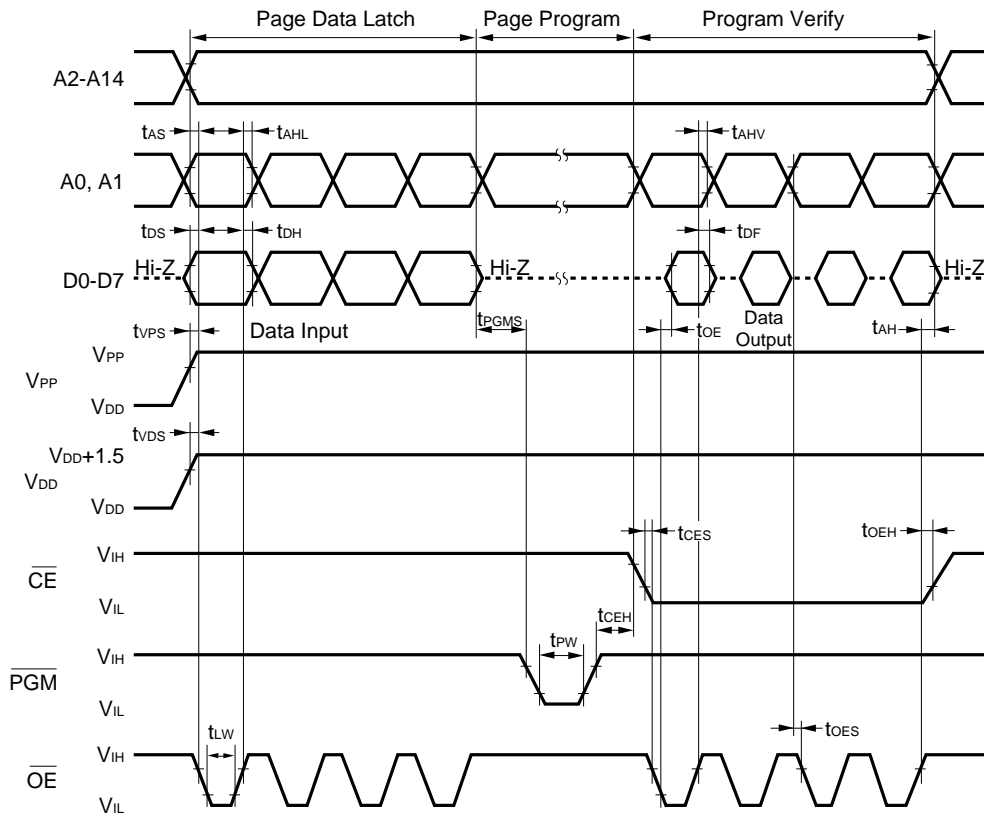
PROM Write Mode Timing (byte program mode)
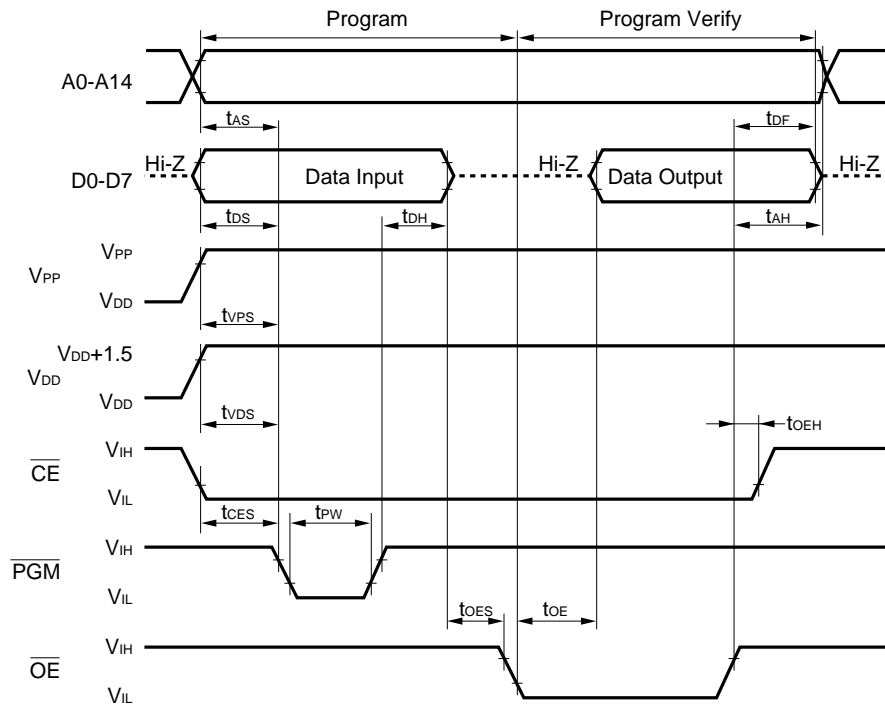
Program | Program Verify

A0-A14

D0-D7   Hi-Z   Data Input   Hi-Z   Data Output   Hi-Z

t_{AS} t_{DF}

t_{DS} t_{DH} t_{AH}

V_{PP} V_{PP} / V_{DD}

t_{VPS}

V_{DD} $V_{DD}+1.5$ / V_{DD} / V_{DD}

t_{VDS} t_{OEH}

$\overline{CE}$ V_{IH} / V_{IL}

t_{CES} t_{PW}

$\overline{PGM}$ V_{IH} / V_{IL}

t_{OES} t_{OE}

$\overline{OE}$ V_{IH} / V_{IL}

Cautions 1. V$_{DD}$ should be applied before V$_{PP}$, and removed after V$_{PP}$.

2. V$_{PP}$ must not exceed +13.5 V including overshoot.

3. Reliability may be adversely affected if removal/reinsertion is performed while + 12.5 V is being applied to V$_{PP}$.

PROM Read Mode Timing

A0-A14   Effective Address

$\overline{CE}$ V_{IH} / V_{IL}

t_{CE}

$\overline{OE}$ V_{IH} / V_{IL}

t_{ACC}**Note 1** t_{OE}**Note 1** t_{DF}**Note 2**

t_{OH}

D0-D7   Hi-Z   Data Output   Hi-Z
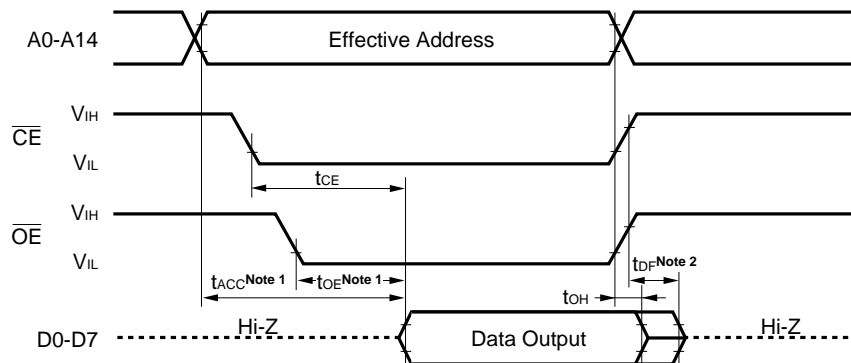
Notes 1. If you want to read within the range of t$_{ACC}$, make the $\overline{OE}$ input delay time from the fall of $\overline{CE}$ a maximum of t$_{ACC}$ – t$_{OE}$.

2. t$_{DF}$ is the time from when either $\overline{OE}$ or $\overline{CE}$ first reaches V$_{IH}$.

PROM Programming Mode Setting Timing