MATRA
DESIGN SEMICONDUCTOR
summary data sheet

MX SERIES
2.0-MICRON 2-LAYER METAL SILICON GATE CMOS GATE ARRAYS

Advance Information
September 1987

FEATURES

- 2.0u (drawn)/1.55u (eff), 2-layer metal CMOS technology
- High perfomance
  - 1.5ns delay through 2-input NAND gate T_A= 25 deg C, V_{DD} = 5V, fanout = 3 + 1000um interconnection
- High I/O-to-gate ratio for I/O-intensive applications
  - Pin counts ranging from 32 to 120
  - Any pin can be I/O, V_{DD} or V_{SS}
  - Gate counts ranging from 90 to 3060
- Programmable current sink/source capability up to 24mA per I/O buffer on each I/O pad
- Up to 96mA sink/source current per output pad with parallel output buffers and appropriate V_{DD} and V_{SS} distribution
- On-chip isolation of V_{DD} and V_{SS} busses between logic and I/O for exceptional output switching capability
- Efficient transistor configuration for logic as well as RAM cells
- Extensive logic macrocell and macrofunction libraries
  - Full range of combinatorial, sequential and I/O macrocells
  - SSI/MSI macrofunctions ideal for decoding, mux/demux, register, and buffer functions
  - LSI macrofunctions (2901/09/10, UART) available
- Highly efficient and flexible RAM implementation capability
  - 1 gate/RAM cell memory efficiency
  - Several RAM macros
  - RAM blocks locatable anywhere in the array
- Complete front-end CAE system (GATEAID PLUS/PC) on IBM PC
- Full range of packages: DIPs, SOICs, LCC/PLCCs, PGAs/PPGAs
- Evaluation chip available

APPLICATIONS

- I/O intensive and/or high current drive applications
- Examples of use
  - Multibus/Versabus/Unibus drivers
  - Logic functions integrating line drivers, e.g., serial data link, motor control, disk control
  - System control functions, e.g., system clock generator, CS/CE decoder
  - Integrated system support functions, e.g., bus decoder/multiplexer/buffer/driver

DESCRIPTION

The MX series of advanced CMOS gate arrays from Matra Design Semiconductor are implemented in state-of-the-art dual-layer metal technology, with effective channel lengths of 1.55um, allowing toggle frequencies up to 100MHz and operating frequencies up to 40-50MHz.

The MX series use a unique patented architecture that provides a very high I/O-to-gate ratio. At the same time, it allows equally efficient logic as well as memory implementation. Each RAM cell requires only 1 gate equivalent (2-input NAND gate).

PRODUCT OUTLINE

Part Number	Number of I/Os	Number of Gates (1)	Part Number	Number of I/Os	Number of Gates (1)
MX32	32	90	MX84	84	1320
MX48	48	240	MX100	100	1960
MX68	68	810	MX120	120	3060

(1) Up to 50% more transistors available when RAM is integrated.

DESIGN TOOLS

The fully integrated GATEAID PLUS/PC design system provides the user a complete set of design capture and analysis tools for implementing logic designs on the MX series. It supports a range of schematic entry options: Hierarchical schematic capture, Boolean equation entry, direct netlist entry, or a combination. The design verification tools consist of a 24-state event driven logic simulator, timing analyzer supporting any set of environmental conditions, waveform analyzer presenting data in a format similar to a logic state analyzer, and a spike analyzer. Testability verification tools consist of a testability analyzer and a fault simulator. The complete package runs on a standard IBM PC/86/186/286/386 system, and supports interfaces to various popular graphics cards, mouse units, printers and plotters.

NOTES

MATRA DESIGN SEMICONDUCTOR (MDS)
2895 Northwestern Parkway
Santa Clara, CA 95051
Phone: 408/986-9000 o Telex: 299-656
Fax: 408/748-1038