MC74VHC14

Hex Schmitt Inverter

The MC74VHC14 is an advanced high speed CMOS Schmitt inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

Pin configuration and function are the same as the MC74VHC04 but the inputs have hysteresis and, with its Schmitt trigger function, the VHC14 can be used as a line receiver which will receive slow input signals.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: t_{PD} = 5.5 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- High Noise Immunity: V_{NIH} = V_{NIL} = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
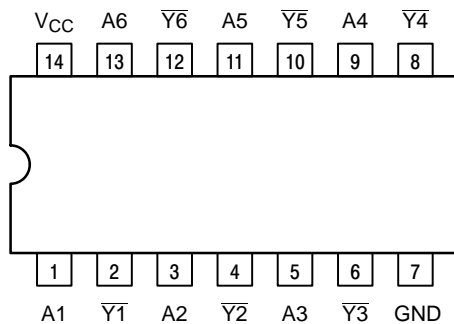- Chip Complexity: 60 FETs or 15 Equivalent Gates

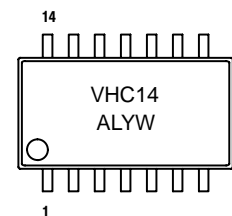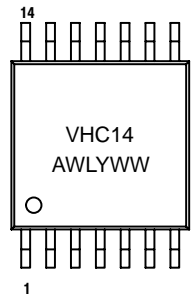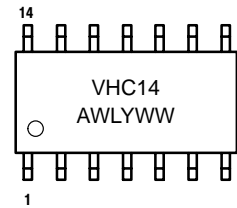**Figure 1. 14–Lead Pinout** (Top View)

FUNCTION TABLE

Inputs	Outputs
A	**$\overline{Y}$**
L	H
H	L

MARKING DIAGRAMS

SO–14
D SUFFIX
CASE 751A–03

VHC14
AWLYWW

TSSOP–14
DT SUFFIX
CASE 948G–01

VHC14
AWLYWW

EIAJ SO–14
DT SUFFIX
CASE 965–01

VHC14
ALYW

A   = Assembly Location
L, WL   = Wafer Lot
Y   = Year
W, WW   = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74VHC14D	SO–14	55 Units/Rail
MC74VHC14DR2	SO–14	2500 Tape & Reel
MC74VHC14DT	TSSOP–14	96 Units/Rail
MC74VHC14DTR2	TSSOP–14	2500 Tape & Reel
MC74VHC14M	EIAJ SO–14	50 Units/Rail
MC74VHC14MEL	EIAJ SO–14	2000 Tape & Reel

MC74VHC14

A1 1 [>o] 2 $\overline{Y1}$

A2 3 [>o] 4 $\overline{Y2}$

A3 5 [>o] 6 $\overline{Y3}$

$Y = \overline{A}$

A4 9 [>o] 8 $\overline{Y4}$

A5 11 [>o] 10 $\overline{Y5}$

A6 13 [>o] 12 $\overline{Y6}$

Figure 2. Logic Diagram
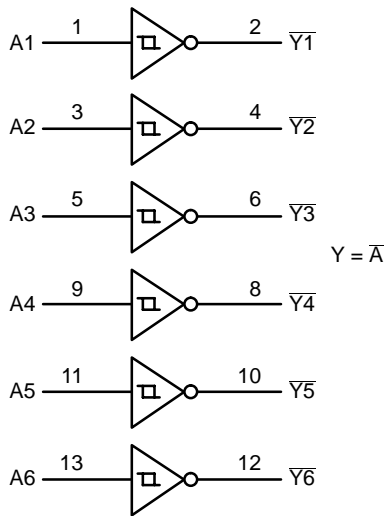
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	Digital Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
P_D	Power Dissipation in Still Air	SOIC Package TSSOP	200 180	mW
T_{STG}	Storage Temperature Range		−65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2.) Machine Model (Note 3.) Charged Device Model (Note 4.)	>2000 >200 N/A	V
$I_{LATCH–UP}$	Latch–Up Performance	Above V_{CC} and Below GND at 125°C (Note 5.)	±300	mA
θ_{JA}	Thermal Resistance, Junction to Ambient	SOIC Package TSSOP	143 164	°C/W

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22–A114–A
3. Tested to EIA/JESD22–A115–A
4. Tested to JESD22–C101–A
5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types		−55	125	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0	100 20	ns/V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25°C$ Min	Typ	Max	$−55°C \leq T_A \leq 125°C$ Min	Max	Unit
V_{T+}	Positive Threshold Voltage (Figure 5)		3.0 4.5 5.5			2.20 3.15 3.85		2.20 3.15 3.85	V
$V_{T−}$	Negative Threshold Voltage (Figure 5)		3.0 4.5 6.0	0.9 1.35 1.65			0.90 1.35 1.65		V
V_H	Hysteresis Voltage (Figure 5)		3.0 4.5 5.5	0.30 0.40 0.50		1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	V
V_{OH}	Minimum High–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = − 50 \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = − 4 mA$ $I_{OH} = − 8 mA$	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 50 \mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 4 mA$ $I_{OL} = 8 mA$	3.0 4.5			0.36 0.36		0.44 0.44	
I_{in}	Maximum Input Leakage Current	$V_{in} = 5.5$ V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	Typ	Max	$−55°C \leq T_A \leq 125°C$ Min	Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A or B to $\overline{Y}$	$V_{CC} = 3.3 \pm 0.3$ V	$C_L = 15$ pF $C_L = 50$ pF		8.3 10.8	12.8 16.3	1.0 1.0	15.0 18.5	ns
		$V_{CC} = 5.0 \pm 0.5$ V	$C_L = 15$ pF $C_L = 50$ pF		5.5 7.0	8.6 10.6	1.0 1.0	10.0 12.0	
C_{in}	Maximum Input Capacitance				4	10		10	pF

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Note 6.)	21	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/6$ (per buffer). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

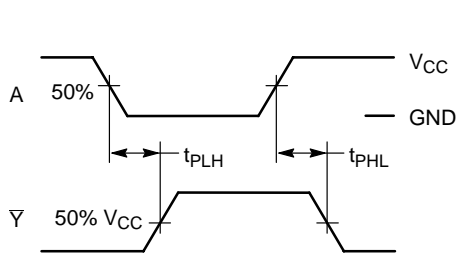| Symbol	Characteristic	$T_A = 25°C$ Typ	Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.4	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	− 0.4	− 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

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Figure 3. Switching Waveforms
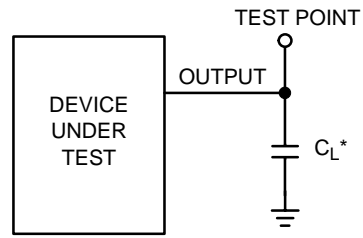
*Includes all probe and jig capacitance

Figure 4. Test Circuit

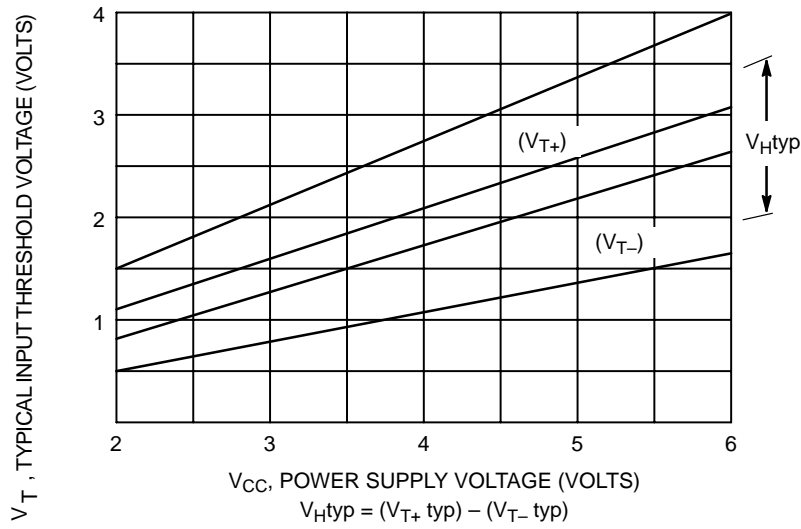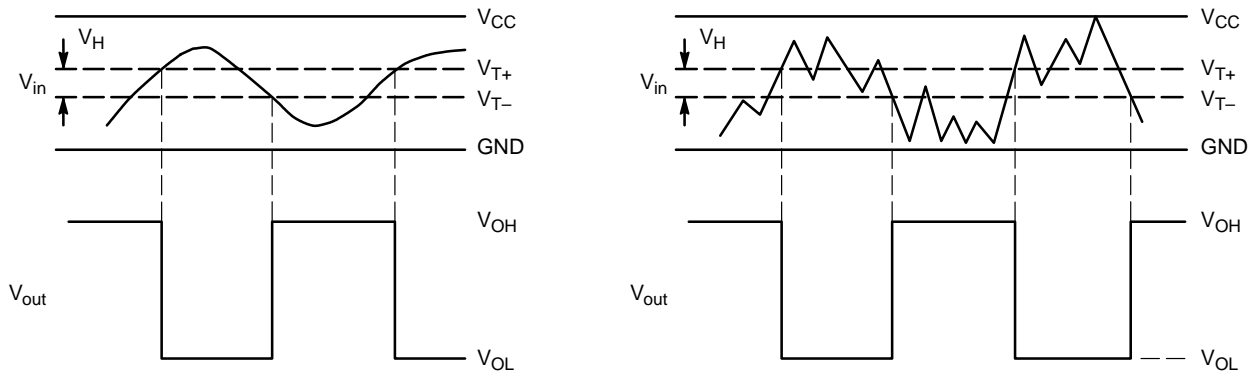$V_H typ = (V_{T+} typ) - (V_{T-} typ)$

Figure 5. Typical Input Threshold, V_{T+}, V_{T-} versus Power Supply Voltage

(a) A Schmitt–Trigger Squares Up
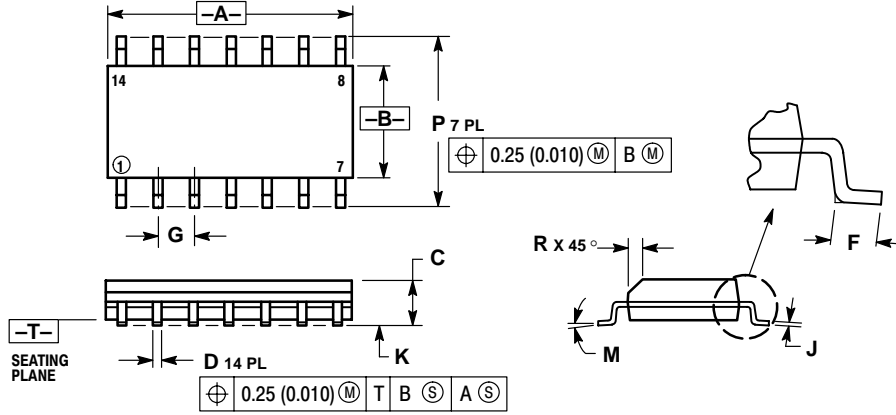Inputs With Slow Rise and Fall Times

(b) A Schmitt–Trigger Offers Maximum
Noise Immunity

Figure 6. Typical Schmitt–Trigger Applications

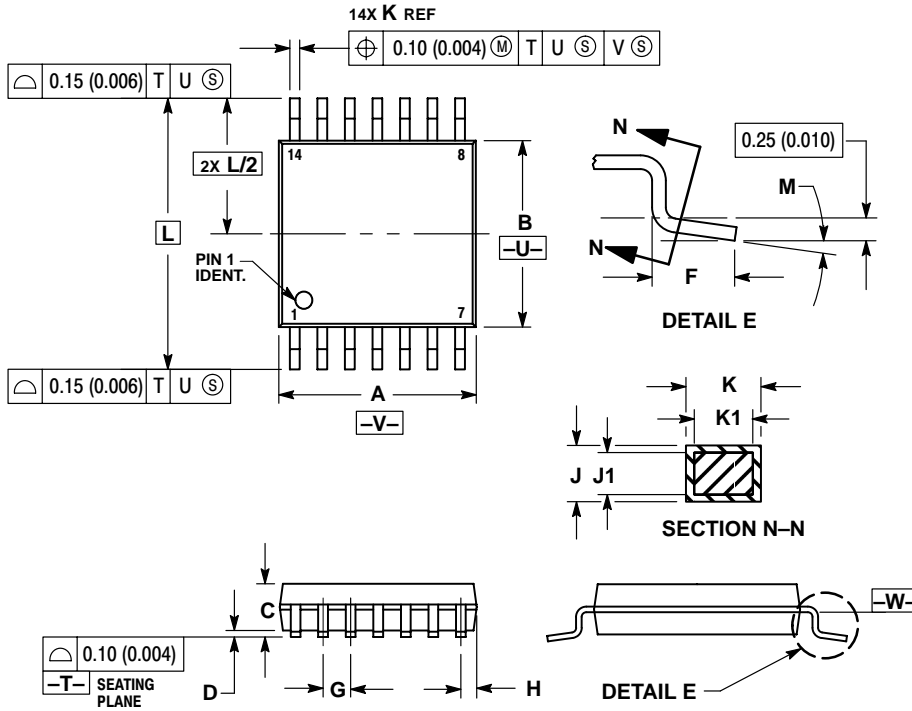## OUTLINE DIMENSIONS

D SUFFIX
SOIC–14
CASE 751A–03
ISSUE F

NOTES:
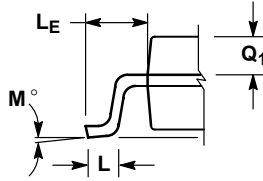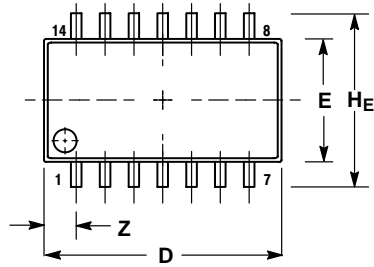1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

⊕ 0.25 (0.010) Ⓜ B Ⓜ

⊕ 0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

MC74VHC14

OUTLINE DIMENSIONS

DT SUFFIX
TSSOP
CASE 948G–01
ISSUE O

14X K REF

$\oplus$ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

△ | 0.15 (0.006) | T | U Ⓢ

2X L/2

L

PIN 1
IDENT.

14   8

B
–U–

1   7

A

–V–

△ | 0.15 (0.006) | T | U Ⓢ

N

0.25 (0.010)

M

N

F

DETAIL E

K

K1

J J1

SECTION N–N

C

△ | 0.10 (0.004)

–T– | SEATING
PLANE

D   G   H

DETAIL E

–W–

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74VHC14

OUTLINE DIMENSIONS

M SUFFIX
SO–14
CASE 965–01
ISSUE O

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

DETAIL P

VIEW P

$\oplus$ 0.13 (0.005) Ⓜ

⌂ 0.10 (0.004)

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