

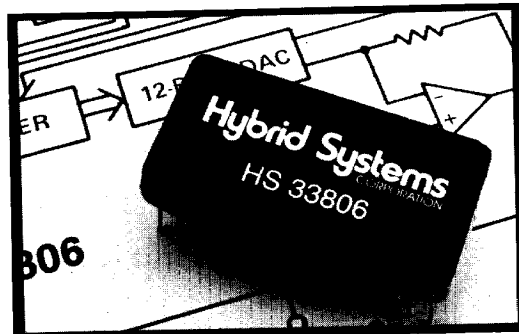
MULTIPLYING, VOLTAGE OUTPUT, μ P COMPATIBLE 12-BIT DAC

FEATURES

- 2- and 4-quadrant multiplying
- Coding: binary; offset binary
- Linearity: $\pm 0.01\%$
- Settling time: $2.5\mu\text{s}$
- μ P compatible
- 28-pin package
- CMOS, TTL compatible
- Double buffered inputs

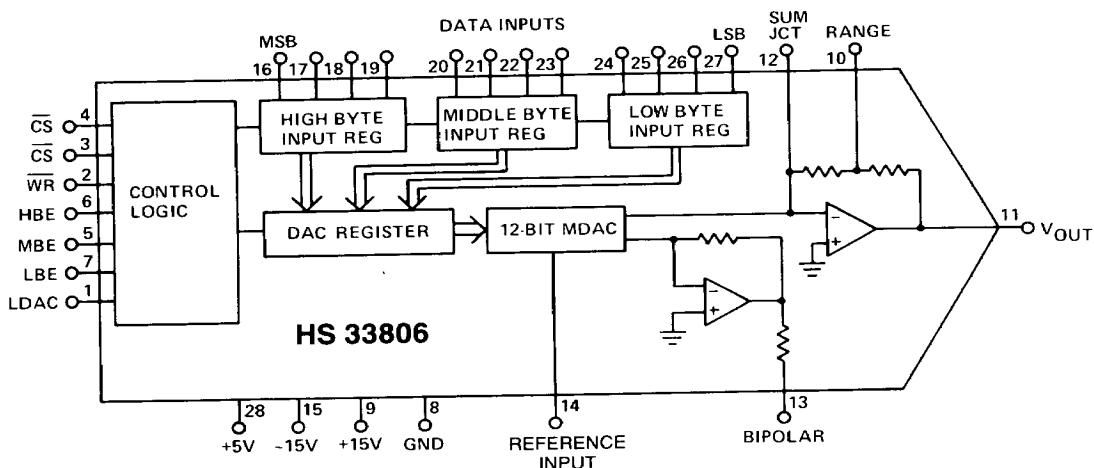
DESCRIPTION

HS33806 is a μ P compatible, complete 12-bit double buffered digital-to-analog converter. To enhance application flexibility, the data input registers have been configured as 3 independent, 4-bit bytes. This enables the user to directly interface to 4, 8, and 12-bit data buses. HS33806 comes complete with interface control logic. The three separate byte enable inputs latch data from the bus into the appropriate primary data latches. The LDAC input transfers data from the primary latches



to the DAC register. In addition to these input functions are two chip select inputs and a read/write input allowing direct memory-map configurations. All input controls are static to allow hardwired configurations. The HS33806 is packaged in a hermetically sealed package and is rated -55°C to $+125^{\circ}\text{C}$. Units are fully screened and processed to MIL-STD-883 requirements.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C unless otherwise noted. Power supply voltages:
+15V, -15V, +5V (±5%), Reference -10.0V)

MODEL	HS 33806
DIGITAL INPUT	
Resolution	12 Bit
Unipolar Code	Binary
Bipolar Code	Offset Binary
Logic Compatibility ^{1,5}	CMOS, TTL
Control Logic Inputs	
I _H @ V _{IH} = 2.4V	20μA
I _L @ V _{IL} = 0.4V	-0.36mA
Data Input Current ⁵	±1μA
REFERENCE INPUT	
Max Input Voltage	±25V
Input Impedance	8k Ω ±50%
Reference Feedthrough (V _{REF} = 20 Vpp) @ 1 kHz	<1 mV
@ 10 kHz	2 mV
Bandwidth	
Small Signal	500 kHz
Full Power	200 kHz
ANALOG OUTPUT	
Scale Factor Accuracy	±0.1% F.S.R.
Initial Offset ²	
Bipolar	10 mV Max
Unipolar	10 mV Max
Voltage Range ²	
Bipolar	±V _{REF} ± V _{REF} /2
Unipolar	0 to -V _{REF} 0 to -V _{REF} /2
STATIC PERFORMANCE	
Integral Linearity ³	±0.015% F.S.R. Max
Differential Linearity	±0.024% F.S.R. Max
Monotonicity	12 Bits
DYNAMIC PERFORMANCE	
Full Scale Transition	
Settling Time	5μS (max) 2.5μS (typ)
Full Scale Transition	
Slew Rate	10V/μS (min)
Delay to Analog Output	
From Bits Input ⁴	220nS
From LDAC	220nS
From CS ⁴ or WE ⁴	225nS
STABILITY	
Scale Factor	2 ppm F.S.R.
Integral Linearity	1 ppm F.S.R. Max
Differential Linearity	1 ppm F.S.R. Max
Offset Drift	
Bipolar	100 μV/°C
Unipolar	100 μV/°C
Monotonicity Temperature Range	-55°C to +125°C
+15V POWER SUPPLY	
+15V Supply Current	12mA
-15V Supply Current	7 mA
PSRR	0.005%/%
+5V POWER SUPPLY	
+5V Supply Current	24mA
TEMPERATURE RANGE	
Operating	-55°C to +125°C
Storage	-65°C to +150°C
MECHANICAL	
Case Style	Case B

NOTES

- Control inputs are TTL and 5V CMOS only; data inputs are fully CMOS and TTL compatible.
- See APPLICATION NOTES for adjustment procedures.
- Specified as "Best-Straight Line".
- Operating the unit with the DAC Register transparent may result in output "glitches" due to logic skewing with the unit.
- Digital Input voltage must not exceed supply voltage or go below -0.5V. "0" < 0.8V; 2.4V < "1" < V_{DD}.

APPLICATIONS INFORMATION

TRANSFER CHARACTERISTICS

UNIPOLAR OPERATION, PIN 11 OPEN

BINARY INPUT	ANALOG OUTPUT	BINARY INPUT	ANALOG OUTPUT
1 1 1 . . . 1 1 1	-V _{REF} · $\frac{4095}{4096}$	0 1 1 . . . 1 1 1	-V _{REF} · $\frac{2047}{4096}$
1 0 0 . . . 0 0 1	-V _{REF} · $\frac{2049}{4096}$	0 0 0 . . . 0 0 1	-V _{REF} · $\frac{1}{4096}$
1 0 0 . . . 0 0 0	-V _{REF} · $\frac{2048}{4096}$	0 0 0 . . . 0 0 0	0

Formula: $V_{OUT} = -V_{REF} \cdot \frac{N}{4096}$ where N represents the code applied to the DAC

UNIPOLAR OPERATION, PIN 11 CONNECTED TO PIN 10

BINARY INPUT	ANALOG OUTPUT	BINARY INPUT	ANALOG OUTPUT
1 1 1 . . . 1 1 1	-½ V _{REF} · $\frac{4095}{4096}$	0 1 1 . . . 1 1 1	-½ V _{REF} · $\frac{2047}{4096}$
1 0 0 . . . 0 0 1	-½ V _{REF} · $\frac{2049}{4096}$	0 0 0 . . . 0 0 1	-½ V _{REF} · $\frac{1}{4096}$
1 0 0 . . . 0 0 0	-½ V _{REF}	0 0 0 . . . 0 0 0	0

Formula: $V_{OUT} = -\frac{1}{2} V_{REF} \cdot \frac{N}{4096}$ where N represents the code applied to the DAC

BIPOLAR OPERATION, PIN 11 OPEN

OFFSET BINARY INPUT	ANALOG OUTPUT	OFFSET BINARY INPUT	ANALOG OUTPUT
1 1 1 . . . 1 1 1	-V _{REF} · $\frac{2047}{2048}$	0 1 1 . . . 1 1 1	+V _{REF} · $\frac{1}{2048}$
1 0 0 . . . 0 0 1	-V _{REF} · $\frac{1}{2048}$	0 0 0 . . . 0 0 1	+V _{REF} · $\frac{2047}{2048}$
1 0 0 . . . 0 0 0	0	0 0 0 . . . 0 0 0	+V _{REF}

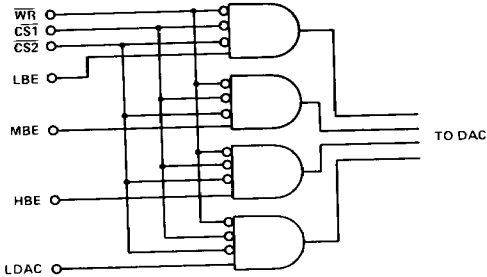
Formula: $V_{OUT} = -V_{REF} \cdot \frac{(N-2048)}{2048}$ where N represents the code applied to the DAC

BIPOLAR OPERATION, PIN 11 CONNECTED TO PIN 10

OFFSET BINARY INPUT	ANALOG OUTPUT	OFFSET BINARY INPUT	ANALOG OUTPUT
1 1 1 . . . 1 1 1	-½ V _{REF} · $\frac{2047}{2048}$	0 1 1 . . . 1 1 1	+½ V _{REF} · $\frac{1}{2048}$
1 0 0 . . . 0 0 1	-½ V _{REF} · $\frac{1}{2048}$	0 0 0 . . . 0 0 1	+½ V _{REF} · $\frac{2047}{2048}$
1 0 0 . . . 0 0 0	0	0 0 0 . . . 0 0 0	+½ V _{REF}

Formula: $V_{OUT} = -\frac{1}{2} V_{REF} \cdot \frac{(N-2048)}{2048}$ where N represents the code applied to the DAC

CONTROL LOGIC FUNCTIONAL DIAGRAM

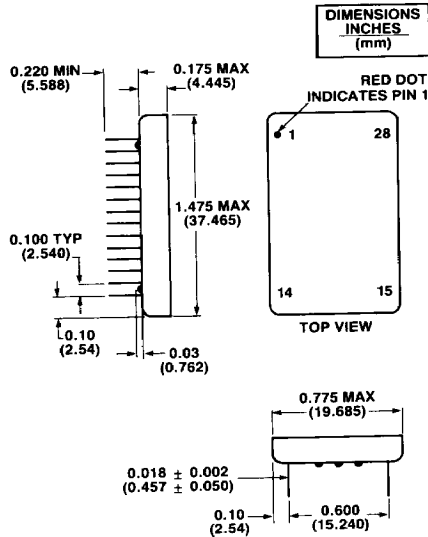


TRUTH TABLE

HS 9338 CONTROL INPUTS							HS 9338 OPERATION
WR	CS1	CS2	LBE	MBE	HBE	LDAC	
1	X	X	X	X	X	X	Device not selected Output reflects previously loaded data
X	1	X					Write data into low byte data register
X	X	1					Write data into middle byte data register
0	0	0	1	0	0	0	Write data into high byte data register
0	0	0	0	1	0	0	Write data into middle byte data register
0	0	0	0	0	1	0	Write data into high byte data register
0	0	0	0	0	0	1	Load DAC register with data in low byte middle byte and high byte data registers
0	0	0	1	1	1	0	Write data simultaneous into all data registers
0	0	0	1	1	1	1	Write data directly into DAC register

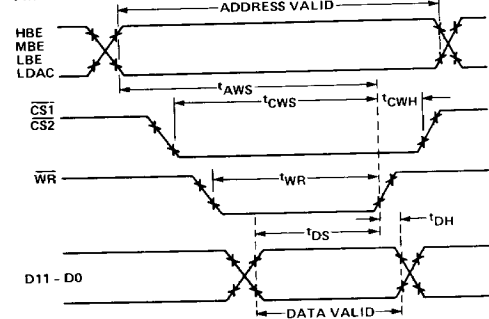
PACKAGE OUTLINE

CASE B



Ceramic or metal package at manufacturer's option.

TIMING DIAGRAM



t_{DS} : Data setup time, 250 nsec t_{CWS} : Chip select to write setup time, 300 nsec
 t_{DH} : Data hold time, 20 nsec t_{CWH} : Chip select to write hold time, 0 nsec
 t_{WR} : Write pulse width, 300 nsec t_{AWS} : Address to write setup time, 250 nsec

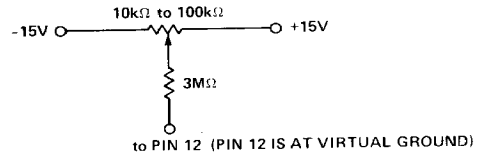
PIN DIAGRAM

PIN	FUNCTION
1	LDAC, LOADS DAC REGISTER AND CHANGES OUTPUT
2	WR, WRITE INPUT, ACTIVATES ALL CONTROLS
3	CS2, CHIP SELECT INPUT 2
4	CS1, CHIP SELECT INPUT 1
5	MBE, MIDDLE BYTE ENABLE, D4 TO D7
6	HBE, HIGH BYTE ENABLE, D8 TO D11
7	LBE, LOW BYTE ENABLE, D0 TO D3
8	GND, GROUND, ANALOG AND DIGITAL GROUND CONNECTED INTERNALLY
9	VCC, +15V SUPPLY
10	OUTPUT RANGE
11	VOU, DAC VOLTAGE OUTPUT
12	SUMJCT, SUMMING JUNCTION OF OUTPUT OPAMP
13	BIPOLAR, CONNECTED TO SUMJCT FOR BIPOLAR OUTPUT RANGE
14	REFERENCE INPUT
15	VEE, -15V SUPPLY
16	D11, DATA INPUT, WEIGHT 2^{-1} , MSB
17	D10, DATA INPUT, WEIGHT 2^{-2}
18	D9, DATA INPUT, WEIGHT 2^{-3}
19	D8, DATA INPUT, WEIGHT 2^{-4}
20	D7, DATA INPUT, WEIGHT 2^{-5}
21	D6, DATA INPUT, WEIGHT 2^{-6}
22	D5, DATA INPUT, WEIGHT 2^{-7}
23	D4, DATA INPUT, WEIGHT 2^{-8}
24	D3, DATA INPUT, WEIGHT 2^{-9}
25	D2, DATA INPUT, WEIGHT 2^{-10}
26	D1, DATA INPUT, WEIGHT 2^{-11}
27	D0, DATA INPUT, WEIGHT 2^{-12} , LSB
28	VDD, +5V SUPPLY, CONTROL LOGIC

OUTPUT CONNECTIONS

RANGE	OUTPUT	CONNECT PIN 12	CONNECT PIN 10	CONNECT PIN 13
0 to -VREF	PIN 11	OPEN	OPEN	OPEN
0 to -VREF/2	PIN 11	OPEN	PIN 11	OPEN
+VREF to -VREF	PIN 11	PIN 13	OPEN	PIN 12
+VREF/2 to +VREF/2	PIN 11	PIN 13	PIN 11	PIN 12

OUTPUT OFFSET ADJUST (OPTIONAL)



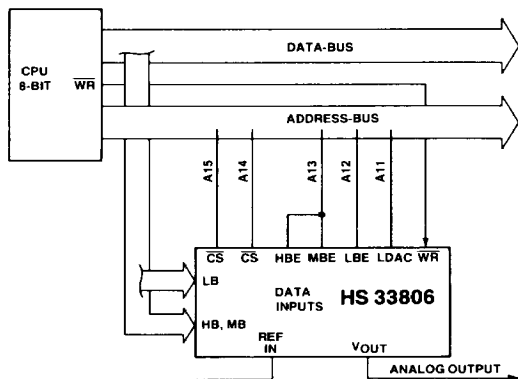
RANGE: ± 25 mV typ

Adjust for $V_{out} = 0.000$ Volt at input code 00...0 for unipolar operation or at input code 10...0 for bipolar operation.

SCALE FACTOR ADJUST: Scale factor is factory trimmed to 0.1% typ. Adjust external reference voltage if initial accuracy is not sufficient.

APPLICATIONS INFORMATION

INTERFACING THE HS 33806 TO AN 8-BIT PROCESSOR USING NO EXTERNAL COMPONENTS

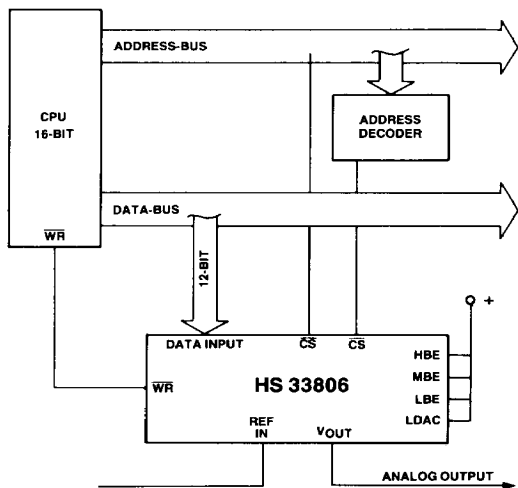


This mode of operation requires 13k bytes of unused addresses. No additional address decoder is necessary. The two chip-select inputs together with the byte-enable and load-DAC inputs are used to control all functions of the DAC. Through selecting the address-lines the user can vary the addresses used to control the DAC. In the above figure the control signals have the following address-configurations (hex):

HBE, MBE	2000
LBE	1000
LDAC	0800

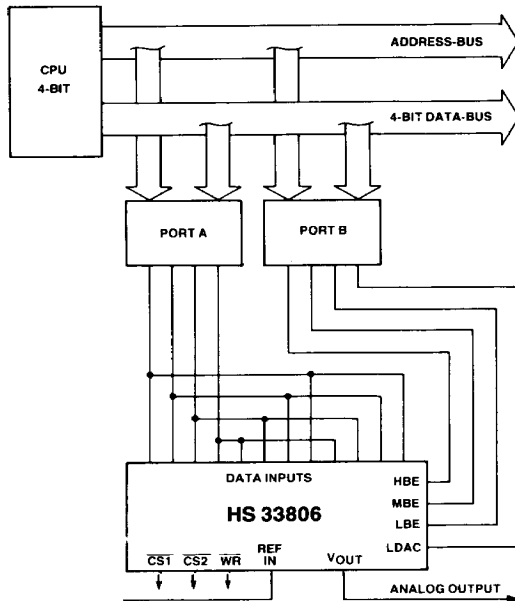
The LDAC input should not be tied together to the LBE input to ensure correct data transfer between the DAC registers.

INTERFACING THE HS 33806 TO A 16-BIT MICROPROCESSOR



Interfacing the HS 33806 to a 16-Bit microprocessor is quite easy, because no multiplexing of the data inputs is necessary. An address decoder and the second chip-select input is used to select the DAC.

INTERFACING THE HS 33806 to a 4-BIT MICROPROCESSOR USING 4-BIT I/O-PORTS



This figure shows how to operate the HS 33806 with two 4-Bit ports. The chip-selects are tied to ground allowing continuous operation; they can be used for operating more DAC's at the same port. In the first step data should appear at the port A outputs; in the second step the control flags should appear on port B.

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 33806	μ P MDAC, Voltage Output, MIL-STD-883 Screening

Specifications subject to change without notice.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the supply voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below -0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.