T-46-23-14

PRELIMINARY **CYM1840**

CYPRESS SEMICONDUCTOR

256K x 32 Static RAM Module

Features

- High-density 8-megabit SRAM module
- High-speed CMOS SRAMs
  — Access time of 20 ns
- Independent byte and word controls
- Low active power
  — 6.2W (max.)
- Hermetic SMD technology
- TTL-compatible inputs and outputs
- Low profile
  — Max. height of .290 in. (HD)
- Small PCB footprint
  — 1.8 sq. in.

Functional Description

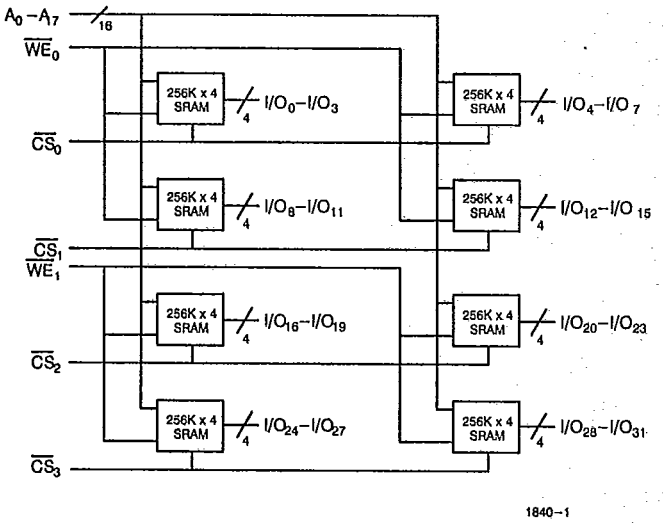
The CYM1840 is a high-performance 8-megabit static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256K x 4 SRAMs in LCC packages mounted on a ceramic substrate with pins. Four chip selects ($\overline{CS_0}$, $\overline{CS_1}$, $\overline{CS_2}$, and $\overline{CS_3}$) are used to independently enable the four bytes. Two write enables ($\overline{WE_0}$ and $\overline{WE_1}$) are used to independently write to either the upper or lower 16-bit word of RAM. Reading or writing can be executed on individual bytes or on any combination of multiple bytes through the proper use of selects and write enables.

Writing to each byte is accomplished when the appropriate chip select ($\overline{CS_X}$) and write enable ($\overline{WE_X}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{17}).

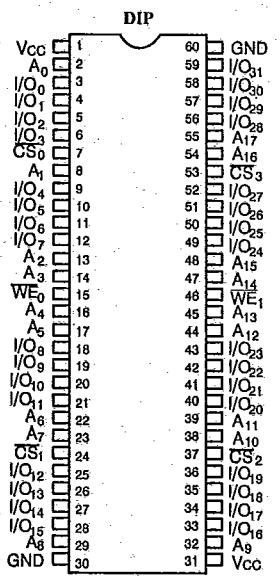
Reading the device is accomplished by taking the chip selects ($\overline{CS_X}$) LOW, while write enables ($\overline{WE_X}$) remain HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The Data input/output pins stay in the high-impedance state when write enables ($\overline{WE_X}$) are LOW or the appropriate chip selects are HIGH.

Logic Block Diagram



Pin Configuration



Selection Guide

		1840–20	1840–25	1840–30	1840–35	1840–45	1840–55
Maximum Access Time (ns)		20	25	30	35	45	55
Maximum Operating Current (mA)	Commercial	1120	1120	1120	1120	1120	1120
	Military				1120	1120	1120
Maximum Standby Current (mA)	Commercial	320	320	320	320	320	320
	Military				320	320	320

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied (HD) ..... −55°C to +125°C

Ambient Temperature with Power Applied (PD) ..... −10°C to +85°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 14.0V

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001V

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Load Current	$GND \le V_I \le V_{CC}$	−20	+20	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled	−50	+50	µA
I_{CC}	V_{CC} Operating Supply Current by 16 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_X \le V_{IL}$		1120	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}, $\overline{CS}_X \ge V_{IH}$, Min. Duty Cycle = 100%		320	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}, $\overline{CS}_X \ge V_{CC} - 0.3V$, $V_{IN} \ge V_{CC} - 0.3V$ or $V_{IN} \le 0.3V$		160	mA

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{INA}	Input Capacitance, Address Pins	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	100	pF
C_{INB}	Input Capacitance, I/O Pins		30	pF
C_{OUT}	Output Capacitance		30	pF

Notes:

1. T_A is the "instant on" case temperature.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested initially and after any design or process changes that may affect these parameters.

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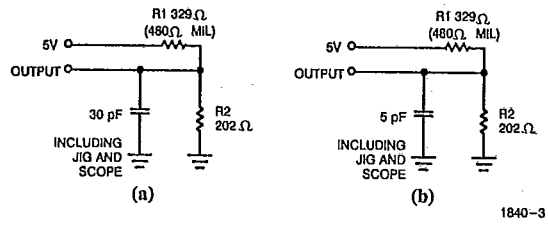
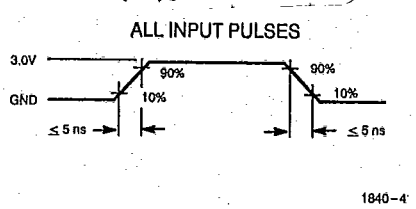
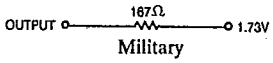
AC Test Loads and Waveforms

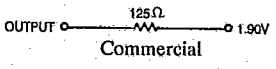




Equivalent to: THÉVENIN EQUIVALENT



Military



Commercial

Switching Characteristics Over the Operating Range[4]

Parameters	Description	1840–20		1840–25		1840–30		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		30		ns
t_{AA}	Address to Data Valid		20		25		30	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		30	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5,6]		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		20		25		30	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	20		25		30		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	18		20		25		ns
t_{AW}	Address Set-Up to Write End	18		20		25		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	13		15		15		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[5]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5,5]	0	15	0	15	0	15	ns

Notes:

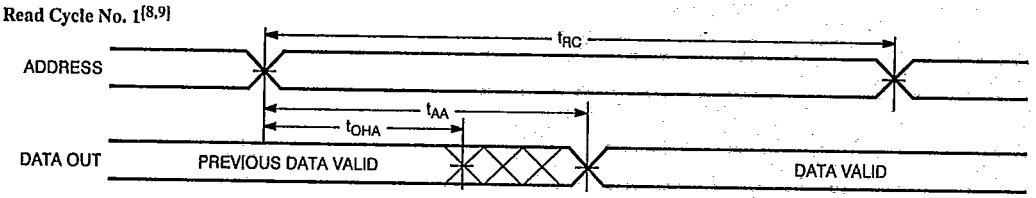
4. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[4] (continued)

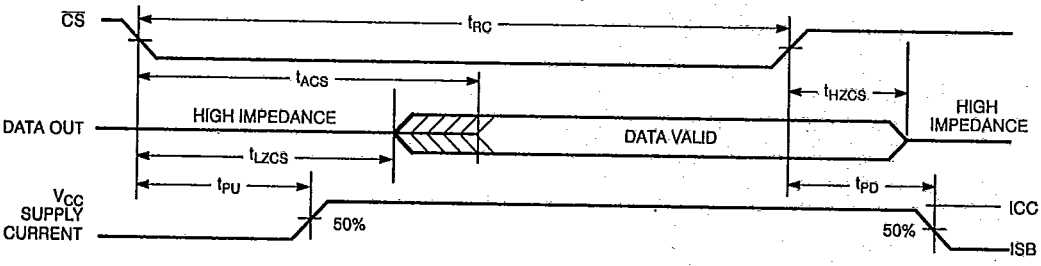
Parameters	Description	1840–35		1840–45		1840–55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5,6]		25		25		25	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		35		45		55	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		50		ns
t_{AW}	Address Set-Up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	6		6		6		ns
t_{SA}	Address Set-Up to Write Start	6		6		6		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		30		40		ns
t_{SD}	Data Set-Up to Write End	25		30		35		ns
t_{HD}	Data Hold from Write End	6		6		6		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[5]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5,6]	0	25	0	25	0	25	ns

Switching Waveforms[8]

Read Cycle No. 1[8,9]



Read Cycle No. 2[8,9]



Notes:
8. Device is continuously selected, $\overline{CS} = V_{IL}$.
9. $\overline{WE}$ is HIGH for read cycle.

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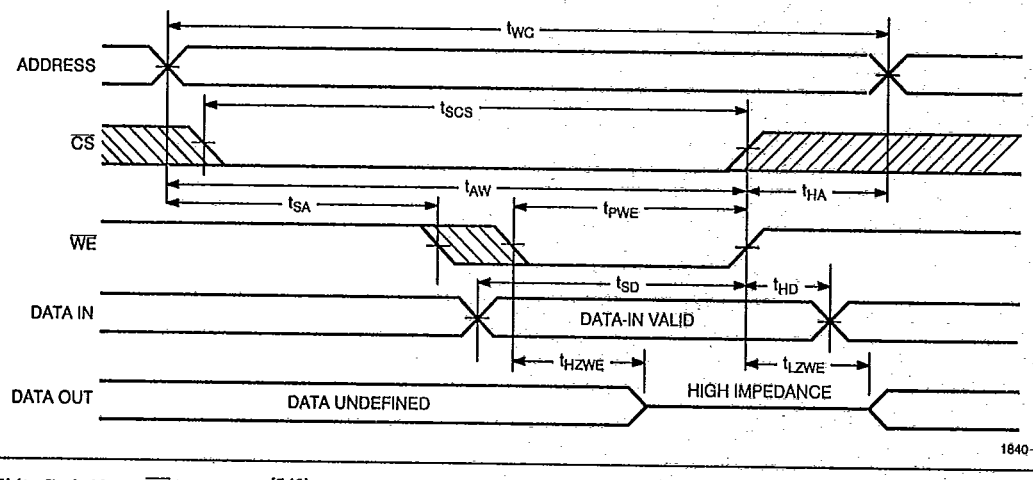
Switching Waveforms[8] (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled)[7]



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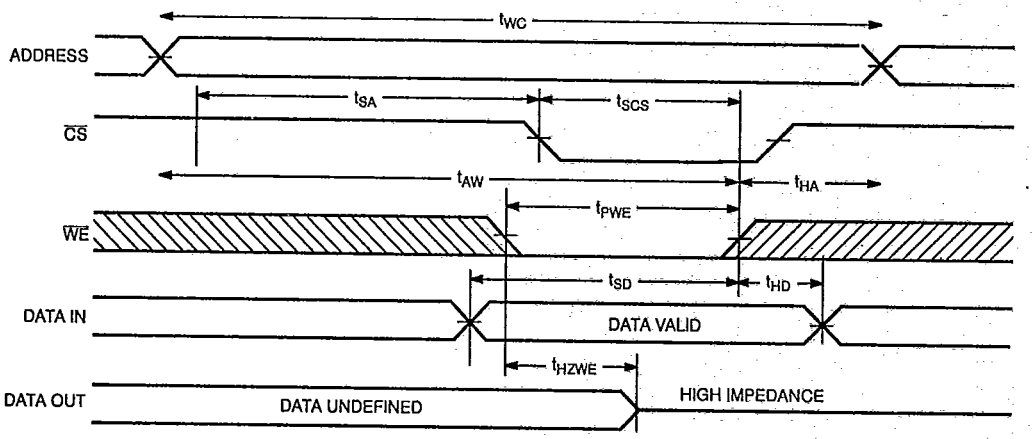
Write Cycle No. 2 ($\overline{CS}$ Controlled)[7,10]



1840-8

Note:
10. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}_X$	$\overline{WE}_X$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

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Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CYM1840PD–20C	PD06	Commercial
25	CYM1840PD–25C	PD06	Commercial
	CYM1840HD–25C	HD11	
30	CYM1840PD–30C	PD06	Commercial
	CYM1840HD–30C	HD11	
35	CYM1840PD–35C	PD06	Commercial
	CYM1840HD–35C	HD11	
	CYM1840HD–35MB	HD11	Military
45	CYM1840PD–45C	PD06	Commercial
	CYM1840HD–45C	HD11	
	CYM1840HD–45MB	HD11	Military
55	CYM1840PD–55C	PD06	Commercial
	CYM1840HD–55C	HD11	
	CYM1840HD–55MB	HD11	Military

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