Semiconductor Corporation

CS4131

Multimedia Digital Audio Controller

Features

- Direct Interface of CS4215 to ISA Bus
- Support for stereo digital audio up to 48 kHz sample rate at 16 bit resolution.
- 16 bit DMA transfers of 8 or 16-bit audio data to and from host PC.
- Full 10 bit I/O address decode for more flexible I/O space usage and EISA bus compatibility.
- 68 Pin PLCC

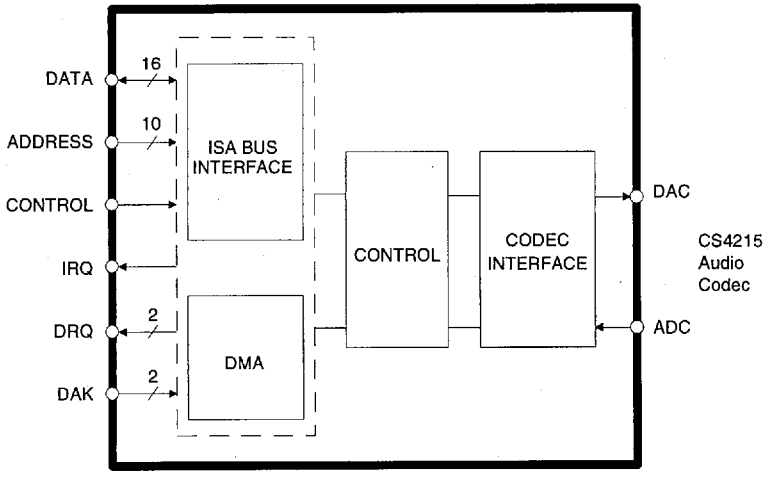
General Description

The CS4131 is a monolithic integrated circuit that provides a digital audio interface between the Crystal CS4215 audio Codec and a personal computer. The CS4131 implements all timer and control functions necessary to record and play back sampled digital audio at sample rates up to 48 kHz. The device is housed in a 68 pin PLCC or 64 pin TQFP.

4

ORDERING INFORMATION:

CS4131-CL	0 to 70°C	68-pin PLCC
CS4131-CQ	0 to 70°C	64-pin TQFP



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

DIGITAL CHARACTERISTICS (T_A = 25 °C)

Parameter	Symbol	Min	Max	Unit
Low Level Output Voltage @I_{OL} max	V_{OL}		+0.4	V
High Level Output Voltage @I_{OH} min	V_{OH}	+2.4		V
High Level Output Current @V_{OH} max	I_{OH}			
2 mA driver			-2	mA
4 mA driver			-4	mA
8 mA driver			-8	mA
12 mA driver			-12	mA
Low Level Output Current @ V_{OL} max	I_{OL}			
2 mA driver			+2	mA
4 mA driver			+4	mA
8 mA driver			+8	mA
12 mA driver			+12	mA
Output tristate current	IOZ	-10	+10	µA
Power Consumption	P_O		150	mW
TTL Inputs				
Low Level Input Voltage (TTL level buffer)	V_{ILTTL}		+0.8	V
High Level Input Voltage (TTL level buffer)	V_{IHTTL}	+2.0		V
Low Level Input Current	I_{IL}		-1	µA
High Level Input Current	I_{IH}		+1	µA
Input Pull-Up Current	I_{IL}	-33	-496	µA
Input Pull-Down Current	I_{IH}	33	496	µA
Schmitt Negative Threshold	V_{t-}	0.8		V
Schmitt Positive Threshold	V_{t+}		2.4	V
Schmitt Hysteresis	V_h	0.4		V
CMOS Inputs				
Low Level Input Voltage (CMOS level buffer)	V_{ILCMOS}		0.3*V_{DD}	V
High Level Input Voltage (CMOS level buffer)	V_{IHCMOS}	0.7*V_{DD}		V
Low Level Input Current	I_{IL}		-1	µA
High Level Input Current	I_{IH}		+1	µA
Input Pull-Up Current	I_{IL}	-33	-496	µA
Input Pull-Down Current	I_{IH}	33	496	µA
Schmitt Negative Threshold	V_{t-}	0.2*V_{DD}		V
Schmitt Positive Threshold	V_{t+}		0.8*V_{DD}	V
Schmitt Hysteresis	V_h	1.0		V

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply Voltage		V_{DD}	-0.3	+7.0	V
DC Input Voltage		V_{IN}	-0.3	V_{DD}+0.3	V
DC Input Current	T_A = 25 °C	I_{IN}	-10	+10	mA
Storage Temperature		T_{stg}	-55	+125	°C
Lead Temperature	10 seconds	T_{lead}		300	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 25°C)

Parameter	Symbol	Min	Max	Units
DC Supply Voltage	V_{DD}	+4.5	+5.5	V
Ambient Temperature	T_A	0	+70	°C

SWITCHING CHARACTERISTICS (T_A = 25 °C; V_{DD} = 4.75V to 5.25 V), outputs loaded with 10pF, ISA data lines with 15pF; Input Levels: Logic 0 = 0V, Logic 1 = V_{DD}

Parameter	Symbol	Min	Max	Unit
Writes to CS4215; 8-bit IO slave mode				
Address, AEN setup to $\overline{IOWC}$ inactive	t_1	7		ns
Address, AEN hold from $\overline{IOWC}$ inactive	t_2	12		ns
Data setup to $\overline{IOWC}$ inactive	t_3	3		ns
Data hold from $\overline{IOWC}$ inactive	t_4	16		ns
$\overline{IOWC}$ active time	t_{4A}	96		ns
Reads from CS4215; 8-bit IO slave mode (Note 1)				
Data valid from $\overline{IORC}$ active	t_5	6	35	ns
Data hold from $\overline{IORC}$ inactive	t_6	4	24	ns
$\overline{IORC}$ active time	t_{6A}	48		ns
Writes to CS4215; 16-bit DMA slave mode (Note 2)				
DRQ inactive from $\overline{DACK}$ active (8-bit mono and stereo, 16-bit mono)	t_7		34	ns
DRQ inactive from $\overline{IOWC}$ or $\overline{IORC}$ active (16-bit stereo)	t_8		41	ns
Data setup to $\overline{IOWC}$ inactive	t_9	3		ns
Data hold from $\overline{IOWC}$ inactive	t_{10}	17		ns
$\overline{IOWC}$ inactive time	t_{11}	90		ns
$\overline{IOWC}$ active time	t_{12}	96		ns
Reads from CS4215; 16-bit DMA slave mode (Note 2)				
$\overline{IORC}$ active time	t_{13}	48		ns
Data valid from $\overline{IORC}$ active	t_{14}	6	34	ns
Data hold from $\overline{IORC}$ inactive	t_{15}	3	25	ns
$\overline{IORC}$ Inactive Time	t_{16}	90		ns
CS4131 Reset				
Internal registers reset from RESDRV active	t_{17}	5	26	ns
RESDRV pulse width (Required by CS4215)	t_{18}	500		ns
Control Bit Outputs (Note 3)				
New control bit output values from $\overline{IOWC}$ inactive	t_{19}	10	32	ns

Notes:
1. These specifications assume an ISA compliant controller which provides an address setup and hold to $\overline{IORC}$.
2. These specifications assume an ISA compliant controller which provides a $\overline{DACK}$ setup and hold relative to $\overline{IOWC}$ for writes to the CS4215, and relative to $\overline{IORC}$ for reads from the CS4215.
3. These outputs cover the signals that are reflections of control bit registers. These include SERD/$\overline{C}$, PDN, and $\overline{AUDRST}$.

SWITCHING CHARACTERISTICS (Continued)

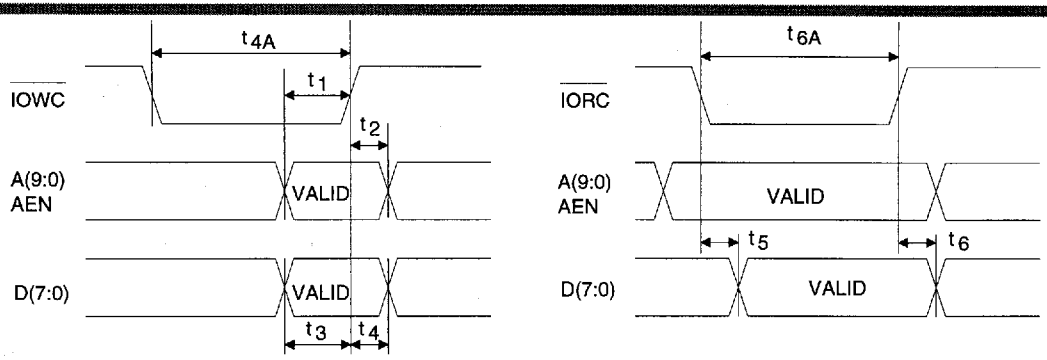
Parameter	Symbol	Min	Max	Unit
Interrupt Output				
"Threshold" DMA operation to INTOUT active	t_{20}	2 BCLK + 4	3 BCLK + 24	ns
INTCLRBIT active write to INTOUT inactive	t_{21}	1 BCLK + 5	2 BCLK + 29	ns
External Buffer Control (Note 4)				
$\overline{IOWC}$ active to $\overline{DBUFENx}$ active	t_{22}	5	29	ns
$\overline{IOWC}$ inactive to $\overline{DBUFENx}$ inactive	t_{23}	10	65	ns
$\overline{IORC}$ active to DBUFDIR active (programmed I/O mode)	t_{24}	4	22	ns
$\overline{IORC}$ active to $\overline{DBUFEN0}$ active (programmed I/O mode)	t_{25}	11	64	ns
$\overline{IORC}$ inactive to $\overline{DBUFENx}$ inactive (both programmed I/O and DMA mode)	t_{26}	5	28	ns
$\overline{IORC}$ inactive to DBUFDIR inactive (programmed I/O mode)	t_{27}	11	65	ns
$\overline{DACK0}$ or $\overline{DACK1}$ active to DBUFDIR active (DMA mode)	t_{28}	4	22	ns
$\overline{DACK0}$ or $\overline{DACK1}$ inactive to DBUFDIR inactive (DMA mode)	t_{29}	5	30	ns
$\overline{IORC}$ active to $\overline{DBUFENx}$ active (DMA mode)	t_{30}	5	29	ns
Serial Bus Interface; CS4215 Master Mode				
SCLK Period	t_{31}	125		ns
SCLK high time	t_{32}	50		ns
SCLK low time	t_{33}	50		ns
FSYNC setup to SCLK falling	t_{34}	3		ns
FSYNC hold from SCLK falling	t_{35}	17		ns
SDIN setup to SCLK falling	t_{36}	3		ns
SDIN hold from SCLK falling	t_{37}	14		ns
SCLK rising to SDOUT	t_{38}	5	46	ns
TSOUT setup to SCLK falling	t_{39}	3		ns
TSOUT hold from SCLK falling	t_{40}	14		ns

Notes: 4. $\overline{DBUFENx}$ refers to $\overline{DBUFEN0}$ or $\overline{DBUFEN1}$

4

SWITCHING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Unit
Serial Bus Interface; CS4215 Slave Mode				
SCLK period. Is BCLK divided by eight	t_{41}	800	1200	ns
SCLK high time	t_{42}	300	700	ns
SCLK low time	t_{43}	300	700	ns
SCLK rising to FSYNC	t_{44}	7	40	ns
SDIN setup to SCLK falling	t_{45}	3		ns
SDIN hold from SCLK falling	t_{46}	14		ns
SCLK rising to SDOUT	t_{47}	5	46	ns
TSOUT setup to SCLK falling	t_{48}	3		ns
TSOUT hold from SCLK falling	t_{49}	14		ns



a. Write Timing b. Read Timing

Figure 1. CS4131 in 8-bit I/O Slave Mode

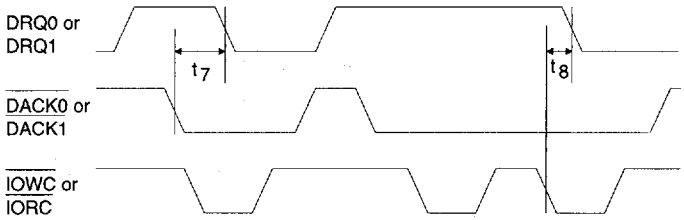
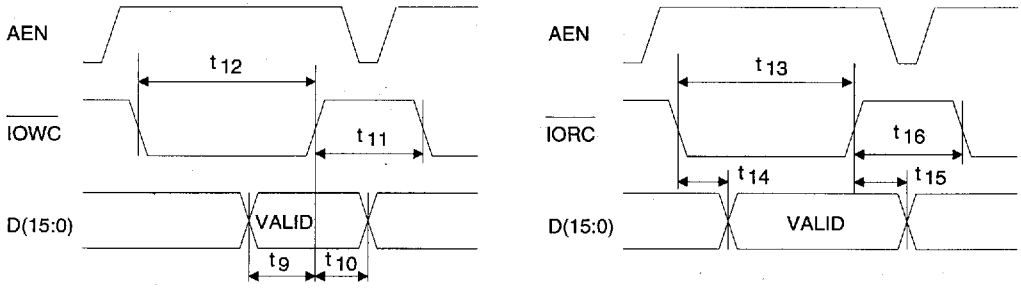


Figure 2. DMA Deassertion



a. Write Timing b. Read Timing

Figure 3. CS4131 in 16-bit DMA Slave Mode

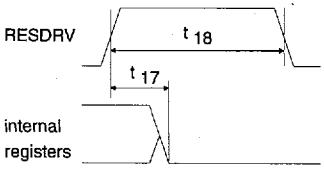


Figure 4. CS4131 Reset Timing

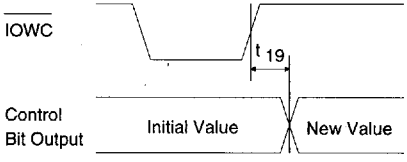


Figure 5. Control Bit Output Timing

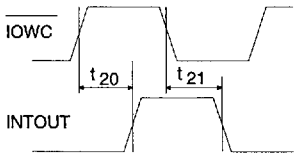


Figure 6. CS4131 Interrupt Output Timing

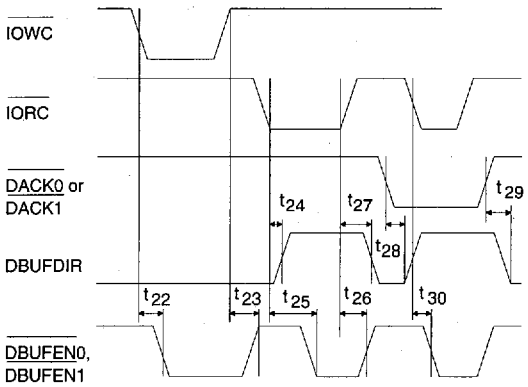
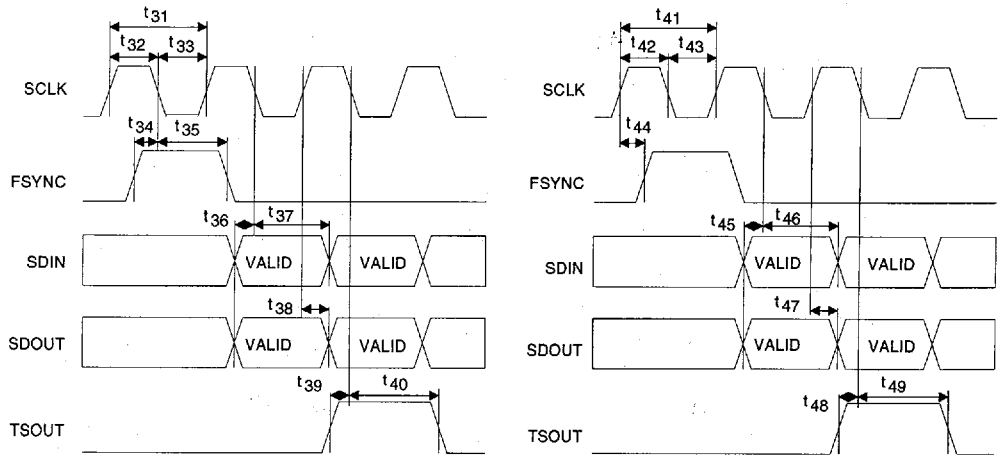


Figure 7. CS4131 External Buffer Control Timing



a. CS4215 in Master Mode

b. CS4215 in Slave Mode

Figure 8. Serial Bus Interface Timing

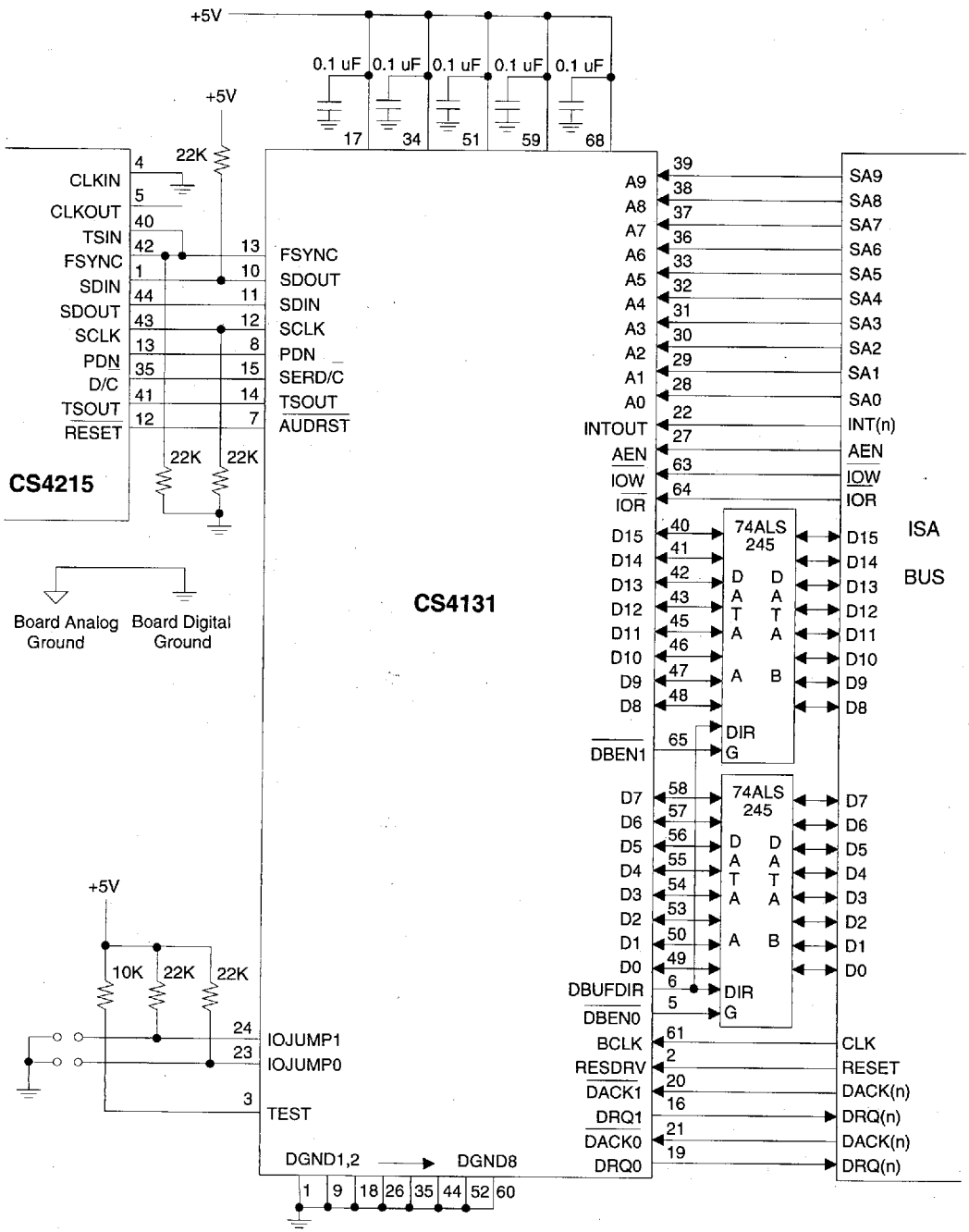


Figure 9. Typical Connection

FUNCTIONAL DESCRIPTION

Overview

The CS4131 provides an interface between the CS4215 and the 16-bit ISA bus. The CS4131 resides on the ISA bus found in the class of desktop computers known as "PC-compatibles", or PC's. It can act as both an I/O and DMA slave.

As an 8-bit I/O slave, the CS4131 decodes its own 16-byte I/O range, from among four possible base addresses, that can be selected via two external pins. The CS4131 is used as an I/O slave primarily to set up its mode of operation.

The CS4131 also acts as a 16-bit DMA slave. It is physically connected to one or two DMA channels. It can use either channel for both input and output, or use one channel for input and the other for output. The CS4131 can tristate one or both DMA request lines to free up the channels it is not using. It is used as a DMA slave for sample transfers to and from the CS4215 Codec.

The CS4131 provides one interrupt request (IRQ) line to notify the software driver when the audio data ring buffer needs servicing.

The CS4131 can sink 12 mA on each data bus pin. For use in systems that require stronger drive on the ISA data lines, two pins are provided to control an external 74ALS245 buffer. In a local bus implementation, no buffers are typically required.

Component Requirements

External pullups or pulldowns may be connected to the two IOJUMP pins if the system designer requires a base I/O location other than the default 240H. The global tristate input is pulled-up internally.

An external pullup is required on SDOUT, and external pulldowns are required on SCLK and FSYNC. Series termination resistors may be added depending on layout proximity of the CS4131 and CS4215. For close spacing, they will not be necessary.

Two 74ALS245 data buffers may be added if the 12 mA drive provided by the CS4131 is insufficient for system requirements. The "A" side of the buffers should connect to the CS4131 data bus and the "B" side of the buffers should connect to the PC data bus.

Connecting to the CS4215

The CS4131 connects to the CS4215 serial interface lines. The CS4131 requires that the CS4215 operate in master mode while recording or playing back samples. It also requires that FSYNC and TSIN be tied together on the CS4215, and the CS4215 be programmed in 128 bits per frame mode (see Control Time Slot 3 in the CS4215 data sheet). The CS4131 always receives FSYNC from the CS4215, except during Control Mode.

Transfer of Data

Write Operation

For writes to the CS4215, the CS4131 takes parallel data from the data bus and shifts it out to the Codec one bit at a time. Before shifting the data out, the CS4131 appends control bits to the data packet, and orders the data correctly according to mono/stereo and 8/16-bit conditions. When fresh data is needed for another packet, the CS4131 issues a DMA request, receives new data, and repeats the shift out operation.

Read Operation

For reads of the CS4215, the CS4131 receives a packet from the CS4215, strips off the relevant bytes according to mono/stereo and 8/16-bit conditions, and loads them into 8-bit registers. It then issues a DMA request, and the ensuing DMA read operation transfers the data from the CS4131 registers to main memory.

Control Mode Operation

For control mode operations, the CS4131 drives D/$\overline{C}$ LO to the CS4215, and takes over driving the SCLK and FSYNC lines. The control packet is formed in the CS4131 by means of I/O writes, and then shifted out under CS4131 control after an I/O write to the CS4131 results in an FSYNC.

The CS4131 acts as an 8-bit slave for programmed I/O operations, and as a 16-bit DMA slave. It is capable of meeting timing for extended ISA "TYPE A" DMA, or for the standard ISA DMA timings.

Reset

The ISA reset signal, RESDRV, resets all registers in the CS4131. The control register bits are all reset low. See descriptions of the control registers for bit interpretations.

I/O Slave Operations

The CS4131 operates as an 8-bit I/O slave meeting standard ISA timing. It occupies a 16-byte address range, with its base address set by the two IOJUMP input pins.

Internal Decode

The CS4131 register set occupies 16 contiguous I/O addresses, beginning at a base address determined by logic levels of the two I/O jumper pins as follows:

IOJUMP1	IOJUMP0	CS4131 Registers Base Address
0	0	240H
0	1	050H
1	0	260H
1	1	250H

Note: in an EISA-based system, the CS4131 can receive a slot-specific AEN, resulting in a base address of X240 for example, when IOJUMP0 and 1 are both 0, and AENX is connected to the CS4131.

Register Set

Table 1 shows the CS4131 register set.

Timeslot Registers

The TIMESLOT registers are used to load and unload the serial shift register.

Figure 10 shows the TIMESLOT and shift register data path.

The data written to the TIMESLOT registers is used to load the shift register that in turn, supplies the CS4215. The data read from the TIMESLOT registers originates from the CS4215, and is held in the registers until it can be written to main system memory (DRAM). To read what was just written to the TIMESLOT registers, the programmer must put the CS4215 into loopback mode, assert FSYNC, and wait at least 70 µs for the shift loopback operation to complete. The TIMESLOT registers can be read back at that point.

TIMESLOT registers 1 through 4 can be written either via programmed I/O writes or DMA operations. Which registers are written to or read

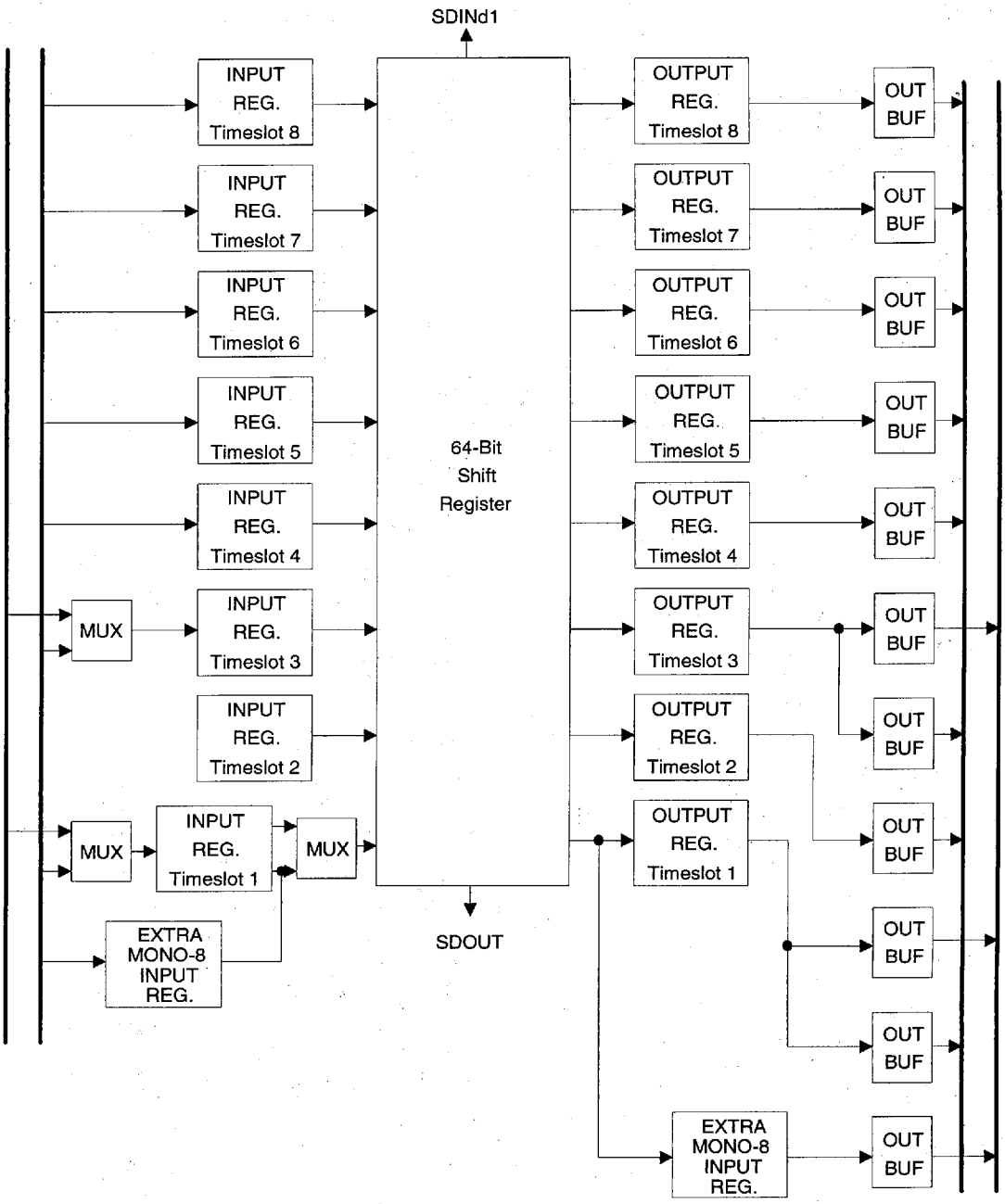


Figure 10 Register Data Path.

Register Name	Offset Address	Function
TIMESLOT1	0000	Byte 1 of packet
TIMESLOT2	0001	Byte 2 of packet
TIMESLOT3	0010	Byte 3 of packet
TIMESLOT4	0011	Byte 4 of packet
TIMESLOT5	0100	Byte 5 of packet
TIMESLOT6	0101	Byte 6 of packet
TIMESLOT7	0110	Byte 7 of packet
TIMESLOT8	0111	Byte 8 of packet
CONTROL REGISTER A	1000	Control register - CS4131 configuration bits.
CONTROL REGISTER B	1001	Control register - CS4131 configuration bits.
DIE REVISION	1010	Holds revision level of the CS4131. First revision holds the signature A0H.
FRAME COUNT READ	1011	Holds current value of internal frame bit counter. Read-only register used for chip test.
STATUS POLL	1100	Holds bits that can be read by software to determine packet transfer and interrupt flag status.
DMA COUNTER LSB READ	1101	Holds current value of LSB of DMA. Read only register used for chip test.
DMA COUNTER MSB READ	1110	Holds current value of MSB of DMA. Read only register used for chip test.
DMA COUNTER LOAD	1111	Upper byte of word that is used to initialize the DMA counter.

Table 1. Register Set Table

Bit	Name	Function
0	DMAOEN	When high, enables DMA from DRAM to CS4131 (Writes to CS4215).
1	DMAIEN	When high, enables DMA from CS4131 to DRAM (Reads of the CS4215).
2	ID/$\overline{C}$	Directly controls SERD/$\overline{C}$ pin on CS4215. When low, puts the CS4215 in control mode.
3	ICMD	When high, allows the CS4131 to drive the bidirectional SCLK and FSYNC lines that connect the CS4131 and CS4215.
4	STEREO	When high, tells the CS4131 that it should assume that the CS4215 is operating in stereo modes.
5	WIDTH16	When high, tells the CS4131 that it should assume that the CS4215 is operating with 16-bit samples.
6	IPDN	Directly controls PDN pin on the CS4215. When high, puts CS4215 into a powered down, "sleep" state. Systems that depend on the CMOUT signal of the CS4215 to always be active should never set this bit high.
7	FSYNCBIT	When ICMD is active, a write of high to this bit will cause a single FYSNC bit to be output to the CS4215. This initiates a control packet transmission. Note that no succeeding write of 0 is required.

Table 2. Control Register A Bit Definitions

Control Register B

Bit	Name	Function
0	DMACNTSEL	When high, DMA writes to CS4131 increment the DMA cycle counter. When low, DMA reads from CS4131 increment the counter.
1	DMAMOD0	Defines DMA pin usage (see DMA mode table), pg. 14
2	DMAMOD1	Defines DMA pin usage (see DMA mode table), pg. 14
3	INTCLRBIT	A write of high to this bit will clear the INT line driven by CS4131. Not that no succeeding write of 0 is required.
4	DMACNTRST	When high, resets the DMA cycle counter.
5	$\overline{\text{SERBUSEN}}$	When low, enables the CS4131 to drive serial bus lines. When high, CS4131 tristates its drivers for these lines.
6	AUDRST	When high, resets the CS4215 and also puts the CS4131 into serial loopback mode.
7	CLRSREN	When high, disables shift operations in the 64-bit shift register.

Table 3. Control Register B Bit Definitions

Status Poll Register

Bit	Name	Function
0	RCVD_TSOUT	Set high when TSOUT received at completion of packet transfer. Reset by read from Timeslot 1.
1	SENT_PKT	Packet sent out to CS4215. Set high at beginning of packet transfer. Reset by write to Timeslot 1.
6	INTOVF	Interrupt overflow. Goes active when a DMA counter terminal count is reached before a pending interrupt for a previous DMA counter terminal count was serviced. Reset by a write of high to INTCLRBIT in Control Register B
7	INTFLG	Interrupt request activated by CS4131 when DMA terminal count is reached. Reflects state of INTOUT pin. Reset by a write of high to INTCLRBIT in Control Register B.

Table 4. Status Poll Register Bit Definitions

from during DMA is determined by the CS4131 byte packing algorithm, described later.

TIMESLOT registers 5 through 8 are only written to via programmed I/O. They do not receive DMA service because they are usually static during sample playback and record operations. Keeping these register values stored in the CS4131 also reduces ISA bus bandwidth requirements.

TIMESLOT registers 5 through 8 can be written to while DMA activity is in progress. These registers may be written to asynchronously, but should be synchronized with the loading of the main shift register as follows:

1) Wait for the RCVD_TSOUT (in Status Poll Register) to go low.
2) Wait for RCVD_TSOUT to go high.
3) Write to time slot Register 5-8 immediately.

DMA Counter LSB Read

This register holds the current value of the LSB of the 16-bit DMA counter. This register is used

for chip test purposes to increase the fault coverage of the test. It is not needed by the software drivers, although it may be used for diagnostics if deemed necessary.

DMA Counter MSB Read

This register holds the current value of the MSB of the 16-bit DMA counter. This register is used for chip test purposes to increase the fault coverage of the test. It is not needed by the software drivers, although it may be used for diagnostics if deemed necessary.

DMA Counter Load Register

The DMA Counter Load register sets the initial count value for the DMA cycle counter. The DMA cycle counter is a 16-bit counter. Its lower eight bits are initialized to zero. The Counter Load Register only initializes the upper eight bits. The DMA counter is an up counter, incrementing its value on each DMA transfer. The DMACNTSEL bit in Control Register B sets the counter to increment on reads or writes.

The load value programmed in the register is inverted before loading into the DMA counter. For example, if the load value programmed was 01H, the counter will be initialized to FE00H. The counter will count 512 DMA operations before an interrupt is generated by the count value reaching FFFFH.

The number of DMA operations before interrupt generation = ((load register value+1) * 256).

Writes to CS4215 Codec

ISA Bus Operation

When DMA is enabled for writes to the CS4215 (via the DMAIEN bit in Control Register A), the CS4131 issues a DMA request (DRQ) as soon as the current contents of the TIMESLOT registers are loaded into the shift register in preparation for a packet output. Once this load occurs, the TIMESLOT registers are free to be loaded with data for the next packet output. (The DMA channel used is determined by the programming of the DMAMOD bits in Control Register B.) The DMA acknowledge ($\overline{\text{DACK}}$) will return from the system board DMA controller. While $\overline{\text{DACK}}$ is active, the DMA controller will execute one or two write cycles to the CS4131. The two cycle case occurs when the CS4131 indicates 16-bit stereo mode. Note that the DMA controller should always be programmed in demand mode. At the beginning of the last cycle that the CS4131 requires, it will deassert its DRQ signal. The data is now in the TIMESLOT register, ready to be loaded into the shift register when the next packet is needed by the CS4131.

Note that the DMA latency required for no sample underruns is approximately equal to the sample period. For example, a 44k Sample/sec rate has a latency requirement of about 22µs, while a 8 k sample/sec rate has a latency requirement of about 125 µs.

Serial Bus Operation

The activation of FSYNC by the CS4215 begins this operation. The CS4131 responds to the FSYNC sampled on the falling edge of SCLK by driving data out on its SDOUT pin on the next rising edge of SCLK. This continues for each SCLK, until the clock after TSOUT is sampled on a falling edge of SCLK.

Reads of the CS4215 Codec

ISA Bus Operation

When DMA is enabled for reads of the Codec (via the DMAIEN bit in Control Register A), the CS4131 issues a DMA request (DRQ) as soon as a packet is loaded into the TIMESLOT registers. The DMA channel used is determined by the

programming of the DMAMOD bits in Control Register B. The DMA acknowledge ($\overline{DACK}$) will return from the system board DMA controller. While $\overline{DACK}$ is active, the DMA controller will execute one or two read cycles from the CS4131. The two cycle case occurs when the CS4131 indicates 16-bit stereo mode. Note that the DMA controller should always be programmed in demand mode. At the beginning of the last cycle that the CS4131 requires, it will deassert its DRQ signal. The DMA cycle will complete with the sample data completely transferred from the CS4215 to the CS4131 to DRAM.

Note that the DMA latency required for no sample overruns is approximately equal to the sample period. For example, a 44k Sample/s rate has a latency requirement of about 22µs.

Serial Bus Operation

The activation of FSYNC by the CS4215 begins this operation. The CS4131 responds to FSYNC sampled on the falling edge of SCLK by loading data from SDIN into the shift register on the next rising edge of SCLK. This continues for each SCLK, until the clock after TSOUT is sampled on a falling edge of SCLK

Byte Ordering and Packing

8-bit Mono Reads

One DMA read operation serves for two samples. A DMA request only occurs after every second sample. The ensuing DMA read contains the first sample data on D(7:0) and the second sample data on D(15:8). Therefore, the first sample received in time goes into the lower memory location.

8-bit Stereo Reads

A DMA request is issued for each sample. The left channel data is driven on D(7:0) and the right channel data on D(15:8). Therefore, the left channel data goes into the lower memory location.

16-bit Mono Reads

A DMA request is issued for each sample. The most significant byte of the sample is driven on D(15:8) and the least significant byte on D(7:0). Therefore, the least significant byte goes into the lower memory location. This conforms to the little-endian standard of Intel x86 processors.

16-bit Stereo Reads

Two DMA reads of the CS4131 are required to load a single packet. These two reads are accomplished with a single DMA request, using the demand transfer mode of the DMA controller. The first DMA read will have the left channel most significant byte on D(15:8), and left channel least significant byte on D(7:0). The second DMA read will have the right channel most significant byte on D(15:8), and right channel least significant byte on D(7:0). The resulting filled memory will look like this:

Memory Offset	Contents
0	Left channel LSB
1	Left channel MSB
2	Right channel LSB
3	Right channel MSB

8-bit Mono Writes

One DMA write operation serves for two samples. A DMA request only occurs after every second sample. The CS4131 will use the data on

DMAMOD1	DMAMOD0	DMA Channel Usage
0	0	Neither channel used. Both DRQ0 and DRQ1 tristated. INTOUT is tristated, too.
0	1	DMA channel 0 is used for both reads from and writes to the CS4215. INTOUT enabled.
1	0	DMA channel 1 is used for both reads form and writes to the CS4215. INTOUT enabled.
1	1	DMA channel 0 is used for reads from the CS4215. DMA channel 1 is used for writes to the CS4215. INTOUT enabled.

Table 5. DMA Mode Table

D(7:0) for its first packet, and the data on D(15:8) for its second packet.

During pause of play (suspended DMA), the CS4131 will still send alternating samples from TIMESLOT1 register and the extra storage register. To avoid an output of Fs/2, set the WIDTH16 bit in Control Register A. When DMA resumes, this bit can be reset.

8-bit Stereo Writes

A DMA request is issued for each sample. The CS4131 will use the data on D(7:0) as left channel data, and the data on D(15:8) as right channel data.

16-bit Mono Writes

A DMA request is issued for each sample. The CS4131 will use the data on D(7:0) as the least significant byte of the sample data, and the data on D(15:8) as the most significant byte of the sample data.

16-bit Stereo Writes

Two DMA writes from the CS4131 are required to unload a single packet. These two writes are accomplished with a single DMA request, using the demand transfer mode of the DMA controller. The first DMA write will expect the left channel most significant byte on D(15:8), and left channel least significant byte on D(7:0). The second DMA write will expect the right channel most significant byte on D(15:8), and right channel least significant byte on D(7:0) The required memory map is shown below:

Memory Offset	Contents
0	Left channel LSB
1	Left Channel MSB
2	Right channel LSB
3	Right channel MSB

DMA and Interrupt Issues

DMA Mode Selection

The CS4131 provides the flexibility of software-selectable DMA channels. Note that the CS4131 must utilize 16-bit DMA channels, which are typically channels 5, 6, and 7 in ISA systems. The channel usage is set by the DMAMOD bits of Control Register B, as shown in Table 5.

DMA Counter

The DMA counter is used to count the number of either DMA writes to the CS4215 or DMA reads from the CS4215, depending upon the setting of the DMACNTSEL bit found in Control Register B. When the counter reaches its terminal value of FFFFH, the INTOUT output of the CS4131 is activated. This interrupt can signal the

software driver that the sample ring buffer in DRAM needs to be serviced. The counter is set to its initial value via the DMA Counter Load Register. This register sets the upper eight bits of the counter to the inverse of the value that is programmed into it. The lower eight bits of the counter are always initialized to FE00H. The counter will count 512 DMA operations before an interrupt is generated by the count value reaching FFFFH.

The number of DMA operations before interrupt generation = ((load register value+1) * 256).

After the counter reaches FFFFH, it rolls over and begins counting again at the value programmed by the DMA Counter Load Register.

Interrupt Output

Generation

The INTOUT signal is generated when the DMA counter reaches FFFFH. it remains active until cleared via the I/O write described below. The state of INTOUT is mirrored in the INTFLG bit in the Status Poll Register.

Clearing

The INTOUT signal is cleared by writing a high to the INTCLRBIT found in Control Register B. If left active in the register, this high will not prevent a succeeding INTOUT from being asserted. Therefore, there is no need to write a low to INTCLRBIT after the first write of a high.

CS4215 Control Mode

Enabling of SCLK and FSYNC

The CS4131 will drive SCLK and FSYNC when the ICMD bit found in Control Register A is high. It is recommended that this bit only be set high when ID/$\overline{C}$ in the same register is low. This will prevent contention with the CS4215 on these lines.

The CS4131 enables these lines synchronously to the new SCLK that will be driven. In other words, when these lines are enabled, there will be no spikes or runt pulses on SCLK, and FSYNC will be initially driven to a clean low. The CS4131 also disables these lines synchronously to SCLK, ensuring that there are no clock spikes or runt pulses.

The synchronization carries a time penalty, so allow 2 µs after the I/O write that modifies ICMD before assuming that the action of the write (SCLK/FSYNC enable or disable) is complete.

SCLK frequency

The SCLK generated by the CS4131 for control mode operations is formed by a divide-by-eight of the ISA BCLK input. Therefore, it will operate at a nominal frequency of 1 MHz.

FSYNC generation

FSYNC is generated for the CS4215 control mode by writing a high to the FSYNCBIT found in Control Register A. Note that no succeeding write of a low is required.

Under normal operation, a second FSYNC cannot be generated until the TSOUT from the first one is received. This can cause a problem with the CS4215, as it does not return TSOUT from the first FSYNC it receives when it goes into control mode. To work around this problem, observe the following procedure.

1) Generate initial FSYNC with FSYNCBIT.

2) Wait a minimum of 100 µs.

3) Allow a second FSYNC to be sent by pulsing the CLRSREN bit found in Control Register B high, then low.

4) Send a second FSYNC by writing to Control Register A with FSYNCBIT high.

5) Read Status Poll Register until RCVD TSOUT is active.

Now the CS4215 should be returning TSOUT to each FSYNC and FSYNC can be asserted using a polling procedure instead of using software timers:

1) Read and write to offset 0 to clear Status Poll Register bits.

2) Generate FSYNC.

3) Read Status Poll Register to determine if TSOUT has been received by the CS4131. If so, read and write to offset 0 to clear Status Poll Register bits.

CS4215 Reset

The CS4215 is reset by two conditions:

1) ISA Bus reset initiated by RESDRV. This also resets all CS4131 logic.

2) XAUDRST bit found in Control Register B is high. Note that this bit also puts the CS4131 into serial loopback mode. XAUDRST does not reset CS4131 logic - it only puts it into loopback mode.

Selective Tristate of Serial Lines

The CS4131 serial lines that interface to the CS4215 are tristated by the CS4131 when the $\overline{\text{SERBUSEN}}$ bit found in Control Register B is driven inactive (high). Note that these lines are not tristated upon power up reset.

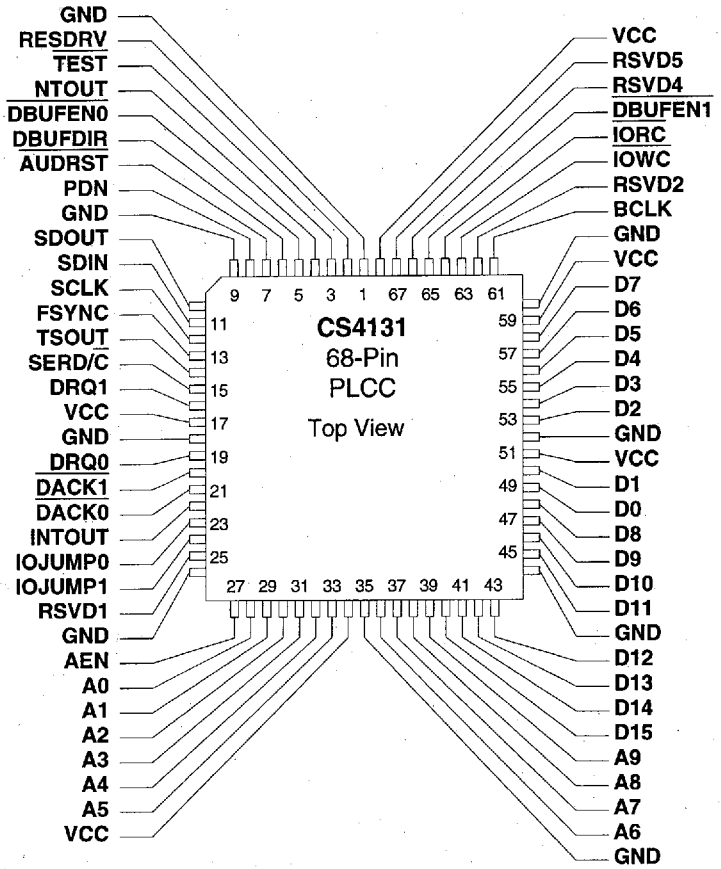
External Buffer Control

The CS4131 data bus lines can sink up to 12 mA per pin. For system applications where greater drive is required, the CS4131 provides control lines for two external 74ALS245 type buffers. The 74ALS245's should have their "A" sides connected to the CS4131, and their "B" sides connected to the ISA data bus. The CS4131 $\overline{\text{DBUFEN0}}$ output should be connected to the $\overline{\text{EN}}$ input of the 74ALS245 that connects to the low order byte of the ISA data bus, and the $\overline{\text{DBUFEN1}}$ output should be connected to the $\overline{\text{EN}}$ input of the 74ALS245 that connects to the high order byte of the ISA data bus. The CS4131 DBUFDIR output should be connected to the DIR input of both 74ALS245's.

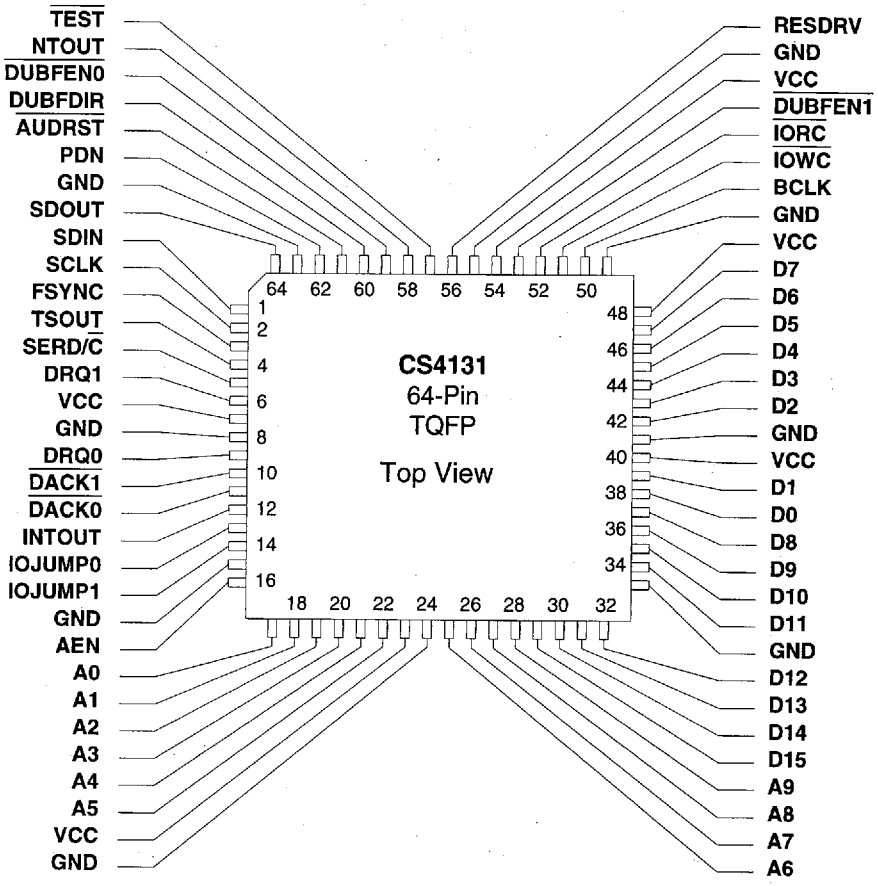
The Loopback Mode

The CS4131 loopback mode is a useful tool for diagnostics. When XAUDRST is active, the shift register output is looped around to its input. After a full frame send, the data written to the TIMESLOT registers can be read back at the same addresses. When in loopback mode, FSYNC must be generated via the FSYNCBIT for a loopback operation. An internal-only version of TSOUT is generated by the CS4131, so the RCVD TSOUT bit may be used to determine when the frame shift operation is complete. Alternatively, a wait after sending FSYNC of about 100 µs may be used.

PIN DESCRIPTIONS



PIN DESCRIPTIONS



Serial Interface Pins

FSYNC - Frame Sync, Pin 13(L), 3(Q)
Frame Synchronization Signal. 4mA CMOS I/O.

SDOUT - Serial Data Output, Pin 10(L), 20(Q)
Serial data out to CS4215. 4mA CMOS Output.

SDIN - Serial Data In, Pin 11(L), 1(Q)
Serial data in from CS4215. CMOS Input, Weak Pull Up.

SCLK - Serial Clock, Pin 12(L), 2(Q)
Serial Clock Signal. 4mA CMOS I/O.

PDN - Power Down, Pin 8(L), 18(Q)
4mA CMOS Output.

SERD/$\overline{C}$ - Serial Data/Control, Pin 15(L), 5(Q)
Serial data/control word indicator. 4mA CMOS Output.

TSOUT - Timeslot Out, Pin 14(L), 4(Q)
End of frame indicator from CS4215. CMOS Input, Weak Pull Down.

$\overline{AUDRST}$ - Pin 7(L), 61(Q)
Reset for CS4215. 4mA CMOS Output

ISA Bus Control

DRQ1 - DMA Channel 1 Request, Pin 16(L), 6(Q)
12mA TTL Output.

DRQ0 - DMA Channel 0 Request, Pin 19(L), 9(Q)
12mA TTL Output.

$\overline{DACK1}$ - DMA Channel 1 Acknowledge, Pin 20(L), 10(Q)
Schmitt TTL Input.

$\overline{DACK0}$ - DMA Channel 0 Acknowledge, Pin 21(L), 11(Q)
Schmitt TTL Input

INTOUT - Interrupt Out, Pin 22(L), 12(Q)
12mA TTL Output.

$\overline{IORC}$ - Pin 64(L), 52(Q)
ISA I/O read signal used for CPU-driven I/O and DMA operations. Schmitt TTL Input.

$\overline{IOWC}$ - Pin 63(L), 51(Q)
ISA I/O write signal used for CPU-driven I/O and DMA operations. Schmitt TTL Input.

AEN - Pin 27(L), 16(Q)
Address can be decoded from address bus when low. TTL Input.

ISA Clock and Reset

BCLK - Bus Clock, Pin 61(L), 50(Q)
Schmitt TTL Input.

RESDRV - ISA Bus Reset Signal, Pin 2(L), 56(Q)
Schmitt TTL Input.

A4 - A9 - Address Lines Used for Decode Register Block, Pins [32, 33, 36 - 39(L)] [21, 22, 25-28(Q)]

TTL Inputs.

A0 - A3 - Address Lines Used for Register Selection, Pins [28 - 31(L)] [17-20(Q)]

TTL Inputs.

D0 - D15 - Parallel Data Bus Bits, Pins [49, 50, 53-58, 48 - 45, 43 - 40(L)] [38, 39, 42-47, 37-34, 32-29(Q)]

12mA TTL I/O.

IOJUMP1 - I/O Jumper 1, Pin 24(L), 14(Q)

Jumper to determine I/O base address. CMOS Input, Weak Pull Up.

IOJUMP0 - I/O Jumper 0, Pin 23(L), 13(Q)

Jumper to determine I/O base address. CMOS Input, Weak Pull Up.

External Buffer Control

$\overline{\text{DBUFEN0}}$ - Data Buffer Enable 0 Pin 5(L), 59(Q)

Enable for external '245 type data buffer that may connect low order byte of ISA and CS4131 data buses. 8mA TTL Output.

$\overline{\text{DBUFEN1}}$ - Data Buffer Enable 1, Pin 65(L), 53(Q)

Enable for external '245 type data buffer that may connect high order byte of ISA and CS4131 data buses. 8mA TTL Output.

DBUFDIR - Data Buffer Direction, Pin 6(L), 60(Q)

Direction control for both '245 type data buffers that may connect ISA and CS4131 data buses. 8mA TTL Output.

Power and Ground Pins

VCC - Digital Power Supply, Pins [17, 34, 51, 59, 68(L)] [7, 23, 40, 48, 54(Q)]

GND - Digital Ground, Pins [1, 9, 18, 26, 35, 44, 52, 60(L)] [55, 63, 8, 15, 24, 33, 41, 49(Q)]

Miscellaneous

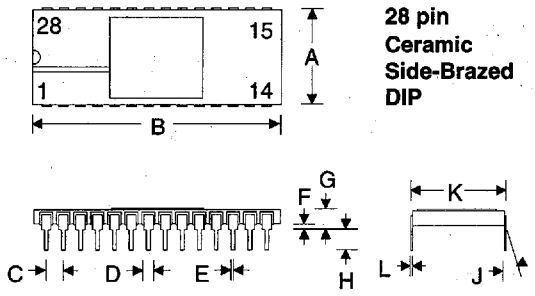
$\overline{\text{TEST}}$ - Pin 3(L), 57(Q)

Tristates all outputs except NTOUT for test purposes. CMOS input, Weak Pull Up.

NTOUT - NAND Tree Output, Pin 4(L), 58(Q)

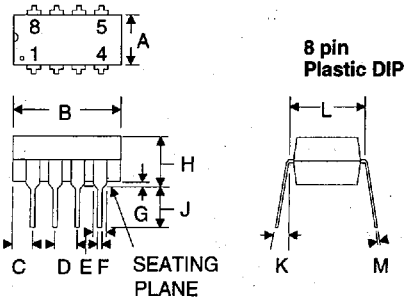
2mA CMOS Output.

MECHANICAL DATA



28 pin Ceramic Side-Brazed DIP

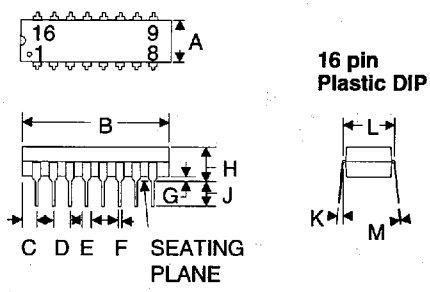
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.73	15.34	0.580	0.604
B	35.20	35.92	1.386	1.414
C	2.54 BSC		0.100 BSC	
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012



8 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	9.14	10.2	0.360	0.400
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

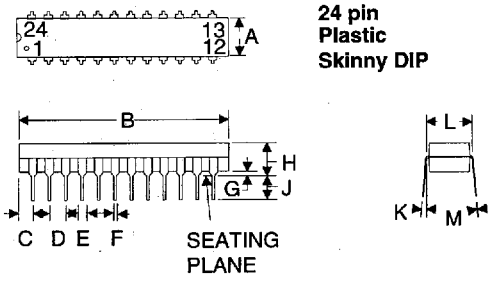
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



16 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.80	19.30	0.740	0.760
C	1.32	2.89	0.015	0.035
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

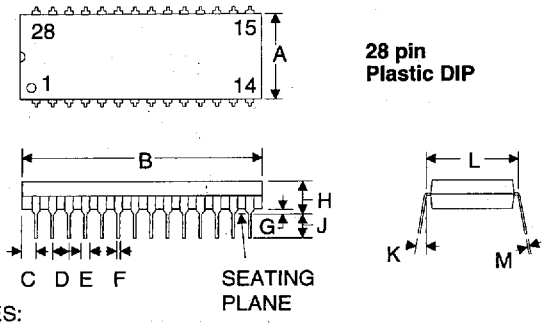
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin
Plastic
Skinny DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015

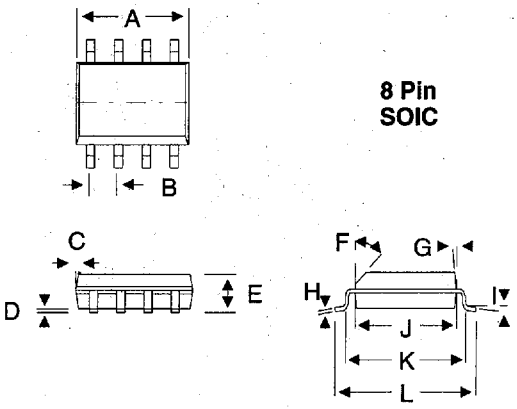
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



28 pin
Plastic DIP

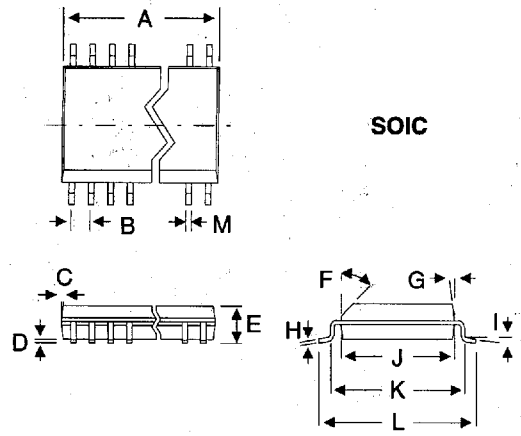
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



8 Pin
SOIC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.25	5.30	0.207	0.209
B	1.27 TYP		0.050 TYP	
C	7° NOM		7° NOM	
D	0.120	0.180	0.005	0.007
E	1.80	1.86	0.071	0.073
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.195	0.205	0.0078	0.0082
I	2°	4°	2°	4°
J	-	-	-	-
K	6.57	6.63	0.259	0.261
L	7.85	7.95	0.308	0.312

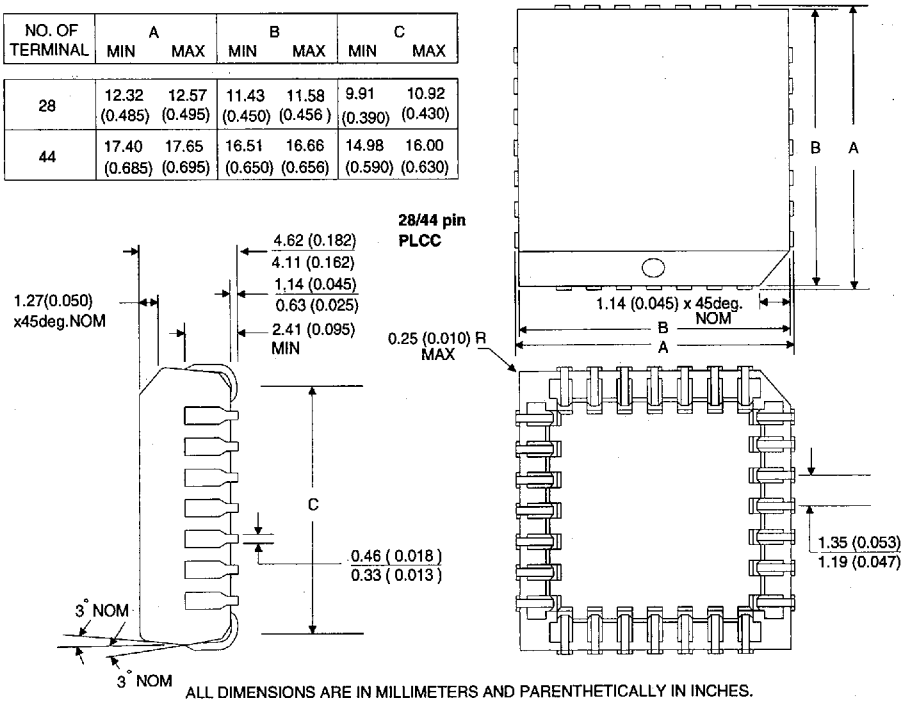


SOIC

pins	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
16	9.91	10.41	0.390	0.410
20	12.45	12.95	0.490	0.510
24	14.99	15.50	0.590	0.610
28	17.53	18.03	0.690	0.710

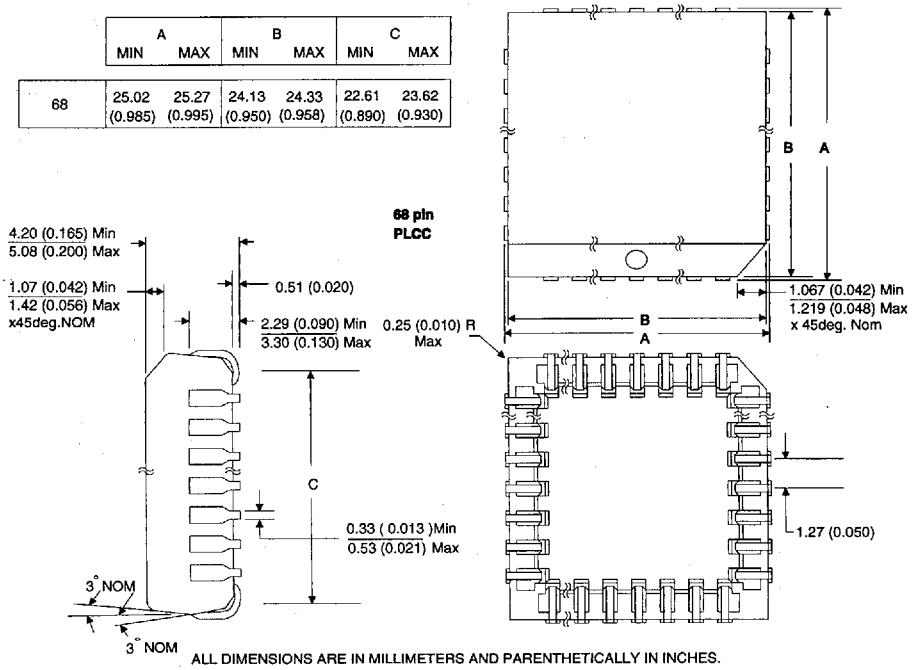
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	see table above			
B	1.27	BSC	0.050	BSC
C	7°	NOM	7°	NOM
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45°	NOM	45°	NOM
G	7°	NOM	7°	NOM
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420
M	0.33	0.51	0.013	0.020

NO. OF TERMINAL	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

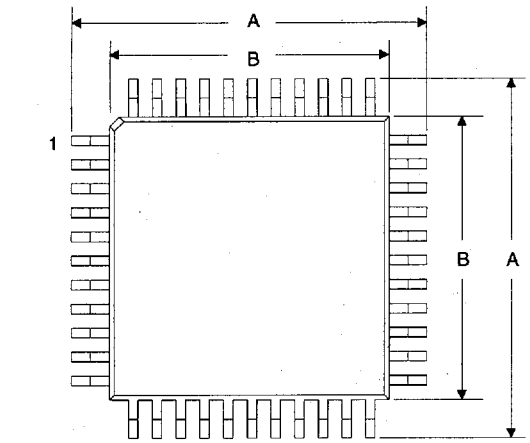
	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
68	25.02 (0.985)	25.27 (0.995)	24.13 (0.950)	24.33 (0.958)	22.61 (0.890)	23.62 (0.930)



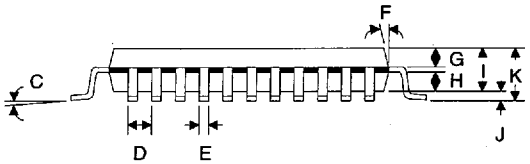
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

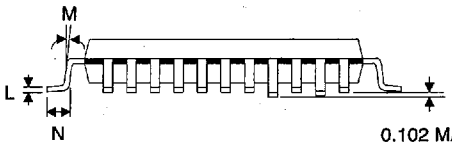
11

44 PIN QUAD FLATPACK

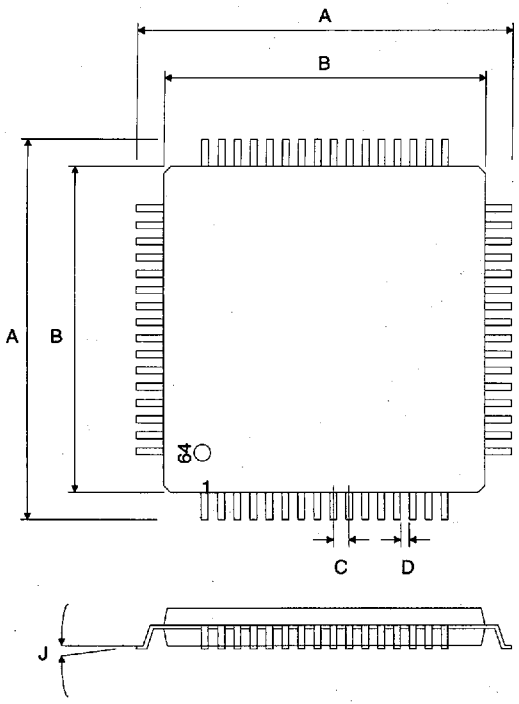


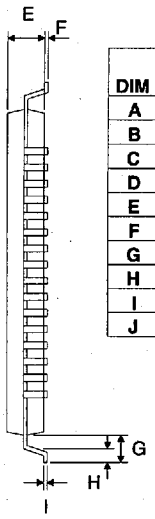
	44 Pin TQFP 1.4 mm Package Thickness			
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.75	12.25	0.463	0.482
B	9.90	10.10	0.390	0.398
C	0°	7°	0°	7°
D	0.80 BSC		0.031 BSC	
E	0.35 BSC		0.014 BSC	
F		12°		12°
G	0.54	0.74	0.021	0.029
H	0.54	0.74	0.021	0.029
I	1.35	1.50	0.053	0.059
J	0.05		0.002	
K		1.60		0.063
L		0.17		0.007
M	2°	10°	2°	10°
N	0.35	0.65	0.014	0.026





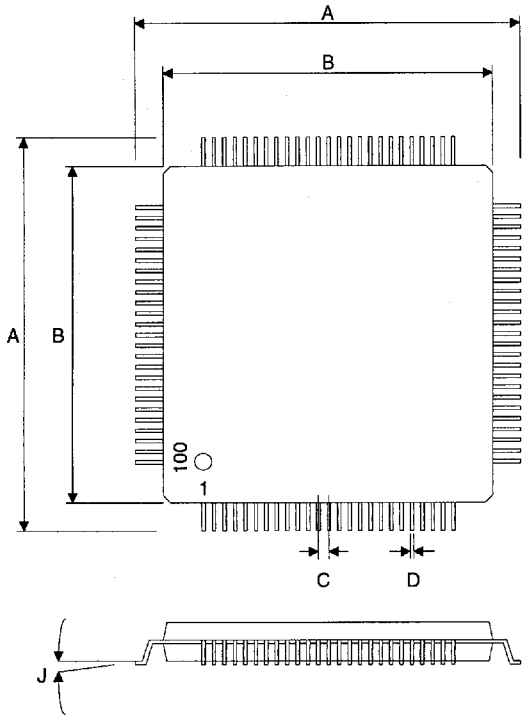
0.102 MAX
Lead Coplanarity

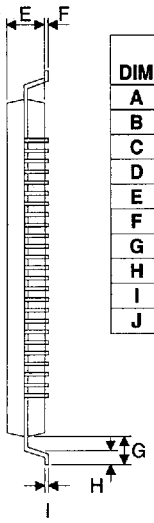




64 Pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.00 BSC		0.472 BSC	
B	10.00 BSC		0.393 BSC	
C	0.50 BSC		0.020 BSC	
D	0.14	0.30	0.005	0.012
E	0.95	1.12	0.037	0.044
F	0.05	0.15	0.002	0.006
G	1.00 BSC		0.039 BSC	
H	0.45	0.75	0.018	0.030
I	0.09	0.18	0.003	0.007
J	0°	7°	0°	7°





100-pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.75	16.25	0.620	0.640
B	13.90	14.10	0.547	0.555
C	0.50 BSC		0.020 BSC	
D	0.10	0.20	0.004	0.012
E	1.25	1.55	0.049	0.061
F	0.00	0.20	0.000	0.008
G	1.00 BSC		0.039 BSC	
H	0.35	0.65	0.014	0.026
I	0.077	0.177	0.003	0.007
J	0°	10°	0°	10°

11