ADVANCE INFORMATION

ADV MICRO (TELECOM)

T-75-11-17

Am7943(A)

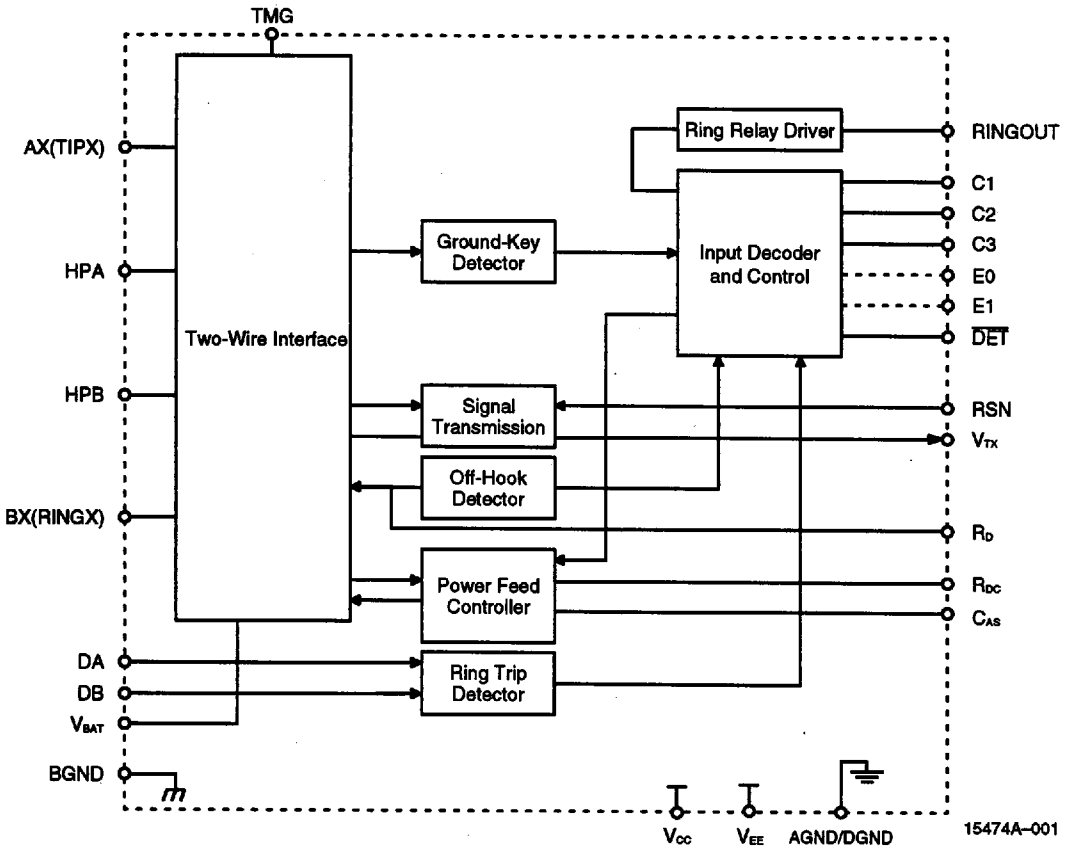
Subscriber Line Interface Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Programmable constant current feed
- Current gain = 200
- Programmable loop detect threshold
- Low standby power
- Performs polarity reversal (A version)
- Ground-key detector
- 0°C to +70°C ambient temperature range
- Tip open state for ground start lines
- –19 V to –56.5 V battery operation
- Two-wire impedance set by single external impedance
- On-hook transmission
- On-chip ring relay driver and relay snubber circuit
- A version satisfies TR-TSY-000057 requirements
- Standard version satisfies EIA/TIA-464-A

BLOCK DIAGRAM



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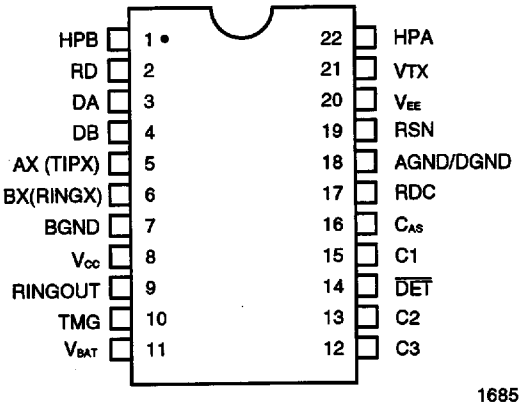
CONNECTION DIAGRAMS

22-Pin Plastic DIP
or
22-Pin Ceramic DIP



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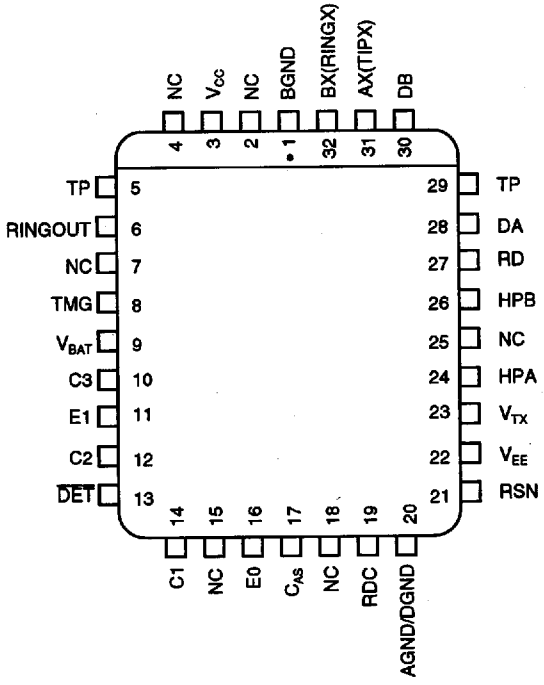
32-Pin PLCC



Notes: 1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate.
3. NC = No connect.

ORDERING INFORMATION
Standard Products

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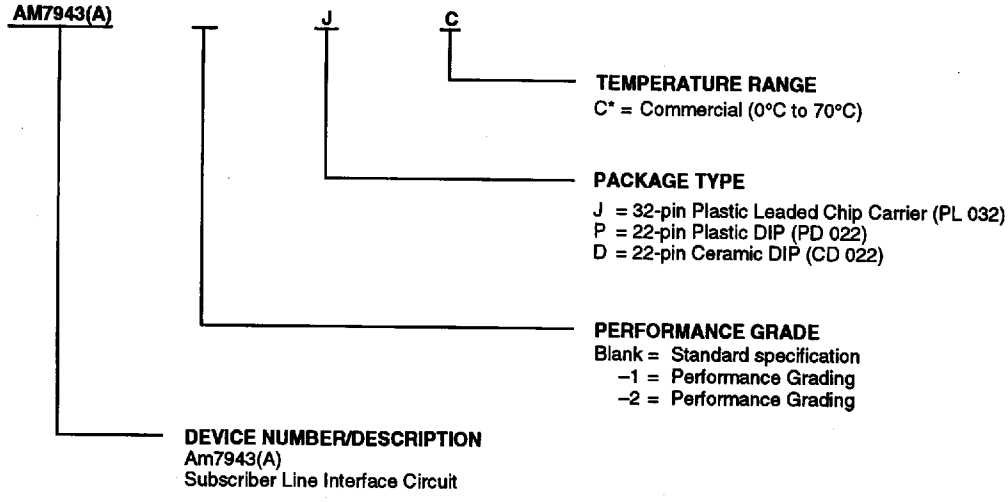
AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM7943(A)	DC, JC, PC
	–1DC, –1JC, –1PC
	–2DC, –2JC, –2PC

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD standard military grade products.

*The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

PIN DESCRIPTION

AGND/DGND
Ground

Analog and Digital ground.

AX(TIPX)
(Output)

Output of A(TIP) power amplifier.

BGND
Ground

Battery (power) ground.

BX(RINGX)
(Output)

Output of B(RING) power amplifier.

C3–C1 Decoder
(Inputs)

TTL compatible. C3 is MSB and C1 is LSB.

DA
Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB
Ring Trip Positive (Input)

Positive input to ring trip comparator.

$\overline{\text{DET}}$
Switch Hook Detector (Output)

When enabled, a logic Low indicates the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E0, E1). The output is open-collector with a built-in 15K pull-up resistor.

E0
Ground-Key Enable (Input)

A logic High enables $\overline{\text{DET}}$. Low disables $\overline{\text{DET}}$ (PLCC only).

E1
Ground-Key Enable (Input)

E1 = Low connects the ground-key or ring-trip detector to $\overline{\text{DET}}$; E1 = High connects the off-hook or ring-trip detector to $\overline{\text{DET}}$ (PLCC only).

HPA

A(TIP) side of high-pass filter capacitor.

HPB

B(RING) side of high-pass filter capacitor.

RD

Threshold modification and filter point for the off-hook detector.

RDC

Connection point for the DC feed current programming network. The other end of the network connects to the Receiver Summing Node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.

RINGOUT
Ring Relay Driver (Output)

Open collector driver with emitter internally connected to BGND.

RSN
Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 200 times the current into this pin. The networks which program receive gain, two-wire impedance, and feed resistance all connect to this node.

V_{BAT}

Battery supply.

V_{CC}

+5-V power supply.

V_{EE}

–5-V power supply.

V_{TX}
Transmit Audio (Output)

This output is a unity gain version of the AX(TIPX) and BX(RINGX) metallic voltage. The other end of the two-wire input impedance programming network connects here.

C_{AS}
Reference Filter Capacitor

A capacitor should be connected to this pin to filter internal anti-saturation reference voltage.

TMG
Thermal Management

A resistor connected from this pin to V_{BAT} reduces the on-chip power dissipation in the normal polarity, active state.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –55°C to +150°C

V_{CC} with respect to AGND/DGND .. –0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND .. +0.4 V to –7.0 V

V_{BAT} with respect to AGND/DGND ... +0.4 V to –70 V

Note: Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass = 0.33 µF.

AGND/DGND with respect to
BGND ..... +1.0 V to –3.0 V

AX(TIPX) or BX(RINGX) to BGND:

Continuous ..... –70 V to +1.0 V
10 ms (F = 0.1 Hz) ..... –70 V to +5.0 V
1 µs (F = 0.1 Hz) ..... –90 V to +10 V
250 ns (F = 0.1 Hz) ..... –120 V to +15 V

Current from AX(TIP) or BX(RING) ..... ±150 mA

Voltage on RINGOUT ..... BGND to +10 V

Current through Relay Driver
or internal driver catch diodes ..... 60 mA

Voltage on Ring Trip Inputs
(DA and DB) ..... V_{BAT} to 0 V

Current into Ring Trip Inputs ..... ±10 mA

C3–C1, E0, E1 to
AGND/DGND ..... –0.4 V to V_{CC} + 0.4 V

Maximum Power Dissipation (see note) ... T_A = 70°C

In 22-pin ceramic DIP package ..... 1.5 W
In 22-pin plastic DIP package ..... 1.25 W
In 32-pin PLCC package ..... 1.74 W

Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never reach this temperature, and operation above 145°C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) ..... 0°C to +70°C

Supply Voltage (V_{CC}) ..... 4.75 V to 5.25 V

V_{EE} ..... –4.75 V to –5.25 V

V_{BAT} ..... –19 V to –56.5 V

AGND/DGND ..... 0 V

BGND with respect to
AGND/DGND ..... –100 mV to +100 mV

Load Resistance on V_{TX} to Ground .... 10 Kohm Min

"–2" performance grade SLICs are functional from –40°C to +85°C. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

Operating ranges define those limits between which the device specifications are guaranteed.

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ELECTRICAL CHARACTERISTICS (see Note 1, page 1-45)

The Am7943 (non-A) device is tested under the following conditions unless otherwise noted. Battery = –24 V, RL = 600 ohms. The Am7943(A) device is tested under the following conditions unless otherwise noted. Battery = –48 V, RL = 900 ohms. All specifications apply to both the Am7943 and Am7943(A) unless noted.

Description	Test Conditions	Notes	P.G.*	Advance Information Min	Typ	Max	Unit
Analog (V_{TX}) Output Impedance					3		ohm
Analog (V_{TX}) Output Offset				–30		+30	mV
Analog (RSN) Input Impedance	300 Hz to 3.4 kHz				1	20	ohm
Longitudinal Impedance at AX or BX						35	ohm
Overload Level	four-wire active state	2		–2.5		+2.5	Vpk
	two-wire active state						
	On-hook, R_{LAC} = 900 ohm Active or Disable State	2		0.95			Vrms
Transmission Performance							
Two-Wire Return Loss (see Test Circuit D)	200 Hz to 3400 Hz	4, 8		26			dB
Longitudinal Balance (two-wire and four-wire, see Test Circuit C); RL = 600 ohms at V_{BAT} = 24 V, RL = 740 ohms at V_{BAT} = 48 V							
Longitudinal to Metallic L-T, L-4	200 Hz to 1 kHz Normal Polarity		–1	54			dB
			–2	63			
				63			
	1 kHz to 3.4 kHz Normal Polarity		–1	54			dB
			–2	58			
				58			
Longitudinal Signal Generation 4-L	300 Hz to 800 Hz Normal Polarity			42			dB
Longitudinal Current	Active State			27	35		mA RMS
	Disable State			27	35		
Insertion Loss (two-wire to four-wire and four-wire to two-wire, see Test Circuits A and B)							
Gain Accuracy	0 dBm, 1 kHz			–0.15		+0.15	dB
Gain Accuracy, Disable Mode	–10 dBm, On-hook, R_{LAC} = 900 ohms			–1.0		+1.0	dB
Variation with Frequency	300 Hz to 3400 Hz Relative to 1 kHz			–0.10		+0.10	dB
Gain Tracking	+7 dBm to –55 dBm Reference: 0 dBm	4		–0.10		+0.10	dB

*P.G. = Performance Grade

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Notes	P.G.	Advance Information Min	Typ	Max	Unit
Balance Return Signal (four-wire to four-wire, see Test Circuit B)							
Gain Accuracy	0 dBm, 1 kHz			–0.15		+0.15	dB
Variation with Frequency	300 Hz to 3400 Hz Relative to 1 kHz	3		–0.10		+0.10	dB
Gain Tracking	±3 dBm to –55 dBm Reference: 0 dBm	4		–0.10		+0.10	dB
Group Delay	f = 1 kHz	4, 9			5.3		µs
Total Harmonic Distortion (two-wire to four-wire or four-wire to two-wire, see Test Circuits A and B)							
Harmonic Distortion 300 Hz to 3400 Hz	two-wire level = 0 dBm				–64	–50	dB
	two-wire level = +7 dBm				–55	–40	
Idle Channel Noise							
C-Message Weighted Noise	two-wire	4		+7		+10	dBrnc
	four-wire			+7		+10	
Psophometric Weighted Noise	two-wire			–83		–80	dBmp
	four-wire			–83		–80	
Line Characteristics, Active Mode (see Figures 1a and 1b)							
Short Loops, Active Mode	Battery = –43 V, R_{LDC} = 600 ohms	4		25	27	29	mA
	Battery = –48 V, R_{LDC} = 600 ohms						
	Battery = –24 V, R_{LDC} = 300 ohms						
Long Loops, Active Mode	Battery = –43 V, R_{LDC} = 1.3 K			23			mA
	Battery = –48 V, R_{LDC} = 1.9 K			18			
Disable Mode	Battery = –48 V, R_{LDC} = 600 ohms			17	19	21	mA
	Battery = –24 V, R_{LDC} = 300 ohms						
Standby Mode	$IL = \frac{\lvert V_{BAT}\rvert - 3\,V}{RL + 1800}$, $T_A = 25°C$			.7IL	IL	1.3IL	mA
Loop Current	Tip open, RL = 0					1	mA
	Disconnect, RL = 0					1	
ILLIM (Itip + Iring)	Tip and Ring Shorted to Ground				100	130	mA
Open Circuit Voltage	Battery = –48 V, Active and Disable			41.3	42.3		V
	Battery = –24 V, Active and Disable			16	17.3		V

*Applies only when switching regulator is used.

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Notes	P.G.	Advance Information Min	Typ	Max	Unit
Power Dissipation, Normal Loop Polarity, Battery = –48 V							
On-Hook, Open Circuit					25	70	mW
On-Hook, Disable Mode					120	210	
On-Hook, Active Mode					160	280	
On-Hook, Standby Mode					35	85	
Off-Hook, Disable Mode	RL = 300 Ω, RTMG = ∞ Battery = –48 V				900	1050	
	Battery = –24 V				470	560	
	RL = 300 Ω, RTMG = 1700				250	600	
Off-Hook, Active Mode	RL = 300 Ω, RTMG = ∞ Battery = –48 V				1.25	1.45	W
	Battery = –24 V				.6	.75	
	RL = 300 Ω, RTMG = 1700				.65	.85	
Off-Hook, Standby Mode	RL = 300 Ω, T_A = 25°C				.88	1.20	
Supply Currents							
V_{CC} On-Hook Supply Current	Open Circuit Mode				1.5	2	mA
	Disable Mode				4	7.5	
	Standby Mode				2	2.5	
	Active Mode				5	8.5	
V_{EE} On-Hook Supply Current	Open Circuit Mode				0.7	2	
	Disable Mode				2	3.5	
	Standby Mode				0.7	2	
	Active Mode				2.5	5	
V_{BAT} On-Hook Supply Current	Open Circuit Mode				0.3	1	
	Disable Mode				2.5	4.7	
	Standby Mode				0.8	1.5	
	Active Mode				3.5	5.7	
Power Supply Rejection Ratio (Vripple = 50 mV RMS), Active Normal Mode							
V_{CC}	50 Hz to 3400 Hz	5		35	45		dB
V_{EE}	50 Hz to 3400 Hz	5		30	45		
V_{BAT}	50 Hz to 3400 Hz	5		35	45		
Effective Int. Resistance	C_{AS} Pin to Ground	4		85	170	255	Kohm
RFI Rejection	100 Hz to 30 MHz (See Figure E)	4				1	mVRMS
Off-Hook Detector							
Current Threshold	I_{DET} = 365/RD			–10		+10	%
Ground-Key Detector Thresholds, Active Mode							
Resistance Threshold	B(Ring) to GND			2.0	5.0	10.0	Kohm
Ground-Key Current Threshold	B(Ring) to GND	6			9		mA
	Midpoint to GND				9		
Ring Trip Detector Input							
Bias Current				–0.5	–0.05		µA
Offset Voltage	Source Resistance = 2 Mohm	7		–50	0	+50	mV

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Notes	P.G.	Advance Information Min	Typ	Max	Unit
Logic Inputs (C1, C2, C3, E0, and E1							
Input High Voltage				2.0			V
Input Low Voltage						0.8	V
Input High Current	All inputs except C3			–75		40	µA
Input High Current	Input C3			–75		150	µA
Input Low Current				–0.4			mA
Logic Output ($\overline{DET}$)							
Output Low Voltage	I_{OUT} = 0.8 mA					0.4	V
Output High Voltage	I_{OUT} = –0.1 mA			2.4			V

Table 1. SLIC Decoding

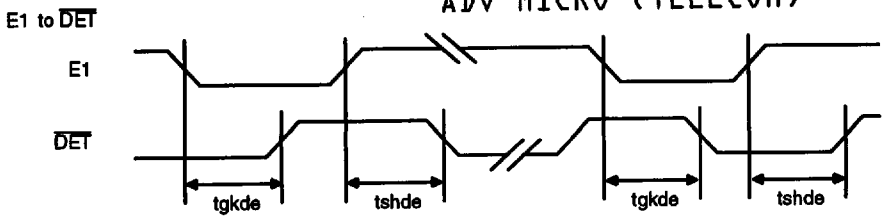
State	C3	C2	C1	Two-Wire Status	$\overline{DET}$ Output E1 = 1	$\overline{DET}$ Output E1 = 0
0	0	0	0	Open Circuit	Ring Trip	Ring Trip
1	0	0	1	Ringing	Ring Trip	Ring Trip
2	0	1	0	Active	Loop Det.	Ground Key
3	0	1	1	Disable	Loop Det.	Ground Key
4	1	0	0	Tip Open	Loop Det.	Ground Key
5	1	0	1	Standby	Loop Det.	Ground Key
6	1	1	0	Active Polarity Reversal	Loop Det.	Ground Key
7	1	1	1	Disable Polarity Reversal	Loop Det.	Ground Key

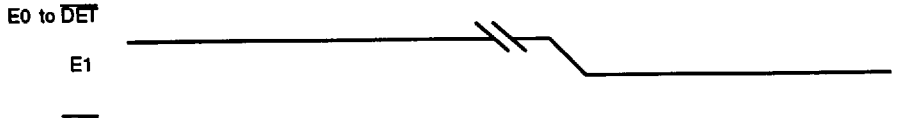
Note: E0 and E1 are internally pulled High and, in the 22-pin DIP package option, are not pinned-out.

SWITCHING CHARACTERISTICS (32-Pin PLCC Only)

Parameter		Test Conditions	Min	Typ	Max	Unit
tgkde	E1 Low to $\overline{DET}$ High (E0 = 1)	Ground-Key Detect Mode RL Open, RG Connected (see Test Circuit H)	–	–	3.8	µs
	E1 Low to $\overline{DET}$ Low (E0 = 1)		–	–	1.1	
tshde	E1 High to $\overline{DET}$ Low (E0 = 1)	Switch Hook Detect Mode R_L = 600 ohms, RG Open (see Test Circuit G)	–	–	1.2	µs
	E1 High to $\overline{DET}$ High (E0 = 1)		–	–	3.8	
tshdd	E0 High to $\overline{DET}$ Low (E1 = 1)				1.1	
tshd0	E0 Low to $\overline{DET}$ High (E1 = 1)				3.8	
tgkdd	E0 High to $\overline{DET}$ Low (E1 = 0)				1.1	
tgkd0	E0 Low to $\overline{DET}$ High (E1 = 0)				3.8	

SWITCHING WAVEFORMS





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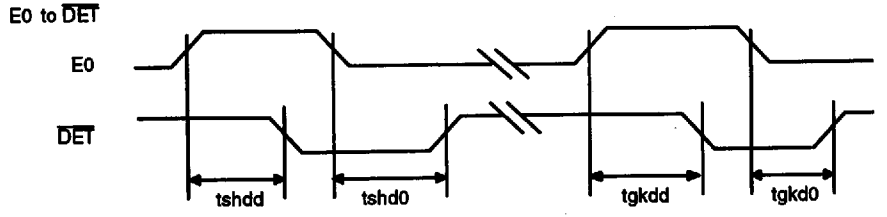

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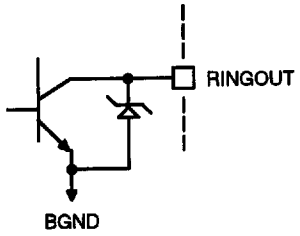
Note: All delays measured at 1.4-V levels.

RELAY DRIVER SPECIFICATIONS



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Description	Test Conditions	Note	Advance Information Min	Typ	Max	Unit
Relay Driver Output (RINGOUT)						
On Voltage	30 mA Sink			+0.3	+0.6	V
Off Leakage	V_{OH} = +5 V				100	µA
Zener Breakover	100 µA		6	7.2		V
Zener On Voltage	30 mA			10		V

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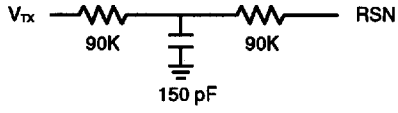
Notes:

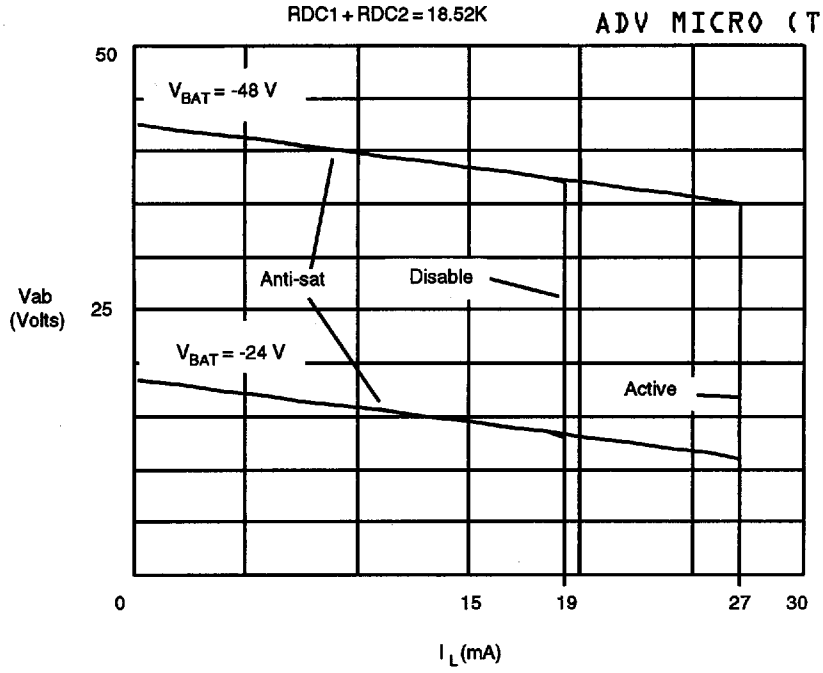
1. Unless otherwise noted, test conditions are: V_{CC} = +5 V, V_{EE} = –5 V, C_{HP} = 0.33 µF, R_{DC1} = R_{DC2} = 9.26 Kohms, C_{DC} = 0.33 µF, RD = 35.4K, C_{AS} = 0.33 µF, and no fuse resistors. For the Am7943 (non-A): Battery = –24 V, RL = 600 ohms, and R_{MG} = ∞. For the Am7943A: Battery = –48 V, RL = 900 ohms, and R_{MG} = 1700 ohms.
2. Overload level is defined when THD = 1%.
3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes the two-wire AC load impedance matches the programmed impedance.
4. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
5. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
6. Midpoint is defined as the connection point between two 300-ohm series resistors connected between A(TIP) and B(RING).
7. Tested with 0 ohm source impedance. Two Mohm is specified for system design only.
8. Assumes the following Z_T network:



9. Group delay can be considerably reduced by using a ZT network such as that shown in Note 8 above. The network will reduce the group delay to less than 2 µs. The effect of group delay on linecard performance may be compensated for by using the SLAC or DSLAC device.

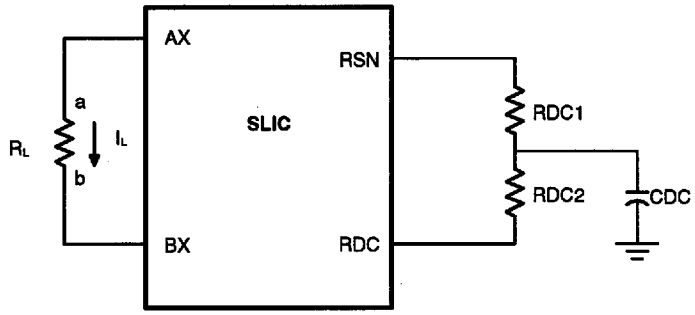
Table 2. User-Programmable Components

$Z_T = 200(Z_{2WIN} - 2R_F)$	Z_T is connected between the V_{TX} and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired two-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between V_{TX} and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G42L} \cdot \frac{200Z_T}{Z_T + 200(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to the RSN. Z_T is defined above, and G42L is the desired receive gain.
$R_{DC1} + R_{DC2} = 500/I_{LOOP}$ $C_{DC} = (1.5\ ms)(R_{DC1} + R_{DC2})/(R_{DC1}R_{DC2})$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant current region.
RD = 365/I_T, CD = 0.5 ms/RD	R_D and C_D form the network connected from R_D to –5 V, and I_T is the threshold current between on-hook and off-hook.
$C_{CAS} = \frac{1}{3.4 \cdot 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor, and fc is the desired filter cut-off frequency.
$R_{MG} \geq \frac{V_{BAT} - 6\ V}{I_{LOOP}}$	R_{MG} is connected from T_{MG} to V_{BAT} and is used to limit power dissipation within the SLIC.



In anti-sat region: $V_L = V_{BAT} - 5.7 - \frac{R_{DC}}{70} \cdot I_L$.

Figure 1a. Load Line (Typical)



Feed Current programmed by R_{DC1} and R_{DC2}.

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Figure 1b. Feed Programming

TEST CIRCUITS

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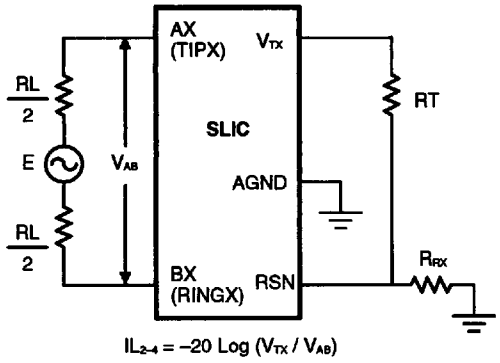
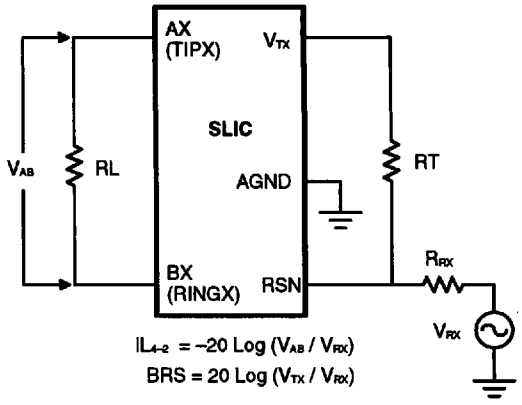


$IL_{2-4} = -20 \text{ Log } (V_{TX} / V_{AB})$

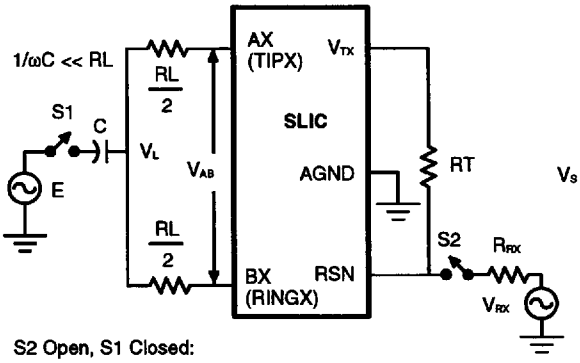
A. Two-to-Four Wire Insertion Loss



$IL_{4-2} = -20 \text{ Log } (V_{AB} / V_{RX})$

$BRS = 20 \text{ Log } (V_{TX} / V_{RX})$

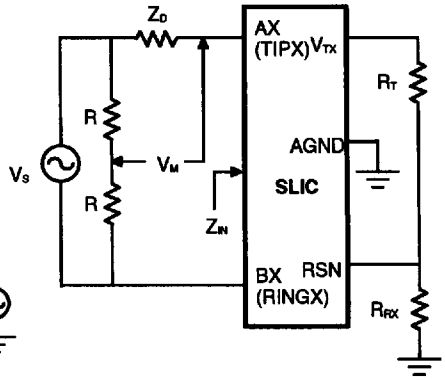
B. Four-to-Two Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed:
L-T Long. Bal. = 20 Log (V_{AB}/E)
L-T Long. Rej. = 20 Log (V_{TX}/E)

S2 Closed, S1 Open:
4-L Long. Sig. Gen. = 20 Log (V_L/V_{RX})

C. Longitudinal Balance (IEEE 455-1984)



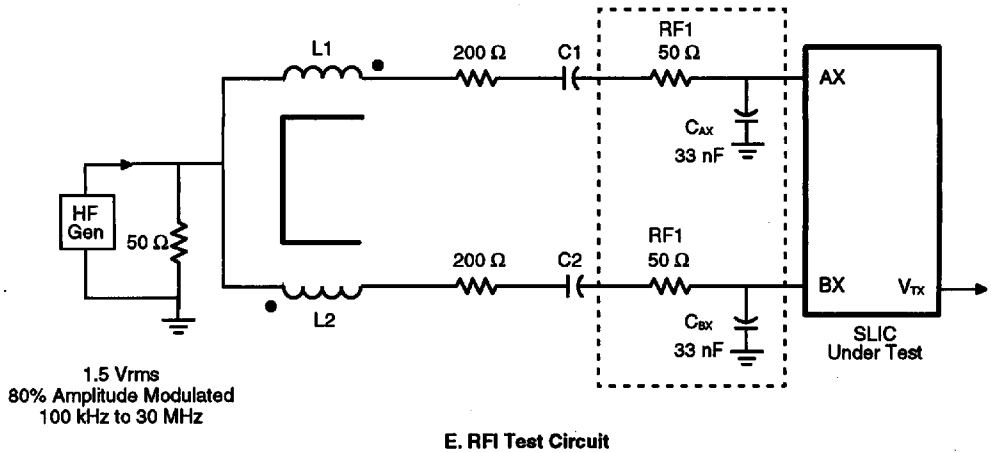
Z_D: The desired impedance (e.g., the characteristic impedance of the line).

Return Loss = $-20 \text{ Log } (2 V_M / V_S)$

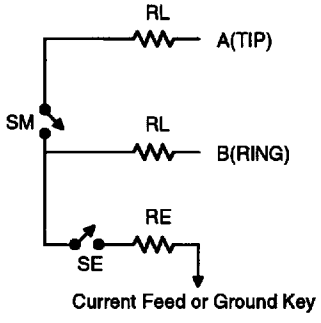
D. Two-Wire Return Loss Test Circuit

15474A-010

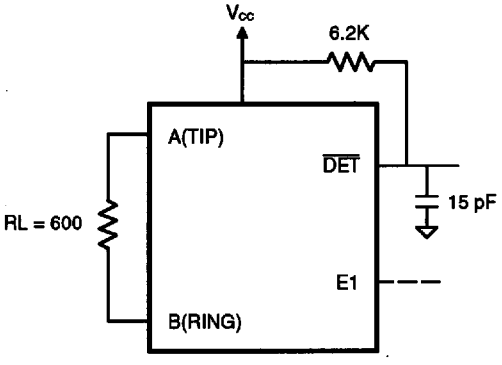
TEST CIRCUITS (continued)



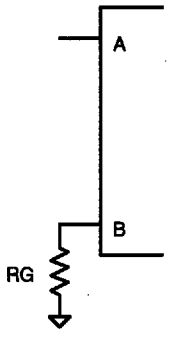
E. RFI Test Circuit



F. Ground-Key Detection Center Point Test



G. Loop Detector Switching



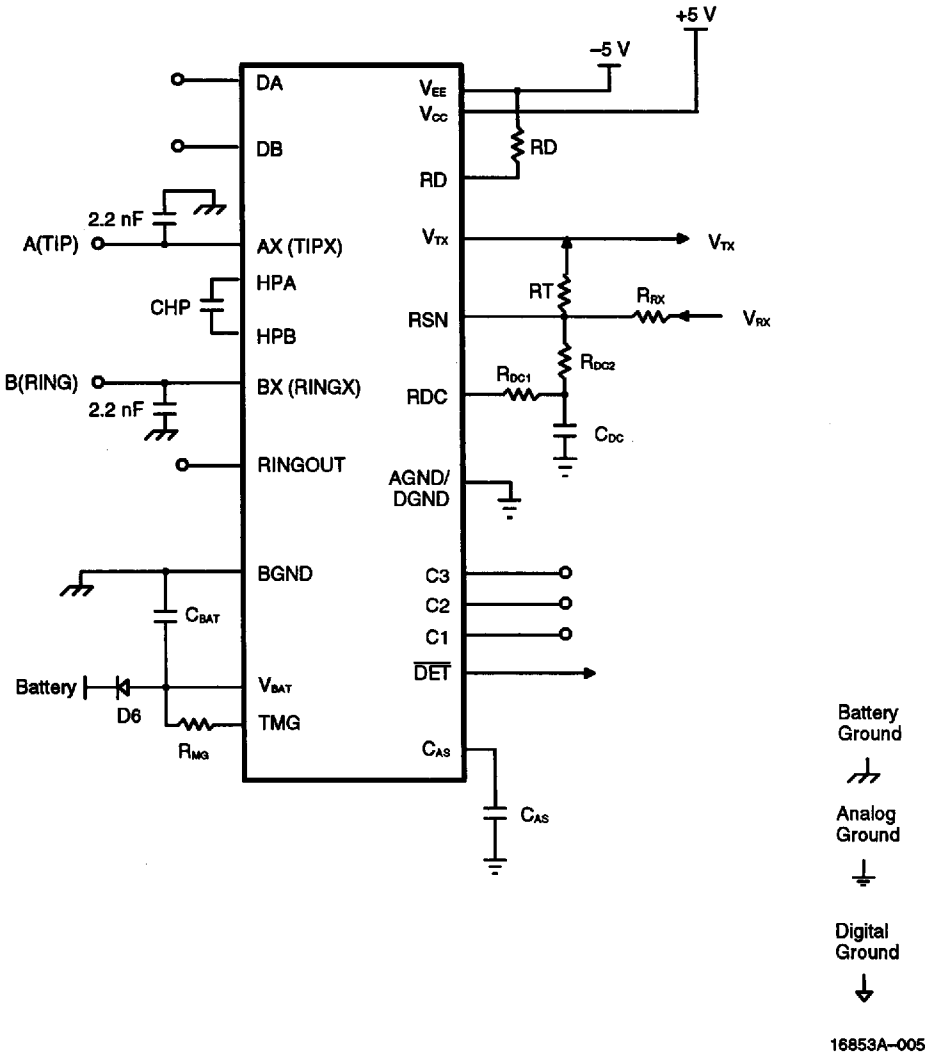
RG: 2K at V_{BAT} = –48 V

H. Ground-Key Switching

15474A-010

TEST CIRCUITS (continued)

ADV MICRO (TELECOM)



I. Am7943 Test Circuit

PBX SLICs

Application Notes

The AMD PBX SLIC Family offers a high degree of versatility for applications in many PBX, DLC, and other types of line circuits. In this section, typical single-channel and multiple-channel applications are described.

Figure 1 shows a detailed schematic of a single line of a basic system using one SLIC and one-half of an Am79C02 DSLAC IC.

In the receive path, the DSLAC IC processes digital PCM voice data into analog signals and inputs them to the SLIC RSN pin through resistor RRX. In the transmit path, the analog output at the SLIC V_{TX} pin is processed by the DSLAC IC and output in serial-digital format to the PCM interface. RRX sets the receive gain, and R_T is used to synthesize the AC two-wire output impedance. Both RT and RRX can be complex to achieve optimized parameters over the voice band.

In the control path, when the line goes off-hook, the SLIC pulls its collector $\overline{DET}$ output down and enables the DSLAC IC serial control data I/O pins, D_{IN} and D_{OUT} (see Figure 1). The microprocessor also recognizes the off-hook, and typically will send a response such as an active state or ring relay release command back to the SLIC, via the DSLAC IC D_{IN} pin and the C3–C1 data bus. The C4 line is also addressed in the same manner, to enable or disable the test relay driver. The E1 pin is addressed directly by the microprocessor as shown.

SLIC monitor and control functions which can be performed using a microprocessor and the circuitry shown in Figure 2 include:

- During the disable state, inform the processor when an off-hook has occurred and send a power-up command to the SLIC.
- Detect an off-hook during ringing and send a command to the SLIC to release the ring relay.
- Detect an on-hook condition during the active state and send a command to the SLIC to enter the disable state.
- Send a line polarity reverse command to the SLIC.
- Command the SLIC into the ground-key sense mode.
- Command the SLIC to energize the ring relay, K_R.
- Command the SLIC to energize the test relay, K_T.

For more detailed information on designing with the AMD SLIC Family, please refer to *The Subscriber Line Interface Circuit Family Application Note*, order #07030.

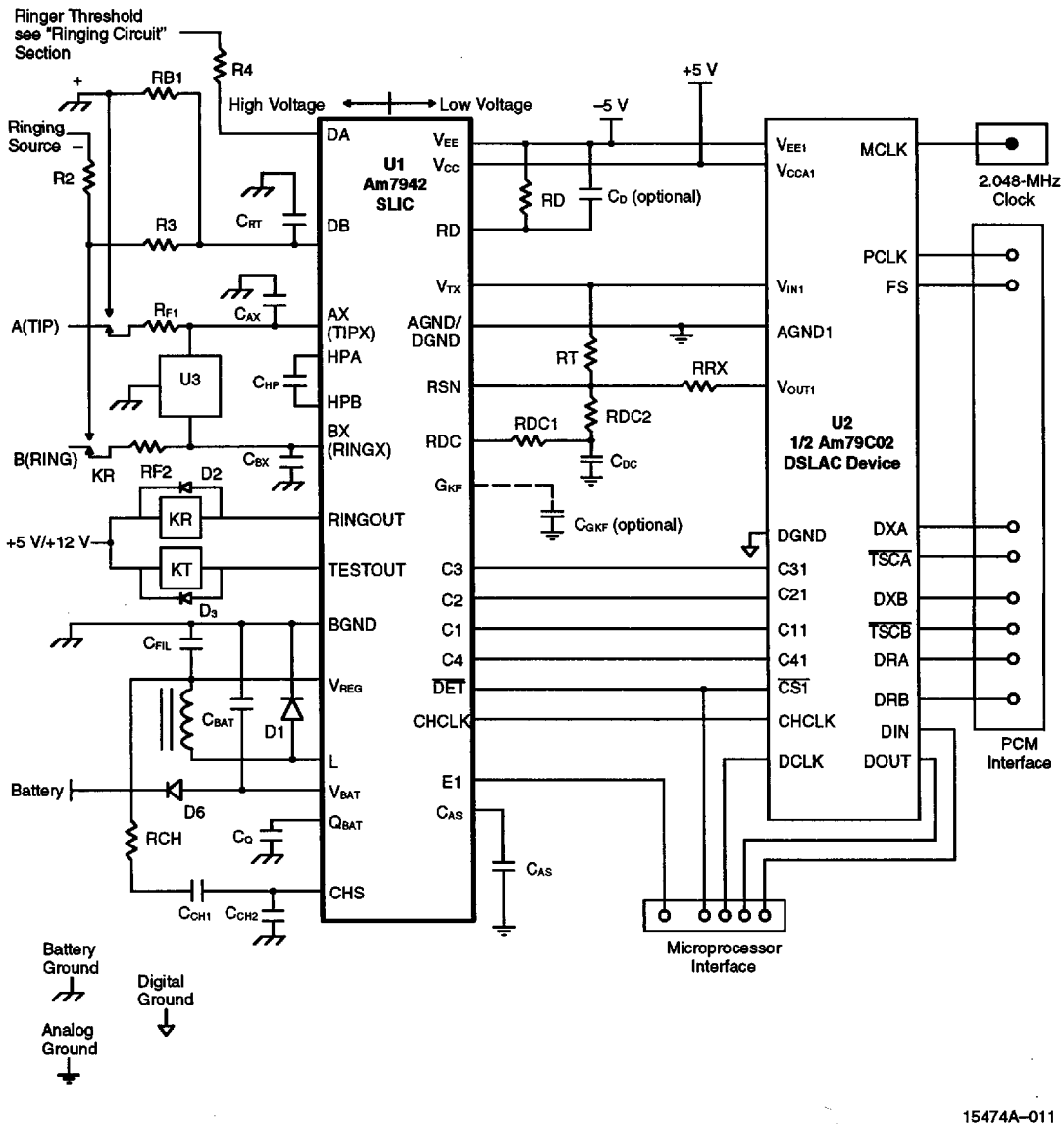
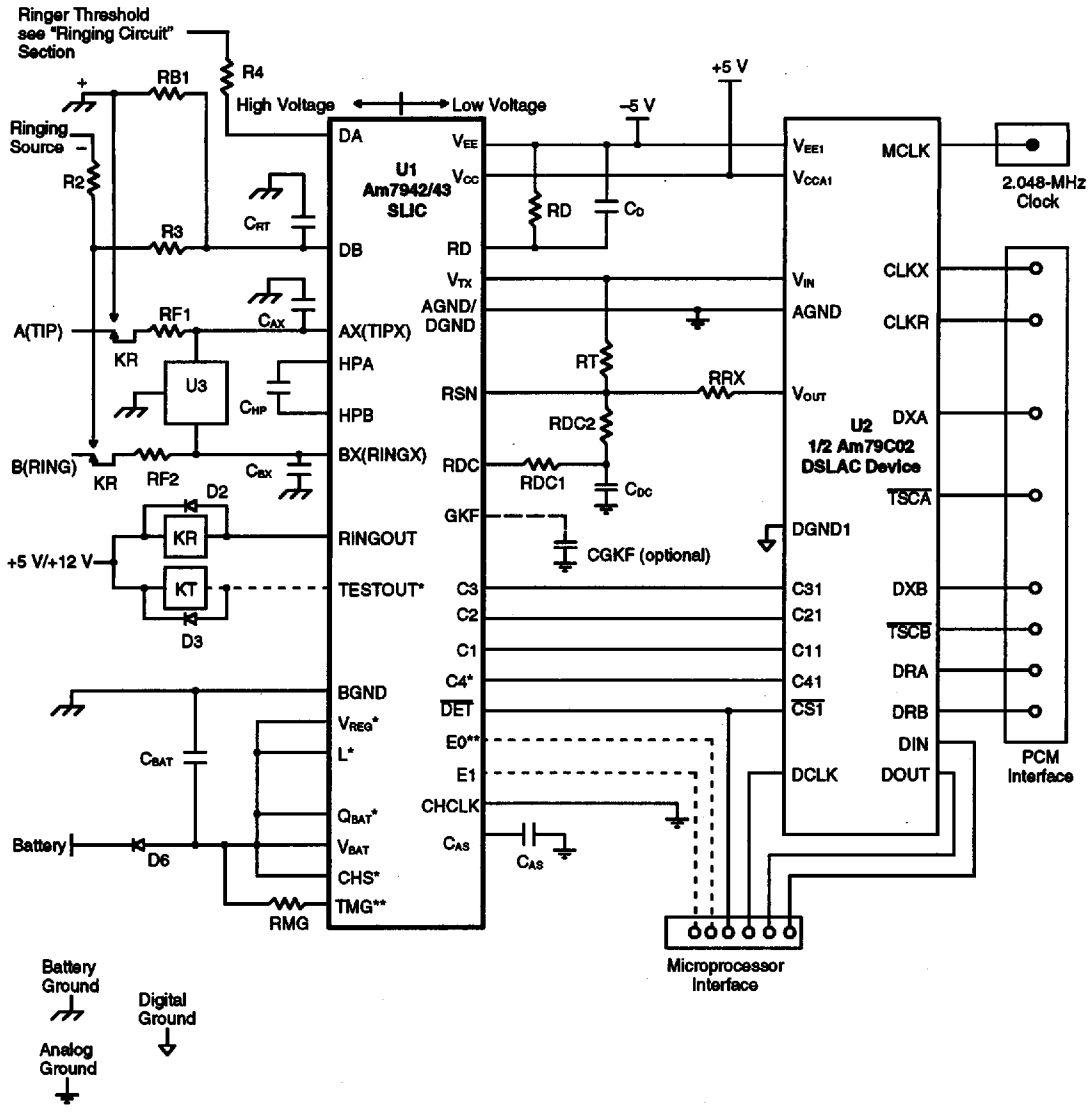


Figure 1. Single Channel of a Dual Channel Subscriber Line Circuit with Switcher Components



15474B-001

*Pin not available on the Am7943.
**Pin not available on the Am7942.

Figure 2. Single Channel of a Dual Channel Subscriber Line Circuit (24-V Battery, Without Switcher Components)

Table 1. Parts List — Single Channel Subscriber Line System

U1	Am7942 or Am7943 SLIC
U2	Am79C02 DSLAC device
K_R, K_T	Relay, 2-C contacts, 1500-V rating
L	Inductor, 1 mH, 5%**
D1	Diode, 100 V, 100 mA, 4 ns**
U3	Dual transient suppressor, Texas Instruments TISP108A or equivalent
D2, D3, D6	Diode 100 V, 100 mA, 10 ns
RF_1, RF_2	Resistor, fuse, 20 ohms to 50 ohms
R2	Resistor, 800 ohms, 3%, 3 W (Ring feed resistor)*
R_{B1}	Resistor, 1 Mohm, 1%, 1/4 W
R3	Resistor, 825K, 1%, 1/4 W
R4	Resistor, 452K, 1%, 1/4 W
R_{CH}	Resistor, 1.3K, 1%, 1/4 W**
RD	Resistor, 35.4K, 1%, 1/4 W (sets off-hook threshold)*
RT	Resistor, 100K, 1%, 1/4 W (sets two-wire impedance)*
R_{RX}	Resistor, 100K, 1%, 1/4 W (sets two-wire impedance)*
R_{DC1}, R_{DC2}	Resistor, 7.14K, 1%, 1/4 W (sets loop current)*
RMG	Resistor 1700 ohms, 5% 2 W (Am7943)
C_{RT1}	Capacitor, 0.1 µF, 20%, 100 V
C_{DC}	Capacitor 0.47 µF, 20%, 10 V
C_{HP}	Capacitor, 0.33 µF, 20%, 100 V
C_{AS}	Capacitor, 0.15 µF, 20%, 100 V
C_{AX}, C_{BX}	Capacitor, 2200 pF, 20%, 100 V
C_{FIL}	Capacitor, 0.47 µF, 10%, 100 V, metalized polyester**
C_{BAT}	Capacitor, 0.47 µF, 20%, 100 V
C_Q	Capacitor, 0.33 µF, 20%, 100 V**
C_{CH1}	Capacitor, 0.015 µF, 10%, 50 V, X7R ceramic**
C_{CH2}	Capacitor, 560 pF, 10%, 100 V, X7R ceramic**
C_D	Capacitor, 0.01 µF, 20%, 10 V (sets off-hook filtering)*
C_{GKF}	Capacitor, 3300 pF, 10%, X7R ceramic

Note: *The parts marked by an asterisk (*) are user-programmable. The values shown can be altered to suit the application.
**The parts marked by a double asterisk (**) are not needed for 24-V battery operation without a switcher.

PHYSICAL DIMENSIONS

Preliminary; package in development. BSC is an ANSI standard for Basic Space Centering. Dimensions are measured in inches or millimeters.

T-90-20

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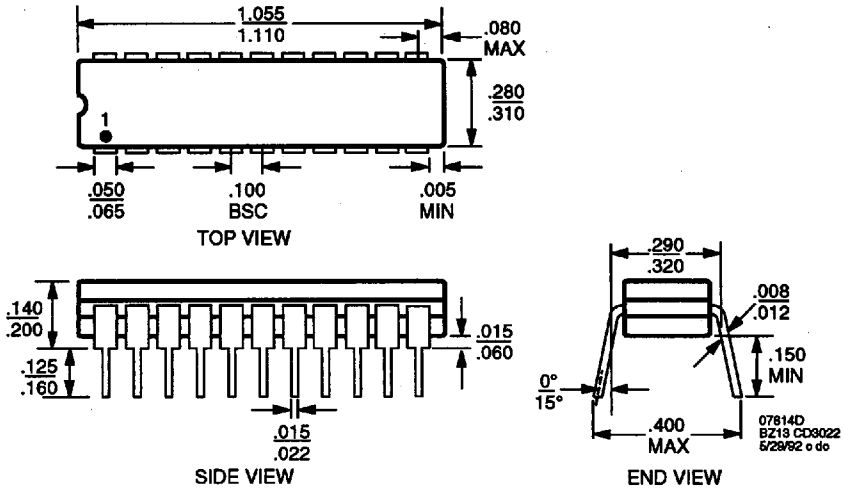

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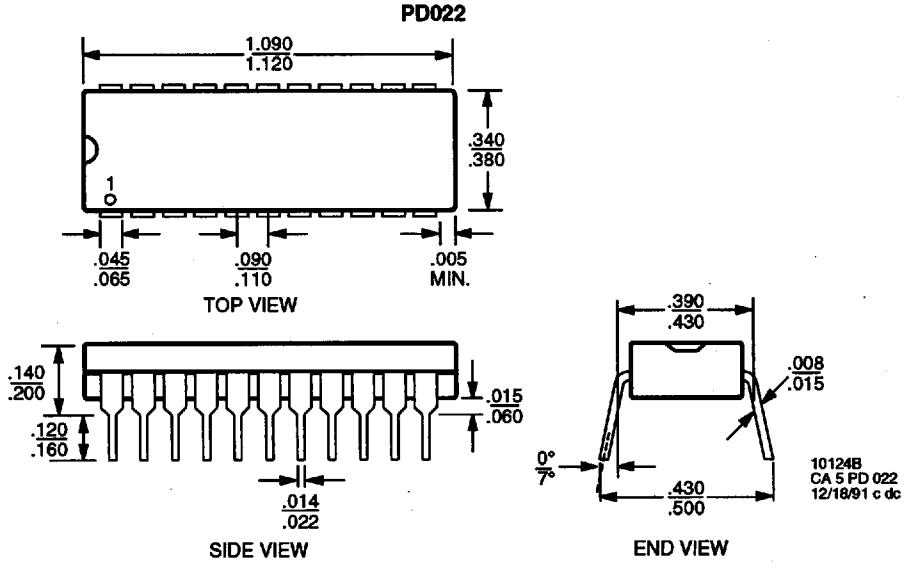

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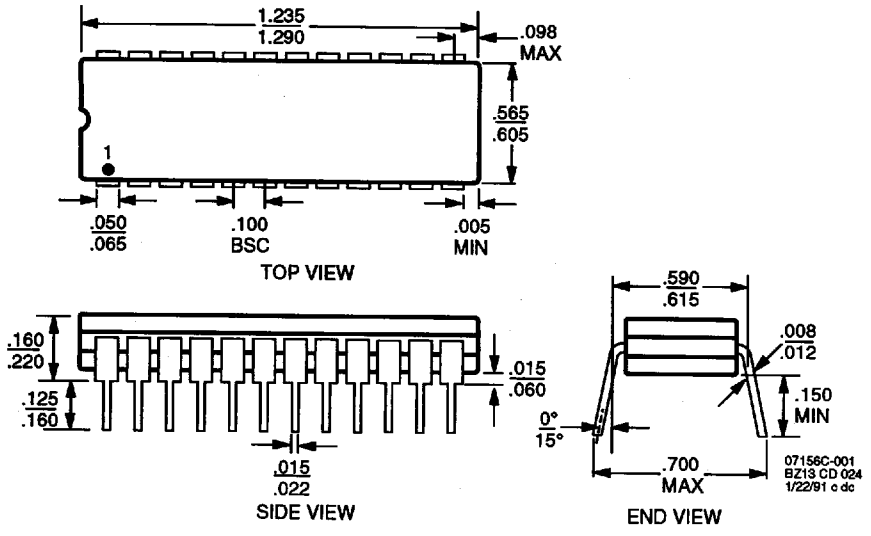
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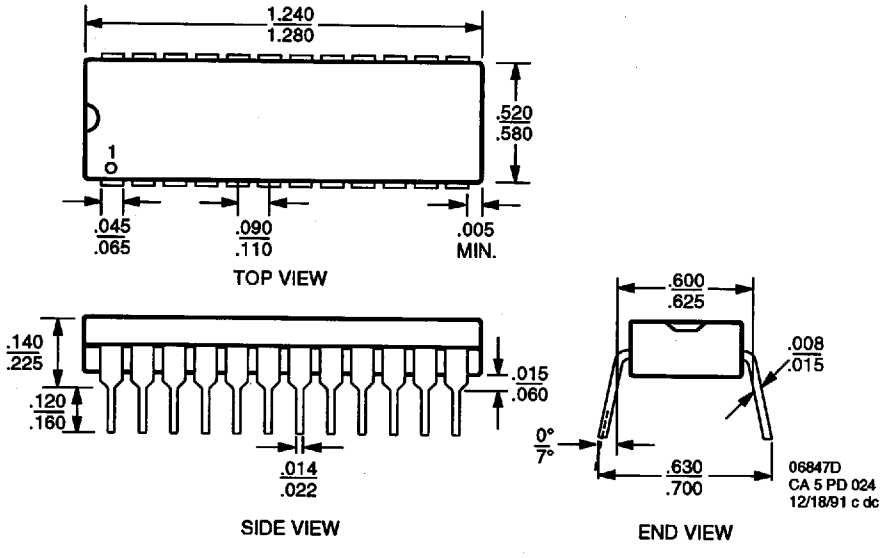
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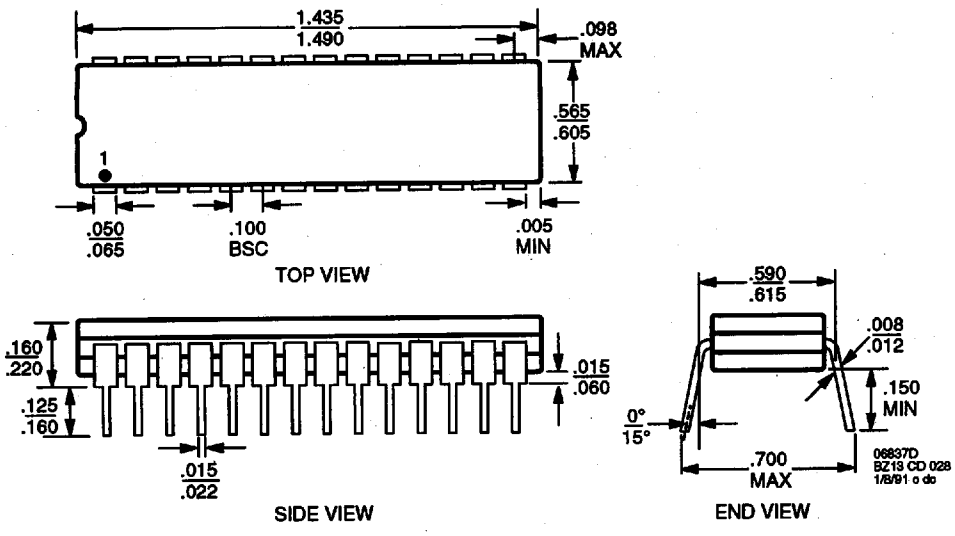
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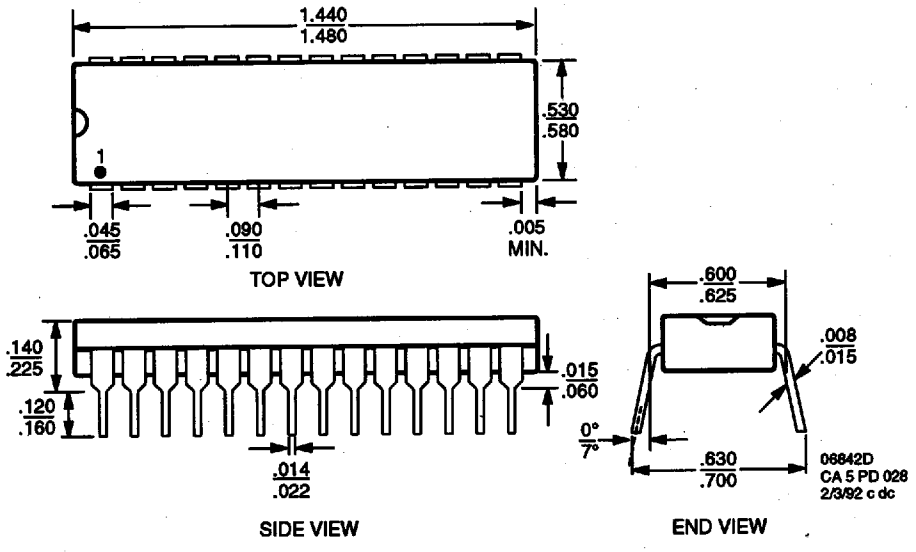
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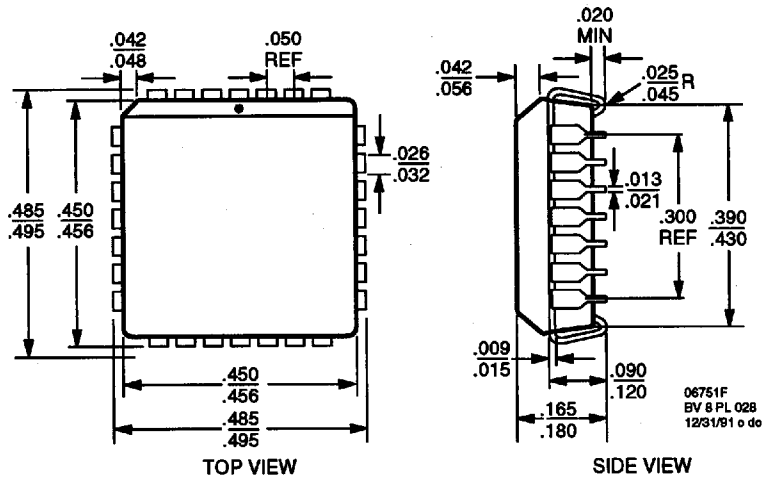
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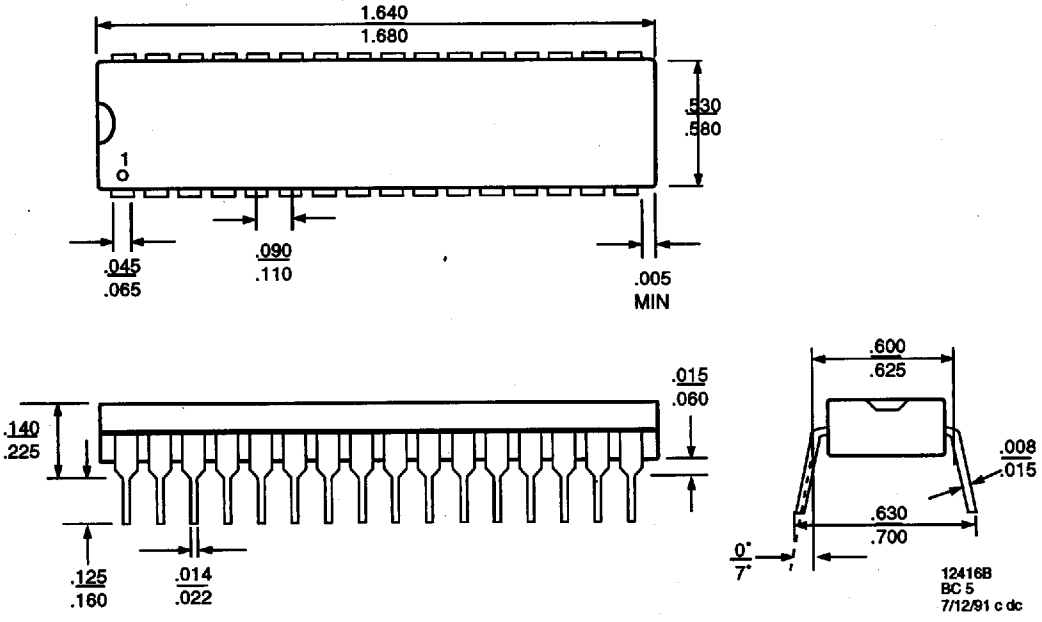
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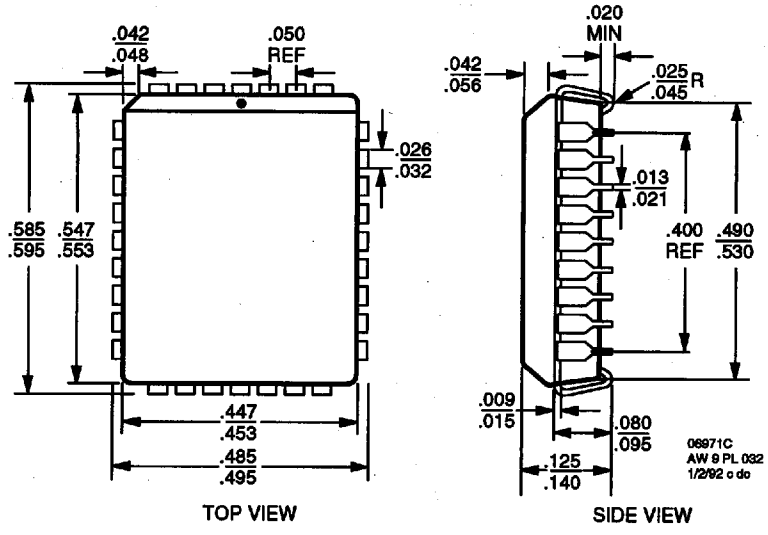
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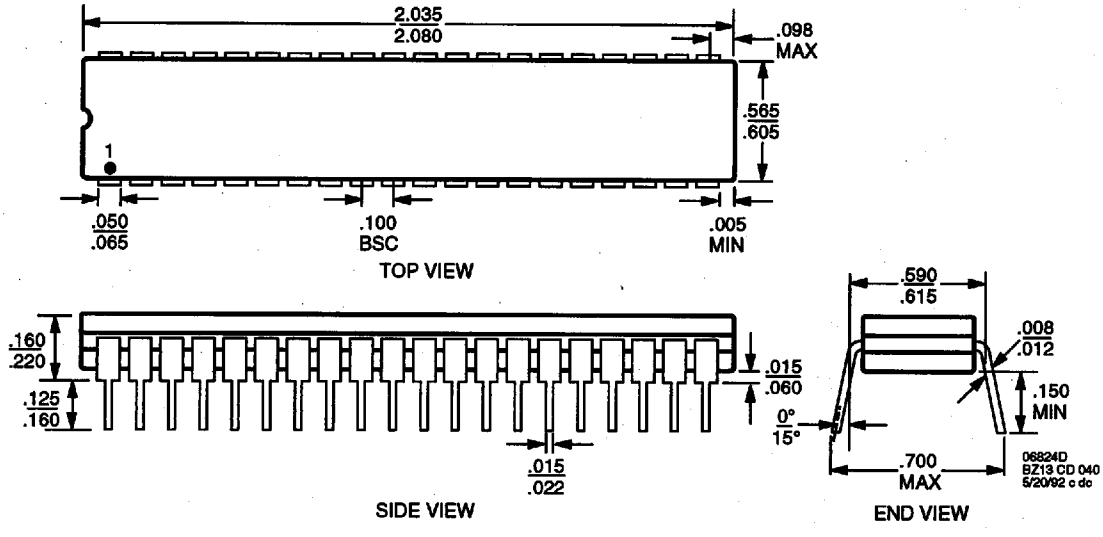
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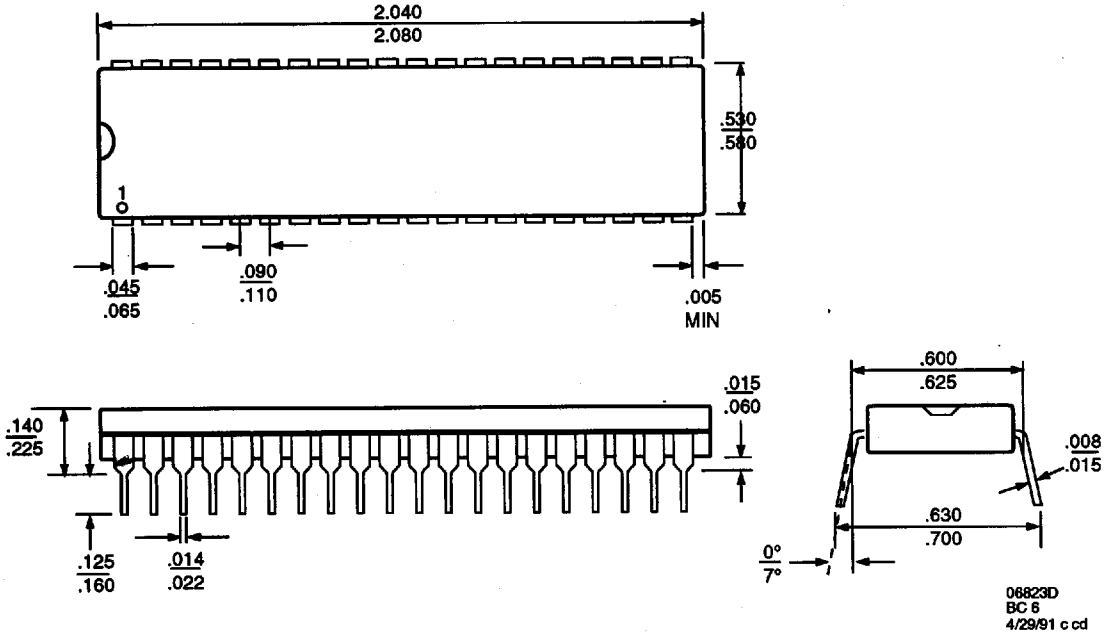

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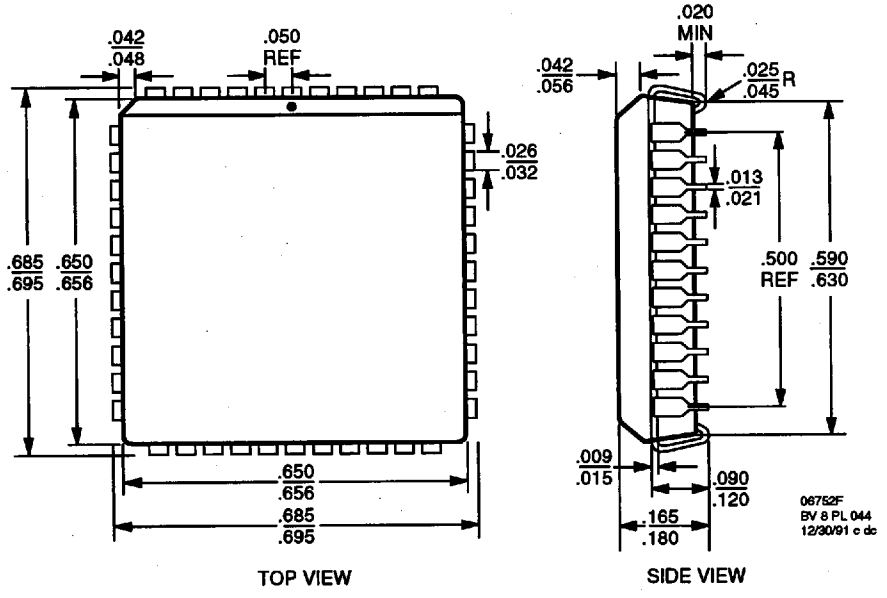

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