Quad, 16 Bit Dac with 10ppm/°C Max On-Chip Reference in 14-Lead TSSOP

Preliminary Technical Data

AD5666

FEATURES

Low Power Quad 16 Bit DAC
12-Bit Accuracy Guaranteed
14-Lead TSSOP Package
On-chip 1.25/2.5V, 10ppm/°C Reference
Power-Down to 200 nA @ 5V, 50 nA @ 3V
3V/5V Power Supply
Guaranteed Monotonic by Design
Power-On-Reset to Zero or Midscale
Three Power-Down Functions
Hardware /LDAC and /CLR functions
SDO Daisy-Chaining Option
Rail-to-Rail Operation
Temperature Range -40°C to +125°C

APPLICATIONS

ProcessControl
Data Acquisition Systems
Portable Battery Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators

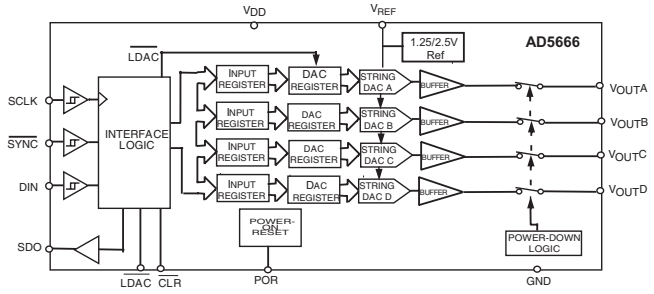

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD5666 DAC is a low power, quad, 16-bit buffered voltage-out DAC. The part operates from a single +2.7V to +5.5V, and is guaranteed monotonic by design.

The AD5666 has an on-chip reference with an internal gain of two. The AD5666-1 has a 1.25V 10ppm/°C max reference and the AD5666-2 has a 2.5V 10ppm/°C max reference. The on-board reference is off at power-up allowing the use of an external reference. The internal reference is turned on by writing to the DAC. The part incorporates a power-on-reset circuit that ensures that the DAC output powers up to zero volts (POR pin low) or midscale (POR pin high) and remains there until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 200nA at 5V and provides software selectable output loads while in power-down mode for any or all DACs channels.

The outputs of all DACs may be updated simultaneously using the /LDAC function, with the added functionality of selecting through software any number of DAC channels to synchronize. There is also an asynchronous active low /*CLR* that clears all DACs to a software selectable code - 0 V, midscale or fullscale .

The AD5666 utilizes a versatile three-wire serial interface that operates at clock rates up to 50 MHz and is compatible with standard SPI™, QSPI™, MICROWIRE™ and DSP interface standards. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved.

PRODUCT HIGHLIGHTS

1. Quad 16-Bit DAC; 12-Bit Accuracy Guaranteed.
2. On-chip 1.25/2.5V, 10ppm/°C max Reference.
3. Available in 14-lead TSSOP package.
4. Selectable Power-On-Reset to Zero volts or Midscale.
5. Power-down capability. When powered down, the DAC typically consumes 50nA at 3V and 200nA at 5V.

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REVISION HISTORY

Revision 0: Initial Version

AD5666–SPECIFICATIONS

(V_{DD} = +4.5 V to +5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; External VREF = Vdd; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Table 1.

	A Grade			B Grade				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**B Version [1],[2] Conditions/Comments**
STATIC PERFORMANCE[3,4]								
Resolution	16			16			Bits	
Relative Accuracy			±32			±16	LSB	See Figure 4
Differential Nonlinearity			±1			±1	LSB	Guaranteed Monotonic by Design. See Figure 5.
Load Regulation			2			2	LSB/mA	VDD=Vref=5V, Midscale Iout=0mA to 15mA sourcing/sinking
Zero Code Error		+1	+9		+1	+9	mV	All Zeroes Loaded to DAC Register. See Figure 8.
Zero Code Error Drift[3]		±20			±20		µV/°C	
Full-Scale Error	-0.15		-1.25	-0.15		-1.25	% of FSR	All Ones Loaded to DAC Register. See Figure 8.
Gain Error			±0.7			±0.7	% of FSR	
Gain Temperature Coefficient		±5			±5		ppm	of FSR/°C
Offset Error		±1	±9		±1	±9	mV	
Offset Temperature Coefficient		1.7			1.7		µV/°C	
DC Power Supply Rejection Ratio[6]		–80			–80		dB	V_{DD} ±10%
DC Crosstalk[6]		28			28		µV	R_L = 2 k. to GND or V_{DD}
		3.5			3.5		µV/mA	Due to Load current change
		-7.3			-7.3		µV	Due to Powering Down (per channel)
OUTPUT CHARACTERISTICS[6]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Capacitive Load Stability		470			470		pF	R_L=∞
		1000			1000		pF	R_L=2 kΩ
DC Output Impedance		1			1		Ω	
Short Circuit Current		50			50		mA	V_{DD}=+5V
Power-Up Time		10			10		µs	Mode. V_{DD}=+5V
REFERENCE INPUTS[3]								
Reference Input voltage		Vdd			Vdd		V	±1% for specified performance
Reference Current		20	30		20	30	µ A	V_{REF} = V_{DD} = +5.5V
Reference Input Range	0		V_{DD}	0		V_{DD}		

[1] Temperature ranges are as follows: B Version: -40°C to +125°C, typical at 25°C.
[2] Linearity calculated using a reduced code range of 485 to 64714. Output unloaded.
[3]DC specifications tested with the outputs unloaded unless stated otherwise.
[4]Linearity is tested using a reduced code range: AD5628 (Code 48 to Code 4047), AD5648 (Code / to Code /), and AD5668 (Code 485 to 64714).
[6]Guaranteed by design and characterization; not production tested.
[8]Interface inactive. All DACs active. DAC outputs unloaded.
[9]All eight DACs powered down.
Specifications subject to change without notice.

	A Grade			B Grade				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**B Version [1,2] Conditions/Comments**
Reference Input Impedance		14.6			14.6		kΩ	Per Dac Channel
REFERENCE OUTPUT								
Output Voltage	2.495	2.5	2.505	2.495	2.5	2.505	V	
Reference TC			±10			±10	ppm/°C	
Reference Output Impedance		2			2		kΩ	
LOGIC INPUTS[3]								
Input Current			±1			±1	µA	
V_{INL}, Input Low Voltage			0.8			0.8	V	V_{DD}=+5 V
V_{INH}, Input High Voltage	2			2			V	V_{DD}=+5 V
Pin Capacitance		3			3		pF	
LOGIC OUTPUTS (SDO)[3]								
Output Low Voltage, V_{OL}			0.4			0.4	V	I_{SINK} = 2 mA
Output High Voltage, V_{OH}	V_{DD} – 1			V_{DD} – 1				I_{SOURCE} = 2 mA
High Impedance Leakage Current			±1			±1	µA	
High Impedance Leakage Current		5			5		pF	
POWER REQUIREMENTS								
V_{DD}	4.5		5.5	4.5		5.5	V	All Digital Inputs at 0 or V_{DD} DAC Active and Excluding Load Current
I_{DD} (Normal Mode)[8]	0.5		4	0.5		4	mA	V_{IH}=V_{DD} and V_{IL}=GND
I_{DD} (All Power-Down Modes)[9]	0.2		1	0.2		1	µA	V_{IH}=V_{DD} and V_{IL}=GND
POWER EFFICIENCY								
I_{OUT}/I_{DD}		89			89		%	I_{LOAD}=2 mA, V_{DD}=+5 V

AC CHARACTERISTICS[1]

(V_{DD} = +4.5 V to +5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; External VREF = Vdd; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter[2]	Min	Typ	Max	Unit	B Version [1] Conditions/Comments
Output Voltage Settling Time					
AD5666		8	10	µs	¼ to ¾ scale settling to ±2LSB
Settling Time for 1LSB Step					
Slew Rate		1		V/µs	
Digital-to-Analog Glitch Impulse		10		nV-s	1 LSB Change Around Major Carry. See Figure 21.
Reference Feedthrough		100		dB	
SDO Feedthrough		4		nV-s	Daisy Chain Mode; SDO Load is 10pF
Digital Feedthrough		0.5		nV-s	
Digital Crosstalk		0.5		nV-s	
Analog Crosstalk		1		nV-s	
DAC-to-DAC Crosstalk		3		nV-s	
Multiplying Bandwidth		200		kHz	VREF = 2V ± 0.1 V p-p.
Total Harmonic Distortion		-80		dB	VREF = 2V ± 0.1 V p-p. Frequency = 10kHz
Output Noise Spectral Density		120		nV/√Hz	DAC code=8400_H, 1kHz
		100		nV/√Hz	DAC code=8400_H, 10kHz
Output Noise		15		µVp-p	0.1Hz to 10Hz;

NOTES
1Guaranteed by design and characterization; not production tested.
2See the Terminology section.
3Temperature range (Y Version): –40°C to +125°C; typical at +25°C.
Specifications subject to change without notice.

AD5666–SPECIFICATIONS

(V_{DD} = +2.7 V to +3.6 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; External VREF = Vdd; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Table Error! Main Document Only..

	A Grade			B Grade				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**B Version [1],[1] Conditions/Comments**
STATIC PERFORMANCE[3,4]								
Resolution	16			16			Bits	
Relative Accuracy			±32			±16	LSB	See Figure 4
Differential Nonlinearity			±1			±1	LSB	Guaranteed Monotonic by Design. See Figure 5.
Load Regulation			4			4	LSB/mA	VDD=Vref=3V, Midscale Iout=0mA to 7.5mA sourcing/sinking
Zero Code Error		+1	+9		+1	+9	mV	All Zeroes Loaded to DAC Register. See Figure 8.
Zero Code Error Drift[1]		±20			±20		µV/°C	
Full-Scale Error	-0.15		-1.25	-0.15		-1.25	% of FSR	All Ones Loaded to DAC Register. See Figure 8.
Gain Error			±0.7			±0.7	% of FSR	
Gain Temperature Coefficient		±5			±5		ppm	of FSR/°C
Offset Error		±1	±9		±1	±9	mV	
Offset Temperature Coefficient		1.7			1.7		µV/°C	
DC Power Supply Rejection Ratio[6]		–80			–80		dB	V_{DD} ±10%
DC Crosstalk[6]		28			28		µV	R_L = 2 k. to GND or V_{DD}
		3.5			3.5		µV/mA	Due to Load current change
		-7.3			-7.3		µV	Due to Powering Down (per channel)
OUTPUT CHARACTERISTICS[6]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Capacitive Load Stability		470			470		pF	R_L=∞
		1000			1000		pF	R_L=2 kΩ
DC Output Impedance		1			1		Ω	
Short Circuit Current		20			20		mA	V_{DD}=+3V Coming Out of Power-Down
Power-Up Time		10			10		ms	Mode. V_{DD}=+3V
REFERENCE INPUTS[3]								
Reference Input voltage		Vdd			Vdd		V	±1% for specified performance
Reference Current		35	45		35	45	µ A	V_{REF} = V_{DD} = +3.6V
Reference Input Range	0		V_{DD}	0		V_{DD}		
Reference Input Impedance		14.6			14.6		kΩ	Per Dac Channel
REFERENCE OUTPUT								
Output Voltage	1.248	1.25	1.252	1.248	1.25	1.252	V	
Reference TC			±10			±10	ppm/°C	

Reference Output Impedance		2			2	kΩ	
LOGIC INPUTS[3]							
Input Current			±1		±1	µA	
V_{INL}, Input Low Voltage			0.8		0.8	V	V_{DD}=+3 V
V_{INH}, Input High Voltage	2			2		V	V_{DD}=+3 V
Pin Capacitance		3			3	pF	
LOGIC OUTPUTS (SDO)[3]							
Output Low Voltage, V_{OL}			0.4		0.4	V	I_{SINK} = 2 mA
Output High Voltage, V_{OH}	V_{DD} – 0.5			V_{DD} – 0.5			I_{SOURCE} = 2 mA
High Impedance Leakage Current			±1		±1	µA	
High Impedance Leakage Current		5			5	pF	
POWER REQUIREMENTS							
V_{DD}	2.7		3.6	2.7	3.6	V	All Digital Inputs at 0 or V_{DD} DAC Active and Excluding Load Current
I_{DD} (Normal Mode)[8]	0.5		3	0.5	3	mA	V_{IH}=V_{DD} and V_{IL}=GND
I_{DD} (All Power-Down Modes)[9]	0.2		1	0.2	1	µA	V_{IH}=V_{DD} and V_{IL}=GND
V_{DD}=2.7 V to +3.6 V							
POWER EFFICIENCY							
I_{OUT}/I_{DD}		89			89	%	I_{LOAD}=2 mA, V_{DD}=+5 V

AC CHARACTERISTICS[1]

(V_{DD} = +2.7 V to +3.6 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; External VREF = Vdd; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter[2]	Min	Typ	Max	Unit	B Version [1] Conditions/Comments
Output Voltage Settling Time					
AD5666		8	10	µs	¼ to ¾ scale settling to ±2LSB
Settling Time for 1LSB Step					
Slew Rate		1		V/µs	
Digital-to-Analog Glitch Impulse		10		nV-s	1 LSB Change Around Major Carry. See Figure 21.
Reference Feedthrough		100		dB	
Digital Feedthrough		0.5		nV-s	
SDO Feedthrough		4		nV-s	Daisy Chain Mode; SDO Load is 10pF
Digital Crosstalk		0.5		nV-s	
Analog Crosstalk		1		nV-s	
DAC-to-DAC Crosstalk		3		nV-s	
Multiplying Bandwidth		200		kHz	VREF = 2V ± 0.1 V p-p.
Total Harmonic Distortion		-80		dB	VREF = 2V ± 0.1 V p-p. Frequency = 10kHz
Output Noise Spectral Density		120		nV/√Hz	DAC code=8400_H, 1kHz
		100		nV/√Hz	DAC code=8400_H, 10kHz
Output Noise		15		µVp-p	0.1Hz to 10Hz;

NOTES
1Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS[1,2,3]

(All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX}		Unit	Conditions/Comments
	V_{DD} = 2.7 V to 3.6 V	V_{DD}= 3.6 V to 5.5 V		
t_1 [1]	20	20	ns min	SCLK Cycle Time
t_2	11	9	ns min	SCLK High Time
t_3	9	9	ns min	SCLK Low Time
t_4	13	13	ns min	$\overline{SYNC}$ to SCLK Falling Edge Setup Time
t_5	4	4	ns min	Data Setup Time
t_6	4	4	ns min	Data Hold Time
t_7	0	0	ns min	SCLK Falling Edge to $\overline{SYNC}$ Rising Edge
t_8	25	20	ns min	Minimum $\overline{SYNC}$ High Time
t_9	13	13	ns min	$\overline{SYNC}$ Rising Edge to SCLK Fall Ignore
t_{10}	0	0	ns min	SCLK Falling Edge to $\overline{SYNC}$ Fall Ignore
t_{11}	20	20	ns min	*LDAC* Pulsewidth Low
t_{12}	20	20	ns min	SCLK Falling Edge to *LDAC* Rising Edge
t_{13}	20	20	ns min	/CLR Pulse Width Low
t_{14}	0	0	ns min	SCLK Falling Edge to *LDAC* Falling Edge
t_{15} [4,5]	20	20	ns max	SCLK Rising Edge to SDO Valid
t_{16} [5]	5	5	ns min	SCLK Falling Edge to *SYNC* Rising Edge
t_{17} [5]	8	8	ns min	*SYNC* Rising Edge to SCLK Rising Edge
t_{18} [5]	0	0	ns min	*SYNC* Rising Edge to *LDAC* Falling Edge

[2]See the Terminology section.
[3]Temperature range (Y Version): –40°C to +125°C; typical at +25°C.
Specifications subject to change without notice.

[1] [3]Maximum SCLK frequency is 50 MHz at V_{DD} = +3.6 V to +5.5 V and 20 MHz at V_{DD} = +2.7 V to +3.6 V.
[1]Guaranteed by design and characterization; not production tested.
[2]All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[3]See Figures 2 and 3.
[4]This is measured with the load circuit of Figure 1. t_{15} determines maximum SCLK frequency in Daisy-Chain mode.
[5]Daisy-chain mode only.
Specifications subject to change without notice.

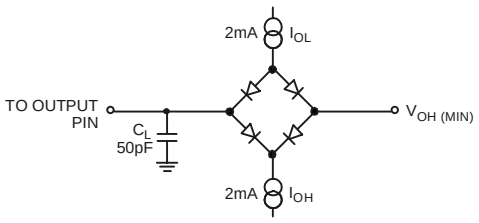

Figure 1. Load Circuit for Digital Output (SDO) T iming Specifications

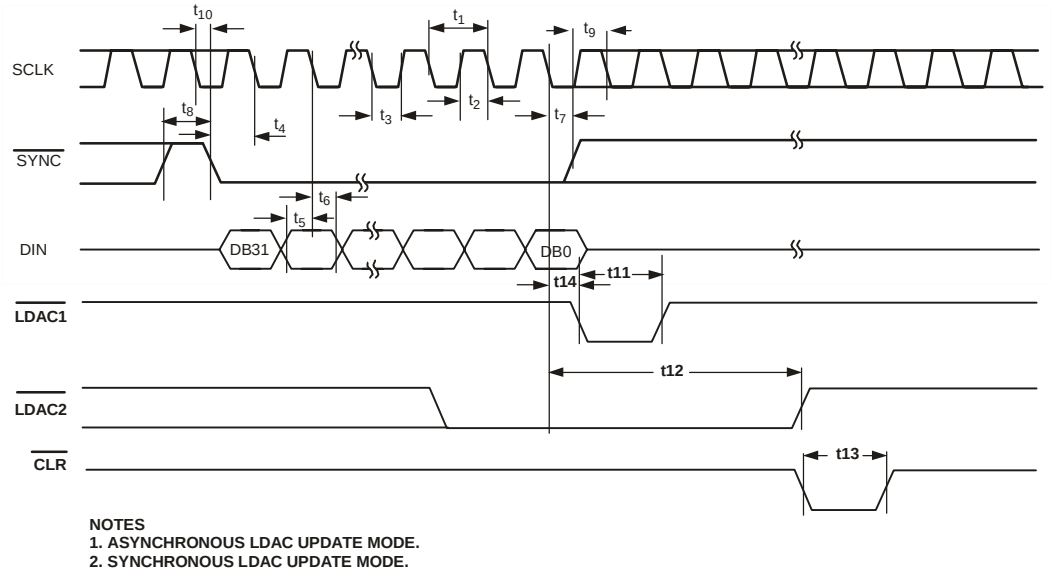

Figure 2. Serial Write Operation

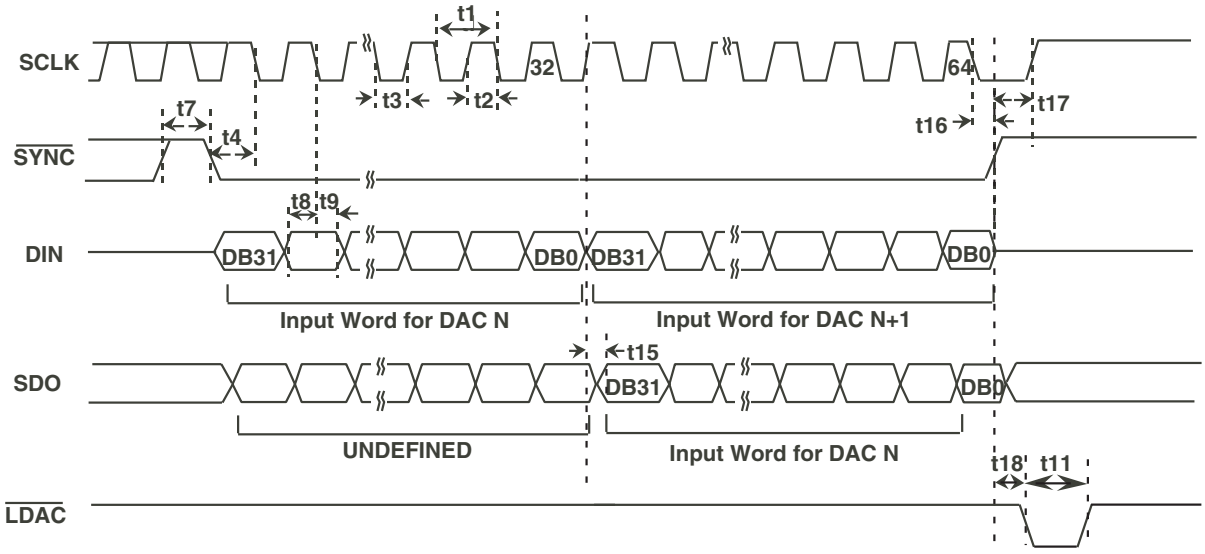

Figure 3. Daisy Chain Timing Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

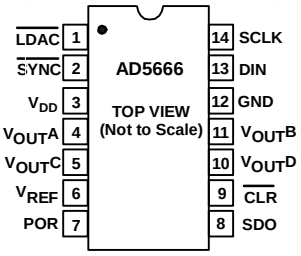

Figure 3. 14-Lead TSSOP (RU-14)

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	*/LDAC*	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows simultaneous update of all DAC outputs. Alternatively, this pin can be tied permanently low.
2	*/SYNC*	Active Low-Control Input. This is the frame synchronization signal for the input data. When *SYNC* goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the following 32 clocks. If *SYNC* is taken high before the 32nd falling edge, the rising edge of *SYNC* acts as an interrupt and the write sequence is ignored by the device.
3	VDD	Power Supply Input. These parts can be operated from 2.5 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	VOUTA	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
5	VOUTC	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
6	VREF	Reference Input/Output Pin
7	POR	Power-On–Reset pin. Tying this pin to GND powers on part to 0V. Tying to V_{DD} powers on part to midscale.
8	SDO	Serial Data Output. Can be used for daisy-chaining a number of these devices together or for reading back the data in the shift register for diagnostic purposes. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock.
9	/CLR	Active Low Control Input that Loads Software selectable code – Zero, midscale, fullscale - to All Input and DAC Registers. Therefore, the outputs also go to selected code. Default clears the output to 0V.
10	VOUTD	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
11	VOUTB	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
12	GND	Ground Reference Point for All Circuitry on the Part.
13	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz.

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(T_A = +25°C unless otherwise noted)

Parameter	Rating
V_{DD} to GND	-0.3 V to +7 V
Digital Input Voltage to GND	-0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	-0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature (T_J Max)	+150°C
TSSOP Package	
Power Dissipation	(T_J Max-T_A)/θ_{JA}
θ_{JA} Thermal Impedance	150.4°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

Relative Accuracy

For the DAC, relative accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 2.

Differential Nonlinearity

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 3.

Offset Error

Offset error is a measure of the difference between VOUT (actual) and VOUT (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5666 with Code ??? loaded into the DAC register.

This is a measure of the offset error of the DAC and the output amplifier (see Figures 2 and 3). It can be negative or positive, and is expressed in mV.

Zero-Code Error

Zero-code error is a measure of the output error when zero code (0000Hex) is loaded to the DAC register. Ideally the output should be 0 V. The zero-code error is always positive in the AD5660 because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mV. A plot of zero-code error vs. temperature can be seen in Figure 6.

Gain Error

This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

Zero-Code Error Drift

This is a measure of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Full-Scale Error

Full-scale error is a measure of the output error when full-scale code (FFFF Hex) is loaded to the DAC register. Ideally the output should be VDD – 1 LSB. Full-scale error is expressed in percent of full-scale range. A plot of full-scale error vs. temperature can be seen in Figure 6.

Total Unadjusted Error

Total Unadjusted Error (TUE) is a measure of the output error

taking the various offset and gain errors into account. A typical TUE vs. code plot can be seen in Figure 4**.**

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed by 1 LSB at the major carry transition (7FFF Hex to 8000 Hex). See Figure 19.

DC Power Supply Rejection Ratio (PSRR)

This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in VOUT to a change in VDD for full-scale output of the DAC. It is measured in dB. VREF is held at 2 V and VDD is varied ±10%.

DC Crosstalk

This is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in μV.

Reference Feedthrough

This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (i.e., *LDAC* is high). It is expressed in dB.

Major-Code Transition Glitch Energy

Major-code transition glitch energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device, but is measured when the DAC is not being written to (*SYNC* held high). It is specified in nV-s and is measured with a fullscale change on the digital input pins, i.e., from all 0s to all 1s and vice versa.

Digital Crosstalk

This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk

This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping *LDAC* high. Then pulse *LDAC* low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk

This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with *LDAC* low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion

This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in dB.

AD5666–TYPICAL PERFORMANCE CHARACTERISTICS

Figure 2. Typical INL Plot

Figure 4. Typical INL Plot

Figure 3. Typical DNL Plot

Figure 5. Typical DNL Plot

Figure 4. Typical Total Unadjusted Error Plot

Figure 6. Typical Total Unadjusted Error Plot

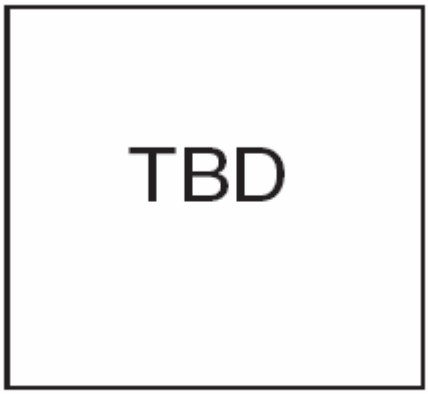

Figure 5. INL Error and DNL Error vs. Temperature

Figure 7. INL Error and DNL Error vs. Temperature

Figure 6. Zero-Scale Error and Full-Scale Error vs. Temperature

Figure 8. Zero-Scale Error and Full-Scale Error vs. Temperature

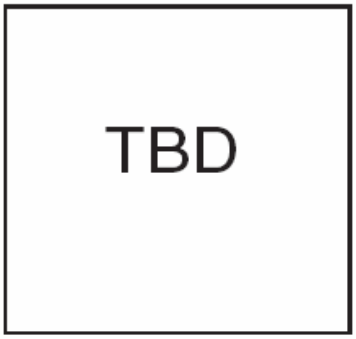

Figure 7. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

Figure 9. I_{DD} Histogram with V_{DD}=3V and V_{DD}=5V

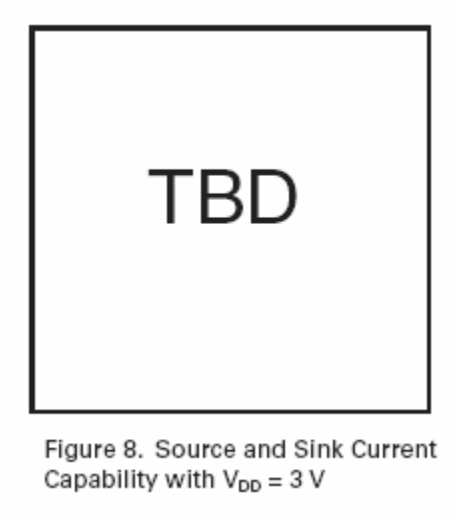

Figure 8. Source and Sink Current Capability with V_{DD} = 3 V

Figure 10. Source and Sink Current Capability with V_{DD}=3V

Figure 9. Source and Sink Current Capability with V_{DD} = 5 V

Figure 11. Source and Sink Current Capability with V_{DD}=5 V

Figure 10. Supply Current vs. Code

Figure 12. Supply Current vs. Code

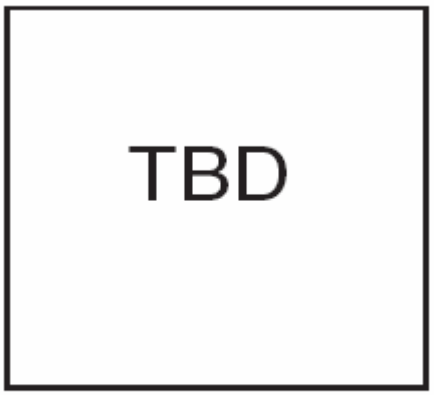

Figure 11. Supply Current vs. Temperature

Figure 13. Supply Current vs. Temperature

Figure 12. Supply Current vs. Supply Voltage

Figure 14. Supply Current vs. Supply Voltage

Figure 13. Power-Down Current vs. Supply Voltage

Figure 15. Power-Down Current vs. Supply Voltage

Figure 14. Supply Current vs. Logic Input Voltage

Figure 16. Supply Current vs. Logic Input Voltage

Figure 15. Full-Scale Settling Time

Figure 17. Full-Scale Settling Time

Figure 16. Half-Scale Settling Time

Figure 18. Half-Scale Settling Time

Figure 17. Power-On Reset to 0 V

Figure 19. Power-On Reset to 0V

Figure 18. Exiting Power-Down (800 Hex Loaded)

Figure 20. Exiting Power-Down (800 Hex Loaded)

Figure 19. Digital-to-Analog Glitch Impulse

Figure 21. Digital-to-Analog Glitch Impulse

GENERAL DESCRIPTION

D/A Section

The AD5666 DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. The parts include an internal 1.25/2.5V, 10ppm/°C reference with an internal gain of two. Figure 22 shows a block diagram of the DAC architecture.

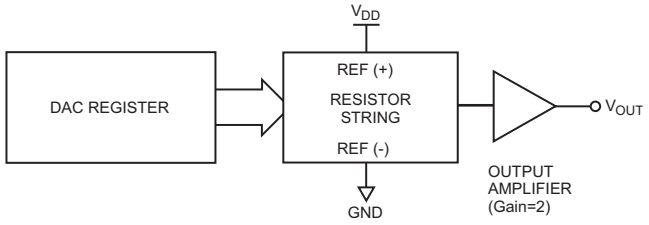

Figure 22. DAC Architecture

Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = Vref(ext) \times \left(\frac{D}{2\hat{}N} \right)$$

$$V_{OUT} = 2 * Vref(\text{int}) \times \left(\frac{D}{2\hat{}N} \right)$$

where *D* = decimal equivalent of the binary code that is loaded to the DAC register;
0 - 65535 for AD5666 (16 bit)

N = the DAC resolution

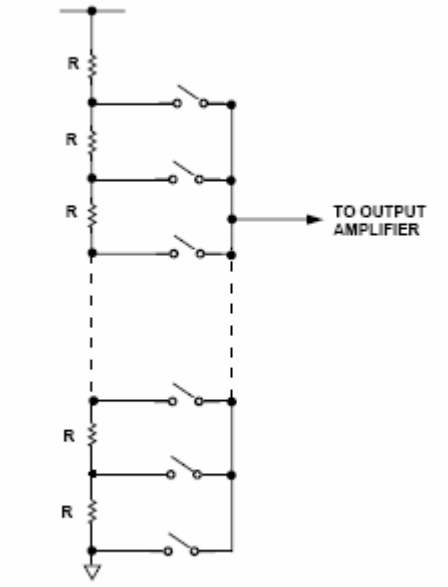

Figure 21. Resistor String

Figure 23. Resistor String

Resistor String

The resistor string section is shown in Figure 23. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output which gives an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 10 and Figure 11. The slew rate is 1 V/μs with a half-scale settling time of 8 μs with the output unloaded.

SERIAL INTERFACE

The AD5666 has a three-wire serial interface ($\overline{\text{SYNC}}$, SCLK and DIN), which is compatible with SPI, QSPI and MICROWIRE interface standards as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line is clocked into the 32-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the AD5666 compatible with high speed DSPs. On the 32nd falling clock edge, the last data bit is clocked in and the programmed function is executed (i.e., a change in DAC register contents and/or a change in the mode of operation). At this stage, the $\overline{\text{SYNC}}$ line may be kept low or be brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. Since the $\overline{\text{SYNC}}$ buffer draws more current when V_{IN} = 2V than it does when V_{IN} = 0.8 V, $\overline{\text{SYNC}}$ should be idled low between write sequences for even lower power operation of the part. As is mentioned above, however, it must be brought high again just before the next write sequence.

Input Shift Register

The input shift register is 32 bits wide (see Figure 24). The first five bits are "don't cares." The next three bits are the Command bits C2-C0, (see Table 1) followed by the 4-bit DAC address A3-A0, (see Table 2) and finally the 16-bit data word. The data word comprises the 16- bit input code followed by 4 don't care bits for the AD5666. See figure 24. These data bits are transferred to the DAC register on the 32nd falling edge of

SCLK.

Daisy-Chaining

For systems that contain several DACs, or where the user wishes to read back the DAC contents for diagnostic purposes, the SDO pin may be used to daisy-chain several devices together and provide serial readback.

The the daisy chain mode is enabled through a software executable DCEN Setup function, Command 1000 is reserved for this DCEN Setup function, see Table 3. The daisy chain mode is software-programmable by setting a bit (DB1) in the DCEN Setup register. The default setting is stand-alone mode where bit DCEN =0. Table 4 shows how the state of the bits corresponds to the mode of operation of the device. input shift register when *SYNC* is low. If more than 32 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the DIN input on the next DAC in the chain, a multi-DAC interface is constructed. Thirty-two clock pulses are required for each DAC in the system. Therefore, the total number of clock cycles must equal 32N, where N is the total number of devices
in the chain. When the serial transfer to all devices is complete, *SYNC* should be taken high. This prevents any further data from being clocked into the input shift register.

A continuous SCLK source may be used if it can be arranged that *SYNC* is held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles may be used and *SYNC* may be taken high some time later.

When the transfer to all input registers is complete, a common *LDAC* signal updates all DAC registers and all analog outputs are updated simultaneously.

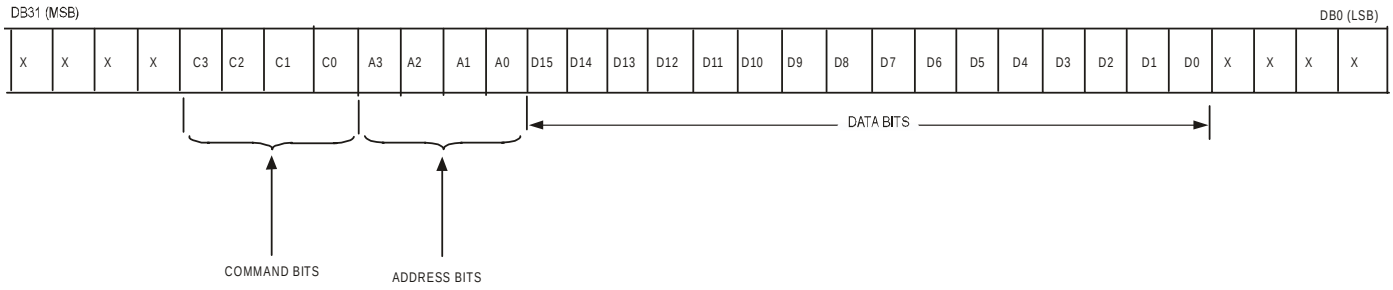

Figure 24a AD5666. Input Register Contents

Command				
C3	**C2**	**C1**	**C0**	
0	0	0	0	Write to Input Register n
0	0	0	1	Update DAC Register n
0	0	1	0	Write to Input Register n, Update All
0	0	1	1	Write to and Update DAC channel n
0	1	0	0	Power Down DAC (Power-up)
0	1	0	1	Load Clear Code Register
0	1	1	0	Load LDAC Register

				(LDAC overwrite)
0	1	1	1	Reset (Power-on-Reset)
1	0	0	0	DCEN/REF Setup Register
1	0	0	1	Reserved
*	*	*	*	Reserved
1	1	1	1	Reserved

Table 1. Command Definition

ADDRESS (n)				
A3	**A2**	**A1**	**A0**	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
1	1	1	1	All DACs

Table2. Address Command

$\overline{\text{SYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 32 falling edges of SCLK and the DAC is updated on the 32nd falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 32nd falling edge this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents or a change in the operating mode occurs—see Figure 25.

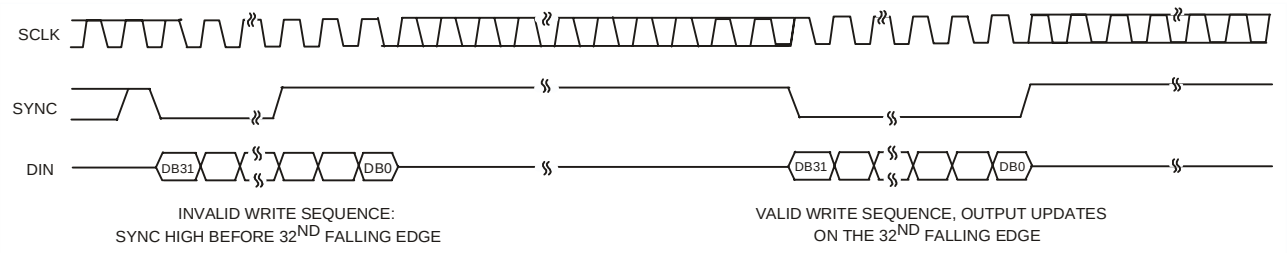

Figure 25. SYNC Interrupt Facility

Reference Setup –External to Internal

The on-board reference is turned off at power-up by default, allowing the use of an external reference. The AD5666 has an on-chip reference with an internal gain of two. The AD5666-1 has a 1.25V 10ppm/°C max reference and the AD5666-2 has a 2.5V 10ppm/°C max reference. The on-board reference can be turned on/off through a software executable REF Setup function, Command 1000 is reserved for this REF Setup function, see Table 3. The reference mode is software-programmable by setting a bit (DB0) in the REF

Setup register. Table 4 shows how the state of the bits corresponds to the mode of operation of the device.

DCEN/REF Setup Register		
DCEN (DB1)	**REF (DB0)**	**Action**
0	0	Stand-Alone Mode – Ref Off
0	1	Stand-Alone Mode – Ref On
1	0	DCEN Mode – Ref Off
1	1	DCEN Mode – Ref On

Table 3. Daisy Chain Enable /Reference Set-up Register

MSB											**LSB**
DB31 – DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB2-DB19**	**DB1**	**DB0**
x	1	0	0	0	x	x	x	x	x	1/0	1/0
Don't Cares	*COMMAND BITS (C3-C0)*				*ADDRESS BITS (A3 – A0)*				Don't Cares	DCEN/REF Setup Register	

Table 4. 32-Bit Input Shift Register Contents for Daisy Chain Enable and Reference Setup Function

Power-On-Reset

The AD5666 family contains a power-on-reset circuit that controls the output voltage during power-up. By connecting the POR pin low the DAC output powers up to zero volts and by connecting the POR pin high the DAC output powers up to midscale. The output remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.
There is also a software executable Reset function that will reset the DAC to the Power-on -Reset code. Command 111 is reserved for this Reset function, see Table 1.

Power-Down Modes

The AD5666 contains four separate modes of operation. Command 100 is reserved for the Power-Down function. See Table 1. These modes are software-programmable by setting two bits (DB19 and DB18) in the control register. Table 3 shows how the state of the bits corresponds to the mode of operation of the device. Any or all DACs, (DacD to DacA) may be powered down to the selected mode by setting the corresponding 4 bits (DB7,6,1,0) to a "1". See Table 6 for contents of the Input Shift Register during power down/up operation.

When both bits are set to 0, the part works normally with its normal power consumption of 250 μA at 5 V. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output

impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor or it is left open-circuited (Three-State). The output stage is illustrated in figure 24.

The bias generator, the output amplifier, the resistor string and other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically (2.5 µs for V_{DD} = 5 V and 5 µs for V_{DD} = 3 V)???. See Figure 20 for a plot.
Any combination of DACs can be powered up by setting PD1 and PD0 to "0" (normal operation). Output powers-up to value in input register (/LDAC Low) or to value in DAC register before Power-Down (/LDAC High).

DB9	DB8	Operating Mode
0	0	Normal Operation Power Down Modes
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three State

Table 3. Modes of Operation for the AD5666

MSB															LSB
DB31 – DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB10— DB19	DB9	DB8	DB4- DB7	DB3	DB2	DB1	DB0
x	0	1	0	0	x	x	x	x	x	PD1	PD0	*X*	DacD	DacC	DacB	DacA
Don't Cares	*COMMAND BITS (C2-C0)*				*ADDRESS BITS (A3 – A0)* *Don't cares*				*Don't Cares*	*Power Down Mode*		*Don't Cares*	*Power Down/Up Channel Selection – Set Bit to a "1" to select*			

Table 6. 32-Bit Input Shift Register Contents of Power Up/Down Function

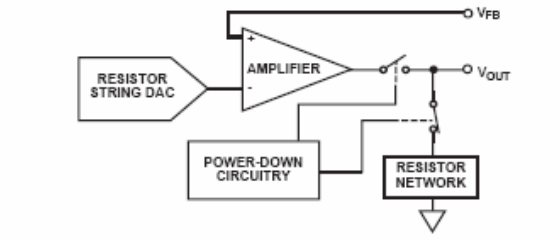

Figure 24. Output Stage During Power-Down

Clear Code Register

The AD5666 gives the option of clearing any one or all DAC channels to 0, midscale or fullscale code. Command 101 is reserved for the Clear Code function. See Table1. These clear code values are software-programmable by setting two bits (DB1 and DB0) in the control register. Table shows how the state of the bits corresponds to the clear code values of the device. Upon execution of the hardware /CLR pin (active LOW), the DAC output is cleared to the clear code register value (default setting is zero). See Table 7 for contents of the

Input Shift Register during the Clear Code Register operation

Clear Code Register		
CR1	**CR0**	**Clears to code**
0	0	0000h
0	1	8000h
1	0	FFFFh
1	1	No operation

Table 6. Clear Code Register

MSB											**LSB**
DB31 – DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB2-DB19**	**DB1**	**DB0**
x	0	1	0	1	1/0	1/0	1/0	1/0	x	1/0	1/0
Don't Cares	*COMMAND BITS (C2-C0)*				*ADDRESS BITS (A3 – A0)*				Don't Cares	Clear Code Register (CR1-CR0)	

Table 7. 32-Bit Input Shift Register Contents Clear Code Function

LDAC Function

The outputs of all DACs may be updated simultaneously using the hardware /LDAC pin.
Synchronous LDAC: The DAC registers are updated after new data is read in on the falling edge of the 32nd SCLK pulse. *LDAC* can be permanently low or pulsed as in Figure 1.
Asynchronous LDAC: The outputs are not updated at the same time that the input registers are written to. When *LDAC* goes low, the DAC registers are updated with the contents of the input register.

The outputs of all DACs may be updated simultaneously using the /LDAC function, with the added functionality of selecting through software any number of DAC channels to synchronize.
Writing to the DAC using command 110, the hardware /LDAC pin can be overwritten by setting the bits of the 4-bit /LDAC register (DB7,DB6, DB1,DB0) . SeeTable 5 for the /LDAC mode of operation. The default for each channel is "0" ie /LDAC pin works normally. Setting the bits to a "1" means the DAC channel will be updated regardless of the state of the /LDAC pin. This gives the added benefit of allowing any combination of channels to be synchronously updated. See Table 8 for contents of the Input Shift Register during the /LDAC overwrite mode of operation.

Load DAC OVERWRITE		
/LDACBITS (DB7-DB0)	**/LDAC PIN**	**/LDAC Operation**
0	1/0	Determined by /LDAC pin
1	x – Don't Care	DAC channels will update, overwriting the /LDAC pin

Table 5. LDAC Overwrite Definition

MSB													LSB
DB31 – DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB4 –DB19**	**DB3**	**DB2**	**DB1**	**DB0**
x	0	1	1	0	x	x	x	x	x	DacD	DacC	DacB	DacA
Don't Cares	*COMMAND BITS (C2-C0)*				*ADDRESS BITS (A3 – A0)* *Don't cares*				*Don't Cares*	Setting /LDAC bit to "1" overwrites /LDAC pin			

Table 8. 32-Bit Input Shift Register Contents for /LDAC Overwrite Function

Power Supply Bypassing and Grounding

When accuracy is important in a circuit it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5666 should have separate analog and digital sections, each having its own area of the board. If the AD5666 is in a system where other devices require an AGND to DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5666.

The power supply to the AD5666 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be physically as close as possible to the device with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), e.g., common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a two-layer board.

OUTLINE DIMENSIONS

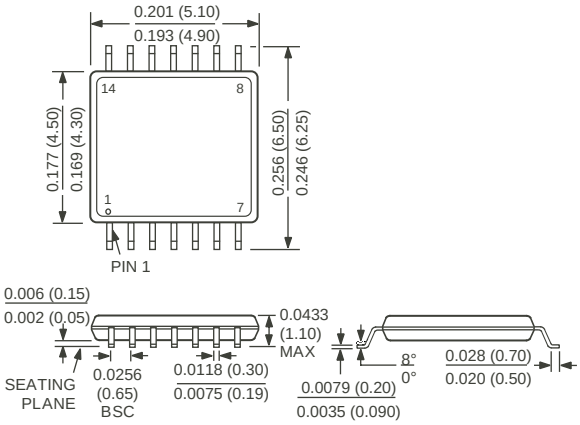

Figure 26. 14-Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Bit	Internal Reference	Package Option1
AD5666BRUZ-1	16	1.25V	RU-14
AD5666BRUZ-2	16	2.5V	RU-14
AD5666ARUZ-2	16	2.5V	RU-14

1 Thin Shrink Small Outline Package (TSSOP)

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