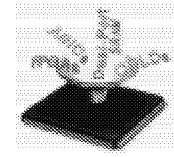
Integrator Series FPGAs: 40MX and 42MX Families (Single-Chip ASIC Alternative)



Features

High Capacity

- 2,000 to 36,000 Available Logic Gates
- Up to 2.5 Kbits Configurable Dual-Port SRAM
- Fast Wide-Decode Circuitry
- Up to 202 User-Programmable I/O Pins

High Performance

- 5.6 ns Clock-to-Out
- 250 MHz Performance
- 5 ns Dual-Port SRAM Access
- 100 MHz FIFOs
- 7.5 ns 35-Bit Address Decode

Ease of Integration

- Mixed Voltage Operation (5.0V or 3.3V I/O).
- Synthesis-Friendly Architecture to Support ASIC Design Methodologies.
- 95–100% Resource Utilization, Using Automatic Place and Route Tools with up to 100% Pin Fixing.
- Deterministic, User-Controllable Timing Via DirectTime Software Tools.
- MX Diagnostics and Debug Supported by Silicon Explorer.
- Supported by Actel Designer Series Development System with Interfaces to Popular Design Environments including Cadence, Exemplar, IST, Mentor Graphics, Synopsys, Synplicity, and Viewlogic.
- Low Power Consumption (500µA less than I_{CC} Stand-By in Stand-By Mode).
- IEEE Standard 1149.1 (JTAG) Boundary Scan Testing
- 5.0V and 3.3V Programmable PCI-Compliant I/O.

General Description

The newest additions to Actel's Integrator Series of programmable logic devices, the 40MX and 42MX families, provide system logic designers with a high performance, cost-effective ASIC alternative in a single FPGA.

Integrator Series Product Profile

Device	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
Capacity						
Gates	2,000	4,000	9,000	16,000	24,000	36,000
ASIC-Equivalent Gates	1,200	2,000	4,000	8,000	14,000	20,000
SRAM Bits	N/A	N/A	N/A	N/A	N/A	2,560
Logic Modules						
Sequential	—	—	348	624	954	1,230
Combinatorial	295	547	336	608	912	1,184
Decode	—	—	N/A	N/A	24	24
Clock-to-Out	9.5 ns	9.5 ns	5.6 ns	6.1 ns	6.1 ns	6.3 ns
SRAM Modules (64x4 or 32x8)	N/A	N/A	N/A	N/A	N/A	10
Dedicated Flip-Flops	—	—	348	624	954	1,230
Maximum Flip-Flops	147	273	516	928	1,410	1,822
Clocks	1	1	2	2	2	6
User I/O (Maximum)	57	69	104	140	176	202
JTAG	No	No	No	No	Yes	Yes
Packages	PL44 PL68 PQ100 VQ80	PL44 PL68 PL84 PQ100 VQ80	PL84 PQ100 PQ160 TQ176 VQ100	PL84 PQ100 PQ160 PQ208 TQ176 VQ100	PL84 PQ160 PQ208 TQ176	PQ208 PQ240 BG272

The MX device architecture is based on Actel's patented antifuse technology implemented in a 0.45µ triple-metal CMOS process. With capacities ranging from 2,000 to 36,000 gates, the synthesis-friendly MX devices provide datapaths up to 250 MHz, are live on power-up, and deliver up to five times lower stand-by power consumption than any other FPGA device. Actel's MX FPGAs provide up to 250 I/Os, and are available in a wide variety of packages and speed grades.

Actel's 42MX family of FPGAs also feature MultiPlex I/O, an advanced architectural feature that supports mixed voltage systems, enables programmable PCI, delivers high-performance operation at both 5.0V and 3.3V, and provides a low-power mode.

MultiPlex I/O supports the most common voltage standards today: pure 5.0V operation, pure 3.3V operation, and mixed 3.3V operation with 5.0V operation input tolerance for maximum performance. Internal array performance is retained in 3.3V systems by using complimentary pass gates that operate as fast at 3.3V as they do at 5.0V.

MultiPlex I/O includes selectable PCI output drives in certain 42MX devices, enabling 100% PCI-compliance for both 5.0V and 3.3V systems. For low-power systems, MultiPlex I/O is used to turn off all inputs and outputs to cut current consumption to below 100µA.

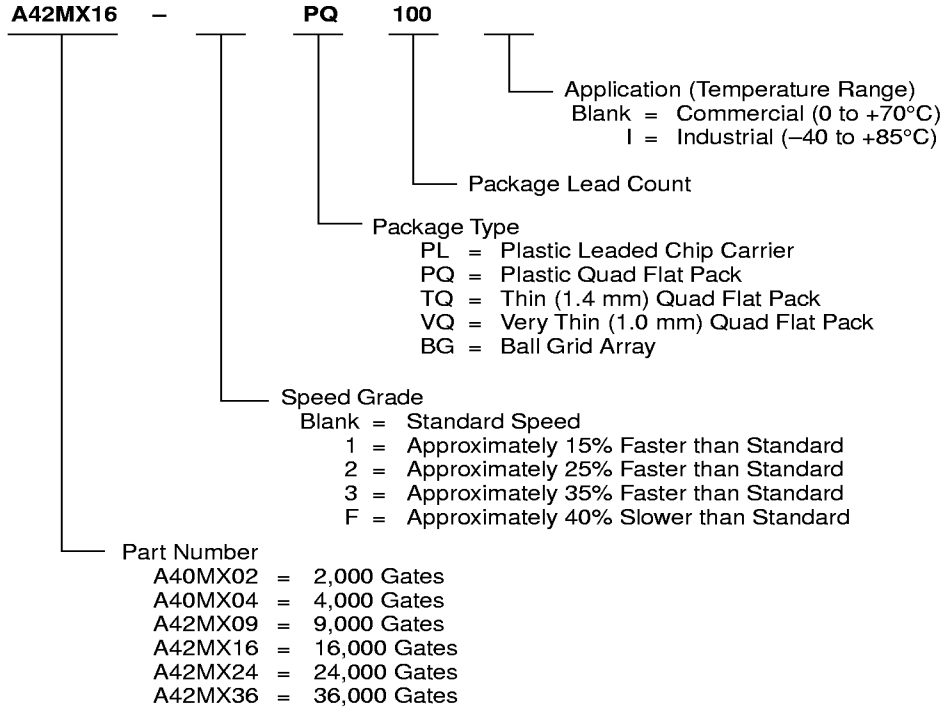
The 42MX FPGA devices also include system-level features such as JTAG, dual-port SRAM, and fast wide-decode modules. The 42MX family offers the industry's fastest dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The large number of storage elements can efficiently address applications requiring wide datapath manipulation, and can perform transformation functions such as telecommunications, networking, and DSP. The 42MX FPGAs were designed to integrate system logic that is typically implemented in multiple CPLDs, PALs, and FPGAs.

The MX PCI Compliant devices were specifically designed to be 100 percent compliant with PCI Local Bus Specification (version 2.1). Combining PCI-compliance with the industry's most synthesis friendly architecture provides the fastest PCI solution of any FPGA, regardless of whether you're designing a PCI interface from scratch or using a third-party synthesizable "core."

A42MX24 and A42MX36 devices offer high-performance, PCI-compliant programmable solution. The MX PCI-compliant devices deliver 200 MHZ on-chip operation and 6.1 nanosecond clock-to-output performance with capacities spanning from 24,000 to 36,000 gates.

Actel's MX PCI Compliant devices provide a high capacity, synthesis friendly programmable solution to PCI applications. The section numbers in the notes denote the pertinent section in the PCI Local Bus Specification version 2.2. MX devices comply 100% to the electrical and timing specifications detailed in the PCI specification. However, as with all programmable logic devices, the performance of the final product depends upon the user's design and optimization techniques.

Ordering Infrmation



Product Plan

	Speed Grade					Application			
	Std	–1*	–2*	–3*	–F*	C	I	M	B
A40MX02 Device									
44-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	—	—
68-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	—	—
100-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
80-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
A40MX04 Device									
44-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	—	—
68-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	—	—
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	—	—
100-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
80-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
A42MX09 Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	—	✔	✔	✔	—	—
100-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
160-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
176-Pin Thin Plastic Quad Flat Pack (TQFP)	✔	✔	✔	—	✔	✔	✔	—	—
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✔	✔	✔	—	✔	✔	✔	—	—
A42MX16 Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	—	✔	✔	✔	—	—
100-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
160-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
176-Pin Thin Plastic Quad Flat Pack (TQFP)	✔	✔	✔	—	✔	✔	✔	—	—
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✔	✔	✔	—	✔	✔	✔	—	—
A42MX24 Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	—	✔	✔	✔	—	—
160-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
176-Pin Thin Plastic Quad Flat Pack (TQFP)	✔	✔	✔	—	✔	✔	✔	—	—
A42MX36 Device									
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
240-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	—	✔	✔	✔	—	—
272-Pin Plastic Ball Grid Array (PBGA)	✔	✔	✔	—	✔	✔	✔	—	—

Applications: *C = Commercial* *I = Industrial* *M = Military* *B = MIL-STD-883*

Availability: *✔ = Available* *P = Planned* *— = Not Planned*

** Speed Grade:* *–1 = Approx. 15% Faster than Standard* *–2 = Approx. 25% Faster than Standard* *–3 = Approx. 35% Faster than Standard* *–F = Approx. 40% Slower than Standard*

Integrator Series devices are supported by Actel's Designer Series development software, which provides a seamless integration into many ASIC design flows. The Designer Series development tools offer automatic place and route (even with pre-assigned pins), static timing analysis, user programming, and debug and diagnostic probe capabilities. The DirectTime tool provides deterministic and controllable timing, allowing the designer to specify the performance requirements of individual paths and system clocks. Using these specifications, the software will automatically optimize the placement and routing of the logic to meet the constraints. Also included with the Designer Series tools is Actel's ACTgen Macro Builder. ACTgen allows the designer quickly to build fast, efficient logic functions such as counters, adders, FIFOs, and RAM.

The Designer Series tools provide designers with the capability to move up to high-level description languages, such as VHDL and Verilog-HDL, or to use schematic design entry with interfaces to most EDA tools. Designer Series is supported on 486 and Pentium PCs and on Sun and HP workstations. The software provides CAE interfaces to Cadence, Mentor Graphics, Escalade, OrCAD, and Viewlogic design environments. Additional development tools are supported through Actel's Industry Alliance Program, including Data I/O (ABEL FPGA) and MINC.

Actel's MX FPGAs provide a high-performance, single-chip solution for shortening the system design and development cycle, and they offer a cost-effective alternative to ASICs. The 40MX and 42MX devices are excellent choices for integrating logic that is currently implemented in multiple PALs, CPLDs, and FPGAs. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

Plastic Device Resources

Device	User I/Os										
	PLCC 44-Pin	PLCC 68-Pin	PLCC 84-Pin	VQFP 80-Pin	VQFP 100-Pin	PQFP 100-Pin	PQFP 160-Pin	PQFP 208-Pin	PQFP 240-Pin	TQFP 176-Pin	BGA 272-Pin
A40MX02	34	57	—	57	—	57	—	—	—	—	—
A40MX04	34	57	69	69	—	69	—	—	—	—	—
A42MX09	—	—	72	—	83	83	101	—	—	104	—
A42MX16	—	—	72	—	83	83	125	140	—	140	—
A42MX24	—	—	72	—	—	—	125	176	—	150	—
A42MX36	—	—	—	—	—	—	—	176	202	—	202

Package Definitions *(Consult your local Actel sales representative for product availability.)*

PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array

Pin Description

CLK, CLKA, CLKB

Clock Clock A and Clock B (Input)

TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground (Input)

Input LOW supply voltage.

I/O Input/Output (Input, Output)

Input, output, tri-state, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the Designer Series software.

MODE Mode (Input)

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). To provide ActionProbe capability, the MODE pin should be held HIGH. To facilitate this the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled HIGH when required.

NC No Connection

Not connected to circuitry within the device.

PRB, I/O Probe A (Output)

Used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB, I/O Probe B (Output)

Used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

QCLKA/B,C,D Quadrant Clock (Input/Output)

Quadrant clock inputs. When not used as a register control signal, these pins can function as general-purpose I/O.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

TCK Test Clock

Clock signal to shift the JTAG data into the device. This pin functions as an I/O when the JTAG fuse is not programmed.

TDI Test Data In

Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.

TDO Test Data Out

Serial data output for JTAG instructions and test data. This pin functions as an I/O when the JTAG fuse is not programmed.

TMS Test Mode Select

Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.

V_{CC} Supply Voltage (Input)

Input HIGH supply voltage.

V_{CCA} Supply Voltage (Input)

Input HIGH supply voltage, supplies array core only.

V_{CCI} Supply Voltage (Input)

Input HIGH supply voltage, supplies I/O cells only.

LP Low Power Mode

Controls the low power mode of all 42MX devices. This pin must be set HIGH to switch the device to low power mode. In low power mode, all I/Os are tri-stated, all input buffers are turned OFF, and the core of the devices is turned OFF. To exit the LOW power mode, the LP pin must be set LOW. This mode is enabled 800 nsec after LP pin is set HIGH.

Note: *TCK, TDI, TDO, TMS are available only on devices containing JTAG circuitry.*

Connecting V_{CC} on MX Devices

40MX

The 40MX FPGAs will operate in 5.0V only systems or 3.3V only systems.

V_{CC}	Input	Output
3.3V	3.3V	3.3V
5.0V	5.0V	5.0V

42MX

The 42MX FPGAs will operate in 5.0V only systems, 3.3V only systems, or mixed 5.0V/3.3V systems.

V_{CCA}	V_{CCI}	Input	Output
3.3V	3.3V	3.3V	3.3V
5.0V	3.3V	3.3V, 5.0V	3.3V
5.0V	5.0V	5.0V	5.0V

Mixed Voltage Power-Up and Power-Down

When powering the device in the mixed voltage mode (V_{CCA} = 5.0V and V_{CCI} = 3.3V), V_{CCA} must be greater than or equal to V_{CCI} throughout the power-up sequence. If V_{CCI} is 0.5V greater than V_{CCA} when both are above 1.5V, then the I/Os input protection junction will be forward biased. This causes the I/Os to draw large amounts of current. When V_{CCA} and V_{CCI} are in the 1.5 to 2.0V region and V_{CCI} is greater than V_{CCA}, all I/Os would momentarily behave as outputs that are in logical high state and I_{CC} rises to high levels. For power-down any sequence with V_{CCA} and V_{CCI} can be implemented.

MX Architectural Overview

The 40MX and 42MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within the Integrator Series are composed of logic modules, routing resources, clock networks, and I/O modules, which are the building blocks for designing fast logic designs. In addition, a subset of devices contain embedded dual-port SRAM and wide decode modules. The dual-port SRAM modules are optimized for high-speed datapath functions such as FIFOs, LIFOs, and scratchpad memory. The "Integrator Series Product Profile" on page 1 lists the specific logic resources contained within each device.

Logic Modules

The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources (Figure 1).

The logic module can implement the four basic logic functions (NAND, AND, OR, and NOR) in gates of two, three, or four inputs. Each function may have many versions with different combinations of active LOW inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs, and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array, since latches and flip-flops can be constructed from logic modules wherever needed in the application.

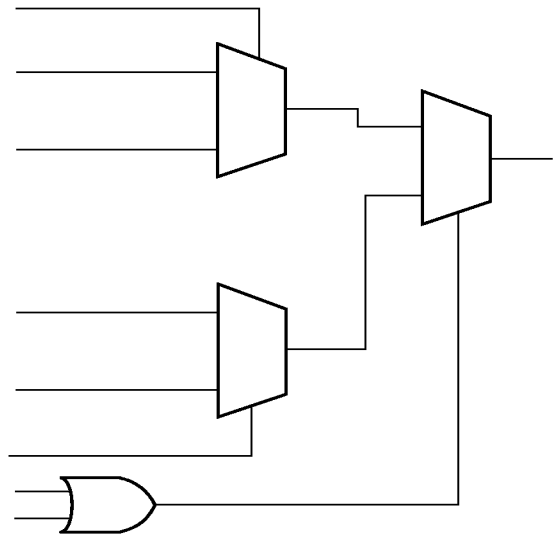


Figure 1 • *40MX Logic Module*

The 42MX devices contain three types of logic modules: combinatorial (C-modules), sequential (S-modules), and decode (D-modules).

The C-module is shown in Figure 2 and implements the following function:

Y=!S1*!S0*D00+!S1*S0*D01+S1*!S0*D10+S1*S0*D11

where

S0=A0*B0

S1=A1+B1

The S-module shown in Figure 3 is designed to implement high-speed sequential functions within a single logic module. The S-module implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D flip-flop or a transparent latch. To increase flexibility, the S-module register can be bypassed so that it implements purely combinatorial logic.

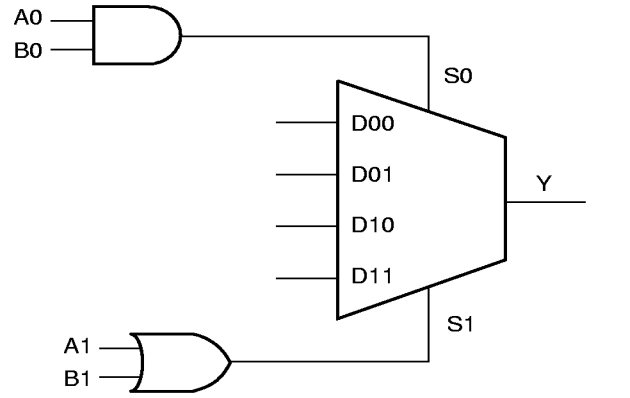


Figure 2 • *C-Module Implementation*

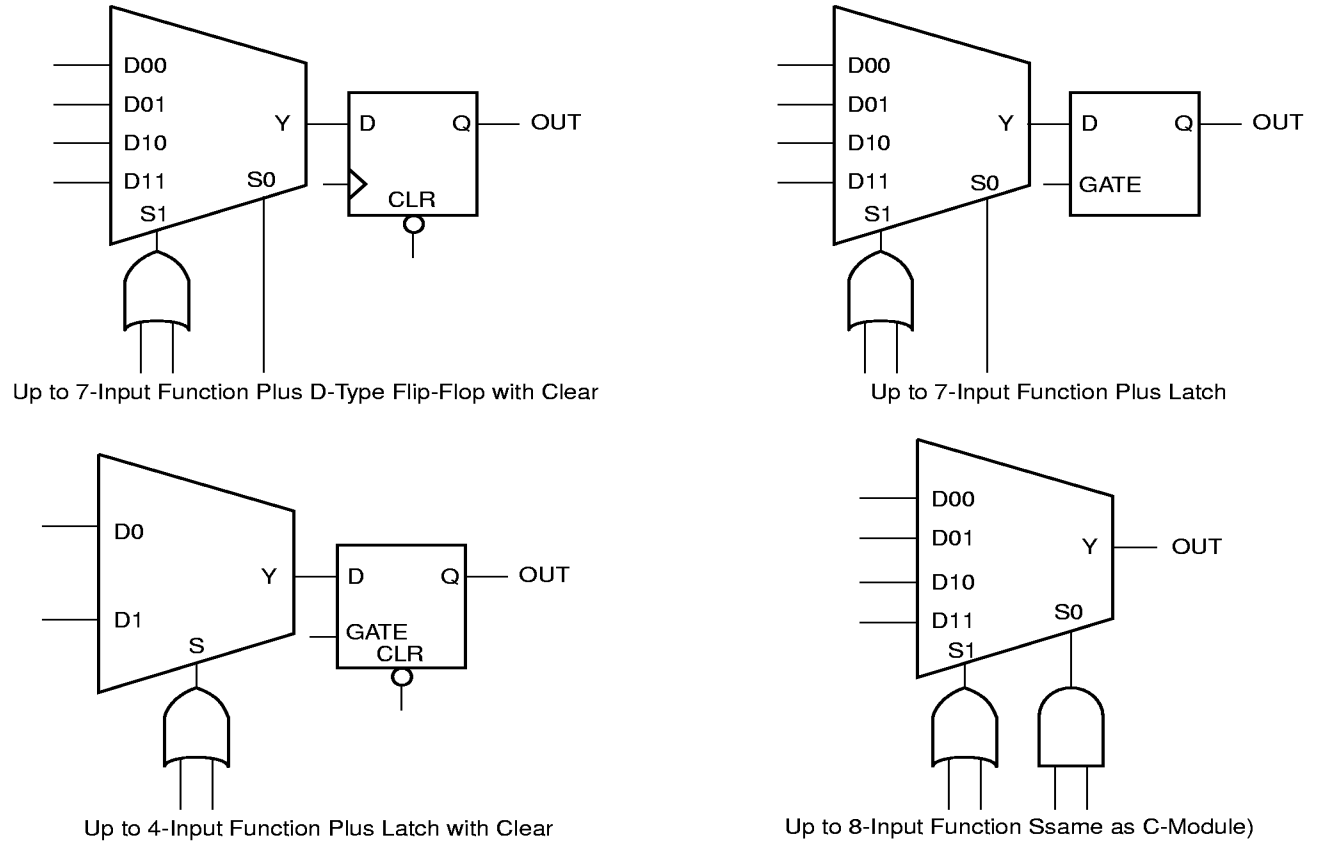


Figure 3 • *S-Module Implementation*

Some of the 42MX devices contain a third type of logic module, D-modules, which are arranged around the peripheries of the devices. D-modules contain wide-decode circuitry, which provides a fast, wide-input AND function similar to that found in product term architectures (Figure 4). The D-module allows 42MX devices to perform wide-decode functions at speeds comparable to CPLDs and PAL devices. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hard-wired to an output pin, or it can be fed back into the array to be incorporated into other logic.

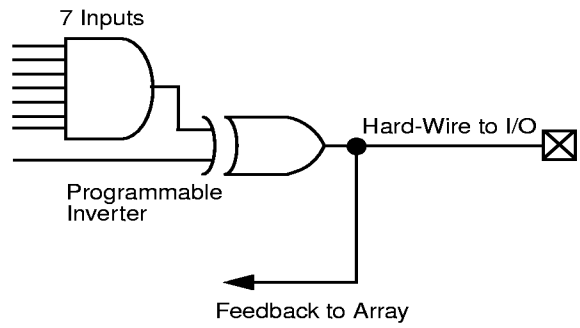


Figure 4 • *D-Module Implementation*

Dual-Port SRAM Modules

Several 42MX devices contain dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. (Refer to the "Integrator Series Product Profile" table, on page 1, for the number of SRAM blocks within a particular device.) SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the 42MX dual-port SRAM block is shown in Figure 5.

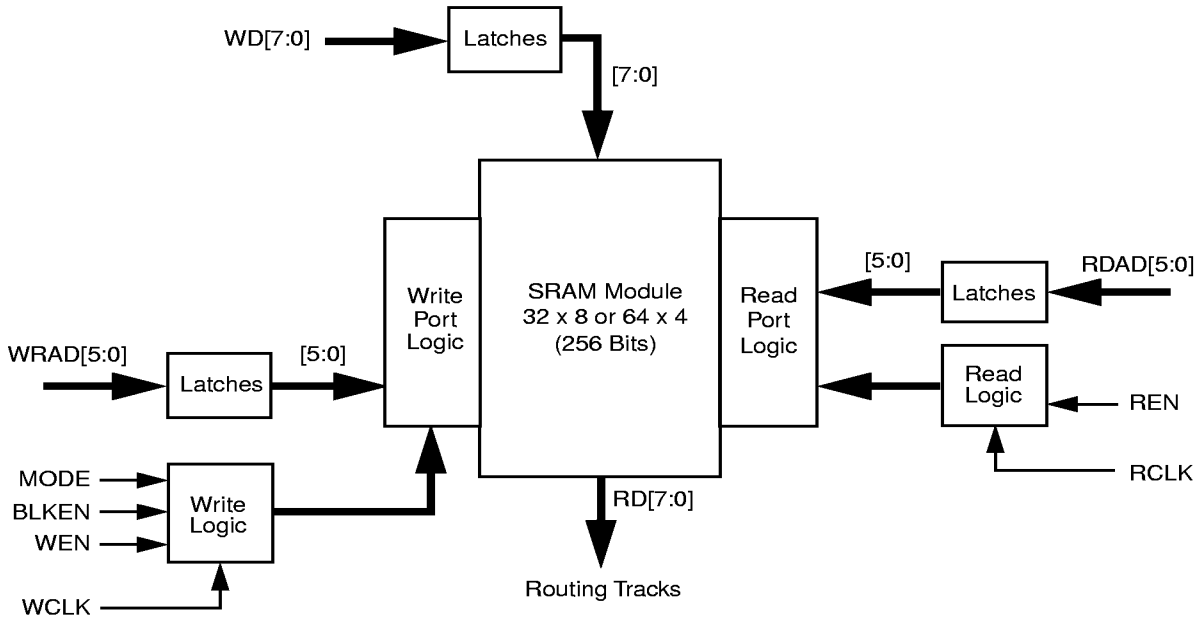


Figure 5 • *42MX Dual-Port SRAM Block*

The 42MX SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]) which are connected to segmented vertical routing tracks.

The 42MX dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring fast FIFO and LIFO queues. Actel's ACTgen Macro Builder provides the capability to quickly design memory functions, such as FIFOs,

LIFOs, and RAM arrays. In addition, unused SRAM blocks can be used to implement registers for other logic within the design.

MultiPlex I/O Modules

The MultiPlex I/O modules provide the interface between the device pins and the logic array. The top of Figure 6 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (Refer to the Macro Library Guide for more information.) All 42MX I/O modules contain a tri-state buffer, with input and output latches that can be configured for input, output, or bi-directional operation.

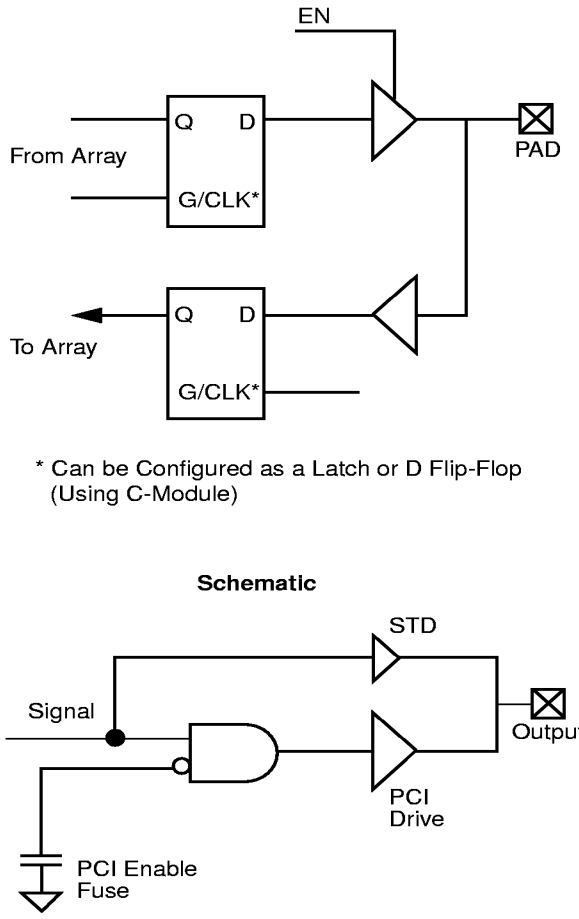


Figure 6 • I/O Module

The Integrator Series devices contain flexible I/O structures, where each output pin has a dedicated output-enable control. The I/O module can be used to latch input or output data, or both, providing a fast set-up time. In addition, the Actel Designer Series software tools can build a D-type flip-flop using a C-module to register input and output signals. To achieve 5.0V or 3.3V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed. When the PCI fuse is not programmed, output drive is standard. (See the bottom portion of Figure 6.)

Actel's Designer Series development tools provide a design library of I/O macrofunctions that can implement all I/O configurations supported by the MX FPGAs.

Routing Structure

The MX architecture uses vertical and horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may be either of continuous length or broken into pieces called *segments*. Varying segment lengths allows the interconnect of over 90% of design tracks to occur with only two antifuse connections. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 7. Non-dedicated horizontal routing tracks are used to route signal nets; dedicated routing tracks are used for global clock networks and for power and ground tie-off tracks.

Vertical Routing

Another set of routing tracks run vertically through the module. Vertical tracks are of three types: input, output, and long, and are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module; each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array, where edge effects occur. Long vertical tracks contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 7.

Antifuse Structures

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly-testable structures as well as efficient programming algorithms. The structure is highly-testable

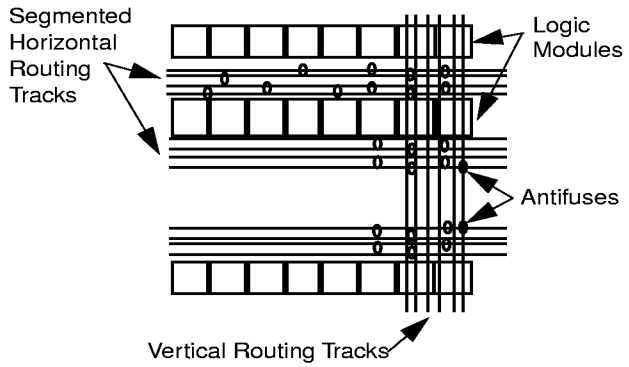


Figure 7 • *Routing Structure*

because there are no pre-existing connections; therefore, temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Clock Networks

The 40MX devices have one global CLK distribution network. Two low-skew, high-fanout clock distribution networks are provided in each 42MX device. These networks are referred to as *CLK0* and *CLK1*. Each network has a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows:

- Externally from the CLKA pad
- Externally from the CLKB pad
- Internally from the CLKINA input
- Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

The user controls the clock module by selecting one of two clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally-generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. The clock input pads can also be used as normal I/Os, bypassing the clock networks. (See Figure 8.)

The 42MX devices that contain SRAM modules have four additional register control resources, called quadrant clock networks (Figure 9). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within

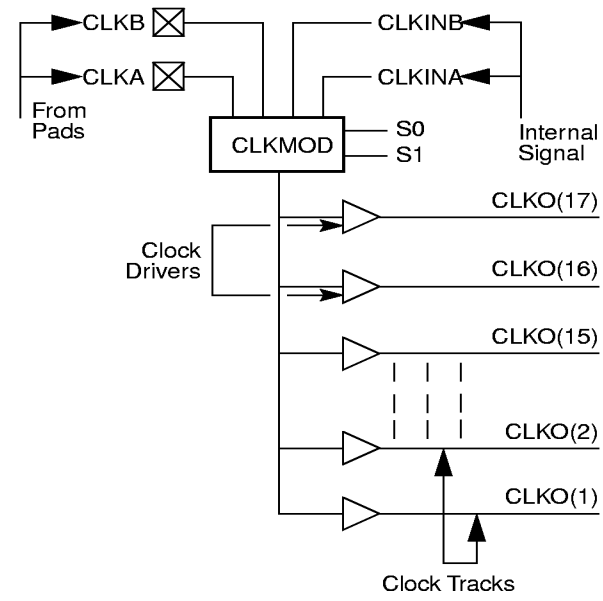


Figure 8 • *Clock Networks*

its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

Test Circuitry

Both 40MX and 42MX devices provide the means to test and debug a design once it is programmed into a device. The 40MX and 42MX devices contain Actel's test circuitry. Once a device has been programmed, the ActionProbe test circuitry allows the designer to probe any internal node during device operation to aid in debugging a design. In addition, 42MX devices contain IEEE Standard 1149.1 (JTAG) Boundary Scan Test.

JTAG Boundary Scan Testing (BST)

Device pin spacing is decreasing with the advent of fine-pitch packages such as TQFP and BGA, and manufacturers are routinely implementing surface-mount technology with multilayer PC boards. The Joint Test Action Group (JTAG) developed IEEE Standard 1149.1 Boundary Scan Test to facilitate board-level testing during manufacturing.

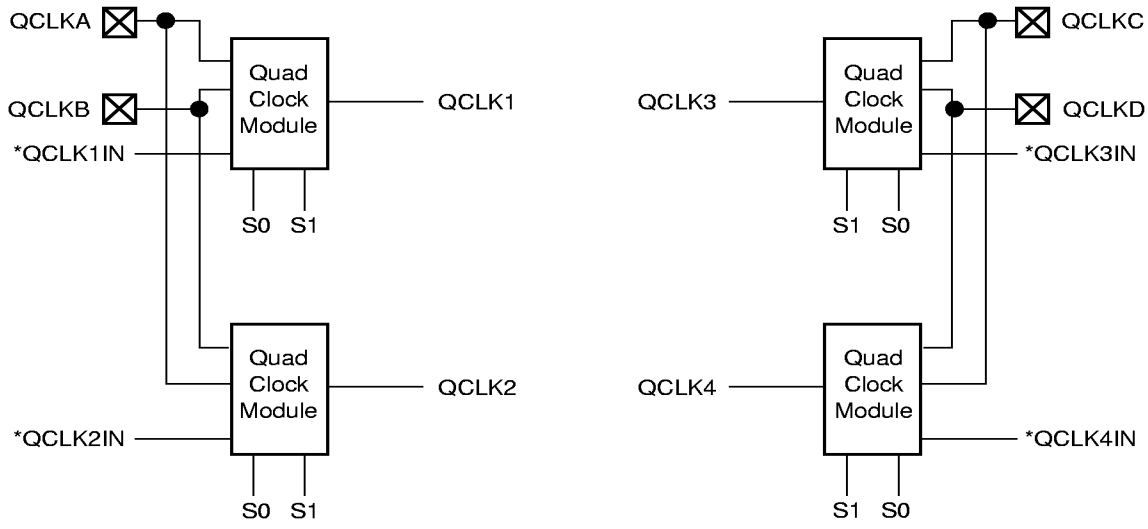
IEEE Standard 1149.1 defines a four-pin Test Access Port (TAP) interface for testing integrated circuits in a system. The 42MX family provides four JTAG BST pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCLK), and Test Mode Select (TMS). Devices are configured in a JTAG "chain" where BST data can be transmitted serially between devices via TDO-to-TDI interconnections. The TMS and TCLK signals

are shared among all devices in the JTAG chain so that all components operate in the same state.

The 42MX family implements a subset of the IEEE Standard 1149.1 BST instruction in addition to a private instruction, which allows the use of Actel's ActionProbe facility with JTAG BST. Refer to the IEEE Standard 1149.1 specification for detailed information regarding JTAG testing.

JTAG Architecture

The 42MX JTAG BST circuitry consist of a Test Access Port (TAP) controller, JTAG instruction register, a JPROBE register, a bypass register, and a boundary scan register. Figure 10 is a block diagram of the 42MX JTAG circuitry.



**QCLK1IN, QCLK2IN, QCLK3IN, and QCKL4IN are internally-generated signals.*

Figure 9 • *Quadrant Clock Network*

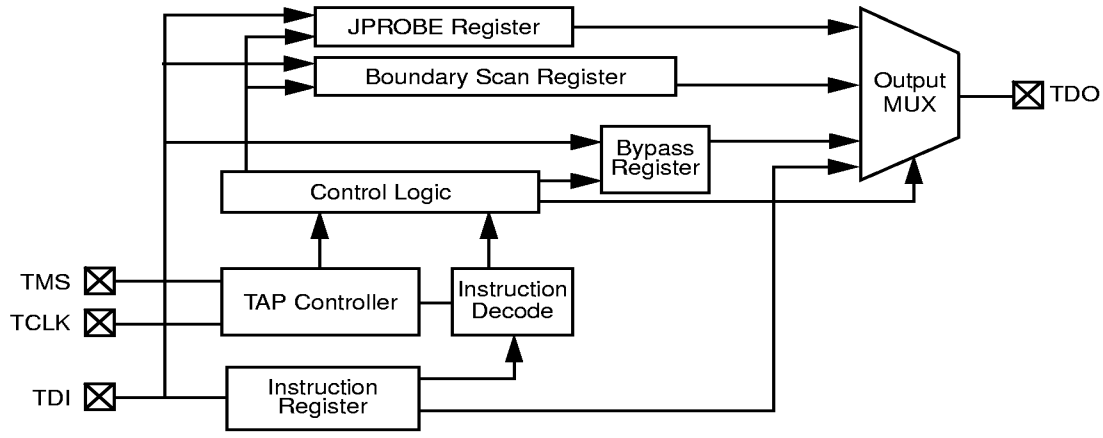


Figure 10 • *JTAG BST Circuitry*

When a device is operating in JTAG BST mode, four I/O pins are used for the TDI, TDO, TMS, and TCLK signals. An active reset (nTRST) pin is not supported; however, the 42MX contains power-on circuitry that resets the JTAG BST circuitry upon power-up. During normal device operation, the JTAG pins should be held LOW to disable the JTAG circuitry. The following table summarizes the functions of the JTAG BST signals.

JTAG Signal	Name	Function
TDI	Test Data In	Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCLK.
TDO	Test Data Out	Serial data output for JTAG instructions and test data.
TMS	Test Mode Select	Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCLK.
TCLK	Test Clock	Clock signal to shift the JTAG data into the device.

JTAG BST Instructions

JTAG BST testing within the 42MX devices is controlled by a Test Access Port (TAP) state machine. The TAP controller drives the three-bit instruction register, a bypass register, and the boundary scan data registers within the device. The TAP controller uses the TMS signal to control the JTAG testing of the device. The JTAG test mode is determined by the bitstream entered on the TMS pin. The table in the next column describes the JTAG instructions supported by the 42MX.

JTAG Reset

The TMS pin is equipped with a pull-up resistor. This allows the TAP controller to remain in or return to the Test-Logic-Reset state when there is no input or when a logical 1 is on the TMS pin. To reset the controller, TMS must be HIGH for at least five TCLK cycles.

ActionProbe

If a device has been successfully programmed and the security fuse has not been programmed, any internal logic or I/O module output can be observed in real time using the ActionProbe circuitry, PRA and/or PRB pins and Actel's Silicon Explorer diagnostic and debug tool kit. Refer to "Using the ActionProbe for System-Level Debug" application note for further information.

Test Mode	Code	Description
EXTEST	000	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
SAMPLE/ PRELOAD	001	Allows a snapshot of the signals at the device pins to be captured and examined during device operation.
INTEST	010	Refer to the IEEE Standard 1149.1 specification.
JPROBE	011	A private instruction allowing the user to connect Actel's Micro Probe registers to the JTAG chain.
USER INSTRUCTION	100	Allows the user to build application-specific instructions such as RAM READ and RAM WRITE.
HIGH Z	101	Refer to the IEEE Standard 1149.1 specification.
CLAMP	110	Refer to the IEEE Standard 1149.1 specification.
BYPASS	111	Enables the bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the JTAG chain.

5.0V Operating Conditions
Mixed 5.0V/3.3V Operating Conditions

Absolute Maximum Ratings[1]

Free Air Temperature Range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source/Sink Current[2]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND – 0.5V, the internal protection diode will be forward-biased and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range[1]	0 to +70	–40 to +85	°C
Power Supply Tolerance	±5	±10	%V_{CC}
V_{CCI}	4.75 to 5.25	4.5 to 5.5	V
V_{CCA}	4.75 to 5.25	4.5 to 5.5	V
V_{CC}	4.75 to 5.25	4.5 to 5.5	V
V_{CCI}[2]	3.14 to 3.47	3.0 to 3.6	V

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial.*
2. *Operating condition for I/O in mixed voltage mode.*

Electrical Specifications

Symbol	Parameter	Commercial		Commercial –F		Industrial		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = –10 mA)[2]	2.4		2.4				V
	(I_{OH} = –6 mA)	3.84		3.84				V
	(I_{OH} = –4 mA)					3.7		V
V_{OL}[1]	(I_{OL} = 10 mA)[2]		0.5		0.5			V
	(I_{OL} = 6 mA)		0.33		0.33		0.40	V
V_{IL}		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500		500	ns
C_{IO} I/O Capacitance[2, 3]			10		10		10	pF
Standby Current, I_{CC}[4]			Note 5 & 6		25.0		Note 6 & 7	mA
$I_{CC(D)}$ Dynamic V_{CC} Supply Current		See "Power Dissipation" on page 19.						
Low Power Mode Standby Current			I_{CC} – 0.5		I_{CC} – 0.5		I_{CC} – 0.5	mA

Notes:

1. *Only one output tested at a time. V_{CC} = min.*
2. *Not tested, for information only.*
3. *Includes worst-case 84-Pin CPGA package capacitance. V_{OUT} = 0 V, f = 1 MHz.*
4. *All outputs unloaded. All inputs = V_{CC} or GND. I_{CC} limit includes I_{PP} and I_{SV} during normal operation.*
5. *A40MX02 and A40MX04 I_{CC} = 3 mA, A42MX09 I_{CC} = 5 mA, A42MX16 I_{CC} = 6 mA, A42MX24 and A42MX36 I_{CC} = 25 mA.*
6. *I_{CC} Max = 2 mA is available by special request. Contact your local Actel Sales representative for additional information.*
7. *A40MX02 and A40MX04 I_{CC} = 10 mA, A42MX09, A42MX16, A42MX24 , and A42MX36 I_{CC} = 25 mA.*

3.3V Operating Conditions

Absolute Maximum Ratings[1]

Free Air Temperature Range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[2]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND – 0.5V, the internal protection diodes will forward-bias and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range[1]	0 to +70	–40 to +85	°C
Power Supply Tolerance	±5	±10	%V
V_{CCI}	3.0 to 3.6	3.0 to 3.6	V
V_{CCA}	3.0 to 3.6	3.0 to 3.6	V

Note:

1. *Ambient temperature (T_A) is used for commercial.*

Electrical Specifications

Parameter		Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = –4 mA)	2.15		3.7		V
	(I_{OH} = –3.2 mA)	2.4				V
V_{OL}[1]	(I_{OL} = 6 mA)		0.4		0.48	V
V_{IL}		–0.3	0.8	–0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500	ns
C_{IO} I/O Capacitance[2, 3]			10		10	pF
Standby Current, I_{CC}[4]			Note 5 & 6		Note 6 & 7	mA
$I_{CC(D)}$ Dynamic V_{CC} Supply Current		See "Power Dissipation" on page 19.				
Low Power Mode Standby Current			I_{CC} – 0.5		I_{CC} – 2.0	mA

Notes:

1. *Only one output tested at a time. V_{CC} = min.*
2. *Not tested, for information only.*
3. *Includes worst-case 84-Pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.*
4. *All outputs unloaded. All inputs = V_{CC} or GND.*
5. *A40MX02 and A40MX04 I_{CC} = 3 mA, A42MX09 I_{CC} = 5 mA, A42MX16 I_{CC} = 6 mA, A42MX24 and A42MX36 I_{CC} = 25 mA.*
6. *I_{CC} Max = 2 mA is available by special request. Contact your local Actel Sales representative for additional information.*
7. *A40MX02 and A40MX04 I_{CC} = 10 mA, A42MX09, A42MX16, A42MX24, and A42MX36 I_{CC} = 25 mA.*

Output Drive Characteristics for 5.0V PCI Signaling

MX PCI device I/O drivers were designed specifically for high-performance PCI systems. Figure 11 shows the typical output drive characteristics of the MX devices. MX output drivers are compliant with the PCI Local Bus Specification.

Table 1 • DC Specification for 5.0V Signaling[1]

			PCI		MX		
Symbol	**Parameter**	**Condition**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Units**
V_{CC}	Supply Voltage		4.75	5.25	4.75	5.25[2]	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	2.0	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		–0.5	0.8	–0.3	0.8	V
I_{IH}	Input High Leakage Current	V_{IN} = 2.7		70	—	10	µA
I_{IL}	Input Low Leakage Current	V_{IN}=0.5		–70	—	–10	µA
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	2.4		3.7		V
V_{OL}	Output Low Voltage	I_{OUT} = 3 mA, 6 mA		0.55	—	0.33	V
C_{IN}	Input Pin Capacitance			10	—	10	pF
C_{CLK}	CLK Pin Capacitance		5	12	—	10	pF
L_{PIN}	Pin Inductance			20	—	< 8 nH[3]	nH

Notes:

1. *PCI Local Bus Specification Section 4.2.1.1.*
2. *Maximum rating for V_{CC} –0.5V to 7.0V. .*
3. *Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.*

Table 2 • AC Specifications for 5.0V Signaling[1]

			PCI		MX		
Symbol	**Parameter**	**Condition**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Units**
I_{CL}	Low Clamp Current	$-5 < V_{IN} \le -1$	$-25 + (V_{IN} + 1) / 0.015$		–60	–10	mA
Slew (r)	Output Rise Slew Rate	0.4V to 2.4V load	1	5	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	2.4V to 0.4V load	1	5	2.8	4.3	V/ns

Note:

1. *PCI Local Bus Specification Section 4.2.1.2.*

Output Drive Characteristics for 3.3V PCI Signaling

Table 3 • DC Specification for 3.3V Signaling[1]

Symbol	Parameter	Condition	PCI		MX		Units
			Minimum	Maximum	Minimum	Maximum	
V_{CC}	Supply Voltage		3.0	3.6	3.0	3.6	V
V_{IH}	Input High Voltage		0.5	V_{CC} + 0.5	0.5	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	0.8	–0.3	0.8	V
I_{IH}	Input High Leakage Current	V_{IN} = 2.7		70		10	µA
I_{IL}	Input Leakage Current			–70		–10	µA
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	0.9		2.3		V
V_{OL}	Output Low Voltage	I_{OUT} = 3 mA, 6 mA		0.1		0.33	V
C_{IN}	Input Pin Capacitance			10		10	pF
C_{CLK}	CLK Pin Capacitance		5	12		10	pF
L_{PIN}	Pin Inductance			20		< 8 nH[3]	nH

Notes:

1. *PCI Local Bus Specification Section 4.2.2.1.*
2. *Maximum rating for V_{CC} –0.5V to 7.0V.*
3. *Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.*

Table 4 • AC Specifications for 3.3V Signaling[1]

Symbol	Parameter	Condition	PCI		MX		Units
			Minimum	Maximum	Minimum	Maximum	
I_{CL}	Low Clamp Current	$-5 < V_{IN} \le -1$	$-25 + (V_{IN} + 1) / 0.015$		–60	–10	mA
Slew (r)	Output Rise Slew Rate	0.2V to 0.6V load	1	4	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	0.6V to 0.2V load	1	4	2.8	4.0	V/ns

Note:

1. *PCI Local Bus Specification Section 4.2.2.2.*

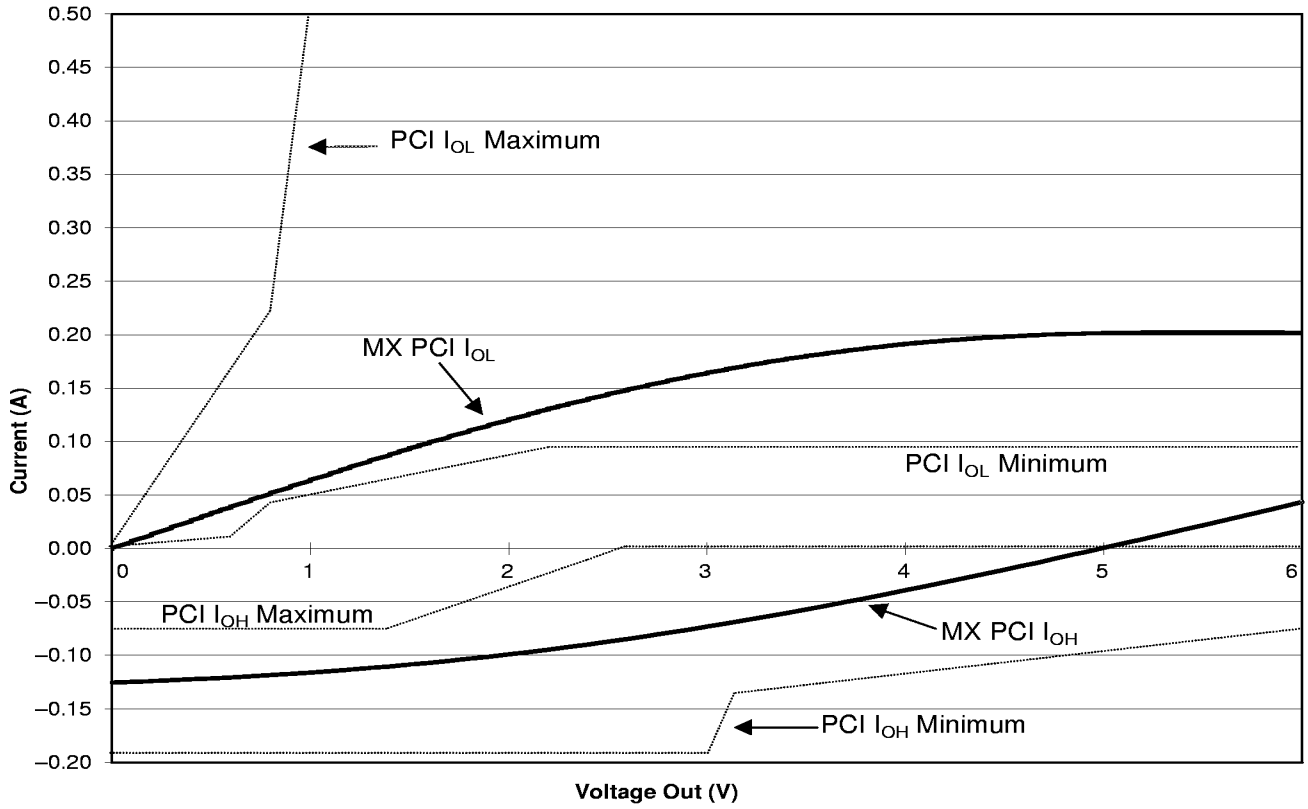


Figure 11 • *Typical Output Drive Characteristics (Based upon measured data)*

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc}, and the junction-to-ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQFP 160-pin package at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp.}}{\theta_{ja}\ (°C/W)} = \frac{150°C - 70°C}{32°C/W} = 2.5\,W$$

Package Type	Pin Count	θja		Maximum Power Dissipation	
		Still Air	300 ft/min	Still Air	300 ft/min
Plastic Quad Flat Pack	100	34°C/W	31°C/W	2.6 W	2.6 W
Plastic Quad Flat Pack	160	32°C/W	24°C/W	2.5 W	3.3 W
Plastic Quad Flat Pack	208	20°C/W	17°C/W	4.0 W	4.7 W
Plastic Leaded Chip Carrier	44	43°C/W	31°C/W	1.9 W	2.6 W
Plastic Leaded Chip Carrier	68	36°C/W	25°C/W	2.2 W	3.2 W
Plastic Leaded Chip Carrier	84	32°C/W	22°C/W	2.5 W	3.6 W
Thin Plastic Quad Flat Pack	176	28°C/W	21°C/W	2.9 W	3.8 W
Very Thin Plastic Quad Flat Pack	80	39°C/W	33°C/W	2.0 W	2.4 W
Very Thin Plastic Quad Flat Pack	100	38°C/W	32°C/W	2.1 W	2.5 W
Plastic Quad Flat Pack	240	19°C/W	16°C/W	4.2 W	5.0 W
Ball Grid Array	272	20°C/W	14.5°C/W	4.0 W	5.5 W

Power Dissipation

General Power Equation

$$P = [I_{CC}standby + I_{CC}active] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

where:

$I_{CC}standby$ is the current flowing when no inputs or outputs are changing.

$I_{CC}active$ is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematic because their values depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Actel FPGAs have small static power components that result in power dissipation lower than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated for commercial, worst-case conditions:

I_{CC}	V_{CC}	Power
2 mA	5.25 V	10.5 mW

The static power dissipation by TTL loads depends on the number of outputs driving HIGH or LOW, and on the DC load current. Again, this number is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33V will generate 42 mW with all outputs driving LOW, and 140 mW with all outputs driving HIGH. The actual dissipation will average somewhere in between, as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency-dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1.

$$\text{Power } (\mu W) = C_{EQ} * V_{CC}^2 * F \quad (1)$$

where:

C_{EQ} is the equivalent capacitance expressed in picofarads (pF).

V_{CC} is power supply in volts (V).

F is the switching frequency in megahertz (MHz).

Equivalent capacitance is calculated by measuring $I_{CCactive}$ at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values for Actel MX FPGAs

Modules (C_{EQM})	3.5
Input Buffers (C_{EQI})	6.9
Output Buffers (C_{EQO})	18.2
Routed Array Clock Buffer Loads (C_{EQCR})	1.4

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piece-wise linear summation over all components.

$$\text{Power} = V_{CC}^2 * [(m \times C_{EQM} * f_m)_{Modules} + (n * C_{EQI} * f_n)_{Inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} \quad (2)$$

where:

m = Number of logic modules switching at frequency f_m

n = Number of input buffers switching at frequency f_n

p = Number of output buffers switching at frequency f_p

q_1 = Number of clock loads on the first routed array clock

q_2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output load capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

Fixed Capacitance Values for Actel FPGAs (pF)

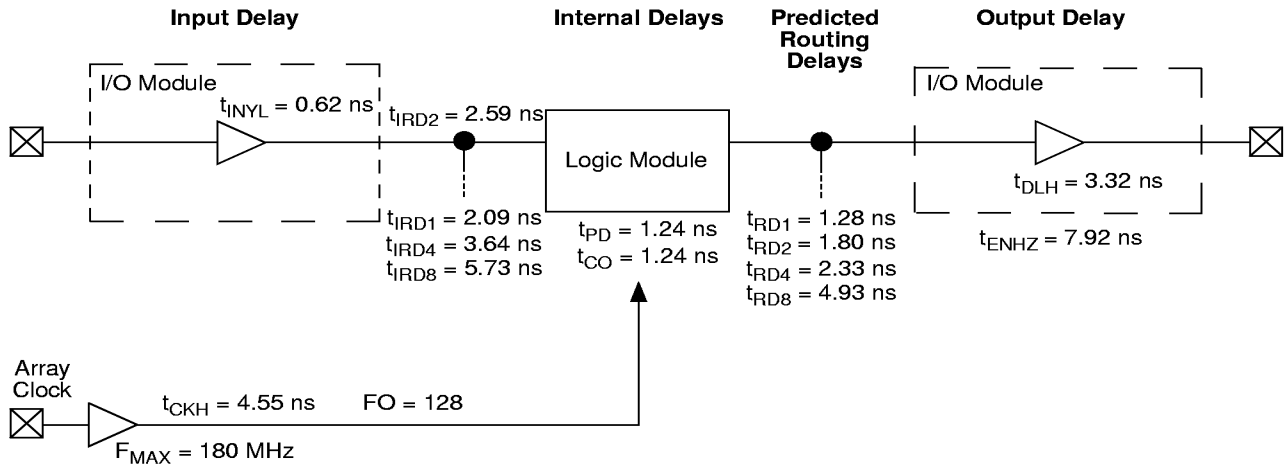
Device Type	r_1 routed_Clk1	r_2 routed_Clk2
A40MX02	41.4	N/A
A40MX04	68.6	N/A
A42MX09	118	118
A42MX16	165	165
A42MX24	185	185
A42MX36	220	220

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines represent worst-case scenarios; these can be used to generally predict the upper limits of power dissipation.

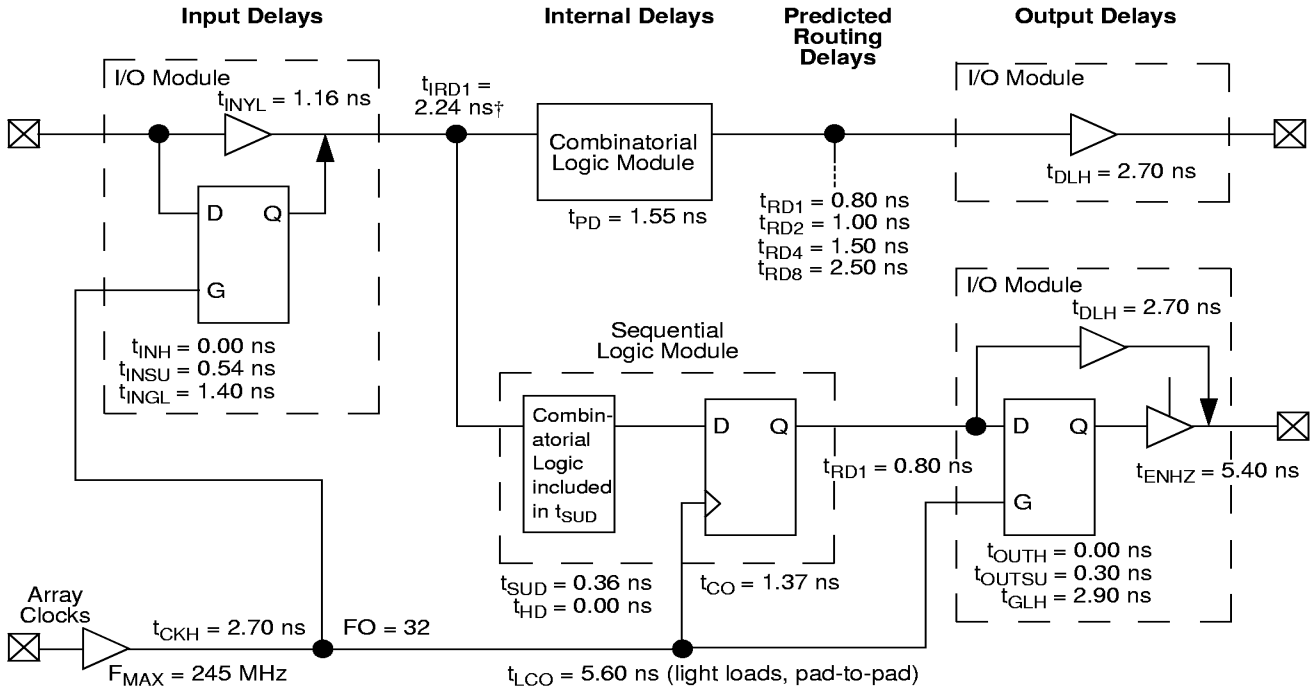
Logic Modules (m)	= 80% of Combinatorial Modules
Inputs Switching (n)	= # of Inputs/4
Outputs Switching (p)	= # Outputs/4
First Routed Array Clock Loads (q_1)	= 40% of Sequential Modules
Second Routed Array Clock Loads (q_2)	= 40% of Sequential Modules
Load Capacitance (C_L)	= 35 pF
Average Logic Module Switching Rate (f_m)	= F/10
Average Input Switching Rate (f_n)	= F/5
Average Output Switching Rate (f_p)	= F/10
Average First Routed Array Clock Rate (f_{q1})	= F
Average Second Routed Array Clock Rate (f_{q2})	= F/2

40MX Timing Model*



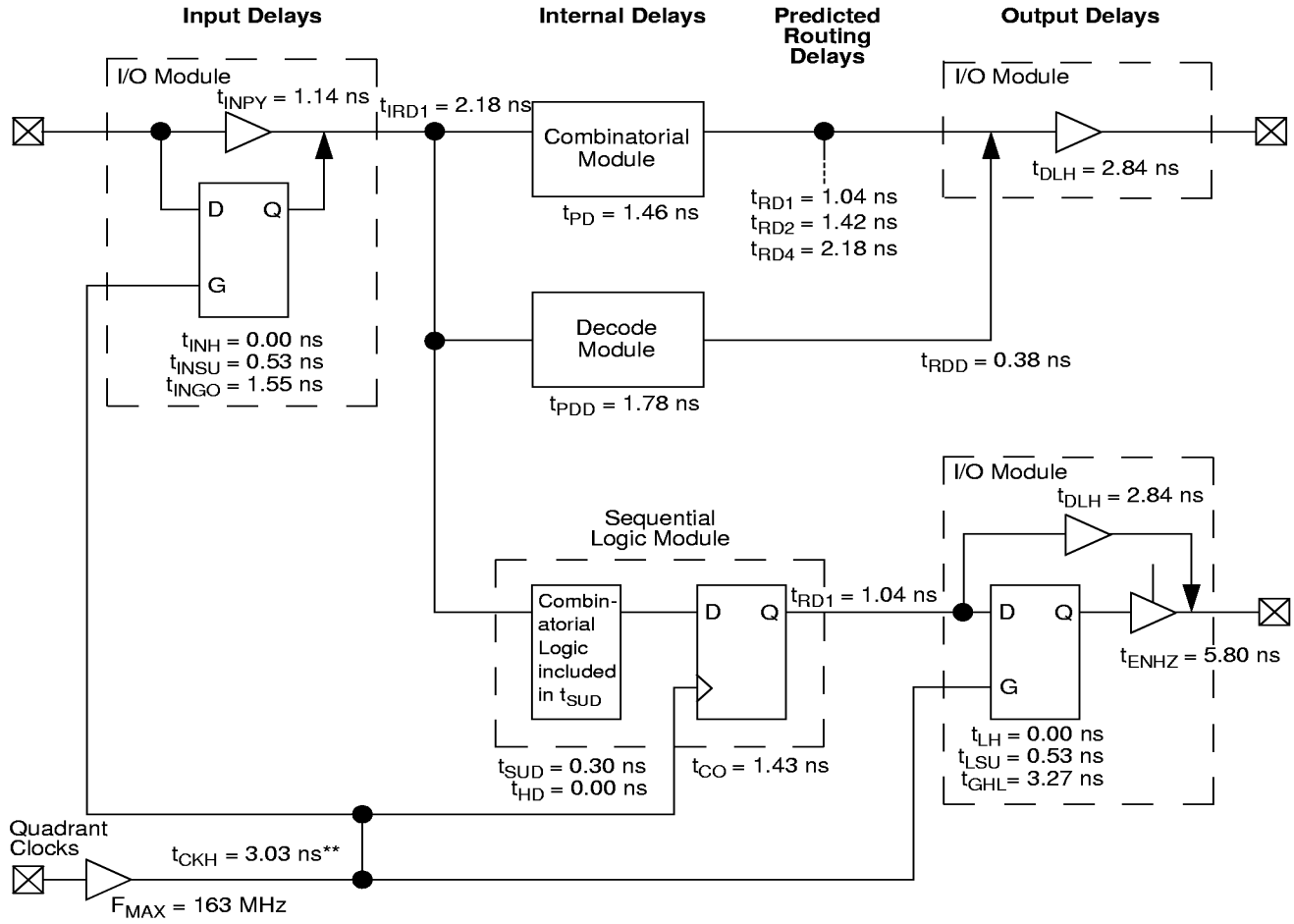
** Values are shown for 40MX '–3 speed' devices at 5.0V worst-case commercial conditions.*

42MX Timing Model*



**Values are shown for A42MX09-2 at 5.0V worst-case commercial conditions* *† Input module predicted routing delay*

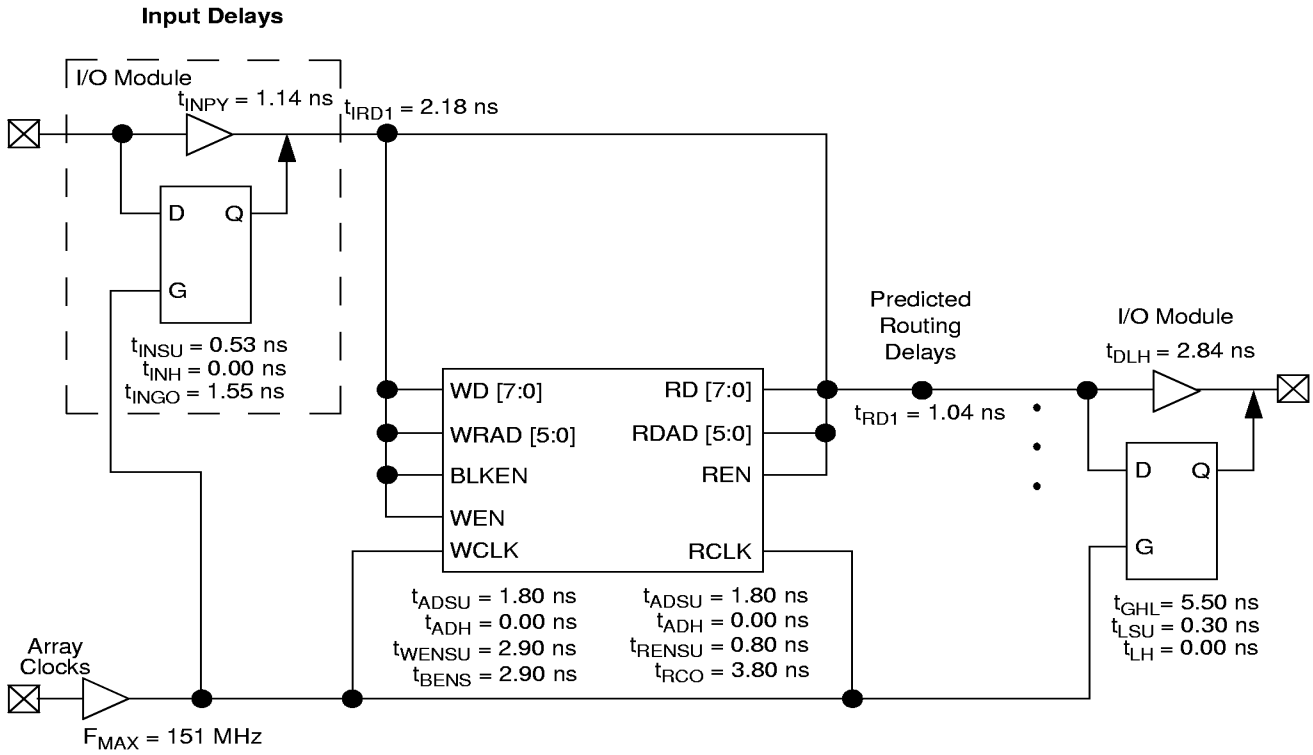
42MX Timing Model (Logic Functions using Quadrant Clocks)*



** Preliminary values are shown for A42MX36-2 at 5.0V worst-case commercial conditions*

*** Load-dependent*

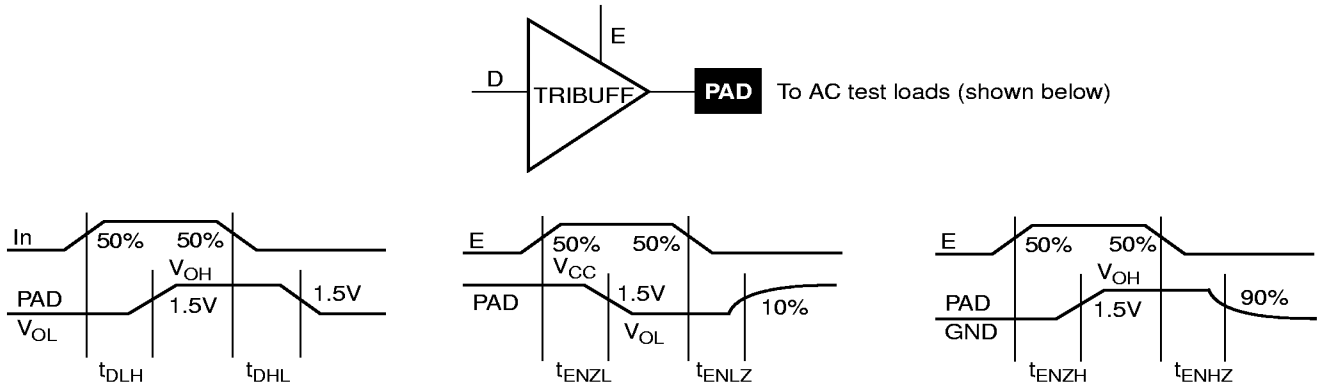
42MX Timing Model (SRAM Functions)*



**Values are shown for A42MX36-2 at 5.0V worst-case commercial conditions.*

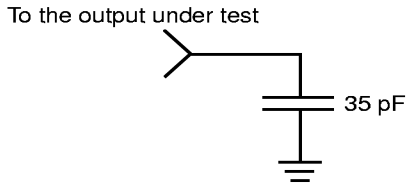
Parameter Measurement

Output Buffer Delays

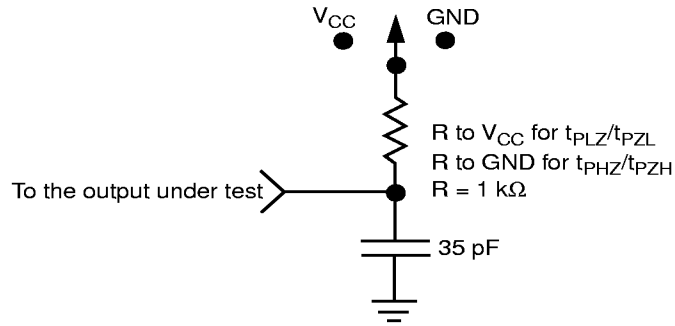


AC Test Loads

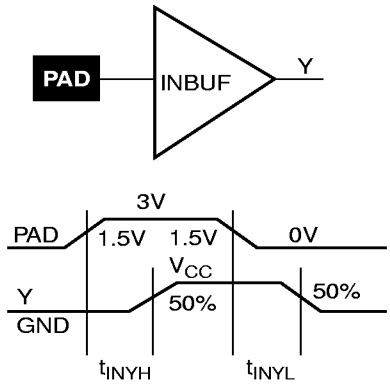
Load 1
(Used to measure propagation delay)



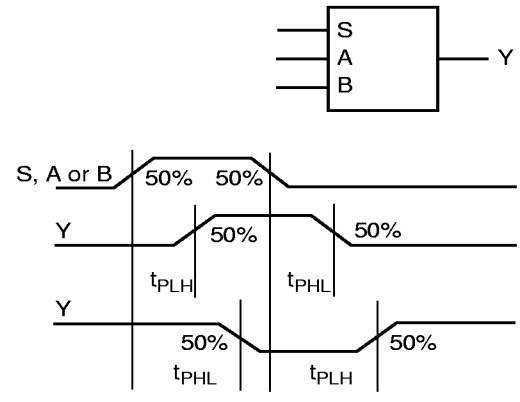
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

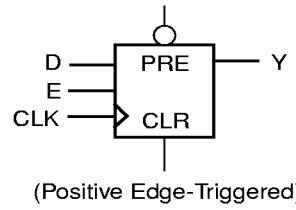


Module Delays

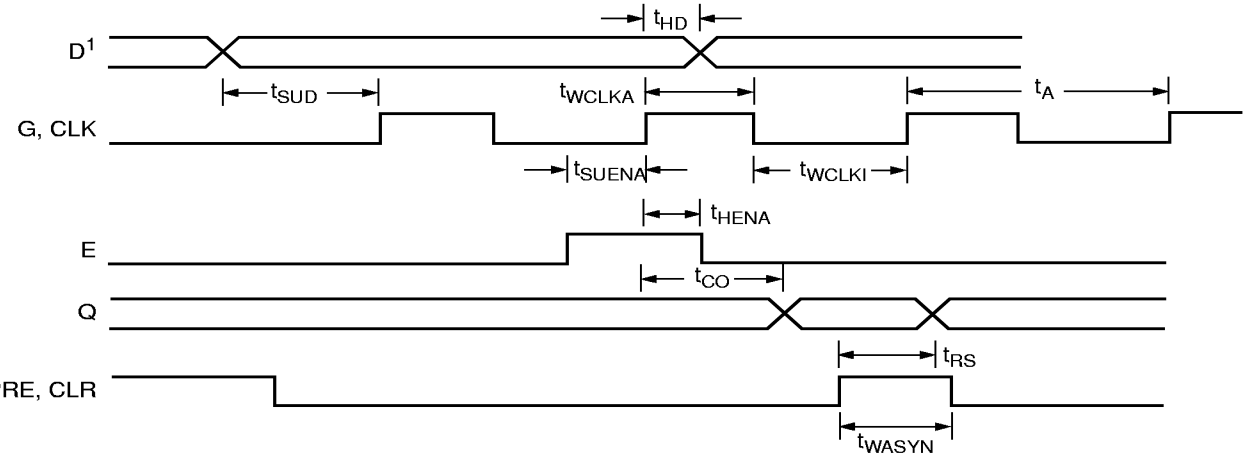


Sequential Module Timing Characteristics

Flip-Flops and Latches



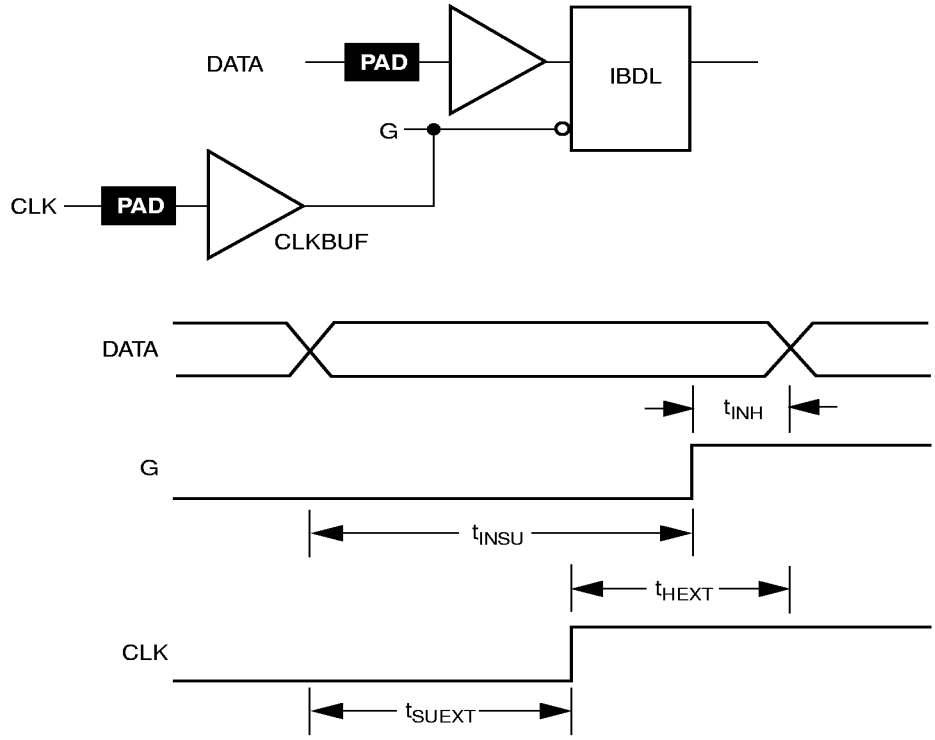
(Positive Edge-Triggered)



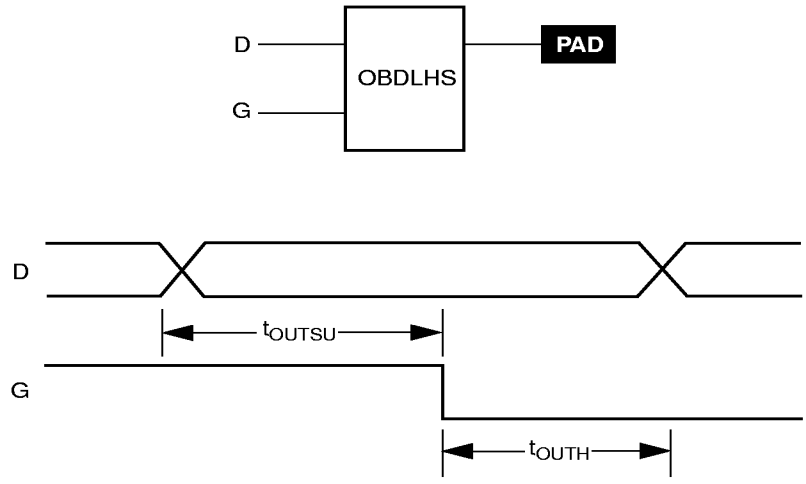
Note: *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

Sequential Timing Characteristics (continued)

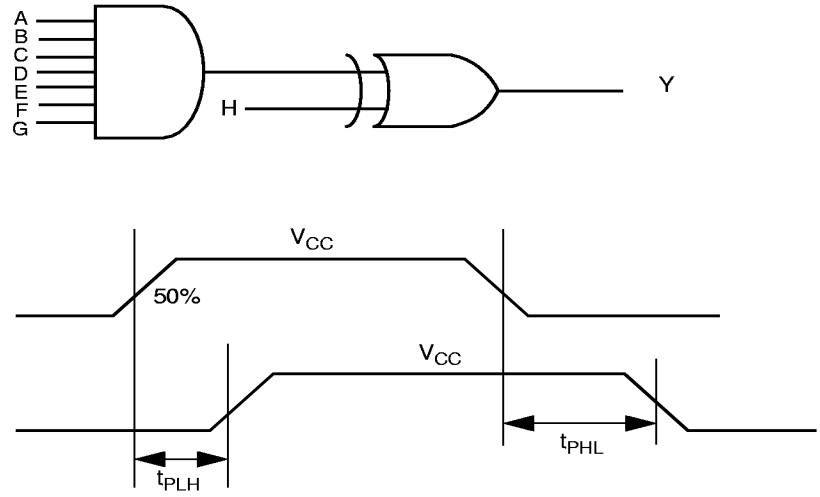
Input Buffer Latches



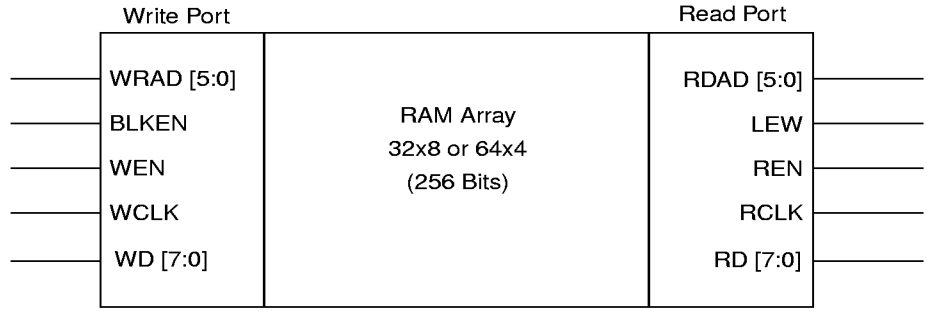
Output Buffer Latches



Decode Module Timing

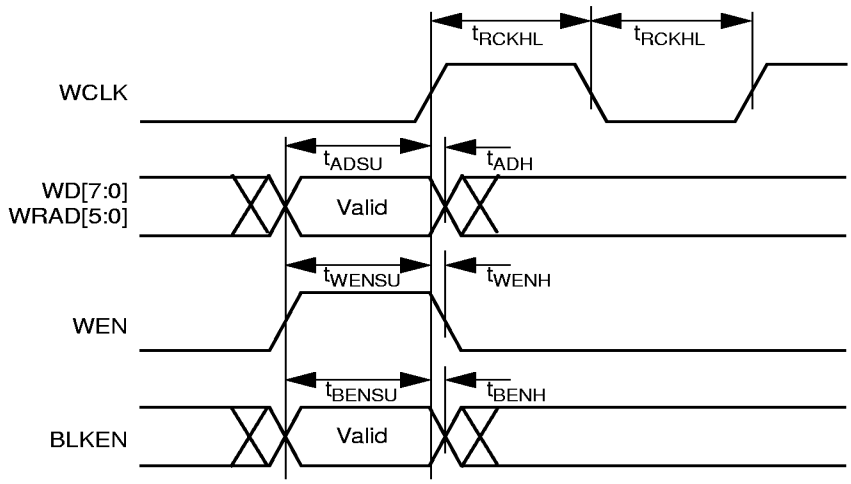


SRAM Timing Characteristics



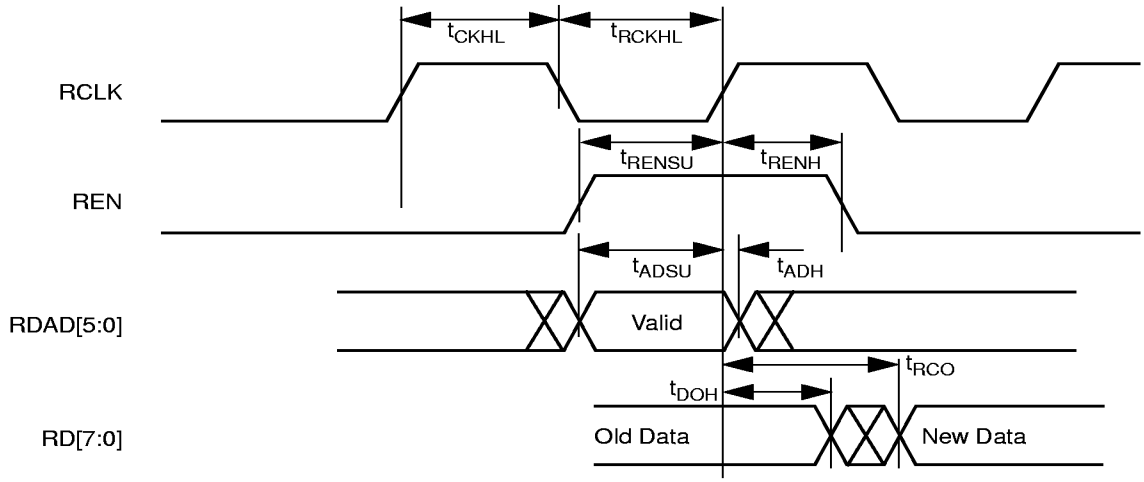
Dual-Port SRAM Timing Waveforms

42MX SRAM Write Operation



Note: *Identical timing for falling edge clock.*

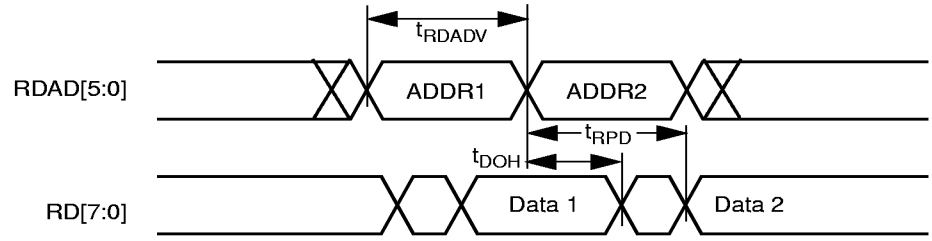
42MX SRAM Synchronous Read Operation



Note: *Identical timing for falling edge clock.*

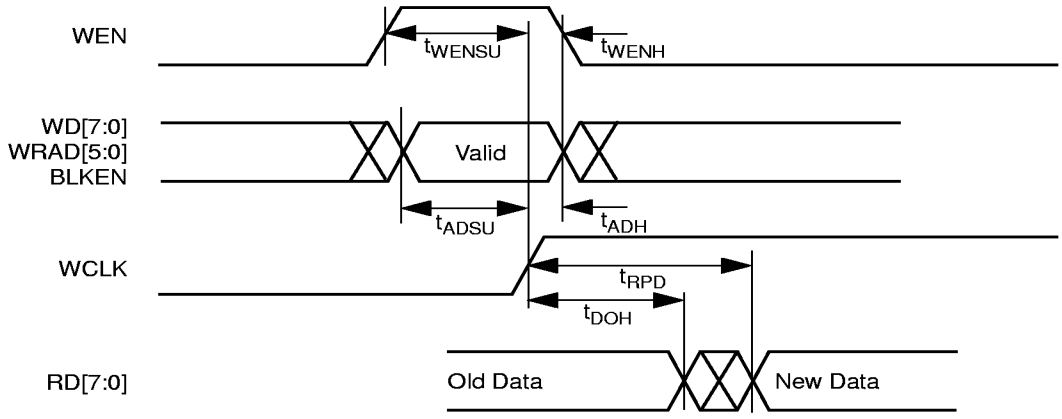
42MX SRAM Asynchronous Read Operation—Type 1

(Read Address Controlled)



42MX SRAM Asynchronous Read Operation—Type 2

(Write Address Controlled)



Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented PLICE antifuse offers an very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 micron lithography, offer nominal levels of 100 ohms resistance and 7.0 femtofarad (fF) capacitance per antifuse.

The Integrator Series fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90% of interconnects using two antifuses.

Timing Characteristics

Timing characteristics for devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all Integrator Series members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after place and route of the user's design is complete. Delay values may then be determined by using the Designer Series utility or by performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays in this data sheet apply to typical nets. The abundant routing resources in the MX architecture allows for deterministic timing using Actel's Designer Series development tools which include DirectTime, a timing-driven place-and-route tool. Using DirectTime, the designer can specify timing-critical nets and system clock frequency. Using these timing specifications, the place-and-route software optimizes the layout of the design to meet the user's specifications.

Long Tracks

Some nets in the design use long tracks which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6% of nets in a fully utilized device require long tracks. Long tracks add approximately 3 ns to 6 ns delay, which is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section.

Timing Derating

A timing derating factor of 0.45 is used to reflect best-case processing. Note that this factor is relative to the standard speed timing parameters, and must be multiplied by the appropriate voltage and temperature derating factors for a given application.

Timing Derating Factor (Temperature and Voltage)

	Industrial	
	Min.	**Max.**
(Commercial Specification) x	0.69	1.11

Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (5.0V)

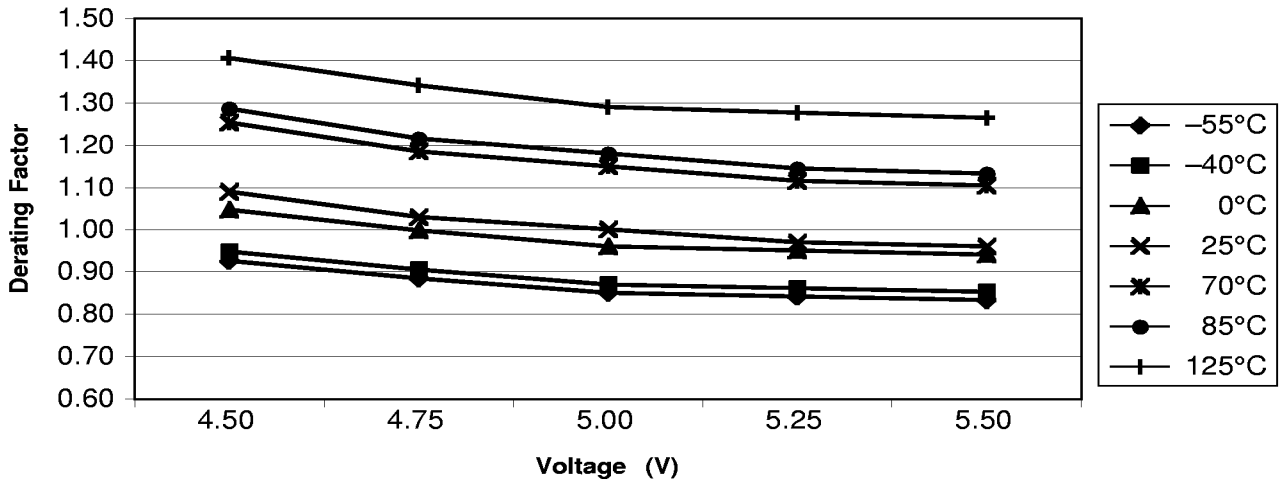
(Maximum Specification, Worst-Case Condition) x	0.85

Note: *This derating factor applies to all routing and propagation delays.*

42MX Temperature and Voltage Derating Factors (Normalized to T_J = 5V, 25°C)

42MX	–55	–40	0	25	70	85	125
4.50	0.93	0.95	1.05	1.09	1.25	1.29	1.41
4.75	0.88	0.90	1.00	1.03	1.18	1.22	1.34
5.00	0.85	0.87	0.96	1.00	1.15	1.18	1.29
5.25	0.84	0.86	0.95	0.97	1.12	1.14	1.28
5.50	0.83	0.85	0.94	0.96	1.10	1.13	1.26

42MX Junction Temperature and Voltage Derating Curves (Normalized to T_J= 5V, 25°C)

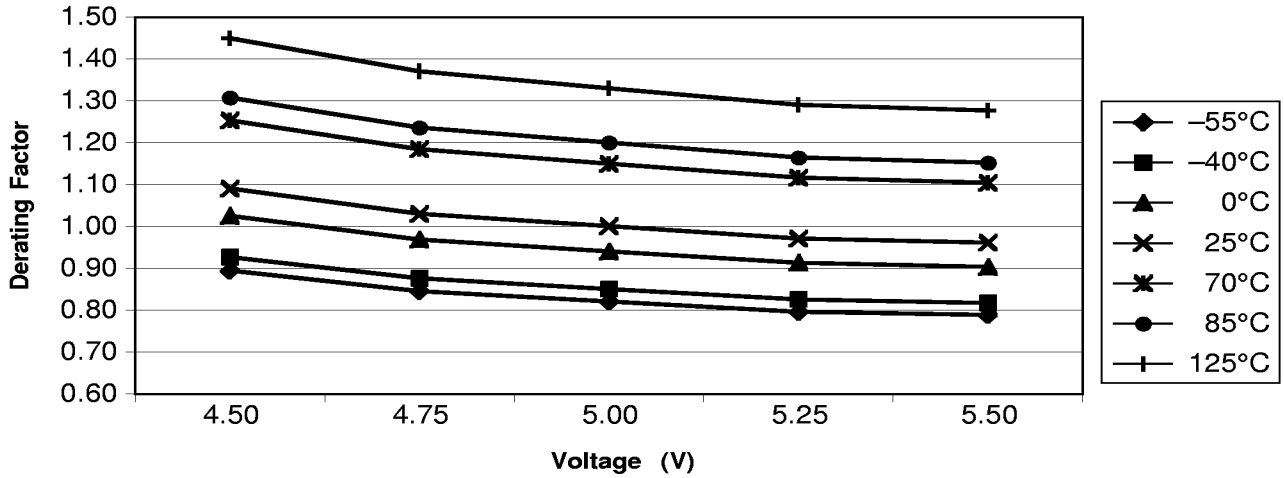


Note: *This derating factor applies to all routing and propagation delays.*

40MX Temperature and Voltage Derating Factors (Normalized to T_J = 5V, 25°C)

40MX	–55	–40	0	25	70	85	125
4.50	0.89	0.93	1.02	1.09	1.25	1.31	1.45
4.75	0.84	0.88	0.97	1.03	1.18	1.24	1.37
5.00	0.82	0.85	0.94	1.00	1.15	1.20	1.33
5.25	0.80	0.82	0.91	0.97	1.12	1.16	1.29
5.50	0.79	0.82	0.90	0.96	1.10	1.15	1.28

40MX Junction Temperature and Voltage Derating Curves (Normalized to T_J= 5V, 25°C)



Note: *This derating factor applies to all routing and propagation delays.*

PCI System Timing Specification

Tables 5 and 6 list the critical PCI timing parameters and the corresponding timing parameter for the MX PCI-compliant devices.

PCI Models

Actel provides synthesizable VHDL and Verilog-HDL models for a PCI target interface, a PCI Target and Target+DMA Master interface. Consult your local Actel sales representative for more details.

Table 5 • *Clock Specification for 33 MHz PCI*

		PCI		A42MX24		A42MX36		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
T_{CYC}	CLK Cycle Time	30	—	4.0	—	4.0	—	ns
T_{HIGH}	CLK High Time	11	—	1.9	—	1.9	—	ns
T_{LOW}	CLK Low Time	11	—	1.9	—	1.9	—	ns

Table 6 • *Timing Parameters for 33 MHz PCI*

		PCI		A42MX24		A42MX36		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
T_{VAL}	CLK to Signal Valid—Bused Signals	2	11	2.0	9.0	2.0	9.0	ns
$T_{VAL(PTP)}$	CLK to Signal Valid—Point-to-Point	2	12	2.0	9.0	2.0	9.0	ns
T_{ON}	Float to active	2	—	2.0	4.0	2.0	4.0	ns
T_{OFF}	Active to Float	—	28	—	8.3[1]	—	8.3[1]	ns
T_{SU}	Input Set-Up Time to CLK—Bused Signals	7	—	1.5	—	1.5	—	ns
$T_{SU(PTP)}$	Input Set-Up Time to CLK—Point-to-Point	10, 12	—	1.5	—	1.5	—	ns
T_H	Input Hold to CLK	0	—	0	—	0	—	ns

Notes:

1. T_{OFF} is system dependent. MX PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.

A40MX02 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75V, T_J = 70°C)

Logic Module Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.24		1.43		1.63		1.90		2.66	ns
t_{PD2}	Dual-Module Macros		2.65		3.06		3.47		4.08		5.71	ns
t_{CO}	Sequential Clock-to-Q		1.24		1.43		1.62		1.90		2.66	ns
t_{GO}	Latch G-to-Q		1.24		1.43		1.62		1.90		2.66	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.24		1.43		1.62		1.90		2.66	ns
Predicted Routing Delays[1]												
t_{RD1}	FO=1 Routing Delay		1.28		1.48		1.67		1.97		2.76	ns
t_{RD2}	FO=2 Routing Delay		1.80		2.08		2.35		2.77		3.88	ns
t_{RD3}	FO=3 Routing Delay		2.33		2.69		3.04		3.58		5.01	ns
t_{RD4}	FO=4 Routing Delay		2.85		3.29		3.72		4.38		6.13	ns
t_{RD8}	FO=8 Routing Delay		4.93		5.69		6.45		7.59		10.63	ns
Sequential Timing Characteristics												
t_{SUD}[2]	Flip-Flop (Latch) Data Input Set-Up	3.06		3.53		4.00		4.70		6.58		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	3.06		3.53		4.00		4.70		6.58		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.25		3.75		4.25		5.00		7.00		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.25		3.75		4.25		5.00		7.00		ns
t_A	Flip-Flop Clock Input Period	4.84		5.59		6.33		7.45		10.43		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		180.90		167.50		154.10		134.00		80.40	MHz

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
2. *Set-up times assume fanout of 3. Further testing information can be obtained from the DirectTime Analyzer utility.*
3. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Designer 3.0 or later DirectTime Analyzer to check the hold time for this macro.*

A40MX02 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			0.70		0.80		0.91		1.07		1.50	ns
t_{INYL}	Pad-to-Y LOW			0.62		0.71		0.81		0.95		1.33	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			2.07		2.39		2.17		3.19		4.47	ns
t_{IRD2}	FO=2 Routing Delay			2.59		2.99		3.39		3.99		5.59	ns
t_{IRD3}	FO=3 Routing Delay			3.12		3.60		4.08		4.80		6.72	ns
t_{IRD4}	FO=4 Routing Delay			3.64		4.20		4.76		5.60		7.84	ns
t_{IRD8}	FO=8 Routing Delay			5.73		6.62		7.50		8.82		12.35	ns
Global Clock Network													
t_{CKH}	Input Low to HIGH	FO = 16		4.55		5.25		5.95		7.00		9.80	
		FO = 128		4.55		5.25		5.95		7.00		9.80	ns
t_{CKL}	Input High to LOW	FO = 16		4.81		5.55		6.29		7.40		10.36	
		FO = 128		4.81		5.55		6.29		7.40		10.36	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 16	2.24		2.58		2.92		3.44		4.82		
		FO = 128	2.35		2.71		3.07		3.61		5.05		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 16	2.24		2.58		2.92		3.44		4.82		
		FO = 128	2.35		2.71		3.07		3.61		5.05		ns
t_{CKSW}	Maximum Skew	FO = 16		0.39		0.45		0.51		0.60		0.84	
		FO = 128		0.53		0.62		0.70		0.82		1.15	ns
t_P	Minimum Period	FO = 16	4.67		5.39		6.10		7.18		10.05		
		FO = 128	4.84		5.59		6.33		7.45		10.43		ns
f_{MAX}	Maximum Frequency	FO = 16		187.60		174.79		159.85		139.00		83.40	
		FO = 128		180.90		167.50		154.10		134.00		80.40	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A40MX02 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data-to-Pad HIGH		3.32		3.83		4.34		5.11		7.15	ns
t_{DHL}	Data-to-Pad LOW		3.98		4.60		5.21		6.13		8.58	ns
t_{ENZH}	Enable Pad Z to HIGH		3.74		4.31		4.89		5.75		8.05	ns
t_{ENZL}	Enable Pad Z to LOW		4.69		5.41		6.13		7.21		10.09	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.92		9.14		10.35		12.18		17.05	ns
t_{ENLZ}	Enable Pad LOW to Z		5.86		6.77		7.67		9.02		12.63	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data-to-Pad HIGH		3.93		4.54		5.14		6.05		8.47	ns
t_{DHL}	Data-to-Pad LOW		3.39		3.92		4.44		5.22		7.31	ns
t_{ENZH}	Enable Pad Z to HIGH		3.37		3.89		4.41		5.19		7.27	ns
t_{ENZL}	Enable Pad Z to LOW		4.88		5.63		6.38		7.51		10.51	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.92		9.14		10.35		12.18		17.05	ns
t_{ENLZ}	Enable Pad LOW to Z		5.86		6.77		7.67		9.02		12.63	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

Notes:

1. Delays based on 35 pF loading.

A40MX02 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 3.0V, T_J = 70°C)

Logic Module Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.73		2.00		2.26		2.66		3.72	ns
t_{PD2}	Dual-Module Macros		3.71		4.28		4.86		5.71		8.00	ns
t_{CO}	Sequential Clock-to-Q		1.73		2.00		2.26		2.66		3.72	ns
t_{GO}	Latch G-to-Q		1.73		2.00		2.26		2.66		3.72	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.73		2.00		2.26		2.66		3.72	ns
Predicted Routing Delays[1]												
t_{RD1}	FO=1 Routing Delay		1.93		2.23		2.52		2.97		4.16	ns
t_{RD2}	FO=2 Routing Delay		2.66		3.07		3.47		4.09		5.72	ns
t_{RD3}	FO=3 Routing Delay		3.39		3.92		4.44		5.22		7.31	ns
t_{RD4}	FO=4 Routing Delay		4.12		4.76		5.39		6.34		8.88	ns
t_{RD8}	FO=8 Routing Delay		7.05		8.14		9.22		10.85		15.19	ns
Sequential Timing Characteristics[2]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	4.28		4.94		5.59		6.58		9.21		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	4.28		4.94		5.59		6.58		9.21		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.55		5.25		5.95		7.00		9.80		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.55		5.25		5.95		7.00		9.80		ns
t_A	Flip-Flop Clock Input Period	6.78		7.82		8.87		10.43		14.60		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		108.54		100.50		92.46		80.40		48.24	MHz

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
2. *Set-up times assume fanout of 3. Further testing information can be obtained from the Direct Time Analyzer utility.*
3. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Designer 3.0 or later Direct Time Analyzer to check the hold yime for this macro.*

A40MX02 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			0.97		1.12		1.27		1.50		2.10	ns
t_{INYL}	Pad-to-Y LOW			0.86		1.00		1.13		1.33		1.86	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			2.90		3.35		3.80		4.47		6.25	ns
t_{IRD2}	FO=2 Routing Delay			3.63		4.19		4.75		5.59		7.82	ns
t_{IRD3}	FO=3 Routing Delay			4.37		5.04		5.71		6.72		9.41	ns
t_{IRD4}	FO=4 Routing Delay			5.10		5.88		6.66		7.84		10.98	ns
t_{IRD8}	FO=8 Routing Delay			8.03		9.26		10.50		12.35		17.29	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 16		6.37		7.35		8.33		9.80		13.72	
		FO = 128		6.37		7.35		8.33		9.80		13.72	ns
t_{CKL}	Input HIGH to LOW	FO = 16		6.73		7.77		8.81		10.36		14.50	
		FO = 128		6.73		7.77		8.81		10.36		14.50	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 16	3.13		3.61		4.09		4.82		6.74		
		FO = 128	3.29		3.79		4.30		5.05		7.08		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 16	3.13		3.61		4.09		4.82		6.74		
		FO = 128	3.29		3.79		4.30		5.05		7.08		ns
t_{CKSW}	Maximum Skew	FO = 16		0.55		0.63		0.71		0.84		1.18	
		FO = 128		0.75		0.86		0.98		1.15		1.61	ns
t_P	Minimum Period	FO = 16	6.53		7.54		8.54		10.05		14.07		
		FO = 128	6.78		7.82		8.87		10.43		14.60		ns
f_{MAX}	Maximum Frequency	FO = 16		112.60		104.88		95.91		83.40		50.04	
		FO = 128		108.54		100.50		92.46		80.40		48.24	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A40MX02 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data-to-Pad HIGH		4.65		5.36		6.08		7.15		10.02	ns
t_{DHL}	Data-to-Pad LOW		5.58		6.44		7.29		8.58		12.01	ns
t_{ENZH}	Enable Pad Z to HIGH		5.23		6.04		6.84		8.05		11.27	ns
t_{ENZL}	Enable Pad Z to LOW		6.56		7.57		8.58		10.09		14.13	ns
t_{ENHZ}	Enable Pad HIGH to Z		11.08		12.79		14.49		17.05		23.87	ns
t_{ENLZ}	Enable Pad LOW to Z		8.21		9.47		10.73		12.63		17.68	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.03		0.04		0.04		0.06	ns/pF
d_{THL}	Delta HIGH to LOW		0.04		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data-to-Pad HIGH		5.51		6.35		7.20		8.47		11.86	ns
t_{DHL}	Data-to-Pad LOW		4.75		5.48		6.21		7.31		10.23	ns
t_{ENZH}	Enable Pad Z to HIGH		4.72		5.45		6.18		7.27		10.17	ns
t_{ENZL}	Enable Pad Z to LOW		6.83		7.89		8.94		10.51		14.72	ns
t_{ENHZ}	Enable Pad HIGH to Z		11.08		12.79		14.49		17.05		23.87	ns
t_{ENLZ}	Enable Pad LOW to Z		8.21		9.47		10.73		12.63		17.68	ns
d_{TLH}	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

Notes:

1. Delays based on 35 pF loading.

A40MX04 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75V, T_J = 70°C)

Logic Module Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.24		1.43		1.62		1.90		2.66	ns
t_{PD2}	Dual-Module Macros		2.25		3.06		3.47		4.08		5.71	ns
t_{CO}	Sequential Clock-to-Q		1.24		1.43		1.62		1.90		2.66	ns
t_{GO}	Latch G-to-Q		1.24		1.43		1.62		1.90		2.66	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.24		1.43		1.62		1.90		2.66	ns
Predicted Routing Delays[1]												
t_{RD1}	FO=1 Routing Delay		1.17		1.59		1.80		2.12		2.97	ns
t_{RD2}	FO=2 Routing Delay		1.90		2.19		2.48		2.92		4.09	ns
t_{RD3}	FO=3 Routing Delay		2.42		2.80		3.17		3.73		5.22	ns
t_{RD4}	FO=4 Routing Delay		2.94		3.40		3.85		4.53		6.34	ns
t_{RD8}	FO=8 Routing Delay		5.04		5.81		6.59		7.75		10.85	ns
Sequential Timing Characteristics												
t_{SUD}[2]	Flip-Flop (Latch) Data Input Set-Up	3.06		3.53		4.00		4.70		6.58		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	3.06		3.53		4.00		4.70		6.58		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.25		3.75		4.25		5.00		7.00		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.25		3.75		4.25		5.00		7.00		ns
t_A	Flip-Flop Clock Input Period	4.84		5.59		6.33		7.45		10.43		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		180.90		167.00		154.10		134.00		80.40	MHz

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
2. *Set-up times assume fanout of 3. Further testing information can be obtained from the DirectTime Analyzer utility.*
3. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Designer 3.0 or later DirectTime Analyzer to check the hold time for this macro.*

A40MX04 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			0.70		0.80		0.91		1.07		1.50	ns
t_{INYL}	Pad-to-Y LOW			0.62		0.71		0.81		0.95		1.33	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			2.07		2.39		2.17		3.19		4.47	ns
t_{IRD2}	FO=2 Routing Delay			2.59		2.99		3.39		3.99		5.59	ns
t_{IRD3}	FO=3 Routing Delay			3.12		3.60		4.08		4.80		6.72	ns
t_{IRD4}	FO=4 Routing Delay			3.64		4.20		4.76		5.60		7.84	ns
t_{IRD8}	FO=8 Routing Delay			5.73		6.62		7.50		8.82		12.35	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 16		4.58		5.29		5.99		7.05		9.87	
		FO = 128		4.58		5.29		5.99		7.05		9.87	ns
t_{CKL}	Input HIGH to LOW	FO = 16		4.84		5.59		6.33		7.45		10.43	
		FO = 128		4.84		5.59		6.33		7.45		10.43	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 16	2.24		2.58		2.92		3.44		4.82		
		FO = 128	2.35		2.71		3.07		3.61		5.05		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 16	2.24		2.58		2.92		3.44		4.82		
		FO = 128	2.35		2.71		3.07		3.61		5.05		ns
t_{CKSW}	Maximum Skew	FO = 16		0.39		0.45		0.51		0.60		0.84	
		FO = 128		0.53		0.62		0.70		0.82		1.15	ns
t_P	Minimum Period	FO = 16	4.69		5.39		6.10		7.18		10.05		
		FO = 128	4.84		5.59		6.33		7.45		10.43		ns
f_{MAX}	Maximum Frequency	FO = 16		187.68		174.79		159.85		139.00		83.40	
		FO = 128		180.90		167.50		154.10		134.00		80.40	MHz

Note:

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A40MX04 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data-to-Pad HIGH		3.32		3.83		4.34		5.11		7.15	ns
t_{DHL}	Data-to-Pad LOW		3.98		4.60		5.21		6.13		8.58	ns
t_{ENZH}	Enable Pad Z to HIGH		3.74		4.31		4.89		5.75		8.05	ns
t_{ENZL}	Enable Pad Z to LOW		4.69		5.41		6.13		7.21		10.09	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.92		9.14		10.35		12.18		17.05	ns
t_{ENLZ}	Enable Pad LOW to Z		5.86		6.77		7.67		9.02		12.63	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.02		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data-to-Pad HIGH		3.93		4.54		5.14		6.05		8.47	ns
t_{DHL}	Data-to-Pad LOW		3.39		3.92		4.44		5.22		7.31	ns
t_{ENZH}	Enable Pad Z to HIGH		3.37		3.89		4.41		5.19		7.27	ns
t_{ENZL}	Enable Pad Z to LOW		4.88		5.63		6.38		7.51		10.51	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.92		9.14		10.35		12.18		17.05	ns
t_{ENLZ}	Enable Pad LOW to Z		4.98		6.77		7.67		9.02		12.63	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

Notes:

1. Delays based on 35 pF loading.

A40MX04 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 3.0V, T_J = 70°C)

Logic Module Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.73		2.00		2.26		2.66		3.72	ns
t_{PD2}	Dual-Module Macros		3.71		4.28		4.86		5.71		8.00	ns
t_{CO}	Sequential Clock-to-Q		1.73		2.00		2.26		2.66		3.72	ns
t_{GO}	Latch G-to-Q		1.73		2.00		2.26		2.66		3.72	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.73		2.00		2.26		2.66		3.72	ns
Predicted Routing Delays[1]												
t_{RD1}	FO=1 Routing Delay		1.93		2.23		2.52		2.97		4.16	ns
t_{RD2}	FO=2 Routing Delay		2.66		3.07		3.47		4.09		5.72	ns
t_{RD3}	FO=3 Routing Delay		3.39		3.92		4.44		5.22		7.31	ns
t_{RD4}	FO=4 Routing Delay		4.12		4.76		5.39		6.34		8.88	ns
t_{RD8}	FO=8 Routing Delay		7.05		8.14		9.22		10.85		15.19	ns
Sequential Timing Characteristics[2]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	4.28		4.94		5.59		6.58		9.21		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	4.28		4.94		5.59		6.58		9.21		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.55		5.25		5.95		7.00		9.80		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.55		5.25		5.95		7.00		9.80		ns
t_A	Flip-Flop Clock Input Period	6.78		7.82		8.87		10.43		14.60		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		108.54		100.50		92.46		80.40		48.24	MHz

Notes:

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Set-up times assume fanout of 3. Further testing information can be obtained from the Direct Time Analyzer utility.*
4. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Designer 3.0 or later Direct Time Analyzer to check the hold time for this macro.*

A40MX04 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			0.97		1.12		1.27		1.50		2.10	ns
t_{INYL}	Pad-to-Y LOW			0.86		1.00		1.13		1.33		1.86	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			2.90		3.35		3.80		4.47		6.25	ns
t_{IRD2}	FO=2 Routing Delay			3.63		4.19		4.75		5.59		7.82	ns
t_{IRD3}	FO=3 Routing Delay			4.37		5.04		5.71		6.72		9.41	ns
t_{IRD4}	FO=4 Routing Delay			5.10		5.88		6.66		7.84		10.98	ns
t_{IRD8}	FO=8 Routing Delay			8.03		9.26		10.50		12.35		17.29	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 16		6.42		7.40		8.39		9.87		13.82	
		FO = 128		6.42		7.40		8.39		9.87		13.82	ns
t_{CKL}	Input HIGH to LOW	FO = 16		6.78		7.82		8.87		10.43		14.60	
		FO = 128		6.78		7.82		8.87		10.43		14.60	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 16	3.13		3.61		4.09		4.82		6.74		
		FO = 128	3.29		3.79		4.30		5.05		7.08		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 16	3.13		3.61		4.09		4.82		6.74		
		FO = 128	3.29		3.79		4.30		5.05		7.08		ns
t_{CKSW}	Maximum Skew	FO = 16		0.55		0.63		0.71		0.84		1.18	
		FO = 128		0.75		0.86		0.98		1.15		1.61	ns
t_P	Minimum Period	FO = 16	6.53		7.54		8.54		10.05		14.07		
		FO = 128	6.78		7.82		8.87		10.43		14.60		ns
f_{MAX}	Maximum Frequency	FO = 16		112.50		104.88		95.91		83.40		50.04	
		FO = 128		108.54		100.50		92.46		80.40		48.24	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A40MX04 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data-to-Pad HIGH		4.65		5.37		6.08		7.15		10.02	ns
t_{DHL}	Data-to-Pad LOW		5.58		6.44		7.29		8.58		12.01	ns
t_{ENZH}	Enable Pad Z to HIGH		5.23		6.04		6.84		8.05		11.27	ns
t_{ENZL}	Enable Pad Z to LOW		6.56		7.57		8.58		10.09		14.13	ns
t_{ENHZ}	Enable Pad HIGH to Z		11.08		12.79		14.49		17.05		23.87	ns
t_{ENLZ}	Enable Pad LOW to Z		8.21		9.47		10.73		12.63		17.68	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.03		0.04		0.04		0.06	ns/pF
d_{THL}	Delta HIGH to LOW		0.04		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data-to-Pad HIGH		5.51		6.35		7.20		8.47		11.86	ns
t_{DHL}	Data-to-Pad LOW		4.75		5.48		6.21		7.31		10.23	ns
t_{ENZH}	Enable Pad Z to HIGH		4.72		5.45		6.18		7.27		10.17	ns
t_{ENZL}	Enable Pad Z to LOW		6.83		7.89		8.94		10.51		14.72	ns
t_{ENHZ}	Enable Pad HIGH to Z		11.08		12.79		14.49		17.05		23.87	ns
t_{ENLZ}	Enable Pad LOW to Z		8.21		9.47		10.73		12.63		17.68	ns
d_{TLH}	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

Notes:

1. Delays based on 35 pF loading.

A42MX09 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75V, T_J = 70°C)

Logic Module Propagation Delays[1]		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.33		1.50		1.77		2.48	ns
t_{CO}	Sequential Clock-to-Q		1.43		1.62		1.91		2.67	ns
t_{GO}	Latch G-to-Q		1.37		1.55		1.82		2.55	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.58		1.79		2.10		2.94	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		0.77		0.87		1.02		1.43	ns
t_{RD2}	FO=2 Routing Delay		1.02		1.16		1.36		1.90	ns
t_{RD3}	FO=3 Routing Delay		1.28		1.45		1.70		2.38	ns
t_{RD4}	FO=4 Routing Delay		1.53		1.73		2.04		2.86	ns
t_{RD8}	FO=8 Routing Delay		2.60		2.90		3.41		4.77	ns
Sequential Timing Characteristics[3, 4]										
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.36		0.41		0.48		0.67		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.45		0.51		0.60		0.84		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.77		4.27		5.02		7.03		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.94		5.59		6.58		9.21		ns
t_A	Flip-Flop Clock Input Period	3.83		4.34		5.10		7.14		ns
t_{INH}	Input Buffer Latch Hold	0.00		0.00		0.00		0.00		ns
t_{INSU}	Input Buffer Latch Set-Up	0.30		0.40		0.40		0.60		ns
t_{OUTH}	Output Buffer Latch Hold	0.00		0.00		0.00		0.00		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.30		0.40		0.40		0.60		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		243.75		224.25		195.00		117.00	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX09 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			1.16		1.32		1.55		2.17	ns
t_{INYL}	Pad-to-Y LOW			0.90		1.02		1.20		1.68	ns
t_{INGH}	G to Y HIGH			1.43		1.62		1.90		2.66	ns
t_{INGL}	G to Y LOW			1.43		1.62		1.90		2.66	ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			2.24		2.54		2.99		4.19	ns
t_{IRD2}	FO=2 Routing Delay			2.51		2.85		3.35		4.69	ns
t_{IRD3}	FO=3 Routing Delay			2.78		3.15		3.71		5.19	ns
t_{IRD4}	FO=4 Routing Delay			3.05		3.46		4.07		5.70	ns
t_{IRD8}	FO=8 Routing Delay			4.13		4.68		5.50		7.70	ns
Global Clock Network											
t_{CKH}	Input LOW to HIGH	FO = 32		2.70		3.04		3.62		5.04	ns
		FO = 256		3.00		3.35		4.00		5.50	ns
t_{CKL}	Input HIGH to LOW	FO = 32		3.92		4.44		5.22		7.31	ns
		FO = 256		4.30		4.87		5.73		8.02	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	1.35		1.53		1.80		2.52		ns
		FO = 256	1.46		1.66		1.95		2.73		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	1.35		1.53		1.80		2.52		ns
		FO = 256	1.46		1.66		1.95		2.73		ns
t_{CKSW}	Maximum Skew	FO = 32		0.34		0.38		0.45		0.63	ns
		FO = 256		0.34		0.38		0.45		0.63	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.00		0.00		0.00		0.00		ns
		FO = 256	0.00		0.00		0.00		0.00		ns
t_{HEXT}	Input Latch External Hold	FO = 32	2.60		3.00		3.50		4.90		ns
		FO = 256	2.43		3.30		3.90		5.46		ns
t_P	Minimum Period	FO = 32	3.72		4.04		4.65		7.75		ns
		FO = 256	4.10		4.46		5.13		8.55		ns
f_{MAX}	Maximum Frequency	FO = 32		268.75		247.25		215.00		129.00	MHz
		FO = 256		243.75		224.25		195.00		117.00	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 3 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst case performance*

A42MX09 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		2.71		3.07		3.61		5.05	ns
t_{DHL}	Data-to-Pad LOW		3.19		3.61		4.25		5.95	ns
t_{ENZH}	Enable Pad Z to HIGH		2.93		3.32		3.90		5.46	ns
t_{ENZL}	Enable Pad Z to LOW		3.24		3.67		4.32		6.05	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.44		6.16		7.25		10.15	ns
t_{ENLZ}	Enable Pad LOW to Z		5.93		6.72		7.90		11.06	ns
t_{GLH}	G-to-Pad HIGH		2.90		3.30		3.78		5.30	ns
t_{GHL}	G-to-Pad LOW		2.90		3.30		3.78		5.30	ns
t_{LSU}	I/O Latch Set-Up	0.54		0.61		0.72		1.01		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.78		6.55		7.70		10.78	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.18		9.27		10.90		15.26	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.03		0.03		0.04		0.06	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.04		0.04		0.05		0.07	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		2.71		3.07		3.61		5.05	ns
t_{DHL}	Data-to-Pad LOW		3.19		3.61		4.25		5.95	ns
t_{ENZH}	Enable Pad Z to HIGH		2.93		3.32		3.90		5.46	ns
t_{ENZL}	Enable Pad Z to LOW		3.24		3.67		4.32		6.05	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.44		6.16		7.25		10.15	ns
t_{ENLZ}	Enable Pad LOW to Z		5.93		6.72		7.90		11.06	ns
t_{GLH}	G-to-Pad HIGH		4.61		5.22		6.14		8.60	ns
t_{GHL}	G-to-Pad LOW		4.61		5.22		6.14		8.60	ns
t_{LSU}	I/O Latch Set-Up	0.54		0.61		0.72		1.01		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.78		6.55		7.70		10.78	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.18		9.27		10.90		15.26	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.03		0.03		0.04		0.06	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. Delays based on 35 pF loading.

A42MX09 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 3.0V, T_J = 70°C)

Logic Module Propagation Delays[1]		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.80		2.13		2.50		3.47	ns
t_{CO}	Sequential Clock-to-Q		2.00		2.30		2.70		3.76	ns
t_{GO}	Latch G-to-Q		1.88		2.13		2.50		3.50	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		2.18		2.47		2.90		4.06	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.10		1.20		1.40		2.00	ns
t_{RD2}	FO=2 Routing Delay		1.40		1.60		1.90		2.67	ns
t_{RD3}	FO=3 Routing Delay		1.80		2.00		2.40		3.33	ns
t_{RD4}	FO=4 Routing Delay		2.10		2.40		2.90		4.00	ns
t_{RD8}	FO=8 Routing Delay		3.60		4.10		4.80		6.68	ns
Sequential Timing Characteristics[3, 4]										
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.50		0.57		0.67		0.94		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.63		0.71		0.84		1.18		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.27		5.97		7.03		9.84		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.91		7.83		9.21		12.90		ns
t_A	Flip-Flop Clock Input Period	5.60		6.20		7.10		9.94		ns
t_{INH}	Input Buffer Latch Hold	0.00		0.00		0.00		0.00		ns
t_{INSU}	Input Buffer Latch Set-Up	0.30		0.34		0.40		0.56		ns
t_{OUTH}	Output Buffer Latch Hold	0.00		0.00		0.00		0.00		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.30		0.34		0.40		0.56		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		146.30		134.60		117.00		70.20	MHz

Notes:

1. *For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX09 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			1.63		1.84		2.17		3.04	ns
t_{INYL}	Pad-to-Y LOW			1.30		1.40		1.70		2.40	ns
t_{INGH}	G to Y HIGH			2.00		2.30		2.70		3.72	ns
t_{INGL}	G to Y LOW			2.00		2.30		2.70		3.72	ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			3.15		3.57		4.20		5.86	ns
t_{IRD2}	FO=2 Routing Delay			3.50		4.00		4.70		6.57	ns
t_{IRD3}	FO=3 Routing Delay			3.90		4.40		5.20		7.27	ns
t_{IRD4}	FO=4 Routing Delay			4.30		4.85		5.70		7.98	ns
t_{IRD8}	FO=8 Routing Delay			5.80		6.55		7.70		10.78	ns
Global Clock Network											
t_{CKH}	Input LOW to HIGH	FO = 32		4.50		5.06		6.03		8.40	ns
		FO = 256		5.00		5.63		6.70		9.33	ns
t_{CKL}	Input HIGH to LOW	FO = 32		5.50		6.20		7.30		10.23	ns
		FO = 256		6.00		6.80		8.00		11.23	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	1.89		2.14		2.52		3.53		ns
		FO = 256	2.05		2.32		2.73		3.82		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	1.89		2.14		2.52		3.53		ns
		FO = 256	2.05		2.32		2.73		3.82		ns
t_{CKSW}	Maximum Skew	FO = 32		0.47		0.54		0.63		0.88	ns
		FO = 256		0.47		0.54		0.63		0.88	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.00		0.00		0.00		0.00		ns
		FO = 256	0.00		0.00		0.00		0.00		ns
t_{HEXT}	Input Latch External Hold	FO = 32	3.70		4.20		4.90		6.86		ns
		FO = 256	4.10		4.60		5.50		7.64		ns
t_P	Minimum Period	FO = 32	6.20		6.74		7.75		12.90		ns
		FO = 256	6.80		7.43		8.54		14.20		ns
f_{MAX}	Maximum Frequency	FO = 32		161.30		148.40		129.00		77.40	MHz
		FO = 256		146.30		134.60		117.00		70.20	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 3 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst case performance*

A42MX09 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		3.79		4.30		5.05		7.08	ns
t_{DHL}	Data-to-Pad LOW		4.46		5.06		5.95		8.33	ns
t_{ENZH}	Enable Pad Z to HIGH		4.10		4.64		5.46		7.64	ns
t_{ENZL}	Enable Pad Z to LOW		4.54		5.14		6.05		8.47	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.61		8.63		10.15		14.21	ns
t_{ENLZ}	Enable Pad LOW to Z		8.30		9.40		11.06		15.48	ns
t_{GLH}	G-to-Pad HIGH		6.45		7.31		8.60		12.03	ns
t_{GHL}	G-to-Pad LOW		6.45		7.31		8.60		12.03	ns
t_{LSU}	I/O Latch Set-Up	0.76		0.86		1.01		1.41		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		9.70		10.90		12.90		18.03	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		13.50		15.40		18.10		25.30	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.00		0.00		0.10		0.008	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.10		0.10		0.10		0.100	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		3.80		5.45		6.41		8.98	ns
t_{DHL}	Data-to-Pad LOW		4.50		4.22		4.97		6.96	ns
t_{ENZH}	Enable Pad Z to HIGH		4.10		4.64		5.46		7.64	ns
t_{ENZL}	Enable Pad Z to LOW		4.54		5.14		6.05		8.47	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.61		8.63		10.15		14.21	ns
t_{ENLZ}	Enable Pad LOW to Z		8.30		9.40		11.06		15.48	ns
t_{GLH}	G-to-Pad HIGH		6.45		7.31		8.60		12.03	ns
t_{GHL}	G-to-Pad LOW		6.45		7.31		8.60		12.03	ns
t_{LSU}	I/O Latch Set-Up	0.76		0.86		1.01		1.41		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		9.70		10.90		12.90		18.03	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		13.50		15.40		18.10		25.30	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.05		0.06		0.07		0.10	ns/pF

Notes:

1. Delays based on 35 pF loading.

A42MX16 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75V, T_J = 70°C)

Logic Module Propagation Delays[1]		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.52		1.73		2.03		2.84	ns
t_{CO}	Sequential Clock-to-Q		1.60		1.81		2.13		2.98	ns
t_{GO}	Latch G-to-Q		1.52		1.73		2.03		2.84	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.74		1.97		2.32		3.25	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		0.86		0.98		1.15		1.61	ns
t_{RD2}	FO=2 Routing Delay		1.15		1.30		1.53		2.14	ns
t_{RD3}	FO=3 Routing Delay		1.43		1.62		1.91		2.67	ns
t_{RD4}	FO=4 Routing Delay		1.72		1.95		2.29		3.21	ns
t_{RD8}	FO=8 Routing Delay		2.86		3.24		3.81		5.33	ns
Sequential Timing Characteristics[3,4]										
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.36		0.41		0.48		0.67		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.75		0.85		1.00		1.40		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.78		4.28		5.04		7.06		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.95		5.61		6.60		9.24		ns
t_A	Flip-Flop Clock Input Period	7.56		8.57		10.08		14.11		ns
t_{INH}	Input Buffer Latch Hold	0.00		0.00		0.00		0.00		ns
t_{INSU}	Input Buffer Latch Set-Up	0.54		0.61		0.72		1.01		ns
t_{OUTH}	Output Buffer Latch Hold	0.00		0.00		0.00		0.00		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.54		0.61		0.72		1.01		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		195.00		179.40		156.00		93.60	MHz

Notes:

1. *For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, point and position whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX16 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			1.17		1.33		1.56		2.18	ns
t_{INYL}	Pad-to-Y LOW			0.90		1.02		1.20		1.68	ns
t_{INGH}	G to Y HIGH			1.56		1.77		2.08		2.91	ns
t_{INGL}	G to Y LOW			1.56		1.77		2.08		2.91	ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			2.03		2.30		2.71		3.79	ns
t_{IRD2}	FO=2 Routing Delay			2.32		2.63		3.09		4.33	ns
t_{IRD3}	FO=3 Routing Delay			2.60		2.95		3.47		4.86	ns
t_{IRD4}	FO=4 Routing Delay			2.89		3.27		3.85		5.39	ns
t_{IRD8}	FO=8 Routing Delay			4.03		4.56		5.37		7.52	ns
Global Clock Network											
t_{CKH}	Input LOW to HIGH	FO = 32		2.90		3.27		3.90		5.42	ns
		FO = 384		3.20		3.60		4.28		5.96	ns
t_{CKL}	Input HIGH to LOW	FO = 32		4.20		4.76		5.60		7.84	ns
		FO = 384		4.95		5.61		6.60		9.24	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	3.53		4.00		4.70		6.58		ns
		FO = 384	4.05		4.59		5.40		7.56		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	3.53		4.00		4.70		6.58		ns
		FO = 384	4.05		4.59		5.40		7.56		ns
t_{CKSW}	Maximum Skew	FO = 32		0.38		0.43		0.50		0.70	ns
		FO = 384		0.38		0.43		0.50		0.70	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.00		0.00		0.00		0.00		ns
		FO = 384	0.00		0.00		0.00		0.00		ns
t_{HEXT}	Input Latch External Hold	FO = 32	3.08		5.49		4.10		5.74		ns
		FO = 384	3.53		4.00		4.70		6.58		ns
t_P	Minimum Period	FO = 32	4.65		5.06		5.81		9.69		ns
		FO = 384	5.12		5.57		6.41		10.68		ns
f_{MAX}	Maximum Frequency	FO = 32		215.00		197.80		172.00		103.20	MHz
		FO = 384		195.00		179.40		156.00		93.60	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A42MX16 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		2.79		3.16		3.72		5.21	ns
t_{DHL}	Data-to-Pad LOW		3.27		3.71		4.36		6.10	ns
t_{ENZH}	Enable Pad Z to HIGH		3.00		3.40		4.00		5.60	ns
t_{ENZL}	Enable Pad Z to LOW		3.32		3.76		4.42		6.19	ns
t_{ENHZ}	Enable Pad HIGH to Z		6.02		6.82		8.02		11.23	ns
t_{ENLZ}	Enable Pad LOW to Z		5.57		6.31		7.42		10.39	ns
t_{GLH}	G-to-Pad HIGH		3.20		3.60		4.30		6.00	ns
t_{GHL}	G-to-Pad LOW		3.20		3.60		4.30		6.00	ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		6.28		7.12		8.38		11.90	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.93		10.12		11.90		16.66	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.03		0.03		0.04		0.06	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.04		0.04		0.05		0.07	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		3.56		4.03		4.74		6.64	ns
t_{DHL}	Data-to-Pad LOW		2.73		3.09		3.64		5.10	ns
t_{ENZH}	Enable Pad Z to HIGH		3.00		3.40		4.00		5.60	ns
t_{ENZL}	Enable Pad Z to LOW		3.32		3.76		4.42		6.19	ns
t_{ENHZ}	Enable Pad HIGH to Z		6.02		6.82		8.02		11.23	ns
t_{ENLZ}	Enable Pad LOW to Z		5.57		6.31		7.42		10.39	ns
t_{GLH}	G-to-Pad HIGH		5.63		6.38		7.51		10.51	ns
t_{GHL}	G-to-Pad LOW		5.63		6.38		7.51		10.51	ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		6.28		7.12		8.38		11.90	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.93		10.12		11.90		16.66	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.03		0.03		0.04		0.06	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. Delays based on 35 pF loading.

A42MX16 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 3.0V, T_J = 70°C)

Logic Module Propagation Delays[1]		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		2.13		2.42		2.84		3.98	ns
t_{CO}	Sequential Clock-to-Q		2.24		2.53		2.98		4.17	ns
t_{GO}	Latch G-to-Q		2.13		2.42		2.84		3.98	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		2.44		2.76		3.25		4.55	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.21		1.37		1.61		2.25	ns
t_{RD2}	FO=2 Routing Delay		1.61		1.82		2.14		3.00	ns
t_{RD3}	FO=3 Routing Delay		2.01		2.27		2.67		3.74	ns
t_{RD4}	FO=4 Routing Delay		2.40		2.73		3.21		4.49	ns
t_{RD8}	FO=8 Routing Delay		4.00		4.53		5.33		7.47	ns
Sequential Timing Characteristics[3, 4]										
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.50		0.57		0.67		0.94		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.00		0.00		0.00		0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	1.05		1.19		1.40		1.96		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.29		6.00		7.06		9.88		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.93		7.85		9.24		12.94		ns
t_A	Flip-Flop Clock Input Period	10.58		12.00		14.11		19.76		ns
t_{INH}	Input Buffer Latch Hold	0.00		0.00		0.00		0.00		ns
t_{INSU}	Input Buffer Latch Set-Up	0.76		0.86		1.01		1.41		ns
t_{OUTH}	Output Buffer Latch Hold	0.00		0.00		0.00		0.00		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.76		0.86		1.01		1.41		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		117.00		107.64		93.60		56.16	MHz

Notes:

1. *For dual-module macros use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX16 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			1.64		1.86		2.18		3.06	ns
t_{INYL}	Pad-to-Y LOW			1.26		1.43		1.68		2.35	ns
t_{INGH}	G to Y HIGH			2.18		2.48		2.91		4.08	ns
t_{INGL}	G to Y LOW			2.18		2.48		2.91		4.08	ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			2.85		3.22		3.79		5.31	ns
t_{IRD2}	FO=2 Routing Delay			3.24		3.68		4.33		6.06	ns
t_{IRD3}	FO=3 Routing Delay			3.64		4.13		4.86		6.80	ns
t_{IRD4}	FO=4 Routing Delay			4.04		4.58		5.39		7.55	ns
t_{IRD8}	FO=8 Routing Delay			5.64		6.39		7.52		10.53	ns
Global Clock Network											
t_{CKH}	Input LOW to HIGH	FO = 32		4.83		5.45		6.50		9.03	ns
		FO = 384		5.33		6.00		7.13		9.93	ns
t_{CKL}	Input HIGH to LOW	FO = 32		5.88		6.66		7.84		10.98	ns
		FO = 384		6.93		7.85		9.24		12.94	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32	6.30		7.14		8.40		11.76		ns
		FO = 384	7.35		8.33		9.80		13.72		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32	5.88		6.66		7.84		10.98		ns
		FO = 384	6.93		7.85		9.24		12.94		ns
t_{CKSW}	Maximum Skew	FO = 32		0.53		0.60		0.70		0.98	ns
		FO = 384		2.42		2.74		3.22		4.51	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32	0.00		0.00		0.00		0.00		ns
		FO = 384	0.00		0.00		0.00		0.00		ns
t_{HEXT}	Input Latch External Hold	FO = 32	4.31		4.88		5.74		8.04		ns
		FO = 384	4.94		5.59		6.58		9.21		ns
t_P	Minimum Period	FO = 32	7.75		8.43		9.71		16.15		ns
		FO = 384	8.55		9.29		10.68		17.81		ns
f_{MAX}	Maximum Frequency	FO = 32		129.00		118.68		103.20		61.92	MHz
		FO = 384		117.00		107.64		93.60		56.16	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A42MX16 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		3.91		4.43		5.21		7.29	ns
t_{DHL}	Data-to-Pad LOW		4.58		5.19		6.10		8.55	ns
t_{ENZH}	Enable Pad Z to HIGH		4.20		4.76		5.60		7.84	ns
t_{ENZL}	Enable Pad Z to LOW		4.64		5.26		6.19		8.66	ns
t_{ENHZ}	Enable Pad HIGH to Z		8.42		9.54		11.23		15.72	ns
t_{ENLZ}	Enable Pad LOW to Z		7.79		8.83		10.39		14.54	ns
t_{GLH}	G-to-Pad HIGH		5.30		6.00		7.16		10.00	ns
t_{GHL}	G-to-Pad LOW		5.30		6.00		7.16		10.00	ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.93		10.12		11.90		16.66	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.50		14.16		16.66		23.32	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.05		0.06		0.07		0.10	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		4.98		5.64		6.64		9.29	ns
t_{DHL}	Data-to-Pad LOW		3.82		4.33		5.10		7.13	ns
t_{ENZH}	Enable Pad Z to HIGH		4.20		4.76		5.60		7.84	ns
t_{ENZL}	Enable Pad Z to LOW		4.64		5.26		6.19		8.66	ns
t_{ENHZ}	Enable Pad HIGH to Z		8.42		9.54		11.23		15.72	ns
t_{ENLZ}	Enable Pad LOW to Z		7.79		8.83		10.39		14.54	ns
t_{GLH}	G-to-Pad HIGH		7.89		8.94		10.51		14.72	ns
t_{GHL}	G-to-Pad LOW		7.89		8.94		10.51		14.72	ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.93		10.12		11.90		16.66	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.50		14.16		16.66		23.32	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.05		0.06		0.07		0.10	ns/pF

Notes:

1. Delays based on 35 pF loading.

A42MX24 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Logic Module Propagation Delays[1]		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Combinatorial Functions										
t_{PD}	Internal Array Module Delay		1.31		1.49		1.75		2.45	ns
t_{PDD}	Internal Decode Module Delay		1.59		1.80		2.12		2.97	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		0.89		1.01		1.19		1.67	ns
t_{RD2}	FO=2 Routing Delay		1.15		1.30		1.53		2.14	ns
t_{RD3}	FO=3 Routing Delay		1.40		1.59		1.87		2.62	ns
t_{RD4}	FO=4 Routing Delay		1.66		1.88		2.21		3.09	ns
t_{RD5}	FO=8 Routing Delay		2.67		3.03		3.56		4.98	ns
Sequential Timing Characteristics[3, 4]										
t_{CO}	Flip-Flop Clock-to-Output		1.43		1.62		1.90		2.66	ns
t_{GO}	Latch Gate-to-Output		1.31		1.49		1.75		2.45	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.35		0.40		0.47		0.66		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.00		0.00		0.00		0.00		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		1.55		1.76		2.07		2.90	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.45		0.51		0.60		0.84		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.68		4.17		4.91		6.87		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.83		5.47		6.44		9.02		ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX24 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

			Preliminary Information								
Input Module Propagation Delays			**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad-to-Y			1.14		1.29		1.52		2.13	ns
t_{INGO}	Input Latch Gate-to-Output			1.39		1.57		1.85		2.59	ns
t_{INH}	Input Latch Hold		0.00		0.00		0.00		0.00		ns
t_{INSU}	Input Latch Set-Up		0.53		0.60		0.70		0.98		ns
t_{ILA}	Latch Active Pulse Width		5.18		5.87		6.90		9.66		ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			2.03		2.30		2.71		3.79	ns
t_{IRD2}	FO=2 Routing Delay			2.29		2.59		3.05		4.27	ns
t_{IRD3}	FO=3 Routing Delay			2.54		2.88		3.39		4.75	ns
t_{IRD4}	FO=4 Routing Delay			2.80		3.17		3.73		5.22	ns
t_{IRD8}	FO=8 Routing Delay			3.81		4.32		5.08		7.11	ns
Global Clock Network											
t_{CKH}	Input LOW to HIGH	FO=32		2.90		3.27		3.90		5.42	ns
		FO=486		3.20		3.60		4.28		5.92	ns
t_{CKL}	Input HIGH to LOW	FO=32		4.05		4.59		5.40		7.56	ns
		FO=486		4.73		5.36		6.30		8.82	ns
t_{PWH}	Minimum Pulse Width HIGH	FO=32	2.40		2.72		3.20		4.48		ns
		FO=486	2.63		2.98		3.50		4.90		ns
t_{PWL}	Minimum Pulse Width LOW	FO=32	2.40		2.72		3.20		4.48		ns
		FO=486	2.63		2.98		3.50		4.90		ns
t_{CKSW}	Maximum Skew	FO=32		0.60		0.68		0.80		1.12	ns
		FO=486		0.60		0.68		0.80		1.12	ns
t_{SUEXT}	Input Latch External Set-Up	FO=32	0.00		0.00		0.00		0.00		ns
		FO=486	0.00		0.00		0.00		0.00		ns
t_{HEXT}	Input Latch External Hold	FO=32	3.08		3.49		4.10		5.74		ns
		FO=486	3.68		4.17		4.90		6.86		ns
t_P	Minimum Period ($1/f_{MAX}$)	FO=32	5.23		5.68		6.50		10.89		ns
		FO=486	5.71		6.21		7.14		11.90		ns
f_{MAX}	Maximum Datapath Frequency	FO=32		191.25		175.95		153.00		91.80	MHz
		FO=486		175.00		161.00		140.00		84.00	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

A42MX24 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Output Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		2.70		3.06		3.60		5.04	ns
t_{DHL}	Data-to-Pad LOW		3.15		3.57		4.20		5.88	ns
t_{ENZH}	Enable Pad Z to HIGH		2.82		3.20		3.76		5.26	ns
t_{ENZL}	Enable Pad Z to LOW		3.13		3.54		4.17		5.84	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.72		6.48		7.62		10.67	ns
t_{ENLZ}	Enable Pad LOW to Z		5.33		6.04		7.10		9.94	ns
t_{GLH}	G-to-Pad HIGH		3.20		3.60		4.30		6.00	ns
t_{GHL}	G-to-Pad LOW		3.20		3.60		4.30		6.00	ns
t_{LSU}	I/O Latch Output Set-Up	0.53		0.60		0.70		0.98		ns
t_{LH}	I/O Latch Output Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		6.08		6.89		8.10		11.34	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		11.78		13.35		15.70		21.98	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		3.45		3.91		4.60		6.44	ns
t_{DHL}	Data-to-Pad LOW		2.61		2.96		3.48		4.87	ns
t_{ENZH}	Enable Pad Z to HIGH		2.82		3.20		3.76		5.26	ns
t_{ENZL}	Enable Pad Z to LOW		3.13		3.54		4.17		5.84	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.72		6.48		7.62		10.67	ns
t_{ENLZ}	Enable Pad LOW to Z		5.33		6.04		7.10		9.94	ns
t_{GLH}	G-to-Pad HIGH		5.42		6.15		7.23		10.12	ns
t_{GHL}	G-to-Pad LOW		5.42		6.15		7.23		10.12	ns
t_{LSU}	I/O Latch Set-Up	0.53		0.60		0.70		0.98		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		6.08		6.89		8.10		11.34	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		11.78		13.35		15.70		21.98	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.03		0.03		0.04		0.06	ns/pF

Notes:

1. Delays based on 35 pF loading.

A42MX24 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Logic Module Propagation Delays[1]		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Combinatorial Functions										
t_{PD}	Internal Array Module Delay		1.84		2.08		2.45		3.43	ns
t_{PDD}	Internal Decode Module Delay		2.23		2.52		2.97		4.16	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.25		1.42		1.67		2.33	ns
t_{RD2}	FO=2 Routing Delay		1.61		1.82		2.14		3.00	ns
t_{RD3}	FO=3 Routing Delay		1.96		2.23		2.62		3.67	ns
t_{RD4}	FO=4 Routing Delay		2.32		2.63		3.09		4.33	ns
t_{RD5}	FO=8 Routing Delay		3.74		4.24		4.98		6.98	ns
Sequential Timing Characteristics[3, 4]										
t_{CO}	Flip-Flop Clock-to-Output		2.00		2.26		2.66		3.72	ns
t_{GO}	Latch Gate-to-Output		1.84		2.08		2.45		3.43	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.49		0.56		0.66		0.92		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.00		0.00		0.00		0.00		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		2.17		2.46		2.90		4.06	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.63		0.71		0.84		1.18		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.16		5.84		6.87		9.62		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.76		7.66		9.02		12.62		ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX24 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

			Preliminary Information								
Input Module Propagation Delays			**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad-to-Y			1.60		1.81		2.13		2.98	ns
t_{INGO}	Input Latch Gate-to-Output			1.94		2.20		2.59		3.63	ns
t_{INH}	Input Latch Hold		0.00		0.00		0.00		0.00		ns
t_{INSU}	Input Latch Set-Up		0.74		0.83		0.98		1.37		ns
t_{ILA}	Latch Active Pulse Width		7.25		8.21		9.66		13.52		ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			2.85		3.22		3.79		5.31	ns
t_{IRD2}	FO=2 Routing Delay			3.20		3.63		4.27		5.98	ns
t_{IRD3}	FO=3 Routing Delay			3.56		4.03		4.75		6.64	ns
t_{IRD4}	FO=4 Routing Delay			3.92		4.44		5.22		7.31	ns
t_{IRD8}	FO=8 Routing Delay			5.33		6.05		7.11		9.96	ns
Global Clock Network											
t_{CKH}	Input LOW to HIGH	FO=32		4.83		5.45		6.50		9.03	ns
		FO=486		5.33		6.00		7.13		9.93	ns
t_{CKL}	Input HIGH to LOW	FO=32		5.67		6.43		7.56		10.58	ns
		FO=486		6.62		7.50		8.82		12.35	ns
t_{PWH}	Minimum Pulse Width HIGH	FO=32	3.36		3.81		4.48		6.27		ns
		FO=486	3.68		4.17		4.90		6.86		ns
t_{PWL}	Minimum Pulse Width LOW	FO=32	3.36		3.81		4.48		6.27		ns
		FO=486	3.68		4.17		4.90		6.86		ns
t_{CKSW}	Maximum Skew	FO=32		0.84		0.95		1.12		1.57	ns
		FO=486		0.84		0.95		1.12		1.57	ns
t_{SUEXT}	Input Latch External Set-Up	FO=32	0.00		0.00		0.00		0.00		ns
		FO=486	0.00		0.00		0.00		0.00		ns
t_{HEXT}	Input Latch External Hold	FO=32	4.31		4.88		5.74		8.04		ns
		FO=486	5.15		5.83		6.86		9.60		ns
t_P	Minimum Period ($1/f_{MAX}$)	FO=32	8.71		9.47		10.80		18.15		ns
		FO=486	9.52		10.35		11.90		19.84		ns
f_{MAX}	Maximum Datapath Frequency	FO=32		114.75		105.57		91.80		55.08	MHz
		FO=486		105.00		96.60		84.00		50.40	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

A42MX24 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Output Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		3.78		4.28		5.04		7.06	ns
t_{DHL}	Data-to-Pad LOW		4.41		5.00		5.88		8.23	ns
t_{ENZH}	Enable Pad Z to HIGH		3.95		4.47		5.26		7.37	ns
t_{ENZL}	Enable Pad Z to LOW		4.38		4.96		5.84		8.17	ns
t_{ENHZ}	Enable Pad HIGH to Z		8.00		9.07		10.67		14.94	ns
t_{ENLZ}	Enable Pad LOW to Z		7.46		8.45		9.94		13.92	ns
t_{GLH}	G-to-Pad HIGH		5.30		6.00		7.16		10.00	ns
t_{GHL}	G-to-Pad LOW		5.30		6.00		7.16		10.00	ns
t_{LSU}	I/O Latch Output Set-Up	0.74		0.83		0.98		1.37		ns
t_{LH}	I/O Latch Output Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		8.51		9.64		11.34		15.88	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		16.49		18.68		21.98		30.77	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		5.32		5.47		6.44		9.02	ns
t_{DHL}	Data-to-Pad LOW		3.90		4.14		4.87		6.82	ns
t_{ENZH}	Enable Pad Z to HIGH		3.95		4.47		5.26		7.37	ns
t_{ENZL}	Enable Pad Z to LOW		3.75		4.96		5.84		8.17	ns
t_{ENHZ}	Enable Pad HIGH to Z		8.00		9.07		10.67		14.94	ns
t_{ENLZ}	Enable Pad LOW to Z		7.46		8.45		9.94		13.92	ns
t_{GLH}	G-to-Pad HIGH		7.59		8.60		10.12		14.17	ns
t_{GHL}	G-to-Pad LOW		7.59		8.60		10.12		14.17	ns
t_{LSU}	I/O Latch Set-Up	0.74		0.83		0.98		1.37		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		8.51		9.64		11.34		15.88	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		16.49		18.68		21.98		30.77	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.04		0.05		0.06		0.08	ns/pF

Notes:

1. Delays based on 35 pF loading.

A42MX36 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Logic Module Propagation Delays		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Combinatorial Functions										
t_{PD}	Internal Array Module Delay		1.46		1.66		1.95		2.73	ns
t_{PDD}	Internal Decode Module Delay		1.78		2.01		2.37		3.32	ns
Predicted Module Routing Delays										
t_{RD1}	FO=1 Routing Delay		1.04		1.18		1.39		1.95	ns
t_{RD2}	FO=2 Routing Delay		1.42		1.61		1.89		2.65	ns
t_{RD3}	FO=3 Routing Delay		1.79		2.03		2.39		3.35	ns
t_{RD4}	FO=4 Routing Delay		2.18		2.47		2.90		4.06	ns
t_{RD5}	FO=8 Routing Delay		3.68		4.17		4.91		6.87	ns
t_{RDD}	Decode-to-Output Routing Delay		0.38		0.43		0.50		0.70	ns
Sequential Timing Characteristics										
t_{CO}	Flip-Flop Clock-to-Output		1.43		1.62		1.90		2.66	ns
t_{GO}	Latch Gate-to-Output		1.43		1.62		1.90		2.66	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.35		0.40		0.47		0.66		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.00		0.00		0.00		0.00		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		1.73		1.96		2.31		3.23	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.75		0.85		1.00		1.40		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.68		4.17		4.91		6.87		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.83		5.47		6.44		9.02		ns

A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Logic Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations										
t_{RC}	Read Cycle Time	7.50		8.50		10.00		14.00		ns
t_{WC}	Write Cycle Time	7.50		8.50		10.00		14.00		ns
t_{RCKHL}	Clock HIGH/LOW Time	3.75		4.25		5.00		7.00		ns
t_{RCO}	Data Valid After Clock HIGH/LOW		3.75		4.25		5.00		7.00	ns
t_{ADSU}	Address/Data Set-Up Time	1.80		2.04		2.40		3.36		ns
t_{ADH}	Address/Data Hold Time	0.00		0.00		0.00		0.00		ns
t_{RENSU}	Read Enable Set-Up	0.68		0.77		0.90		1.26		ns
t_{RENH}	Read Enable Hold	3.75		4.25		5.00		7.00		ns
t_{WENSU}	Write Enable Set-Up	3.00		3.40		4.00		5.60		ns
t_{WENH}	Write Enable Hold	0.00		0.00		0.00		0.00		ns
t_{BENS}	Block Enable Set-Up	3.08		3.49		4.10		5.74		ns
t_{BENH}	Block Enable Hold	0.00		0.00		0.00		0.00		ns
Asynchronous SRAM Operations										
t_{RPD}	Asynchronous Access Time		9.00		10.20		12.00		16.80	ns
t_{RDADV}	Read Address Valid	9.75		11.10		13.00		18.20		ns
t_{ADSU}	Address/Data Set-Up Time	1.80		2.04		2.40		3.36		ns
t_{ADH}	Address/Data Hold Time	0.00		0.00		0.00		0.00		ns
t_{RENSUA}	Read Enable Set-Up to Address Valid	0.68		0.77		0.90		1.26		ns
t_{RENHA}	Read Enable Hold	3.75		4.25		5.00		7.00		ns
t_{WENSU}	Write Enable Set-Up	3.00		3.40		4.00		5.60		ns
t_{WENH}	Write Enable Hold	0.00		0.00		0.00		0.00		ns
t_{DOH}	Data Out Hold Time		1.35		1.53		1.80		2.52	ns

A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

			Advanced Information								
Input Module Propagation Delays			**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad-to-Y			1.14		1.29		1.52		2.13	ns
t_{INGO}	Input Latch Gate-to-Output[1]			1.55		1.76		2.07		2.90	ns
t_{INH}	Input Latch Hold[1]		0.00		0.00		0.00		0.00		ns
t_{INSU}	Input Latch Set-Up[1]		0.53		0.60		0.70		0.98		ns
t_{ILA}	Latch Active Pulse Width[1]		5.18		5.87		6.90		9.66		ns
Input Module Predicted Routing Delays											
t_{IRD1}	FO=1 Routing Delay			2.18		2.47		2.91		4.07	ns
t_{IRD2}	FO=2 Routing Delay			2.56		2.90		3.41		4.77	ns
t_{IRD3}	FO=3 Routing Delay			2.93		3.32		3.91		5.47	ns
t_{IRD4}	FO=4 Routing Delay			3.32		3.76		4.42		6.19	ns
t_{IRD8}	FO=8 Routing Delay			4.82		5.47		6.43		9.00	ns
Global Clock Network											
t_{CKH}	Input LOW to HIGH	FO=32		3.03		3.42		4.02		5.63	ns
		FO=635		3.33		3.76		4.43		6.20	ns
t_{CKL}	Input HIGH to LOW	FO=32		4.20		4.76		5.60		7.81	ns
		FO=635		5.40		6.12		7.20		10.08	ns
t_{PWH}	Minimum Pulse Width HIGH	FO=32	1.95		2.21		2.60		3.64		ns
		FO=635	2.18		2.47		2.90		4.06		ns
t_{PWL}	Minimum Pulse Width LOW	FO=32	1.95		2.21		2.60		3.64		ns
		FO=635	2.18		2.47		2.90		4.06		ns
t_{CKSW}	Maximum Skew	FO=32		0.83		0.94		1.00		1.40	ns
		FO=635		0.83		0.94		1.00		1.40	ns
t_{SUEXT}	Input Latch External Set-Up	FO=32	0.00		0.00		0.00		0.00		ns
		FO=635	0.00		0.00		0.00		0.00		ns
t_{HEXT}	Input Latch External Hold	FO=32	3.15		3.57		4.20		5.88		ns
		FO=635	3.68		4.17		4.90		6.86		ns
t_P	Minimum Period ($1/f_{MAX}$)	FO=32	6.10		6.64		7.63		12.72		ns
		FO=635	6.61		7.19		8.26		13.77		ns
f_{HMAX}	Maximum Datapath Frequency	FO=32		163.75		150.65		131.00		78.60	MHz
		FO=635		151.25		139.15		121.00		72.60	MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

		Advanced Information								
Output Module Timing		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		2.84		3.21		3.78		5.29	ns
t_{DHL}	Data-to-Pad LOW		3.29		3.73		4.39		6.15	ns
t_{ENZH}	Enable Pad Z to HIGH		2.95		3.34		3.93		5.50	ns
t_{ENZL}	Enable Pad Z to LOW		3.26		3.69		4.34		6.08	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.84		6.62		7.79		10.91	ns
t_{ENLZ}	Enable Pad LOW to Z		5.45		6.18		7.27		10.18	ns
t_{GLH}	G-to-Pad HIGH		3.27		3.70		4.35		6.09	ns
t_{GHL}	G-to-Pad LOW		3.27		3.70		4.35		6.09	ns
t_{LSU}	I/O Latch Output Set-Up	0.53		0.60		0.70		0.98		ns
t_{LH}	I/O Latch Output Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		6.30		7.14		8.40		11.76	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		8.63		9.78		11.50		16.10	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.08		0.09		0.10		0.14	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.08		0.09		0.10		0.14	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		3.92		4.45		5.23		7.32	ns
t_{DHL}	Data-to-Pad LOW		2.73		3.09		3.64		5.10	ns
t_{ENZH}	Enable Pad Z to HIGH		2.95		3.34		3.93		5.50	ns
t_{ENZL}	Enable Pad Z to LOW		3.26		3.69		4.34		6.08	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.84		6.62		7.79		10.91	ns
t_{ENLZ}	Enable Pad LOW to Z		5.45		6.18		7.27		10.19	ns
t_{GLH}	G-to-Pad HIGH		5.59		6.33		7.45		10.43	ns
t_{GHL}	G-to-Pad LOW		5.59		6.33		7.45		10.43	ns
t_{LSU}	I/O Latch Set-Up	0.53		0.60		0.70		0.98		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		6.30		7.14		8.40		11.76	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		8.63		9.78		11.50		16.10	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.08		0.09		0.10		0.14	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.08		0.09		0.10		0.14	ns/pF

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

A42MX36 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Logic Module Propagation Delays		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Combinatorial Functions										
t_{PD}	Internal Array Module Delay		2.05		2.32		2.73		3.82	ns
t_{PDD}	Internal Decode Module Delay		2.49		2.82		3.32		4.65	ns
Predicted Module Routing Delays										
t_{RD1}	FO=1 Routing Delay		1.46		1.65		1.95		2.72	ns
t_{RD2}	FO=2 Routing Delay		1.98		2.25		2.65		3.70	ns
t_{RD3}	FO=3 Routing Delay		2.51		2.84		3.35		4.68	ns
t_{RD4}	FO=4 Routing Delay		3.05		3.45		4.06		5.68	ns
t_{RD5}	FO=8 Routing Delay		5.16		5.84		6.87		9.62	ns
t_{RDD}	Decode-to-Output Routing Delay		0.53		0.60		0.70		0.98	ns
Sequential Timing Characteristics										
t_{CO}	Flip-Flop Clock-to-Output		2.00		2.26		2.66		3.72	ns
t_{GO}	Latch Gate-to-Output		2.00		2.26		2.66		3.72	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.49		0.56		0.66		0.92		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.00		0.00		0.00		0.00		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		2.43		2.75		3.23		4.53	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	1.05		1.19		1.40		1.96		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		0.00		0.00		0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.16		5.84		6.87		9.62		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.76		7.66		9.02		12.62		ns

A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information								
Logic Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations										
t_{RC}	Read Cycle Time	10.50		11.90		14.00		19.60		ns
t_{WC}	Write Cycle Time	10.50		11.90		14.00		19.60		ns
t_{RCKHL}	Clock HIGH/LOW Time	5.30		6.00		7.00		9.80		ns
t_{RCO}	Data Valid After Clock HIGH/LOW		5.30		6.00		7.00		9.80	ns
t_{ADSU}	Address/Data Set-Up Time	2.50		2.80		3.40		4.80		ns
t_{ADH}	Address/Data Hold Time	0.00		0.00		0.00		0.00		ns
t_{RENSU}	Read Enable Set-Up	12.00		1.10		1.30		1.80		ns
t_{RENH}	Read Enable Hold	5.30		6.00		7.00		9.80		ns
t_{WENSU}	Write Enable Set-Up	4.20		4.80		5.60		7.80		ns
t_{WENH}	Write Enable Hold	0.00		0.00		0.00		0.00		ns
t_{BENS}	Block Enable Set-Up	4.30		4.90		5.70		8.00		ns
t_{BENH}	Block Enable Hold	0.00		0.00		0.00		0.00		ns
Asynchronous SRAM Operations										
t_{RPD}	Asynchronous Access Time		12.60		14.30		16.80		23.50	ns
t_{RDADV}	Read Address Valid	13.70		15.50		18.20		25.50		ns
t_{ADSU}	Address/Data Set-Up Time	2.50		2.80		3.40		4.76		ns
t_{ADH}	Address/Data Hold Time	0.00		0.00		0.00		0.00		ns
t_{RENSUA}	Read Enable Set-Up to Address Valid	1.00		1.10		1.30		1.80		ns
t_{RENHA}	Read Enable Hold	5.30		6.00		7.00		9.80		ns
t_{WENSU}	Write Enable Set-Up	4.20		4.80		5.60		7.80		ns
t_{WENH}	Write Enable Hold	0.00		0.00		0.00		0.00		ns
t_{DOH}	Data Out Hold Time		2.00		2.10		2.50		3.50	ns

A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

			Preliminary Information								
Input Module Propagation Delays			**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad-to-Y			1.60		1.81		2.13		2.98	ns
t_{INGO}	Input Latch Gate-to-Output[1]			2.17		2.46		2.90		4.06	ns
t_{INH}	Input Latch Hold[1]		0.00		0.00		0.00		0.00		ns
t_{INSU}	Input Latch Set-Up[1]		0.74		0.83		0.98		1.37		ns
t_{ILA}	Latch Active Pulse Width[1]		7.25		8.21		9.66		13.52		ns
Input Module Predicted Routing Delays											
t_{IRD1}	FO=1 Routing Delay			3.06		3.46		4.07		5.70	ns
t_{IRD2}	FO=2 Routing Delay			3.58		4.06		4.77		6.68	ns
t_{IRD3}	FO=3 Routing Delay			4.11		4.65		5.47		7.66	ns
t_{IRD4}	FO=4 Routing Delay			4.64		5.26		6.19		8.66	ns
t_{IRD8}	FO=8 Routing Delay			6.75		7.65		9.00		12.60	ns
Global Clock Network											
t_{CKH}	Input LOW to HIGH	FO=32		5.05		5.70		6.70		9.38	ns
		FO=635		5.55		6.26		7.40		10.33	ns
t_{CKL}	Input HIGH to LOW	FO=32		5.88		6.66		7.84		10.98	ns
		FO=635		7.56		8.57		10.08		14.11	ns
t_{PWH}	Minimum Pulse Width HIGH	FO=32	2.73		3.09		3.64		5.10		ns
		FO=635	3.05		3.45		4.06		5.68		ns
t_{PWL}	Minimum Pulse Width LOW	FO=32	2.73		3.09		3.64		5.10		ns
		FO=635	3.05		3.45		4.06		5.68		ns
t_{CKSW}	Maximum Skew	FO=32		1.16		1.31		1.54		2.16	ns
		FO=635		1.16		1.31		1.54		2.16	ns
t_{SUEXT}	Input Latch External Set-Up	FO=32	0.00		0.00		0.00		0.00		ns
		FO=635	0.00		0.00		0.00		0.00		ns
t_{HEXT}	Input Latch External Hold	FO=32	4.41		5.00		5.88		8.23		ns
		FO=635	5.15		5.83		6.86		9.60		ns
t_P	Minimum Period ($1/f_{MAX}$)	FO=32	10.18		11.06		12.70		21.20		ns
		FO=635	11.02		11.98		13.77		22.96		ns
f_{HMAX}	Maximum Datapath Frequency	FO=32		98.25		90.39		78.60		47.16	MHz
		FO=635		90.75		83.49		72.60		43.56	MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

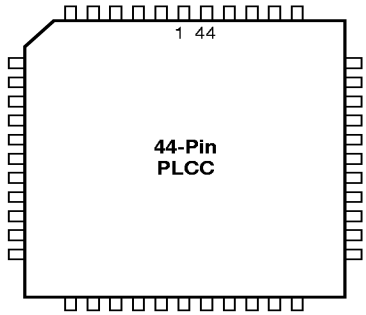
		Preliminary Information								
Output Module Timing		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		3.97		4.50		5.29		7.41	ns
t_{DHL}	Data-to-Pad LOW		4.61		5.22		6.15		8.60	ns
t_{ENZH}	Enable Pad Z to HIGH		4.13		4.68		5.50		7.70	ns
t_{ENZL}	Enable Pad Z to LOW		4.56		5.16		6.08		8.51	ns
t_{ENHZ}	Enable Pad HIGH to Z		8.18		9.27		10.91		15.27	ns
t_{ENLZ}	Enable Pad LOW to Z		7.63		8.65		10.18		14.25	ns
t_{GLH}	G-to-Pad HIGH		5.45		6.16		7.25		10.15	ns
t_{GHL}	G-to-Pad LOW		5.45		6.16		7.25		10.15	ns
t_{LSU}	I/O Latch Output Set-Up	0.74		0.83		0.98		1.37		ns
t_{LH}	I/O Latch Output Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		8.82		10.00		11.76		16.46	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		12.08		13.69		16.10		22.54	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.11		0.12		0.14		0.20	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.11		0.12		0.14		0.20	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data-to-Pad HIGH		5.49		6.22		7.32		10.25	ns
t_{DHL}	Data-to-Pad LOW		3.82		4.33		5.10		7.13	ns
t_{ENZH}	Enable Pad Z to HIGH		4.13		4.68		5.50		7.70	ns
t_{ENZL}	Enable Pad Z to LOW		4.56		5.16		6.08		8.51	ns
t_{ENHZ}	Enable Pad HIGH to Z		8.18		9.27		10.91		15.27	ns
t_{ENLZ}	Enable Pad LOW to Z		7.63		8.65		10.18		14.25	ns
t_{GLH}	G-to-Pad HIGH		7.82		8.87		10.43		14.60	ns
t_{GHL}	G-to-Pad LOW		7.82		8.87		10.43		14.60	ns
t_{LSU}	I/O Latch Set-Up	0.74		0.83		0.98		1.37		ns
t_{LH}	I/O Latch Hold	0.00		0.00		0.00		0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		8.82		10.00		11.76		16.46	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		12.08		13.69		16.10		22.54	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.11		0.12		0.14		0.20	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.11		0.12		0.14		0.20	ns/pF

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

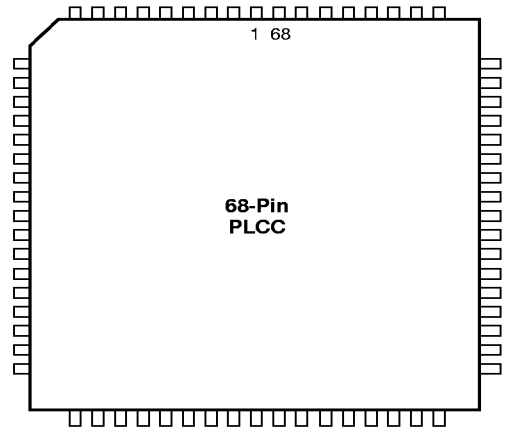
Package Pin Assignments

44-Pin PLCC



Signal	A40MX02 Function	A40MX04 Function
3	V_{CC}	V_{CC}
10	GND	GND
14	V_{CC}	V_{CC}
16	V_{CC}	V_{CC}
21	GND	GND
25	V_{CC}	V_{CC}
32	GND	GND
33	CLK, I/O	CLK, I/O
34	MODE	MODE
35	V_{CC}	V_{CC}
36	SDI, I/O	SDI, I/O
37	DCLK, I/O	DCLK, I/O
38	PRA, I/O	PRA, I/O
39	PRB, I/O	PRB, I/O
43	GND	GND

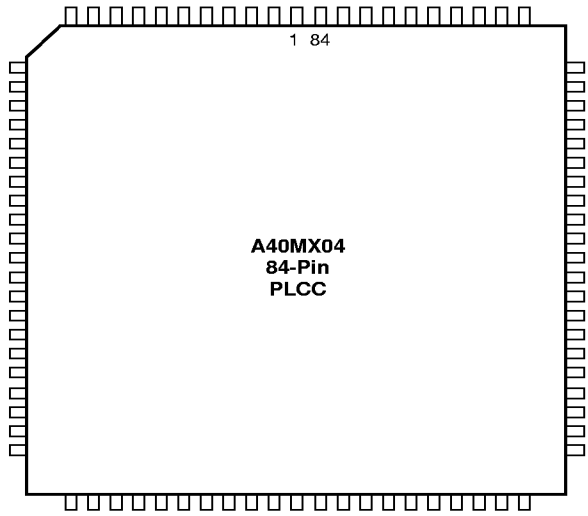
68-Pin PLCC



Signal	A40MX02 Function	A40MX04 Function
4	V_{CC}	V_{CC}
14	GND	GND
15	GND	GND
21	V_{CC}	V_{CC}
25	V_{CC}	V_{CC}
32	GND	GND
38	V_{CC}	V_{CC}
49	GND	GND
52	CLK, I/O	CLK, I/O
54	MODE	MODE
55	V_{CC}	V_{CC}
56	SDI, I/O	SDI, I/O
57	DCLK, I/O	DCLK, I/O
58	PRA, I/O	PRA, I/O
59	PRB, I/O	PRB, I/O
66	GND	GND

Package Pin Assignments (continued)

84-Pin PLCC



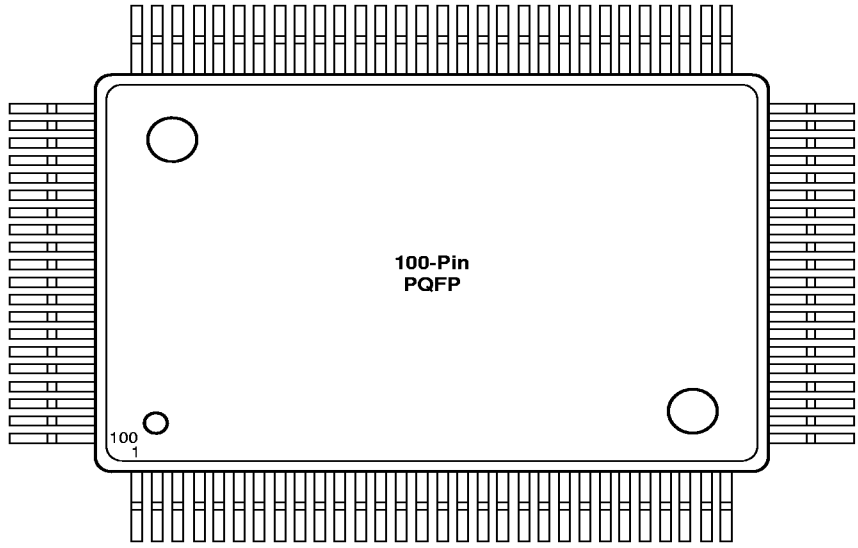
Signal	A40MX04 Function
4	V_{CC}
12	NC
18	GND
19	GND
25	V_{CC}
26	V_{CC}
33	V_{CC}
40	GND
46	V_{CC}
60	GND
61	GND
64	CLK, I/O
66	MODE
67	V_{CC}
68	V_{CC}
72	SDI, I/O
73	DCLK, I/O
74	PRA, I/O
75	PRB, I/O
82	GND

Notes:

1. *NC: Denotes 'No Connection'.*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Package Pin Assignments (continued)

100-Pin PQFP



Pin	A40MX02 Function	A40MX04 Function
1	NC	NC
2	NC	NC
3	NC	NC
4	NC	NC
5	NC	NC
6	PRB, I/O	PRB, I/O
13	GND	GND
19	V_{CC}	V_{CC}
27	NC	NC
28	NC	NC
29	NC	NC
30	NC	NC
31	NC	I/O
32	NC	I/O
33	NC	I/O
36	GND	GND
37	GND	GND
43	V_{CC}	V_{CC}
44	V_{CC}	V_{CC}
48	NC	I/O
49	NC	I/O
50	NC	I/O
51	NC	NC
52	NC	NC

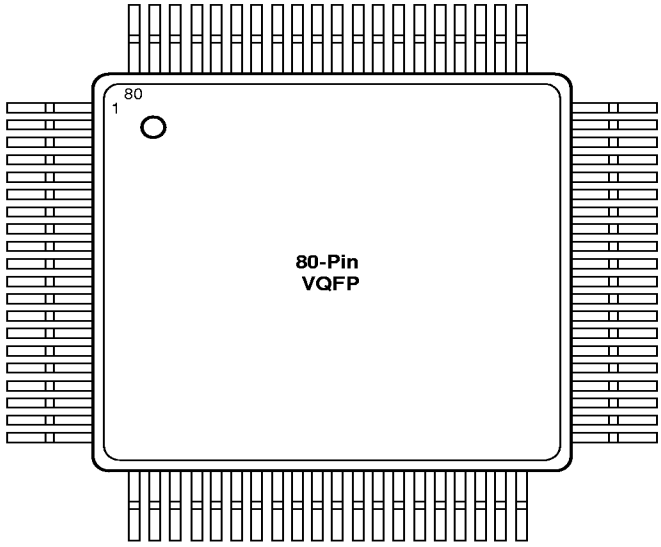
Pin	A40MX02 Function	A40MX04 Function
53	NC	NC
54	NC	NC
55	NC	NC
56	V_{CC}	V_{CC}
63	GND	GND
69	V_{CC}	V_{CC}
77	NC	NC
78	NC	NC
79	NC	NC
80	NC	I/O
81	NC	I/O
82	NC	I/O
86	GND	GND
87	GND	GND
90	CLK, I/O	CLK, I/O
92	MODE	MODE
93	V_{CC}	V_{CC}
94	V_{CC}	V_{CC}
95	NC	I/O
96	NC	I/O
97	NC	I/O
98	SDI, I/O	SDI, I/O
99	DCLK, I/O	DCLK, I/O
100	PRA, I/O	PRA, I/O

Notes:

1. *NC: Denotes 'No Connection'.*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Package Pin Assignments (continued)

80-Pin VQFP



Pin	A40MX02 Function	A40MX04 Function
2	NC	I/O
3	NC	I/O
4	NC	I/O
7	GND	GND
13	V_{CC}	V_{CC}
17	NC	I/O
18	NC	I/O
19	NC	I/O
20	V_{CC}	V_{CC}
27	GND	GND
33	V_{CC}	V_{CC}
41	NC	I/O
42	NC	I/O
43	NC	I/O

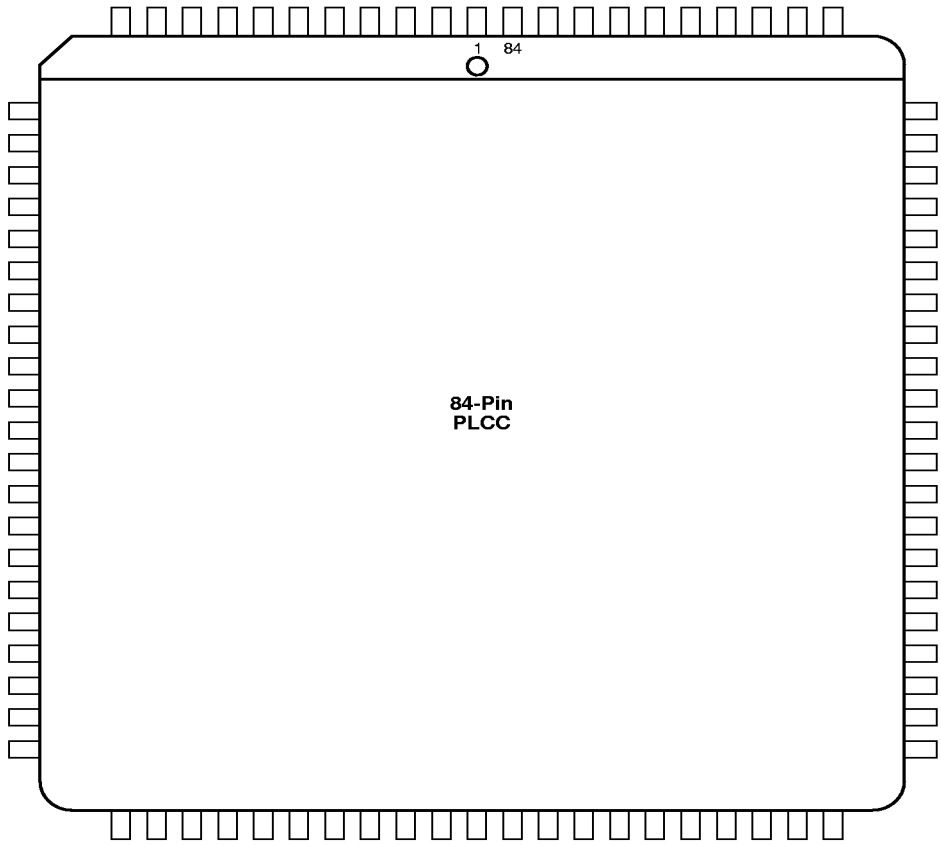
Pin	A40MX02 Function	A40MX04 Function
47	GND	GND
50	CLK, I/O	CLK, I/O
52	MODE	MODE
53	V_{CC}	V_{CC}
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
68	GND	GND
74	V_{CC}	V_{CC}

Notes:

1. *NC: Denotes 'No Connection'.*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Package Pin Assignments (continued)

84-Pin PLCC Package (Top View)



84-Pin PLCC Package

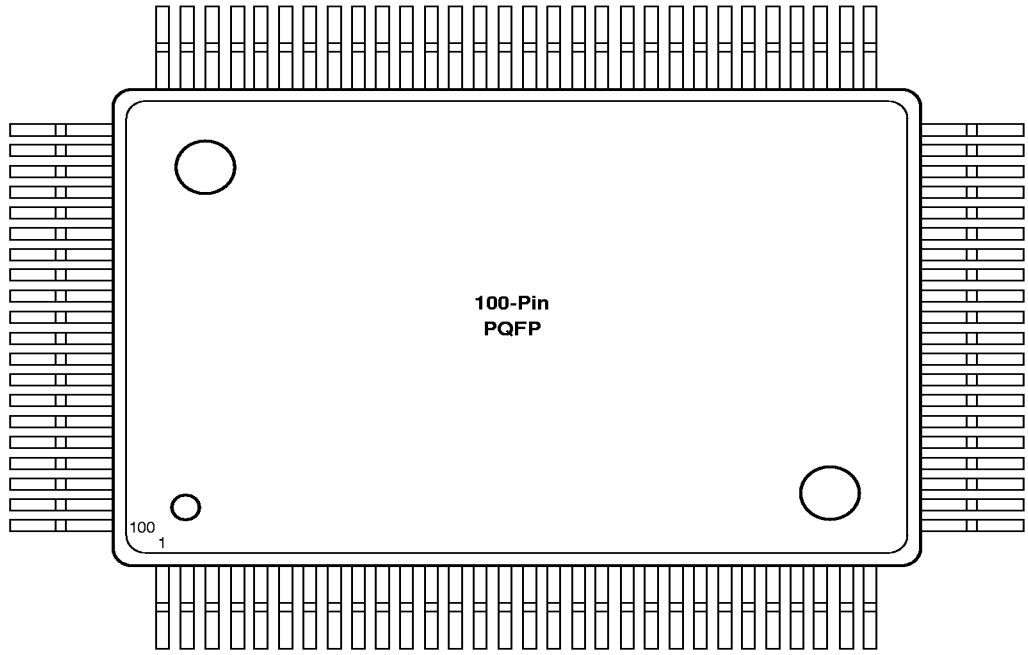
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
2	CLKB, I/O	CLKB, I/O	CLKB, I/O
4	PRB, I/O	PRB, I/O	PRB, I/O
5	I/O	I/O	I/O (WD)
6	GND	GND	GND
8	I/O	I/O	I/O (WD)
9	I/O	I/O	I/O (WD)
10	DCLK, I/O	DCLK, I/O	DCLK, I/O
12	MODE	MODE	MODE
22	V_{CCA}	V_{CCI}	V_{CCI}
23	V_{CCI}	V_{CCA}	V_{CCA}
28	GND	GND	GND
34	I/O	I/O	TMS, I/O
35	I/O	I/O	TDI, I/O
36	I/O	I/O	I/O (WD)
38	I/O	I/O	I/O (WD)
39	I/O	I/O	I/O (WD)
43	V_{CCA}	V_{CCA}	V_{CCA}
44	I/O	I/O	I/O (WD)
45	I/O	I/O	I/O (WD)
46	I/O	I/O	I/O (WD)
47	I/O	I/O	I/O (WD)
49	GND	GND	GND
50	I/O	I/O	I/O (WD)
51	I/O	I/O	I/O (WD)
52	I/O	I/O	TDO (WD)
62	I/O	I/O	TCK, I/O
63	GND (LP)	GND (LP)	GND (LP)
64	V_{CCA}	V_{CCA}	V_{CCA}
65	V_{CCI}	V_{CCI}	V_{CCI}
70	GND	GND	GND
76	SDI, I/O	SDI, I/O	SDI, I/O
78	I/O	I/O	I/O (WD)
79	I/O	I/O	I/O (WD)
80	I/O	I/O	I/O (WD)
81	PRA, I/O	PRA, I/O	PRA, I/O
83	CLKA, I/O	CLKA, I/O	CLKA, I/O
84	V_{CCA}	V_{CCA}	V_{CCA}

Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module.*
2. *Wide-decode I/O (WD) can also be general-purpose user I/O.*
3. *NC: Denotes 'No Connection'.*
4. *All unlisted pin numbers are user I/Os.*
5. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Package Pin Assignments (continued)

100-Pin PQFP Package (Top View)



100-Pin PQFP Package

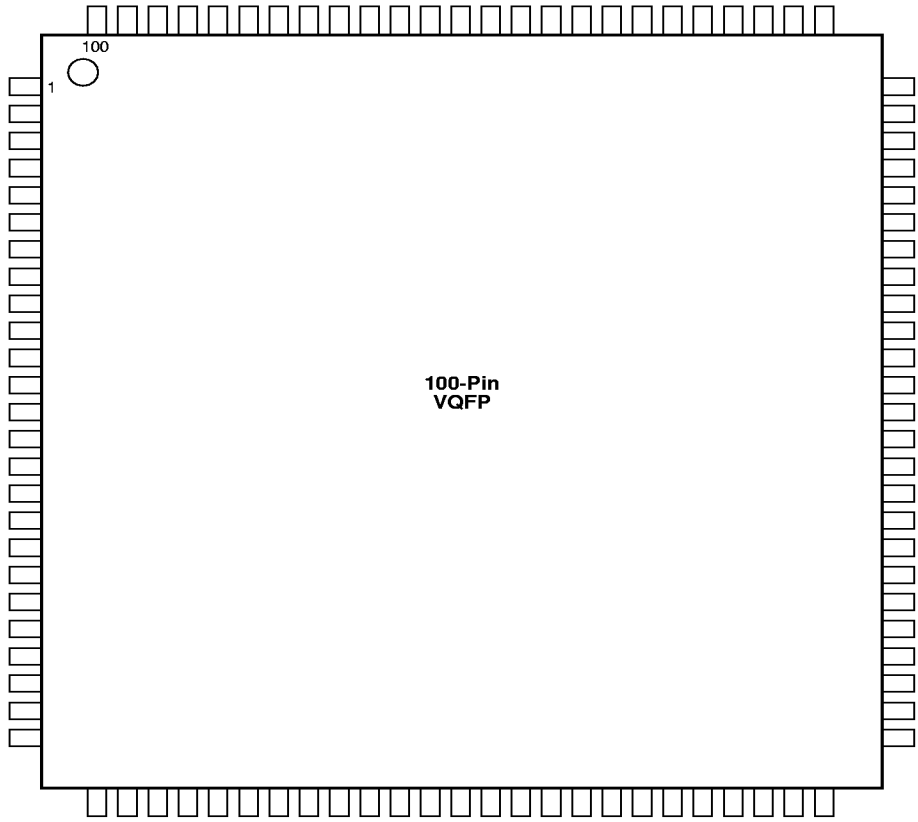
Pin Number	A42MX09 PQ100 Function	A42MX16 PQ100 Function
2	DCLK, I/O	DCLK, I/O
4	MODE	MODE
7	I/O	I/O
9	GND	GND
14	I/O	I/O
15	I/O	I/O
16	V_{CCA}	V_{CCA}
17	V_{CCI}	V_{CCA}
20	I/O	I/O
22	GND	GND
32	I/O	I/O
34	GND	GND
38	I/O	I/O
40	V_{CCA}	V_{CCA}
44	I/O	I/O
46	GND	GND
55	I/O	I/O
57	GND	GND
62	I/O	I/O
63	I/O	I/O
64	GND (LP)	GND (LP)
65	V_{CCA}	V_{CCA}
66	V_{CCI}	V_{CCI}
67	V_{CCA}	V_{CCA}
70	I/O	I/O
72	GND	GND
77	I/O	I/O
79	SDI, I/O	SDI, I/O
82	I/O	I/O
84	GND	GND
85	I/O	I/O
87	PRA, I/O	PRA, I/O
88	I/O	I/O
89	CLKA, I/O	CLKA, I/O
90	V_{CCA}	V_{CCA}
92	CLKB, I/O	CLKB, I/O
94	PRB, I/O	PRB, I/O
96	GND	GND
100	I/O	I/O

Notes:

1. *NC: Denotes 'No Connection'.*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Package Pin Assignments (continued)

100-Pin VQFP Package (Top View)



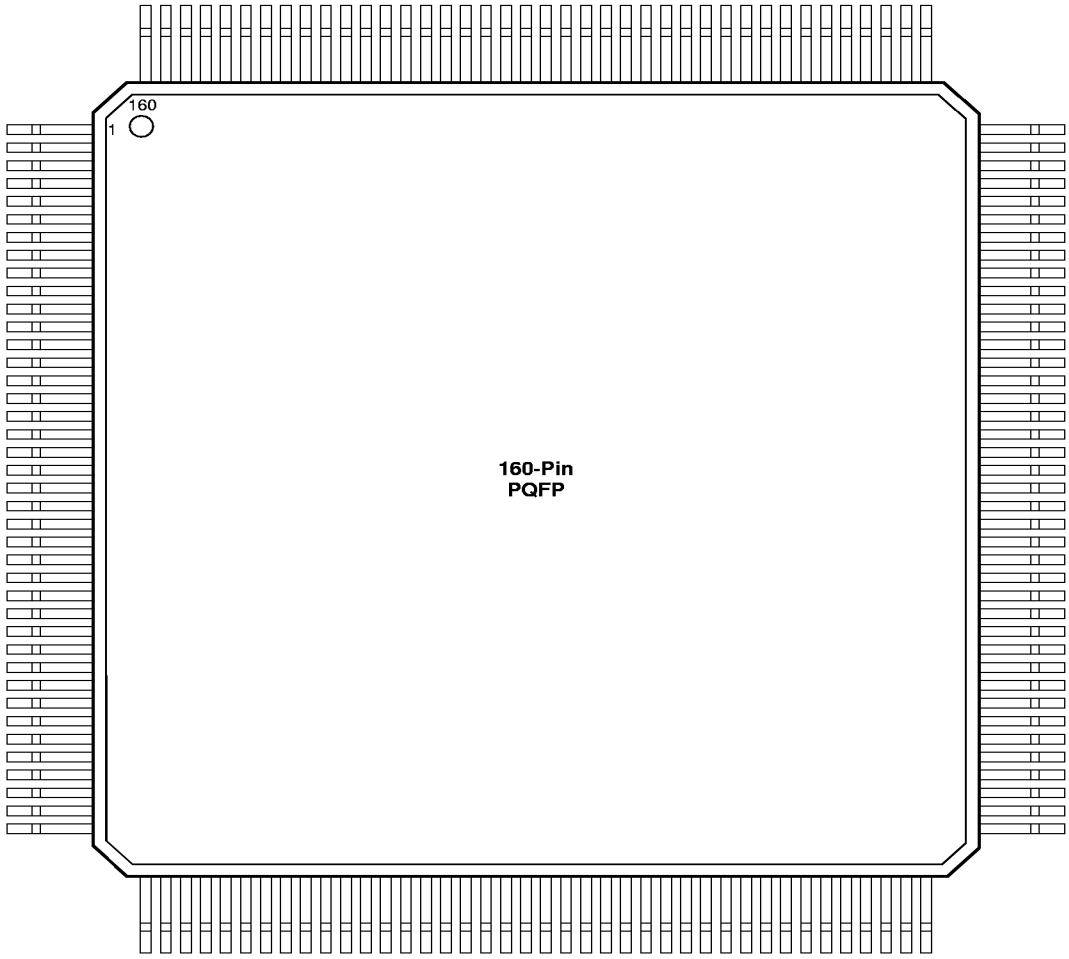
100-Pin VQFP Package

Pin Number	A42MX09 VQ100 Function	A42MX16 VQ100 Function
1	I/O	I/O
2	MODE	MODE
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	GND
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	V_{CCA}	NC
15	V_{CCI}	V_{CCI}
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	GND	GND
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	V_{CCA}	V_{CCA}
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	GND	GND
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	SDO, I/O	SDO, I/O

Pin Number	A42MX09 VQ100 Function	A42MX16 VQ100 Function
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	GND	GND
56	I/O	I/O
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	GND (LP)	GND (LP)
63	V_{CCA}	V_{CCA}
64	V_{CCI}	V_{CCI}
65	V_{CCA}	V_{CCA}
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	GND	GND
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	SDI, I/O	SDI, I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	GND	GND
83	I/O	I/O
84	I/O	I/O
85	PROBA, I/O	PROBA, I/O
86	I/O	I/O
87	CLKA, I/O	CLKA, I/O
88	V_{CCA}	V_{CCA}
89	I/O	I/O
90	CLKB, I/O	CLKB, I/O
91	I/O	I/O
92	PROBB, I/O	PROBB, I/O
93	I/O	I/O
94	GND	GND
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	DCLK, I/O	DCLK, I/O

Package Pin Assignments (continued)

160-Pin PQFP Package (Top View)



Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module.*
2. *Wide-decode I/O (WD) can also be general-purpose user I/O.*
3. *NC: Denotes 'No Connection'.*
4. *All unlisted pin numbers are user I/Os.*
5. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

160-Pin PQFP Package

Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
2	DCLK, I/O	DCLK, I/O	DCLK, I/O
3	NC	I/O	I/O
4	I/O	I/O	I/O (WD)
5	I/O	I/O	I/O (WD)
6	NC	V_{CCI}	V_{CCI}
7	I/O	I/O	I/O
10	NC	I/O	I/O
11	GND	GND	GND
12	NC	I/O	I/O
13	I/O	I/O	I/O (WD)
14	I/O	I/O	I/O (WD)
16	PRB, I/O	PRB, I/O	PRB, I/O
18	CLKB, I/O	CLKB, I/O	CLKB, I/O
20	V_{CCA}	V_{CCA}	V_{CCA}
21	CLKA, I/O	CLKA, I/O	CLKA, I/O
23	PRA, I/O	PRA, I/O	PRA, I/O
24	NC	I/O	I/O (WD)
25	I/O	I/O	I/O (WD)
26	I/O	I/O	I/O
28	NC	I/O	I/O
29	I/O	I/O	I/O (WD)
30	GND	GND	GND
31	NC	I/O	I/O (WD)
34	I/O	I/O	I/O
35	NC	V_{CCI}	V_{CCI}
36	I/O	I/O	I/O (WD)
37	I/O	I/O	I/O (WD)
38	SDI, I/O	SDI, I/O	SDI, I/O
40	GND	GND	GND
44	GND	GND	GND
49	GND	GND	GND
52	NC	I/O	I/O
54	NC	V_{CCA}	V_{CCA}
57	V_{CCA}	V_{CCA}	V_{CCA}
58	V_{CCI}	V_{CCI}	V_{CCI}
59	GND	GND	GND
60	V_{CCA}	V_{CCA}	V_{CCA}
61	GND (LP)	GND (LP)	GND (LP)
62	I/O	I/O	TCK, I/O
64	GND	GND	GND
69	GND	GND	GND
70	NC	I/O	I/O
75	NC	I/O	I/O
77	NC	I/O	I/O
79	NC	I/O	I/O
80	GND	GND	GND
82	I/O	I/O	TDO, I/O

Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
83	I/O	I/O	I/O (WD)
84	I/O	I/O	I/O (WD)
86	NC	V_{CCI}	V_{CCI}
87	I/O	I/O	I/O
88	I/O	I/O	I/O (WD)
89	GND	GND	GND
90	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
96	I/O	I/O	I/O (WD)
97	I/O	I/O	I/O
98	V_{CCA}	V_{CCA}	V_{CCA}
99	GND	GND	GND
100	NC	I/O	I/O
103	NC	I/O	I/O
106	I/O	I/O	I/O (WD)
107	I/O	I/O	I/O (WD)
109	GND	GND	GND
110	NC	I/O	I/O
111	I/O	I/O	I/O (WD)
112	I/O	I/O	I/O (WD)
114	NC	V_{CCI}	V_{CCI}
115	I/O	I/O	I/O (WD)
116	NC	I/O	I/O (WD)
118	I/O	I/O	TDI, I/O
119	I/O	I/O	TMS, I/O
120	GND	GND	GND
124	NC	I/O	I/O
125	GND	GND	GND
129	NC	I/O	I/O
130	GND	GND	GND
131	I/O	I/O	I/O
135	NC	V_{CCA}	V_{CCA}
138	NC	V_{CCA}	V_{CCA}
139	V_{CCI}	V_{CCI}	V_{CCI}
140	GND	GND	GND
141	NC	I/O	I/O
145	GND	GND	GND
146	NC	I/O	I/O
150	NC	V_{CCA}	V_{CCA}
151	NC	I/O	I/O
152	NC	I/O	I/O
153	NC	I/O	I/O
154	NC	I/O	I/O
155	GND	GND	GND
159	MODE	MODE	MODE
160	GND	GND	GND

Package Pin Assignments (continued)

208-Pin PQFP Package (Top View)

Notes:

1. *I/O (WD) : Denotes I/O pin with an associated wide-decode module.*
2. *Wide-decode I/O (WD) can also be general-purpose user I/O.*
3. *NC: Denotes 'No Connection'.*
4. *All unlisted pin numbers are user I/Os.*
5. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*
6. *RQFP has an exposed circular metal heat sink on the top surface.*

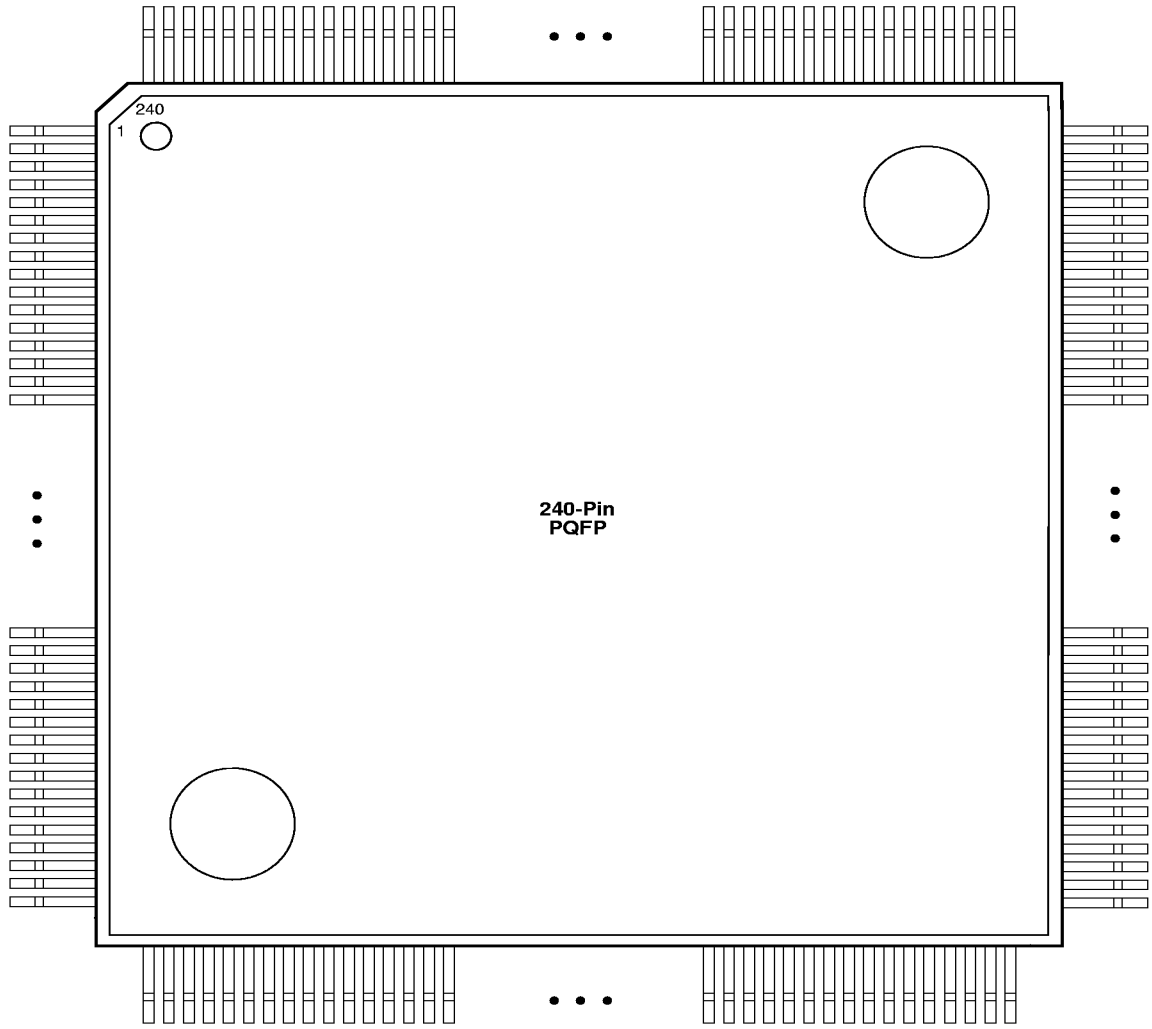
208-Pin PQFP Package

Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 PQ208 Function
1	GND	GND	GND
2	NC	V_{CCA}	V_{CCA}
3	MODE	MODE	MODE
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
9	NC	I/O	I/O
10	NC	I/O	I/O
11	NC	I/O	I/O
13	I/O	I/O	I/O
15	I/O	I/O	I/O
16	NC	I/O	I/O
17	V_{CCA}	V_{CCA}	V_{CCA}
19	I/O	I/O	I/O
20	I/O	I/O	I/O
22	GND	GND	GND
24	I/O	I/O	I/O
26	I/O	I/O	I/O
27	GND	GND	GND
28	V_{CCI}	V_{CCI}	V_{CCI}
29	V_{CCA}	V_{CCA}	V_{CCA}
30	I/O	I/O	I/O
32	V_{CCA}	V_{CCA}	V_{CCA}
33	I/O	I/O	I/O
38	I/O	I/O	I/O
40	I/O	I/O	I/O
41	NC	I/O	I/O
42	NC	I/O	I/O
43	NC	I/O	I/O
45	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
50	NC	I/O	I/O
51	NC	I/O	I/O
52	GND	GND	GND
53	GND	GND	GND
54	I/O	TMS, I/O	TMS, I/O
55	I/O	TDI, I/O	TDI, I/O
57	I/O	I/O (WD)	I/O (WD)
58	I/O	I/O (WD)	I/O (WD)
59	I/O	I/O	I/O
60	V_{CCI}	V_{CCI}	V_{CCI}
61	NC	I/O	I/O
62	NC	I/O	I/O
65	I/O	I/O	QCLKA, I/O
66	I/O	I/O (WD)	I/O (WD)
67	NC	I/O (WD)	I/O (WD)
68	NC	I/O	I/O
70	I/O	I/O (WD)	I/O (WD)
71	I/O	I/O (WD)	I/O (WD)
74	I/O	I/O	I/O
77	I/O	I/O	I/O
78	GND	GND	GND
79	V_{CCA}	V_{CCA}	V_{CCA}
80	NC	V_{CCI}	V_{CCI}
81	I/O	I/O	I/O
83	I/O	I/O	I/O
85	I/O	I/O (WD)	I/O (WD)
86	I/O	I/O (WD)	I/O (WD)
89	NC	I/O	I/O
90	NC	I/O	I/O
91	I/O	I/O	QCLKB, I/O
93	I/O	I/O (WD)	I/O (WD)
94	I/O	I/O (WD)	I/O (WD)
95	NC	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	V_{CCI}	V_{CCI}	V_{CCI}
100	I/O	I/O (WD)	I/O (WD)
101	I/O	I/O (WD)	I/O (WD)
103	I/O	TDO, I/O	TDO, I/O

Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 PQ208 Function
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	V_{CCA}	V_{CCA}
107	I/O	I/O	I/O
108	I/O	I/O	I/O
110	I/O	I/O	I/O
112	NC	I/O	I/O
113	NC	I/O	I/O
114	NC	I/O	I/O
115	NC	I/O	I/O
117	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
126	GND	GND	GND
128	I/O	TCK, I/O	TCK, I/O
129	GND (LP)	GND (LP)	GND (LP)
130	V_{CCA}	V_{CCA}	V_{CCA}
131	GND	GND	GND
132	V_{CCI}	V_{CCI}	V_{CCI}
133	V_{CCA}	V_{CCA}	V_{CCA}
136	V_{CCA}	V_{CCA}	V_{CCA}
137	I/O	I/O	I/O
138	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
144	I/O	I/O	I/O
146	NC	I/O	I/O
147	NC	I/O	I/O
148	NC	I/O	I/O
149	NC	I/O	I/O
150	GND	GND	GND
151	I/O	I/O	I/O
152	I/O	I/O	I/O
154	I/O	I/O	I/O
155	I/O	I/O	I/O
156	I/O	I/O	I/O
157	GND	GND	GND
159	SDI, I/O	SDI, I/O	SDI, I/O
161	I/O	I/O (WD)	I/O (WD)
162	I/O	I/O (WD)	I/O (WD)
164	V_{CCI}	V_{CCI}	V_{CCI}
165	NC	I/O	I/O
166	NC	I/O	I/O
168	I/O	I/O (WD)	I/O (WD)
169	I/O	I/O (WD)	I/O (WD)
171	NC	I/O	QCLKD, I/O
176	I/O	I/O (WD)	I/O (WD)
177	I/O	I/O (WD)	I/O (WD)
178	PRA, I/O	PRA, I/O	PRA, I/O
180	CLKA, I/O	CLKA, I/O	CLKA, I/O
181	NC	I/O	I/O
182	NC	V_{CCI}	V_{CCI}
183	V_{CCA}	V_{CCA}	V_{CCA}
184	GND	GND	GND
186	CLKB, I/O	CLKB, I/O	CLKB, I/O
187	I/O	I/O	I/O
188	PRB, I/O	PRB, I/O	PRB, I/O
190	I/O	I/O (WD)	I/O (WD)
191	I/O	I/O (WD)	I/O (WD)
193	NC	I/O	I/O
194	NC	I/O (WD)	I/O (WD)
195	NC	I/O (WD)	I/O (WD)
196	I/O	I/O	QCLKC, I/O
197	NC	I/O	I/O
201	NC	I/O	I/O
202	V_{CCI}	V_{CCI}	V_{CCI}
203	I/O	I/O (WD)	I/O (WD)
204	I/O	I/O (WD)	I/O (WD)
206	I/O	I/O	I/O
207	DCLK, I/O	DCLK, I/O	DCLK, I/O
208	I/O	I/O	I/O

Package Pin Assignments (continued)

240-Pin PQFP Package (Top View)



Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module.*
2. *Wide-decode I/O (WD) can also be general-purpose user I/O.*
3. *NC: Denotes 'No Connection'.*
4. *All unlisted pin numbers are user I/Os.*
5. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

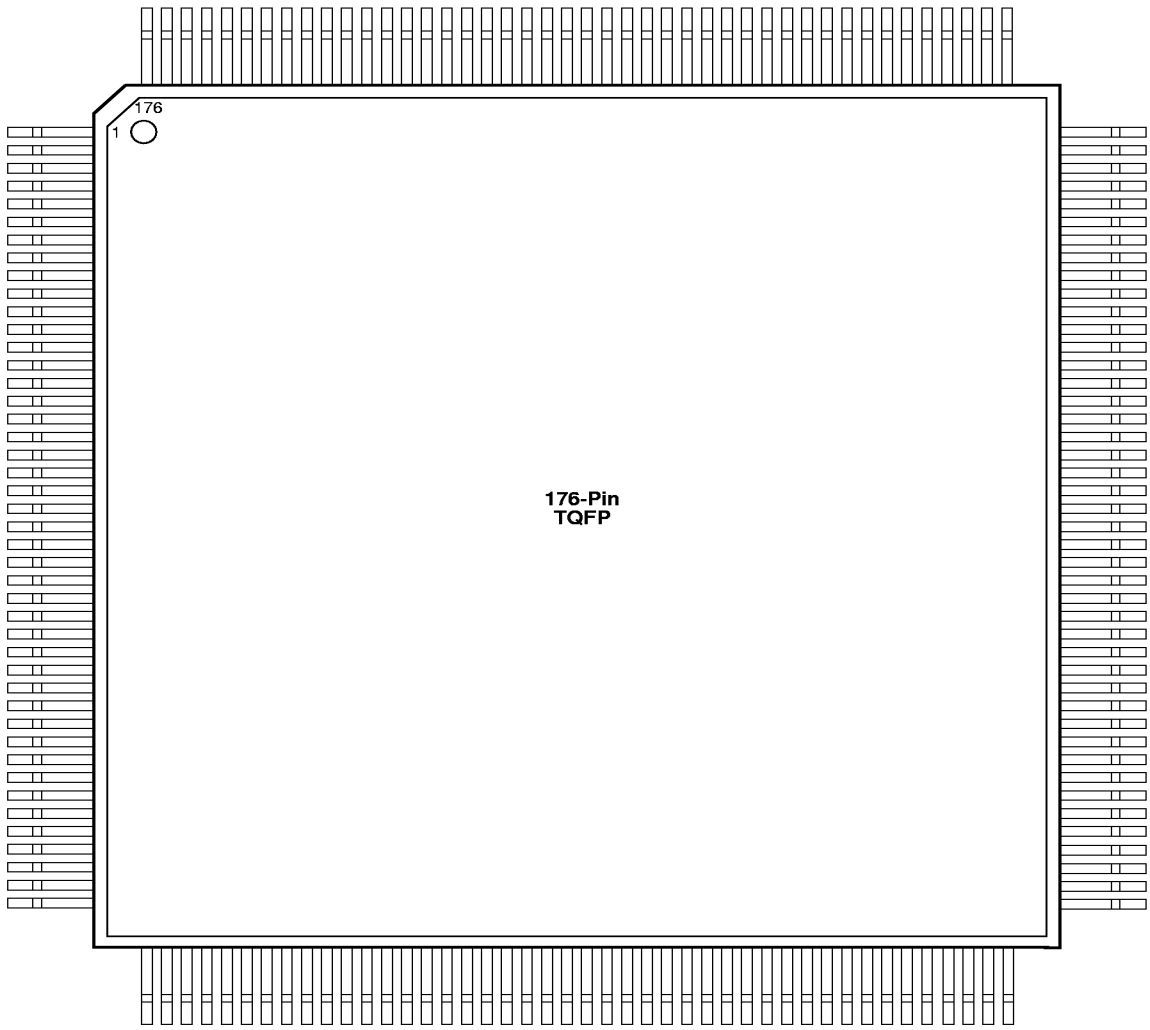
240-Pin PQFP Package

Pin Number	A42MX36 Function
2	DCLK, I/O
6	I/O (WD)
7	I/O (WD)
8	V_{CCI}
15	QCLKC, I/O
17	I/O (WD)
18	I/O (WD)
21	I/O (WD)
22	I/O (WD)
24	PRB, I/O
26	CLKB, I/O
28	GND
29	V_{CCA}
30	V_{CCI}
32	CLKA, I/O
34	PRA, I/O
37	I/O (WD)
38	I/O (WD)
45	QCLKD, I/O
47	I/O (WD)
48	I/O (WD)
52	V_{CCI}
54	I/O (WD)
55	I/O (WD)
57	SDI, I/O
59	V_{CCA}
60	GND
61	GND
71	V_{CCI}
85	V_{CCA}
88	V_{CCA}
89	V_{CCI}
90	V_{CCA}
91	GND (LP)
92	TCK, I/O
94	GND
108	V_{CCI}
118	V_{CCA}

Pin Number	A42MX36 Function
119	GND
120	GND
121	GND
123	TDO, I/O
125	I/O (WD)
126	I/O (WD)
128	V_{CCI}
132	I/O (WD)
133	I/O (WD)
135	QCLKB, I/O
142	I/O (WD)
143	I/O (WD)
150	V_{CCI}
151	V_{CCA}
152	GND
159	I/O (WD)
160	I/O (WD)
163	I/O (WD)
164	I/O (WD)
166	QCLKA, I/O
172	V_{CCI}
174	I/O (WD)
175	I/O (WD)
178	TDI, I/O
179	TMS, I/O
180	GND
181	V_{CCA}
182	GND
192	V_{CCI}
206	V_{CCA}
209	V_{CCA}
210	V_{CCI}
219	V_{CCA}
227	V_{CCI}
237	GND
238	MODE
239	V_{CCA}
240	GND

Package Pin Assignments (continued)

176-Pin TQFP Package (Top View)



Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module.*
2. *Wide-decode I/O (WD) can also be general-purpose user I/O.*
3. *NC: Denotes 'No Connection'.*
4. *All unlisted pin numbers are user I/Os.*
5. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

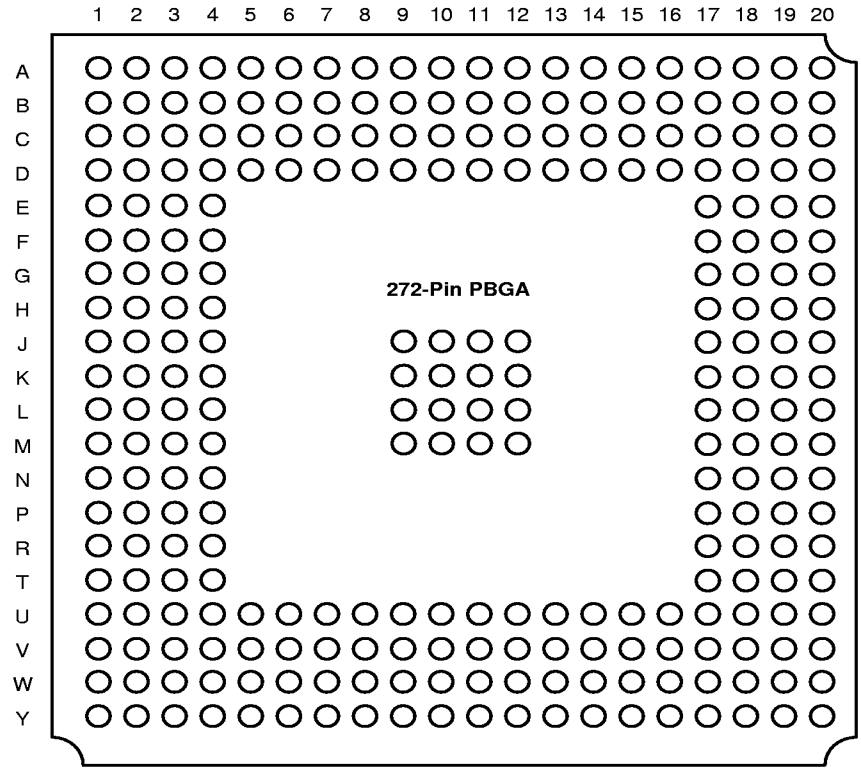
176-Pin TQFP Package

Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	GND	GND	GND
2	MODE	MODE	MODE
8	NC	NC	I/O
10	NC	I/O	I/O
11	NC	I/O	I/O
13	NC	V_{CCA}	V_{CCA}
18	GND	GND	GND
19	NC	I/O	I/O
20	NC	I/O	I/O
22	NC	I/O	I/O
23	GND	GND	GND
24	NC	V_{CCI}	V_{CCI}
25	V_{CCA}	V_{CCA}	V_{CCA}
26	NC	I/O	I/O
27	NC	I/O	I/O
28	V_{CCI}	V_{CCA}	V_{CCA}
29	NC	I/O	I/O
33	NC	NC	I/O
37	NC	I/O	I/O
38	NC	NC	I/O
45	GND	GND	GND
46	I/O	I/O	TMS, I/O
47	I/O	I/O	TDI, I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O (WD)
50	I/O	I/O	I/O (WD)
52	NC	V_{CCI}	V_{CCI}
54	NC	I/O	I/O
55	NC	I/O	I/O (WD)
56	I/O	I/O	I/O (WD)
57	NC	NC	I/O
59	I/O	I/O	I/O (WD)
60	I/O	I/O	I/O (WD)
61	NC	I/O	I/O
64	NC	I/O	I/O
66	NC	I/O	I/O
67	GND	GND	GND
68	V_{CCA}	V_{CCA}	V_{CCA}
69	I/O	I/O	I/O (WD)
70	I/O	I/O	I/O (WD)
73	I/O	I/O	I/O
74	NC	I/O	I/O
75	I/O	I/O	I/O
77	NC	NC	I/O (WD)
78	NC	I/O	I/O (WD)
80	NC	I/O	I/O
81	I/O	I/O	I/O
82	NC	V_{CCI}	V_{CCI}
84	I/O	I/O	I/O (WD)
85	I/O	I/O	I/O (WD)
86	NC	I/O	I/O
87	I/O	I/O	TDO, I/O
89	GND	GND	GND
96	NC	I/O	I/O

Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
97	NC	I/O	I/O
101	NC	NC	I/O
103	NC	I/O	I/O
106	GND	GND	GND
107	NC	I/O	I/O
108	NC	I/O	TCK, I/O
109	GND (LP)	GND (LP)	GND (LP)
110	V_{CCA}	V_{CCA}	V_{CCA}
111	GND	GND	GND
112	V_{CCI}	V_{CCI}	V_{CCI}
113	V_{CCA}	V_{CCA}	V_{CCA}
114	NC	I/O	I/O
115	NC	I/O	I/O
116	NC	V_{CCA}	V_{CCA}
117	I/O	I/O	I/O
121	NC	NC	I/O
124	NC	I/O	I/O
125	NC	I/O	I/O
126	NC	NC	I/O
133	GND	GND	GND
135	SDI, I/O	SDI, I/O	SDI, I/O
136	NC	I/O	I/O
137	I/O	I/O	I/O (WD)
138	I/O	I/O	I/O (WD)
139	I/O	I/O	I/O
140	NC	V_{CCI}	V_{CCI}
141	I/O	I/O	I/O
143	NC	I/O	I/O
144	NC	I/O	I/O (WD)
145	NC	NC	I/O (WD)
146	I/O	I/O	I/O
147	NC	I/O	I/O
149	I/O	I/O	I/O
150	I/O	I/O	I/O (WD)
151	NC	I/O	I/O (WD)
152	PRA, I/O	PRA, I/O	PRA, I/O
154	CLKA, I/O	CLKA, I/O	CLKA, I/O
155	V_{CCA}	V_{CCA}	V_{CCA}
156	GND	GND	GND
158	CLKB, I/O	CLKB, I/O	CLKB, I/O
160	PRB, I/O	PRB, I/O	PRB, I/O
161	NC	I/O	I/O (WD)
162	I/O	I/O	I/O (WD)
163	I/O	I/O	I/O
165	NC	NC	I/O (WD)
166	NC	I/O	I/O (WD)
168	NC	I/O	I/O
169	I/O	I/O	I/O
170	NC	V_{CCI}	V_{CCI}
171	I/O	I/O	I/O (WD)
172	I/O	I/O	I/O (WD)
173	NC	I/O	I/O
175	DCLK, I/O	DCLK, I/O	DCLK, I/O

Package Pin Assignments (continued)

272-Pin BGA Package (Top View)



Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module.*
2. *Wide-decode I/O (WD) can also be general-purpose user I/O.*
3. *NC: Denotes 'No Connection'.*
4. *All unlisted pin numbers are user I/Os.*
5. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

272-Pin BGA

Ball	A42MX36 Function
C3	GND
C2	MODE
D3	I/O
E3	I/O
C1	I/O
D2	I/O
F3	I/O
D1	I/O
E2	I/O
G3	I/O
F2	I/O
E1	I/O
G2	I/O
F1	I/O
H3	I/O
G1	I/O
H2	I/O
H1	I/O
J3	I/O
J2	I/O
J1	I/O
K1	I/O
K2	I/O
K3	I/O
L1	I/O
L2	I/O
L3	V_{CCA}
M1	I/O
M2	I/O
N1	I/O
N2	I/O
M3	I/O
P1	I/O
R1	I/O
P2	I/O
R2	I/O
N3	I/O
T1	I/O
T2	I/O
U1	I/O
P3	I/O
R3	I/O

Ball	A42MX36 Function
U2	I/O
T3	I/O
U3	I/O
V1	I/O
V2	I/O
W3	I/O
Y3	I/O
U4	I/O
T4	I/O
V4	GND
W4	TMS, I/O
Y4	TDI, I/O
V5	I/O
W5	I/O
Y5	I/O (WD)
U6	I/O (WD)
V6	I/O
W6	I/O
Y6	I/O
U7	I/O
V7	I/O
W7	I/O
Y7	QCLKA, I/O
U8	I/O
V8	I/O (WD)
W8	I/O (WD)
Y8	I/O
V9	I/O
U9	I/O (WD)
W9	I/O (WD)
Y9	I/O
Y10	I/O
W10	I/O
V10	I/O
Y11	I/O
W11	I/O
V11	I/O
Y12	I/O
W12	I/O
V12	I/O
U12	I/O
Y13	I/O

Ball	A42MX36 Function
W13	I/O (WD)
V13	I/O (WD)
Y14	I/O
U13	I/O
W14	I/O
Y15	I/O
V14	I/O
W15	I/O
U14	QCLKB, I/O
Y16	I/O
V15	I/O (WD)
W16	I/O (WD)
Y17	I/O
U15	I/O
V16	I/O
W17	I/O
Y18	I/O (WD)
W18	I/O (WD)
V17	I/O
V18	TDO, I/O
U17	I/O
U18	GND
V19	I/O
T18	I/O
V20	I/O
U19	I/O
P17	I/O
R18	I/O
U20	I/O
T19	I/O
P18	I/O
T20	I/O
R19	I/O
R20	I/O
N18	I/O
P19	I/O
M17	I/O
P20	I/O
N19	I/O
N20	I/O
M18	I/O
M19	I/O

Ball	A42MX36 Function
M20	I/O
L18	I/O
L19	I/O
L20	TCK, I/O
K20	GND (LP)
K19	V_{CCA}
K18	V_{CCA}
J20	I/O
J19	I/O
K17	I/O
H20	I/O
J18	I/O
H19	I/O
G20	I/O
G19	I/O
F20	I/O
H18	I/O
F19	I/O
E20	I/O
G18	I/O
H17	I/O
E19	I/O
D20	I/O
F18	I/O
E18	I/O
D19	I/O
C20	I/O
F17	I/O
D18	I/O
C19	I/O
C18	I/O
D17	GND
B18	I/O
C17	SDI, I/O
A18	I/O
B17	I/O (WD)
C16	I/O (WD)
D15	I/O
A17	I/O
B16	I/O
C15	I/O
A16	I/O (WD)

272-Pin BGA

Ball	A42MX36 Function
B15	I/O (WD)
A15	I/O
C14	QCLKD, I/O
B14	I/O
A14	I/O
D13	I/O
C13	I/O
B13	I/O
A13	I/O
C12	I/O (WD)
B12	I/O (WD)
A12	I/O
D11	I/O
C11	PRA, I/O
B11	I/O
A11	CLKA
A10	I/O
B10	I/O
C10	CLKB
A9	I/O
B9	PRB, I/O
C9	I/O
D9	I/O (WD)
A8	I/O (WD)
B8	I/O
C8	I/O

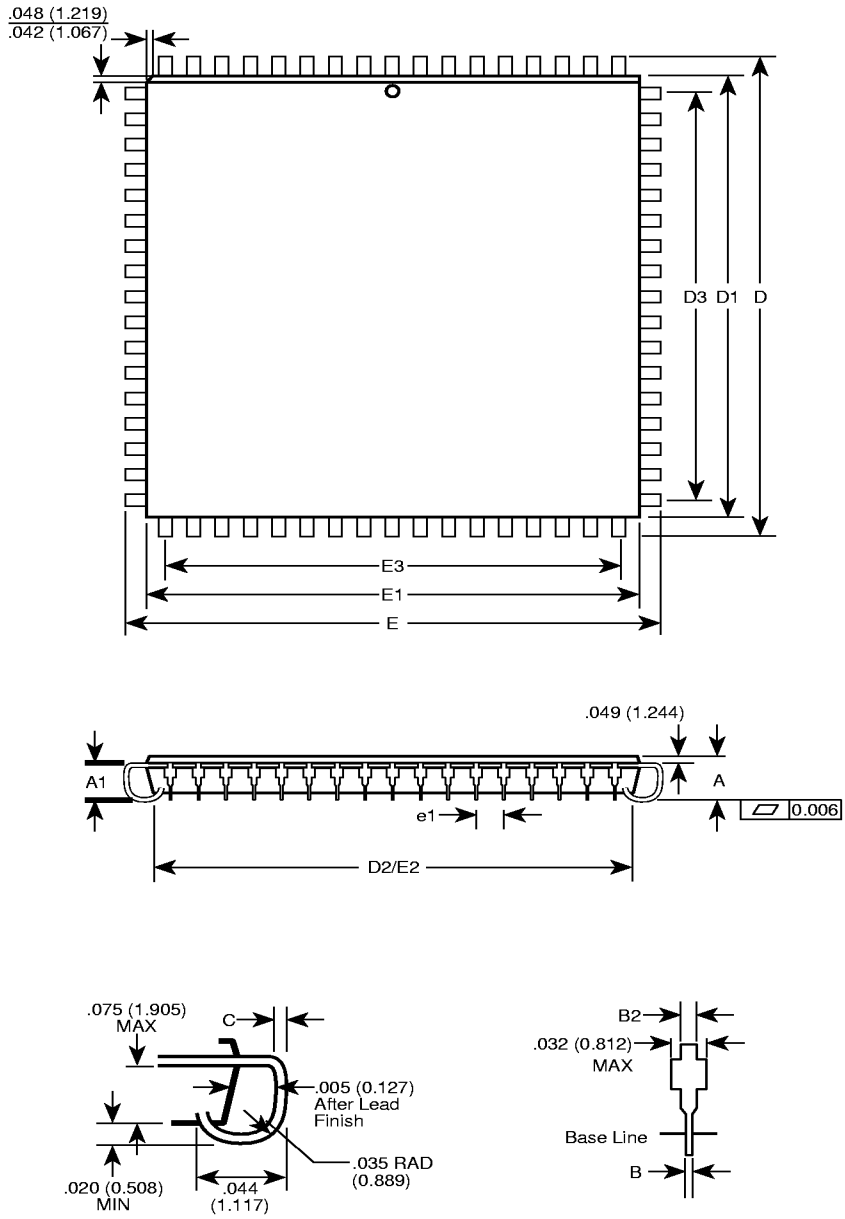
Ball	A42MX36 Function
A7	I/O (WD)
B7	I/O (WD)
A6	I/O
C7	QCLKC, I/O
B6	I/O
D7	I/O
A5	I/O
B5	I/O
C6	I/O
D6	I/O
A4	I/O (WD)
C5	I/O (WD)
B4	I/O
A3	I/O
C4	I/O
B3	DCLK, I/O
D4	I/O
A1	GND
A19	GND
A2	GND
A20	GND
B1	GND
B19	GND
B2	GND
B20	GND
J10	GND

Ball	A42MX36 Function
J11	GND
J12	GND
J9	GND
K10	GND
K11	GND
K12	GND
K9	GND
L10	GND
L11	GND
L12	GND
L9	GND
M10	GND
M11	GND
M12	GND
M9	GND
V3	GND
W1	GND
W19	GND
W2	GND
W20	GND
Y1	GND
Y19	GND
Y2	GND
Y20	GND
D10	V_{CCI}
D12	V_{CCI}

Ball	A42MX36 Function
D14	V_{CCI}
D5	V_{CCI}
E17	V_{CCI}
F4	V_{CCI}
G17	V_{CCI}
G4	V_{CCI}
J4	V_{CCI}
K4	V_{CCI}
L17	V_{CCI}
M4	V_{CCI}
N17	V_{CCI}
N4	V_{CCI}
R17	V_{CCI}
R4	V_{CCI}
U11	V_{CCI}
U16	V_{CCI}
U5	V_{CCI}
D16	V_{CCA}
D8	V_{CCA}
E4	V_{CCA}
H4	V_{CCA}
J17	V_{CCA}
L4	V_{CCA}
P4	V_{CCA}
T17	V_{CCA}
U10	V_{CCA}

Package Mechanical Drawings

Plastic Leaded Chip Carrier (PLCC)



Plastic Leaded Chip Carrier Packages (PLCC)

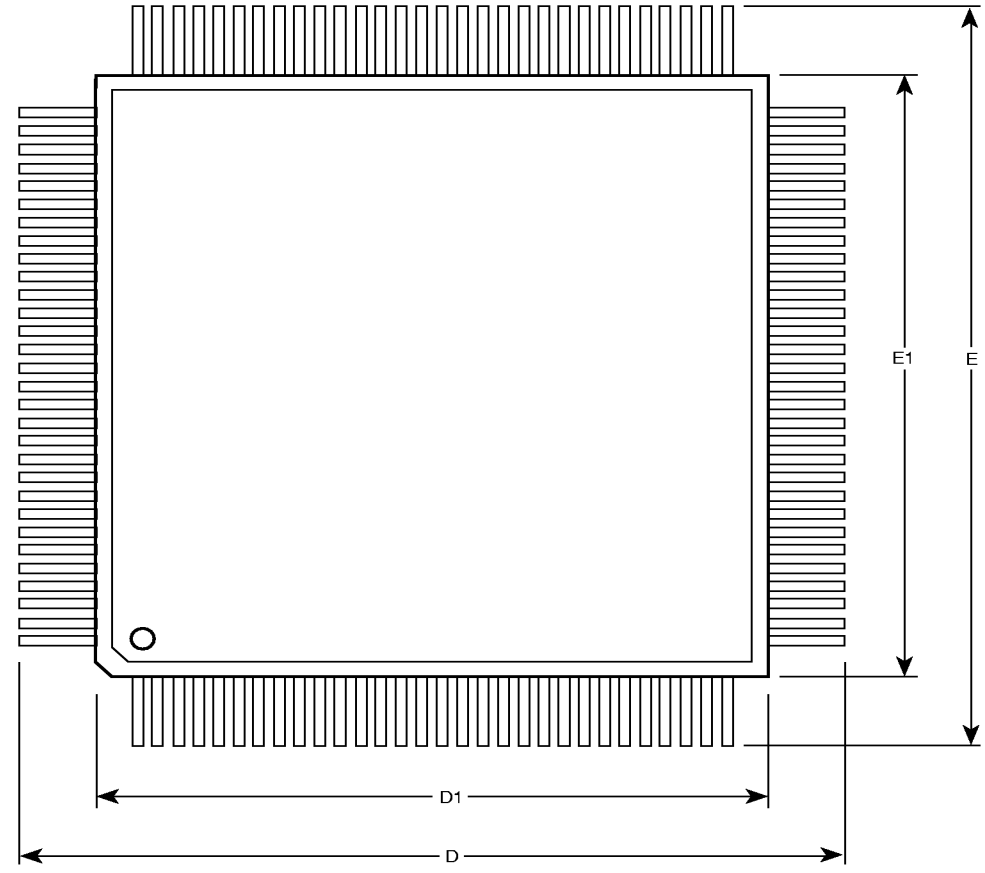
JEDEC Equivalent	PLCC 44 MS007 AE VAR		PLCC 68 MS007 AE VAR		PLCC 84 MS007 AE VAR	
Dimension	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
A	0.155	0.175	0.155	0.175	0.155	0.175
A1	0.090	0.130	0.090	0.130	0.090	0.130
B	0.013	0.027	0.013	0.027	0.013	0.027
B2	0.026	0.032	0.026	0.032	0.026	0.032
C	0.007	0.013	0.005	0.011	0.005	0.011
D/E	0.670	0.710	0.970	1.010	1.170	1.210
D1/E1	0.640	0.660	0.940	0.960	1.140	1.160
D2/E2	0.590	0.630	0.890	0.930	1.090	1.130
D3/E3	.50 nominal		.80 nominal		1.00 nominal	
e1	0.050 BSC		0.050 BSC		0.050 BSC	

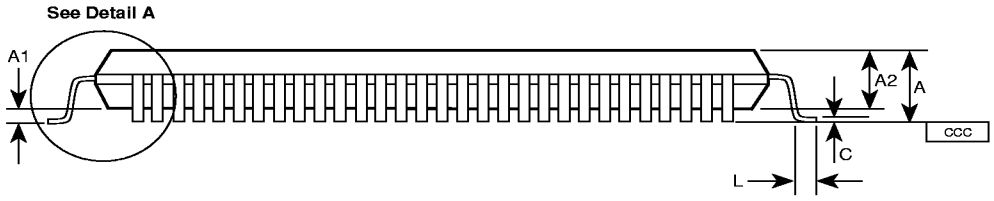
Notes:

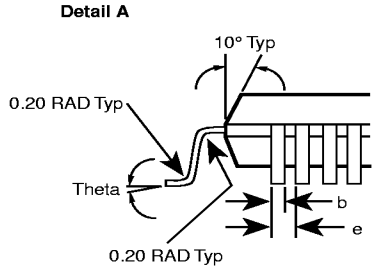
1. *All dimensions are in inches.*
2. *BSC—Basic Spacing between Centers.*

Package Mechanical Drawings (continued)

Plastic Quad Flat Pack (PQFP, RQFP, TQFP, VQFP)

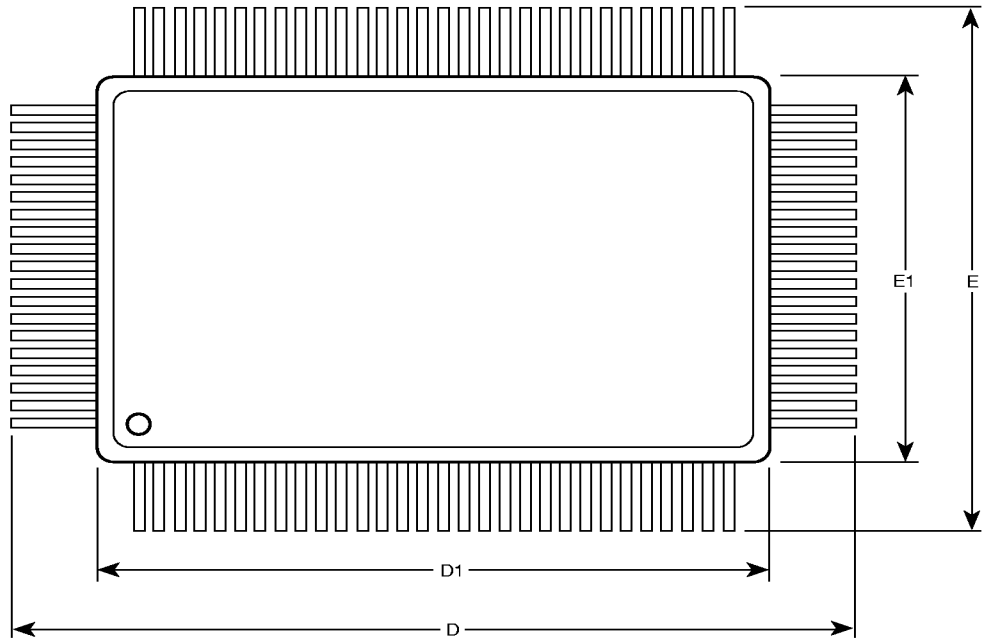


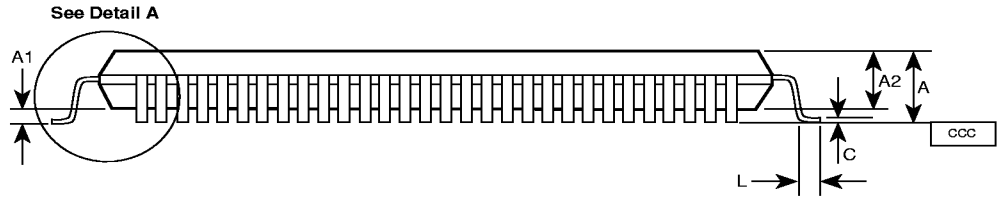


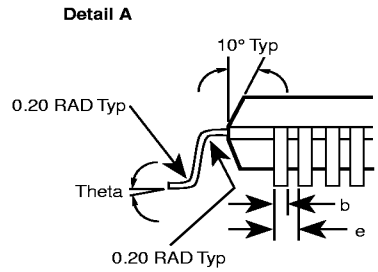


Package Mechanical Drawings (continued)

Plastic Quad Flat Pack
Rectangular Package (PQ100)







Plastic Quad Flat Packages (PQFP)

JEDEC Equivalent	PQFP 100 MO-108			PQFP 160 MO-108			PQFP 208 MO-143		
Dimension	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A			3.40		3.70	4.10			4.10
A1	0.25	0.33		0.25	0.33		0.25	0.33	
A2	2.55	2.80	3.05	3.17	3.37	3.67	3.17	3.37	3.67
b	0.22		0.38	0.22		0.38	0.15		0.30
c	0.13		0.23	0.13		0.23	0.13		0.23
D	22.95	23.20	23.45	30.95	31.90	31.45	30.35	30.60	30.85
D1	19.90	20.00	20.10	27.90	28.00	28.10	27.9	28.00	28.10
E	16.95	17.20	17.45	30.95	31.20	31.45	30.35	30.60	30.85
E1	13.90	14.00	14.10	27.90	28.00	28.10	27.9	28.00	28.1
e		0.65 BSC			0.65 BSC			0.50 BSC	
L	0.73	0.88	1.03	0.73	0.88	1.03	0.50		0.75
ccc			0.10			0.10			0.10
Theta	0		7 deg	0		7 deg	0		7 deg

Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*

Plastic Quad Flat Packages (PQFP)

JEDEC Equivalent	PQFP 240 MO-143		
Dimension	**Min.**	**Nom.**	**Max.**
A		3.78	4.10
A1	0.25	0.38	
A2	3.20	3.40	3.60
b	0.17		0.27
c	0.09		0.20
D/E	34.35	34.60	34.85
D1/E1	31.90	32.00	32.10
e		0.50 BSC	
L	0.50	0.6	0.75
ccc			0.10
Theta	0		7 deg

Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*

Thin Quad Flat Packs (TQFP and VQFP)

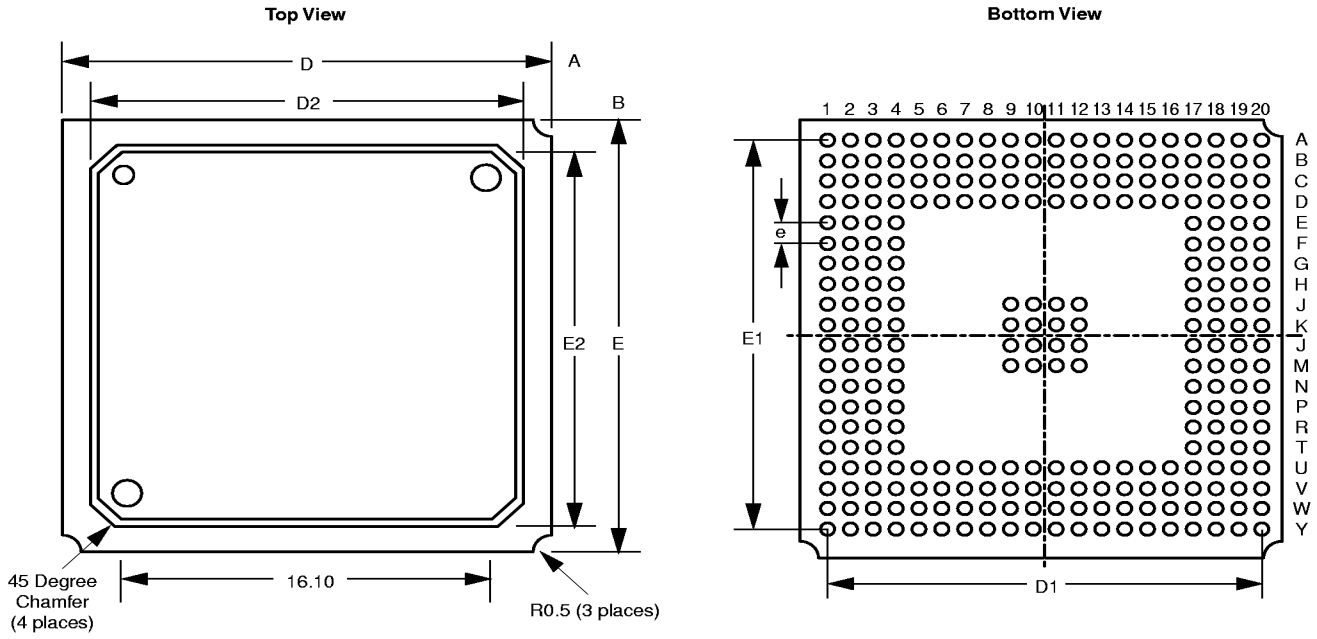
JEDEC Equivalent	TQFP 176 MO-136			VQFP 80 MO-136			VQFP 100 MO-136		
Dimension	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A			1.60			1.20			1.20
A1	0.05	0.10	0.15	0.05	0.10	0.15	0.05	0.10	0.15
A2	1.35	1.40	1.45	0.95		1.05	0.95		1.05
b	0.17		0.27	0.22		0.38	0.17		0.27
c	0.09		0.20	0.09		0.20	0.09		0.20
D/E	2.575	26.00	26.25	15.75	16.00	16.25	15.75	16.00	16.25
D1/E1	23.90	24.00	24.1	13.90	14.00	14.10	13.90	14.00	14.10
e		0.50 BSC			0.65 BSC			0.50 BSC	
L	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75
ccc			0.10			0.10			0.10
Theta	0		7 deg	0		7 deg	0		7 deg

Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*

Package Mechanical Drawings (continued)

Plastic Ball Grid Array (BGA272)



Power Ball Grid Array (PBGA)

JEDEC Equivalent	PBGA272		
Dimension	**Min.**	**Nom.**	**Max.**
A	2.18	2.33	2.50
A1	0.50	0.60	0.70
A2	1.15	1.17	1.19
D	26.80	27.00	27.20
D1		24.13 BSC	
D2	23.90	24.00	24.10
E	26.80	27.00	27.20
E1		24.13 BSC	
E2	23.90	24.00	24.10
b	0.60	0.75	0.90
c	0.53	0.56	0.61
aaa			0.15
bbb			0.20
ccc			0.25
e		1.27 typ.	

Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*