NEC

NEC Electronics Inc.

CB-C8

0.5-Micron CMOS Cell-Based ASIC

Design Manual

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CONTENTS

PREFACE

This design manual contains design rules and guidelines for designing logic circuits and layouts on NEC's CMOS cell-based ASIC CB-C8 Family.

Read this manual thoroughly and observe all of the restrictions and precautions to insure a successful design of your cell-based ASIC.

CHAPTER 1   GENERAL DESCRIPTION

NEC's CB-C8 family of cell-based ASICs (μPD93600, μPD94600, μPD95600, and μPD96600) feature high-speed, high integration and low power consumption.

NEC provides customers with a powerful library of macros based on general-purpose LSIs from which you may select specific megafunctions and integrate all functions onto a single chip.

Table 1-1 CB-C8 General Specification List

Master Name		μPD93600	μPD94600	μPD95600	μPD96600
Megafunction block (Excluding memory macros)		Not available		Available	
ROM code		Not available	Available	Not available	Available
Delay time	Internal gate	0.22 ns F/O = 2, ℓ = 2 mm, Power gate			
	Input buffer	0.36 ns (F/O = 2, ℓ = 2 mm)			
	Output buffer	1.46 ns (C$_L$ = 15 pF, I$_{OL}$ = 9 mA)			
Power consumption	Internal gate	2.08 μW/MHz/gate (F302 conversion) 1.25 μW/MHz/gate (L302 conversion)			
	Input buffer	TBA			
	Output buffer	TBA			
Ambient temperature		—40 to +85 °C			
Supply voltage		3.3 V ± 0.3 V (3.0 V ± 10 %*)			
I/O interface level		CMOS compatible (5 V interface available)			
Technology (Design rule)		0.5 μm Silicon gate CMOS			
Packaging[Note]	QFP :	44, 52, 64, 80, 100, 120, 136, 160, 184, 208			
	TQFP:	64, 80, 100, 120*			
	LQFP	144*, 160*, 176*, 208*			
	QFP(FP):	100, 120, 144, 160, 176, 208, 240, 256*, 272*, 304			
	PLCC:	68, 84			
	PGA :	72, 132, 176, 208, 280, 364			

Note   The packages above are subject to change at any time. Consult NEC Electronics Inc. concerning current status.

Remark 1.   When a megafunction is incorporated, the range of assurance may change depending on the incorporated megafunction.

2.   *Indicates a product which is being developed or its development is being examined.

QUALITY GRADE

Standard

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to understand quality specifications on the devices described herein and their recommended applications.

CHAPTER 2   BASIC ARCHITECTURE OF CB-C8

2.1 Chip Architecture

The architectural elements of the CB-C8 family are shown and explained below.

```
┌──────┐   ┌─────────────────┐   ┌───────────────────────┐
│ Chip │───│ Internal circuit │───│   Megafunction block   │
└──────┘   └─────────────────┘   └───────────────────────┘
                                 ┌───────────────────────────────┐   ┌────────────────┐
                                 │ Customer specified function block │──│ Functional cell │
                                 └───────────────────────────────┘   └────────────────┘
           ┌─────────────────┐   ┌───────────────┐
           │ Interface block  │───│   Pre-buffer   │
           └─────────────────┘   └───────────────┘
                                 ┌───────────────┐
                                 │   Main buffer  │
                                 └───────────────┘
```
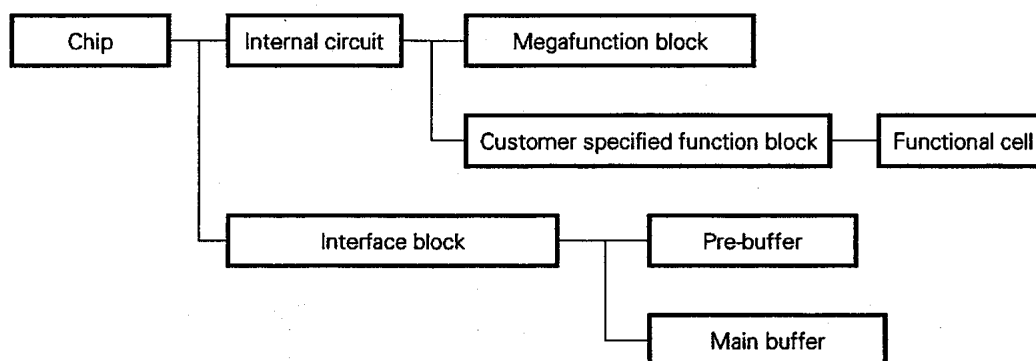
Megafunction block	Large gate count function block, such as a CPU macro or FDC macro. May also be a memory macro, such as compiled RAM or ROM.
Customer specified function block	The block of logic, typicaly designed by customer, using functional cells provided in the NEC library.
Functional cell	Primitive block which offers such basic functions such as OR, AND, and F/F.
Interface block	The block used to interface to external pins.
Pre-buffer	Pre-buffer, part of the interface block, is used to control the Main Buffer.
Main buffer	Buffer to interface with an external block. The main buffer and pre-buffer make up an interface block.
Internal circuit	All circuits except for the interface blocks.

Remark: Input buffer, output buffer, and bidirectional buffer are collectively called an interface block.

2.2   Chip Layout

The CB-C8 is a cell-based IC product based on the building block system. Megafunctions that are the equivalent of NEC's standard ICs, such as NA7150x, and customer specified logic can all be integrated on to a single chip.

An example of a typical chip layout is shown below.
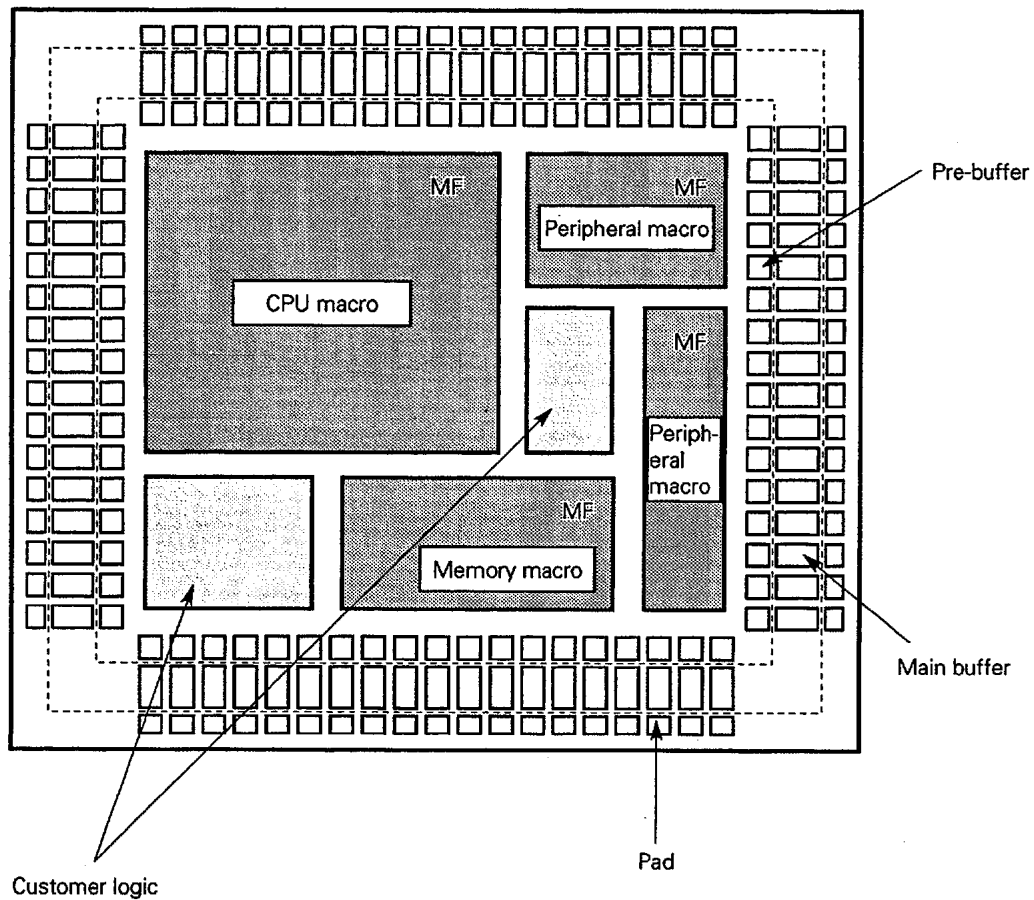
Remark   MF = megafunction.

3.1 Development Flow

The development environment for designing a CB-C8 cell-based IC uses "Open CAD, Ver. 3.2". Please confirm with NEC the latest version to use before beginning your design.

```
                          ┌─────────────────┐
                          │  System design  │
                          └─────────────────┘
                 ┌──────────────┴──────────────┐
        ┌─────────────────┐            ┌─────────────────┐
        │ Memory compiler │            │ Logic synthesis │
        └─────────────────┘            └─────────────────┘
                 └──────────────┬──────────────┘
                  ┌──────────────────────────────────┐
                  │ Schematic entry, test pattern design │
                  └──────────────────────────────────┘
                                │
                  ┌──────────────────────────────┐
                  │   Design rule check (DRC)     │
                  └──────────────────────────────┘
```

Simulation with estimated wiring length

Customer specified logic separate simulation Note 2

Simulation for test circuit Note 2

Total chip simulation

IE (in-circuit emulator) preparation Note 3

Floor plan (wiring length estimation) Note 2   calculation of estimated wiring length

Program preparation, debug

Placement and routing

Simulation with actual wiring length

Customer specified logic separate simulation

Total chip simulation

Fault simulation Note 1

Power simulation Note 1

Design review

ROM code Note 4

Mask generation

Notes: 1. Optional, some tools do not support this function.
        2. These simulations are necessary when megafunction blocks are included in the design.
        3. In-circuit Emulator is needed when a CPU macro is included in the design.

3.2 Explanation of Development Flow

Item	Description
System design	Defines the specifications of the overall system before commencing a detailed design and implementing basic functions. Allows circuit to be built cheaply and efficiently.
Memory compiler	Memory compiler generates free size RAM/ROM by defining the size of bit and word in a memory macro.
Logic synthesis	Logic synthesis tool (Design Analyzer) generates the gate level netlist from VHDL description.
Design rule check (DRC)	Circuit design rule check program verifies any restrictions on connections and indicates any violations.
Customer specified logic separate simulation	When using megafunctions, such as a CPU macro, the resulting circuit can often contain several hundred thousand gates, with the CPU macro alone contributing much to the cell count. Therefore, to develop an ASIC efficiently, simulate the customer specified logic separately and remove any bugs from it before simulating the entire circuit.
Simulation for test circuit	During the production test of a CB-C8 circuit, the same test pattern is used for the entire circuit that was applied to individual megafunction blocks. Simulation of the test circuit confirms that the connections of the test circuit are correct and can be used in production test.
Floor plan	Floor planning tools specify the layout and interconnections of megafunctions and customer specified function blocks. Chip size and wiring length of each net are also estimated in this process.
Calculation of estimated wiring length	This tool calculates the estimated wiring length between blocks, for all the blocks in the circuit. It is done very accurately, taking into consideration the size of the steps used and the block separation in the second layer of the circuit.
Total chip simulation	This step checks whether or not a circuit has problems by simulating the entire circuit, using estimated wiring lengths, calculated from the floor plan.
Power simulation	Power consumption can be simulated by time units. It is recommend that you input a test pattern similar to your actual operation and evaluate average power consumption over time.
Fault simulation	The fault detection ratio of the customer's test pattern as applied to the circuit can be calculated. Cell information which cannot be detected by the test pattern is also output.
Simulation with actual wiring length	Customer specified logic simulation using actual wiring lengths is performed for the entire chip.
IE preparation	When a CPU macro is included, an in-circuit emulator (IE) should be prepared to assist in the development of the application software.

CHAPTER 4 SYSTEM DESIGN

The following items should be considered in the early stages of your CB-C8 design. By doing so, a cell-based system, with all of the required functions may be created efficiently and at a low cost.

4.1 Estimating Power Consumption

4.2 Layout Consideration for Customer Specified Logic Circuit Design

4.3 Test Consideration for Circuit Design

4.4 Debugger Consideration for Circuit Design

4.5 Total Chip Simulation Consideration for Circuit Design

4.6 Estimation and Allocation of Power Supply Pin

4.7 Package Selection

The following pages review these items in detail.

4.1 Estimating Power Consumption

Once the specifications of a cell-based ASIC are set, estimating its power consumption is a crucial first step. If the power consumption of the chip exceeds the power dissipation capability of the package selected, then the designer must either change to a package with lower thermal resistance or make circuit modifications to lower power consumption. These changes can cause a significant delay in a project and generate cost overruns. Estimating power consumption as accurately as possible in the beginning of a design can avoid these costly and time consuming mistakes.

The procedures to estimate the power consumption of cell-based ASICs are as follows:

(1) Estimate the power consumption of each macro (megafunction block, customer specified function block, and I/O buffer) and determine the total.

- For a megafunction block, refer to the specifications of each block in the **CB-C8 Family User's Manual for Megafunctions** or the **CB-C8 Family User's Manual for Memory Macros.**
- For customer specified function block and interface blocks, refer to **10.3 Power Consumption of Functional Cells and Interface Blocks.**

(2) It is likely that the total power consumption estimated in procedure (1) exceeds the allowable power dissipation limit of the package. To come up with a more realistic value, estimate the power consumption of the megafunction blocks that likely will be operating simultaneously. Use this method to ensure that it is still below the power dissipation rating of the package.

Remark: For the allowable power consumption of individual packages, see **9.5 Maximum Allowable Power Consumption for Each Package.**

4.2 Layout Consideration for Customer Specified Logic Circuit Design

When customer specified logic is designed in the CB-C8, generally the wiring lengths between functional cells becomes long in proportion to the scale of customer's specified logic.

In a CB-C8 circuit, the block separation information of the second hierarchy, can be reflected in the layout as group placement.

Therefore, when designing large-scale customer specified logic (more than 10 K gates), it is recommend that this logic be designed into a few groups of several thousand gates each and placed throughout the core of the circuit, depending on the individual functions. The wiring length between some blocks will be longer than that of a single block. However, the internal block wiring lengths will be remarkably shorter.

The program used during simulation to calculate estimated wiring length, does so in a very accurate fashion. Wire lengths are estimated, one by one from the gate scale in each block. This is based on block separation information in the second hierarchy.

First hierarchy circuit diagram

Placement in group can be specified in the block unit.

NA70008H

Customer specified logic
COKE

ROM

Customer specified logic
MIZORO

RAM

CBC8TOP

SHEET1
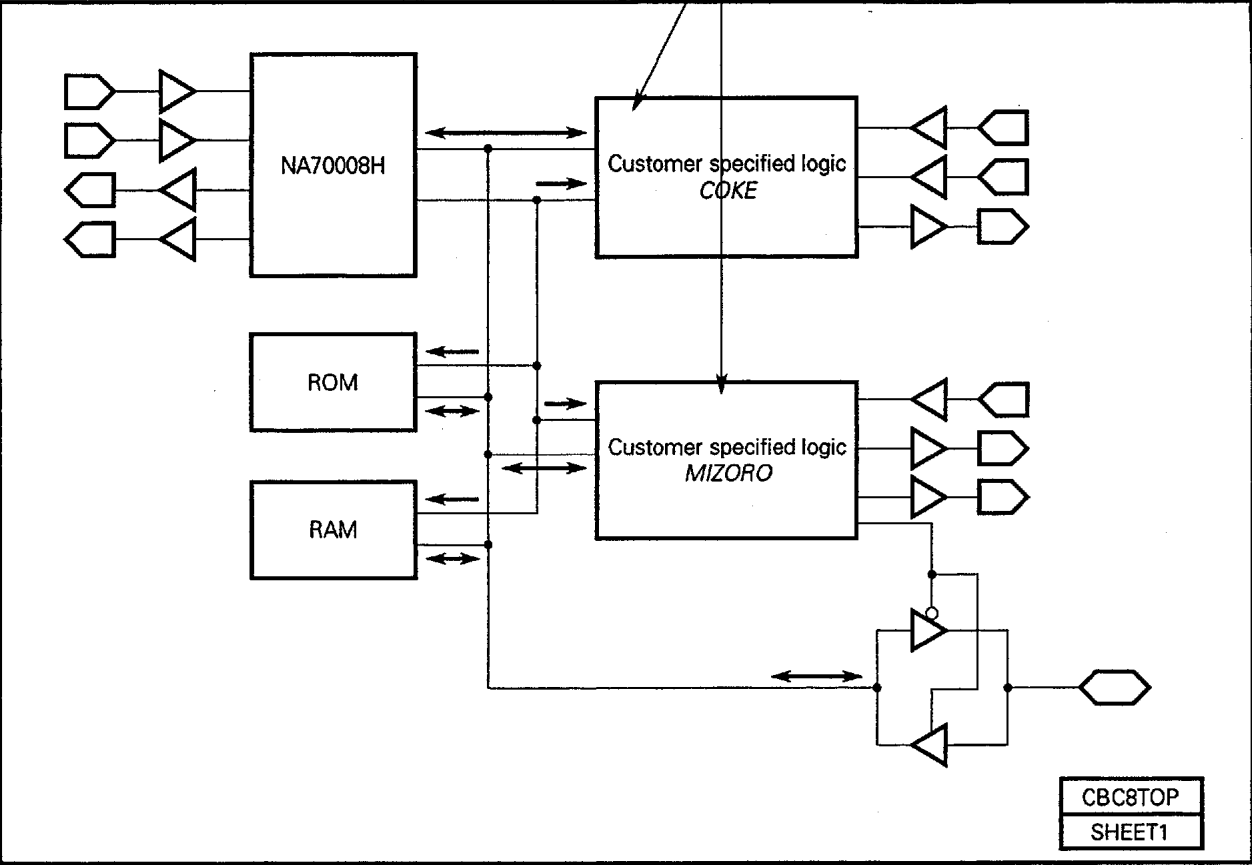
First hierarchy

CB-C8 TOP circuit diagram

Second hierarchy

NA70008H

ROM

RAM

COKE

MIZORO

Third hierarchy

ENO

TOMI

MARU

KUMA

Customer specified logic

Customer specified logic
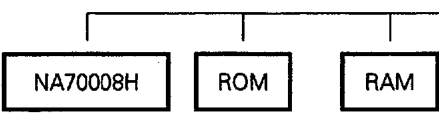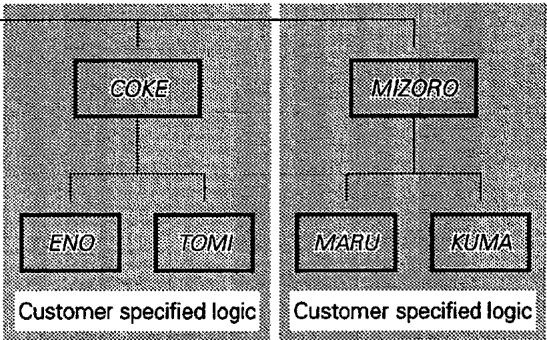
Placement in group and estimation of wiring
length can be performed in this unit.

4.3 Test Consideration for Circuit Design

When a megafunction block is integrated into CB-C8, it must be tested as a separate function block. To facilitate the design of each megafunction test, NEC uses a "test bus" method to check the circuit design, the same as the CB-C7. However, note that there are some different points from the test specification of the CB-C7. The major differences with CB-C7 are as follows:

1) The interface block in the CB-C8 is the one with the test circuit.
2) "SPT" and "LKT" pins of interface block changed to "TMC1" and "TMC2" pins in the CB-C8, respectively.
3) "Leak test mode" in the CB-C7 changed to "LFT test mode" and "Iᴅᴅ test mode".

4.3.1 Megafunction separate test

The procedure to configure the test circuit for megafunctions is described below.

Some megafunctions have unique test circuits. Refer to the CB-C8 Family User's Manual Megafunction section for details.

(1) Megafunction

Megafunction blocks that can be used for most CB-C8 designs have five types of pins, as shown below:

Fig. 4-1 NA70008H Pin Out
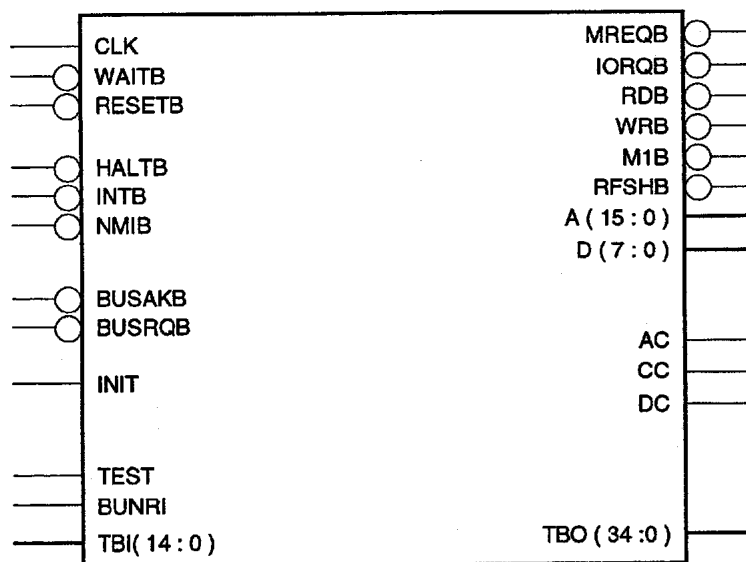
- Normal pins : Pins used for normal operations (e.g. CLK, RESETB)
- BUNRI   : Mode selection pin to select normal mode or test mode
- TEST   : Control pin of the test bus in conjunction with the BUNRI pin
- TBIxx   : Test bus input pin
- TBOxx   : Test bus output pin

As shown in the circuit diagram for the megafunction, NA70008H, when the BUNRI pin is set to LOW, normal pins will be valid. When the BUNRI is set to HIGH, normal input pins become invalid, normal output pins are set to HIGH, 3-state output pins are set to Hi-Z and normal bidirectional pins are set to input mode. These conditions set the test mode.

During test mode (BUNRI = HIGH), when the TEST pin is set to LOW, input test pins (TBIxx) become invalid and the output test pins (TBOxx) are set to high impedance. When the TEST pin is set to HIGH, the input test pins (TBIxx) and the output test pins (TBOxx) both become valid.

Mode selection and pin status is shown below.

Mode Selection		Normal pins				Test-Bus pins		Mode	
BURNI	TEST	Input	Output	3-state Output	Bidirectional	Input	Output		
0	x	Valid	Valid	Valid	Valid	Ignore Note	Hi-Z	Normal Mode	
1	0	Ignore Note	x	Hi-Z	Input Note	Ignore Note	Hi-Z	Test mode	Stand By
	1	Ignore Note	x	Hi-Z	Input Note	Valid	Valid		Test

Note: Hi-Z input is allowed.

Remark: Be sure not to input a high-impedance to functional cells or to the input pins of a megafunction. Any exceptions to this rule, which allows high-impedance inputs to input pins, are described in the **CB-C8 Family User's Manual Block Library** or the **CB-C8 Family Megafunction User's Manual.**

x indicates don't care; Hi-Z represents high-impedance.

(2) Interface block with test circuit

In the CB-C8, the interface blocks incorporate test circuits, as part of each input, output, and bidirectional buffer. The exception to this rule are unique interface blocks, such as oscillation blocks.

As shown in the following figure, there are two kinds of buffers with test circuts; TIN type (xxxxAH) which become input pins in test mode and TOUT types (xxxxAN) which become output pins during test mode.

Fig. 4-2 Example of Interface Blocks with Test Circuit
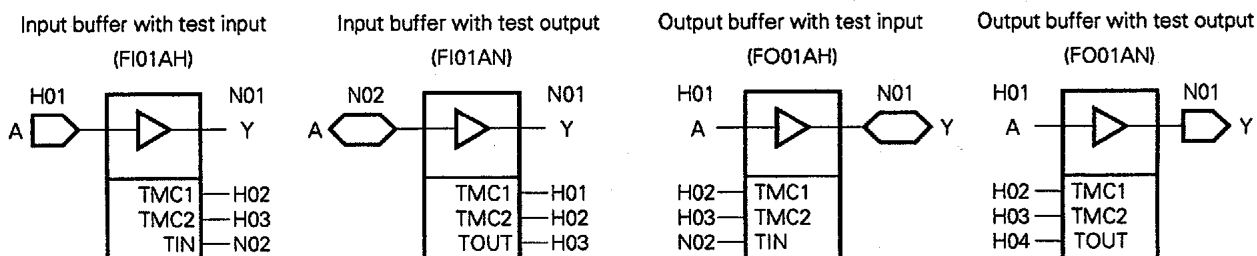
- **Normal pins** : Pins used in normal operations. (e.g. H01, N01)
- **TMC1**   : Test mode selection pin.
- **TMC2**   : Test mode selection pin.
- **TIN**   : Test output pin, which transmits a signal input from an external pin during the megafunction test mode.
- **TOUT**   : Test input pin that receives a signal from the TOUT pin and transmits it to an external pin during the megafunction test mode. (A bus holder is provided to prevent a high impedance state on output test bus lines during the normal mode.)

TMC1	TMC2	Mode
0	0	Normal mode
0	1	LFT (I_{OLH} MIN.) test mode[Note]
1	1	I_{DD} test mode[Note]
1	0	Megafunction test mode

Notes: LFT test mode : Test mode to minimize the output current for simultaneous ON counter-measure at final test.

I_{DD} test mode : Test mode to isolate the pull-up/down resistor, in order to measure the static consumption current correctly during final test.

(3) Circuit design for megafunction separate test

This section describes the procedure for designing a test circuit for use with various megafunctions. A sample circuit is used to illustrate the procedure.

(Example) Circuit configuration:

Megafunction $\left\{\begin{array}{l} \text{NA70008H : 1 block} \\ \text{NA71055H : 1 block} \end{array}\right.$

Customer specified logic   : 1 block

↓

Different modes that need to be set:

① Normal mode

② NA70008H separate test mode

③ NA71055H separate test mode

④ Customer specified logic separate test mode

In CB-C8, be sure to set two lines for the TMC1 and TMC2 control signals of mode selection pin of interface block with test circuit as dedicated test input pins. For the interface block for inputting the TMC1 and TMC2 signals, do not use the block with pull-up/down resistor (when using the block, consult NEC).

At this time, TIN output of TMC1 and TMC2 input interface blocks should be left open.

This is for executing the test with the mode set to LFT test mode or I$_{DD}$ test mode only for interface block as NEC test item in normal mode or customer specified logic separate test mode.

For the test mode setting pin, except for these two lines (test input pins of TMC1 and TMC2), set as follows:

(a-1)   When the number of dedicated pins as test mode setting pins are the smallest:

Input pin for controlling TMC1   : 1 (dedicated) $\left.\begin{array}{l} \\ \\ \end{array}\right\}$ fixed

Input pin for controlling TMC2   : 1 (dedicated)

- -

Input pin for selecting normal mode/test mode   : 1 (dedicated)

Other necessary test mode setting input pin   : M (shared)

---

3 + M pins

From example above,

Normal mode : 1 type

Test mode   : 3 types → realized with M pins

$\quad$ M = log$_2$ (number of test modes) ^{*1} = round-up of (log$_2$3) = 2

$\quad$ *1 ... Round-up under decimal point

In this case, three dedicated test mode setting pins and two shared test mode setting pins are necessary.

(a-2)   When the total number of test mode setting pins are the smallest:

Input pin for controlling TMC1   : 1 (dedicated)

Input pin for controlling TMC2   : 1 (dedicated)

- -

Mode setting input pin   : N (dedicated)

---

2 + N pins

From description on page 14,

the mode to be considered : 4 types → realized with N pins

$N = \log_2$ (number of setting modes to be considered) [2] = round-up of $(\log_2 4) = 2$

[2] ... Round-up under decimal point

In this case, four dedicated test mode setting pins are necessary.

(b) Number of test bus pins (can be used with customer using pin)

First of all, count the number of test bus input pins (TBIxx) and test bus output pins (TBOxx) for each megafunction separately.

Megafunction	TBIxx	TBOxx
NA70008H	15	35
NA71055H	38 (MAX.)	42 (MAX.)

The next step is to find the maximum number of input test bus pins and output test bus pins required. In this example, the maximum number of TBIxx pins are 38 and for TBOxx the maximum number is 42. This means that a total of 80 test bus pins are necessary for the design.

(c) Replacement of interface blocks with test circuit

Based on these test bus pins counted at (b) above, input interface blocks which incorporate test circuits. In this example, it is necessary to input the 38 normal buffers with interface blocks with test circuits (TIN type), and the 42 normal buffers by interface blocks with test pins (TOUT type).

For the pin not connected to the test bus (the pin not used for megafunction separate test), use the interface block with test circuit of TIN type. For these TMC1 and TMC2 inputs of interface block, input the same signal as TMC1 and TMC2 inputs of interface block connected to the test bus (Dedicated test input pins: Signals from TMC1 and TMC2) (see Fig. 4-3).

(d) Number of test bus

To configure the test bus, connect the TIN pin of the interface block with test pin and TBIxx pin of the megafunction. The TOUT pin of the I/O buffer is also connected to TBOxx pin of the megafunction.

Fig. 4-3 Test Bus Configuration
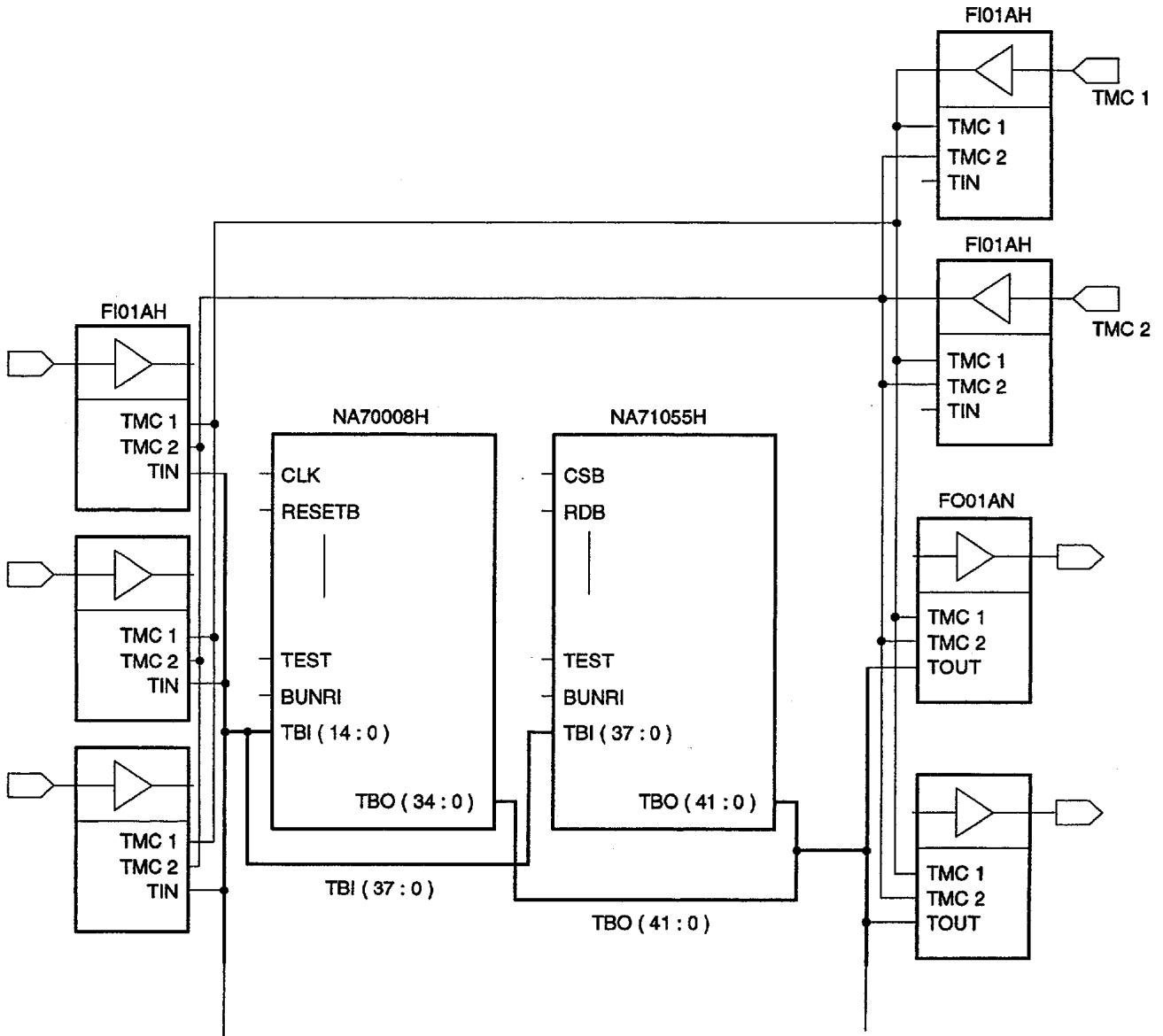
(e) Test Bus Control Circuit Design

Next, create a decoder for setting modes. For example, in circuit (d), to perform a separate test of the NA70008H megafunction, set the control pin of each block as shown in the table below.

Block Type	Mode Selection	State of Control Pin
FO01AN	Test mode	TMC1=1, TMC2=0
NA70008H	Test mode Test bus : valid	BUNRI = 1, TEST = 1
NA71055H	Test mode Test bus input : ignore Test bus output : Hi-Z	BUNRI = 1, TEST = 0

Under these conditions, a separate test for the NA70008H is possible. A test signal input from the external pin is applied to the test bus input pin (TBIxx) of the NA70008H through TIN. A signal from the test bus output pin (TBOxx) is applied to the external pin through the TOUT pin of FO01AN. The settings for the test control pins for each test are summarized below.

Tested Block		Interface block		NA70008H		NA71055H	
		TMC1	TMC2	BUNRI	TEST	BUNRI	TEST
Normal operation		0	0	0	×	0	×
NA70108H		1	0	1	1	1	0
NA71055H		1	0	1	0	1	1
Customer specified logic		0	0	1	0	1	0
	Note	0	1				
LFT	Note	0	1	0	×	0	×
IDD	Note	1	1	0	×	0	×

Note: Used when testing with an NEC tester.

Remark: For the test of customer specified logic, refer to **4.3.3 Test consideration for customer specified logic circuit.**

The test circuit, which can perform the separate tests of the megafunctions just described, is shown in Fig.4-4.

Fig. 4-4 Test Bus Control Circuit
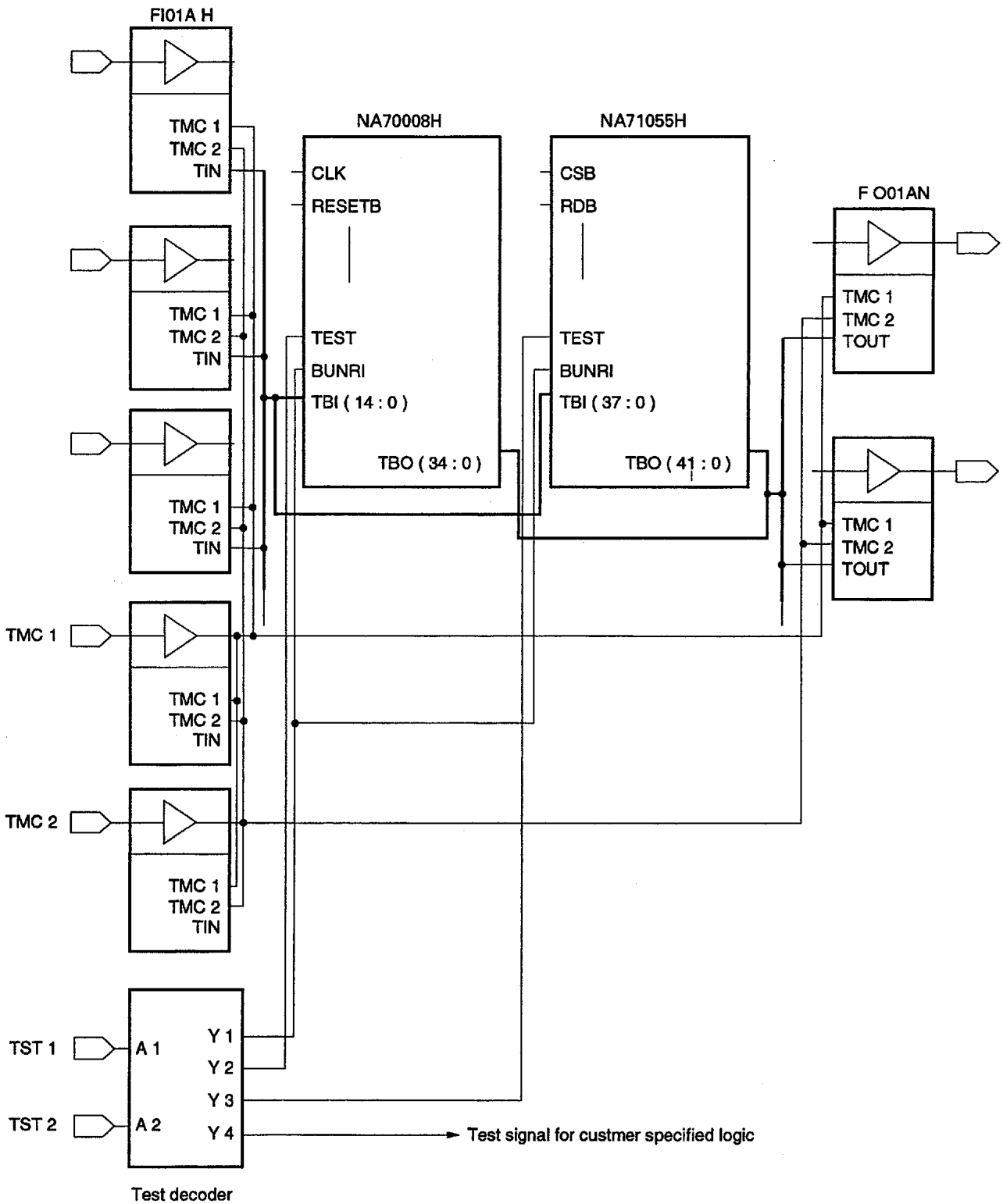
Fig. 4-5 shows an example of the decoder circuit used for setting the test mode (in actual operation, consideration for fan-out adjustments may be necessary).

Fig. 4-5 Example of Decoder Circuit for Setting Test Mode

TMC1	TMC2	A 1	A 2	Tested block
0	0	0	0	Normal operation
0	1	0	0	LFT
1	0	0	1	NA70008H
1	0	1	0	NA71055H
1	1	0	0	IDD
0	1/0	1	1	Customer specified logic
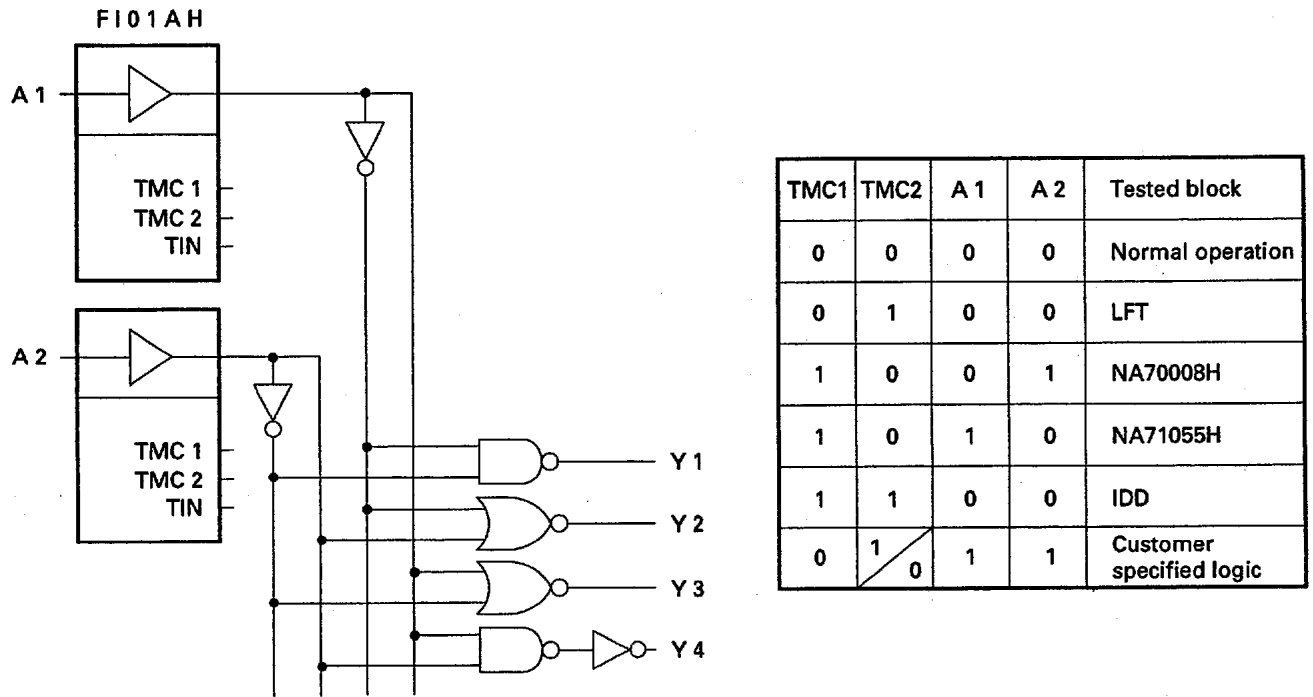
4.3.2 Megafunction control pin

Megafunctions have control pins to control the signal direction or state of their bidirectional pins and the 3-state signals that exist in their corresponding standard products.

(1) Megafunction control pin

There are four types of pins for megafunctions. In the case of the NA70008H, examples of each are shown in parenthesis.

- Input pin (e.g. CLK)
- Output pin (e.g. HALTB)
- Bidirectional pin (e.g. DATA BUS)
- 3-state output pin (e.g. WRB: output is high impedance during hold request.)

There is also a control pin that indicates the status of the bidirectional pin and the 3-state output pin. The relationship between the control pin, and the status of the bidirectional pin, and the 3-state output pin are tabulated below.

	Control pin	Status
Bidirectional pin	H	Input
	L	Output
3-state pin	H	High-impedance
	L	Output active

(2) Using the control pin

(a) Control of bidirectional buffer or 3-state buffer

Control pins are used to control a bidirectional buffer or a 3-state buffer as shown in the following circuit.

Fig. 4-6 Control of Bidirectional Buffer or 3-State Buffer
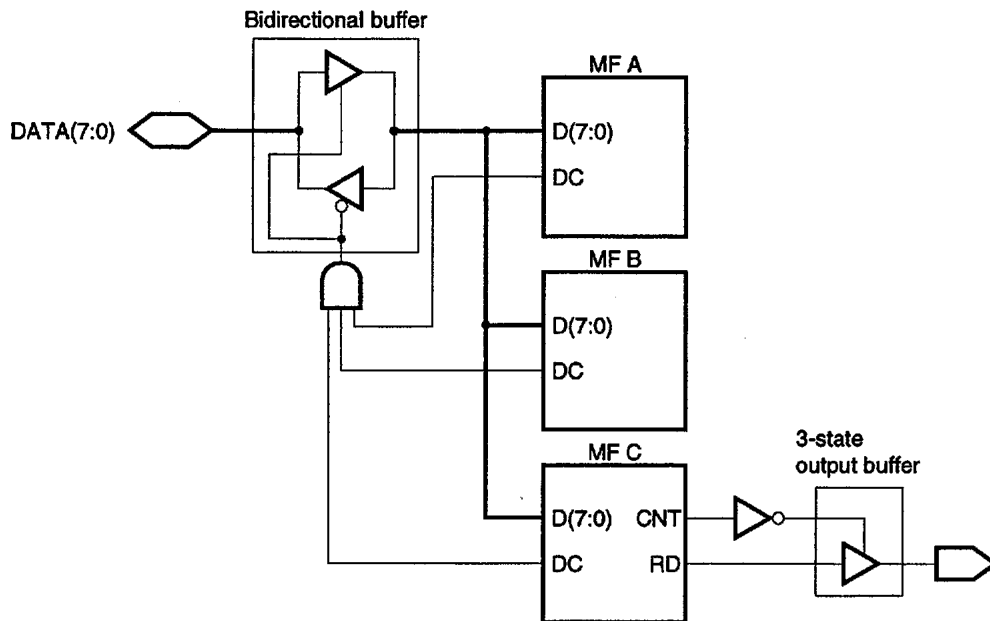
Remark DC and CNT are control pins.

(b) Preventing high impedance output

The 3-state and bidirectional pins of a megafuction have some parts which are set to high-impedance (Hi-Z) during megafunction separate test. It may be necessary to avoid this high-impedance state when testing the entire circuit. The following is an example of a circuit that may be used to prevent the outputs of the megafunction from being at a high impedance. At present, the following CB-C8 function blocks do not have a problem during test, even if a Hi-Z state exists when setting the value of the specific input pin.

AND/NAND type: F312, L312, F332, F313, L313, F333, F302, L302, F322, F303, L303, F323
OR/NOR type: F212, L212, F232, F213, L213, F233, F202, L202, F222, F203, L203, F223
Latch type: L901, L902

When inputting the Hi-Z state, be sure to cut-off the generation and propagation of the "X" output due to Hi-Z by other input signals. (In the case of a gate, define the output with another input signal. In the case of a latch, hold the latch state, etc.)

In the event that these precautions are not enough, it is possible that leakage currents will flow and cause a default. If you prefer to use a function block that is not listed in this document, please contact NEC to verify its compatibility. There may be some block functions that cannot be used in a CB-C8 design.

Fig. 4-7 Example of How to Prevent High Impedance Output
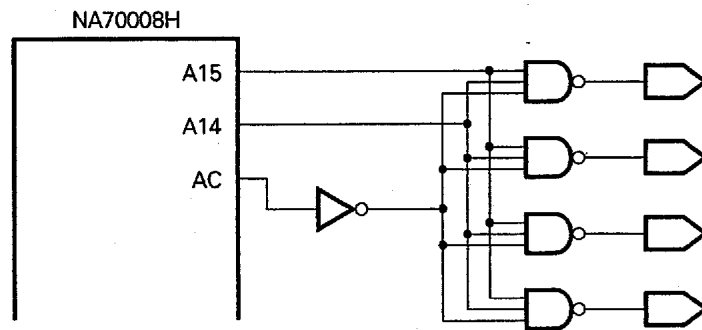
Remark The control pin cannot be used for any other purpose than what is described above.

4.3.3   Test consideration for customer specified logic circuit

The following three points on testability need to be considered when designing a customer specified logic circuit.

- Testability of the customer specified function block must be high.
- The number of test pins should be as small as possible.
- The number of test patterns should be as small as possible.
  To determine the limit on the number of test patterns, refer to 7.3 Limits to Number of Test Patterns.

To meet this test pattern restriction, it is recommended that any customer specified logic, incorporate its own test circuit structure, so it can be tested separately.

In this regard, note that a customer specified function block cannot be connected to the test pins: TIN and TOUT. If these pins are used, the tester cannot judge when a problem is found, regardless of whether the problem is caused by a megafunction or by the customer specified logic.

There will be no test problem if the customer specified function block is completely isolated and can be simulated from external pin separately. An example of a suitable test procedure for a customer specified function block is as follows:

(1) Set all other megafunctions to standby in test mode (BUNRI = 1, TEST = 0).
     Set the interface blocks with the test circuit to normal mode.

(2) Prepare one signal pin as a separate test for just the customer specified logic.
     For details, refer to **4.3.1 (3) Circuit design for megafunction separate test.**

(3) Except for normal pins, add test pins and any required test circuits for customer
     specified logic as shown on page 22.

- UBUNRI : Mode selection pin to select normal mode or test mode.
- UTEST : Control pin of the test input bus in conjunction with the BUNRI pin.
- UTBIxx : Test bus input pin equivalent to test bus input pin of megafunction.

Mode Selection		Normal pins			Test-Bus pin	Mode	
UBUNRI	UTEST	Input	Output	Bidirectional	UTBIxx Note 2		
0	x	Valid	Valid	Valid	Ignore	Normal Mode	
1	0	Ignore Note 1	Valid	Input Note 1	Ignore	Test mode	Stand By
	1	Ignore Note 1	Valid	Valid	Valid		Test

Notes: 1. Input high-impedance is allowed.
2. Input pin only. Not including the input portion of bidirectional pin.

(4) Connect the normal output pin of the input buffer with the test circuit and the test bus input pin (UTBIxx) of the customer specified logic.

(5) Connect the output of the selector and the normal input pin of the output buffer with the test pin. Connect the normal buffer signal to one of the input pins of the selector, and connect the output of the customer specified logic to another input pin of the selector. In the separate testing of the customer specified function block, the test signal must be connected to the control pin of the selector in order for the output of the customer specified logic to be enabled during the test.

By using the above procedure, most customer specified function blocks can be accessed directly from the external pins. This will make it much easier to execute the separate simulation of a customer specified function block.

4.4 Debugger Consideration for Circuit Design

NEC does not provide a software debugger for its CPU macros, such as the NA70008H. Therefore, a designer needs to develop an emulator by using a general-purpose emulator and a standard LSI chip.

To meet this need, the CPU core for the CB-C8 has some extra pins which a standard CPU does not have. For example, there is a bidirectional buffer control pin on the NA70008H. When creating a CB-C8 circuit using these macros, pay attention to the correspondence of the pins.

For details, refer to **CHAPTER 8 CREATING DEBUGGER.**

4.5 Total Chip Simulation Consideration for Circuit Design

Refer to **CHAPTER 6 TOTAL CHIP SIMULATION.**

4.6 Estimation and Allocation of Power Supply Pin

In this section, the number of power supply pins and their allocations are described.

When including analog circuits, analog-only power supply pins are also necessary, in addition to the pins described below.

4.6.1 Estimating the number of power supply pins

Estimation of the number of power supply pins should be performed by the following procedure:

(1) First, estimate the required number of supply pins by each item below.

    (a) Preventing simultaneous switching of output buffer

        Refer to **9.2 Power Supply Pin Location and Oscillator Allocatable Pins** and **9.3 Restriction on Simultaneous Output Buffer Operation.**

    (b) Power supply for DC drive (when including DC drive pin)

        Simultaneous switching restrictions of output buffer is in general for AC operation, but also for DC operation, that is, DC current value in simultaneous switching is limited. If there is no DC drive pin, there is no need to consider this regulation.

        This subject is now under discussion. Please contact NEC.

    (c) Oscillation circuit

        One V_{DD} pin and one GND pin are required for one oscillation circuit.

(2) Next, estimate the total number of power supply pins.

In estimating the total number of power supply pins, the power supply pin can be used for both DC drive circuit and for preventing simultaneous switching. The total number of power supply pins can be calculated by the following formulas.

$$\boxed{\text{Total number of V}_{DD} = \text{V}_{MAX} + \text{V}_{OSC}}$$

V$_{MAX}$: Either the number of V$_{DD}$ pins for DC drive or for preventing simultaneous switching whichever is larger.

V$_{OSC}$: Number of V$_{DD}$ pins for oscillation circuit

$$\boxed{\text{Total number of GND} = \text{G}_{MAX} + \text{G}_{OSC}}$$

G$_{MAX}$: Either the number of GND pins for DC drive or for preventing simultaneous switching whichever is larger.

G$_{OSC}$: Number of GND pins for oscillation circuit

4.6.2 Concept of power supply allocation

Consider the following items in allocating power supply pins (V$_{DD}$, GND):

(1) When there are many DC drive output buffers, allocate GND pins (for I$_{OL}$) or V$_{DD}$ (for I$_{OH}$) adjacent to or around the output buffers.

(2) When there are many simultaneous switching buffers, allocate GND pins (for H → L change) or V$_{DD}$ pins (for L → H change) adjacent to or around the output buffers.

(3) When there is an internal oscillation circuit, allocate power supply pins on both sides of the oscillation circuit as shown in Fig. 4-8. (Depending on the position of oscillation circuit, package type, and the step size used, non-connected pins may be placed adjacent to the oscillation circuit. In this case, allocate the V$_{DD}$ or GND pin on both sides of the non-connected pins. When the existing V or GND is allocated adjacent to the oscillation circuit, allocate the lacking V$_{DD}$or GND to the other side.)

Be sure not to allocate pins, such as a reset pin, near the oscillation pins, due to the fact that it may cause noise.

Fig. 4-8 Allocation of Power Supply Pins
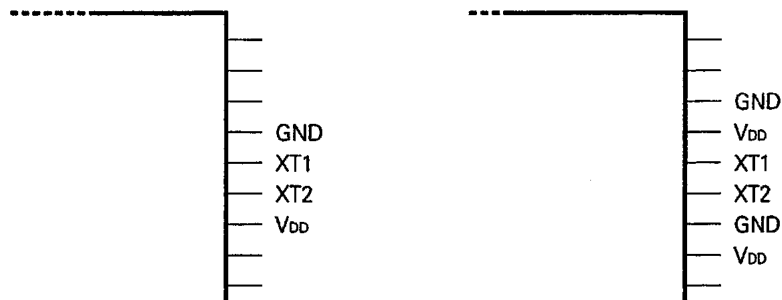
4.7 Package Selection

Consideration should be given to the following notes on selecting packages:

(1) The power consumption calculated in **4.1 Estimating Power Consumption** should be the same as or lower than the allowable power consumption of the package.

(2) When including a megafunction, it should satisfy the number of pins calculated in **4.3 Test Consideration for Circuit Design.**

(3) The number of power supply pins should satisfy the number calculated in **4.6 Estimation and Allocation of Power Supply Pin.**

(4) Circuit scale provided in **9.7 Step Size and Package Availability** should be satisfied.

(5) When including an analog master, non-connected pins may generate depending on macro type. Take this into consideration when discussing the number of interface blocks.

CHAPTER 5 CIRCUIT DESIGN

5.1 Customer Specified Function Block Design

The CB-C8 can integrate a circuit of several hundred thousand gates in NAND gate conversion into one chip. Therefore, when designing such a large scale circuit, it should be treated in accordance with the design techniques normally associated with any large scale integrated circuit. Synchronous circuits and circuits including asynchronous circuits, which are often used in gate array and standard cell designs, should be avoided.

The following procedures should be considered for use in the design of any customer specified function blocks in a CB-C8 cell-based ASIC:

(1) A multi-phase clock or single-phase clock synchronous design is recommended. In principle, do not create any asynchronous circuits. When creating the single-phase clock synchronous circuit, be sure to use clock tree synthesis[Note 1].

(2) Do not use the "set" or "reset" functions of a latch or flip-flop (F/F) for any purpose other than initialization (Note that the RS-latch is an exception.).

(3) Unify the trigger timing of any state machines[Note 2].
    (In the case of D-F/Fs, unify them to the F/F which latches data at the rising edge of a clock input.)

(4) Design should be modular.

(5) The interface between modules should be standardized.

Notes: 1. Clock tree synthesis is a program to keep down the relative skew that may exist when laying out the clock line in a high-drive buffer tree structure. It can be used by implementing the FCTS (function block). Pay attention to the TAT.

2. "State machine" represents a block (F/F, latch, etc.) which has the ability to record its own state.

5.1.1 Synchronous circuit

Asynchronous circuits are not recommended for a CB-C8 design, because such circuit configurations tend to cause malfunction due to clock skew [Note]. Design all circuits using multi-phase clock technique or single-phase clocked circuit using the clock tree synthesis.

> **Note:** When clock signals, derived from the same clock source are input to multiple F/Fs, some buffers may need to be added to meet the fan-out restrictions. The delay caused by such buffers or wirings may shift the clock timings of the F/Fs. This phenomenon is called "clock skew." When clock skews are generated, time margin for set-up and hold times are insufficient, causing malfunction.

(1) Asynchronous circuit

In principle, asynchronous circuit should not be created.

Creating a circuit sure to operate correctly regardless of the delay time due to wirings is allowed.

(2) Synchronous circuit with multi-phase clock

If there is no problem on processing speed, using a synchronous circuit structure with a multi-phase clock is highly recommended. Usually, designing with synchronous circuits is not popular, because it is more difficult than using asynchronous circuits. Here, the general methods commonly used by various LSI manufacturers are described.

The multi-phase clock, shown in Fig. 5-1, is the most popular method for designing general-purpose LSI circuits (such as a CPU). For example, when a CPU specifies three clocks per state, such a CPU is considered to use a 3-phase clock.

Fig. 5-1 Example of 4-Phase Clock
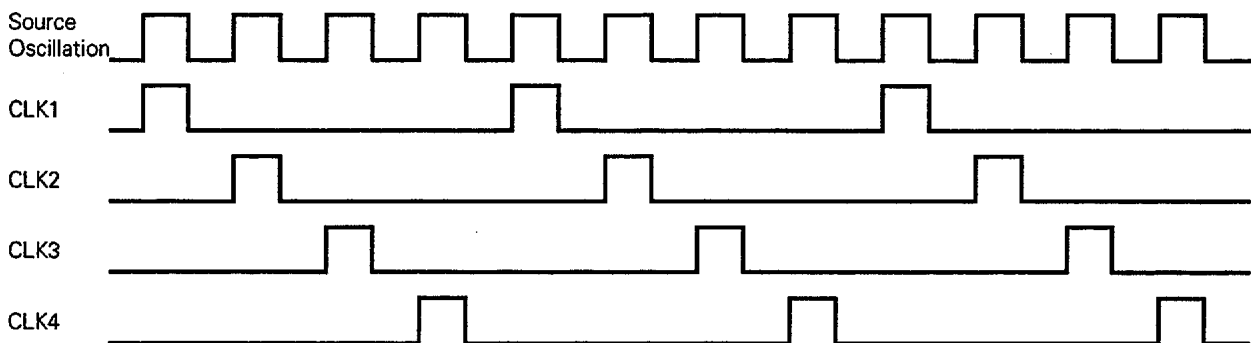
Using a multi-phase clock provides several advantages, as listed on the following pages.

(a) Easy assurance of set-up and hold time for a latch or F/F

As shown below, it is easy to secure the set-up and hold times of latches by using CLK1 and CLK2 alternately. For example, in the case of Fig. 5-2, the set-up time for latch 2 is the "Source Oscillator Frequency - Delay Time of the Combined Circuit A".

Fig. 5-2 Assurance of Set-up and Hold Times for Latch
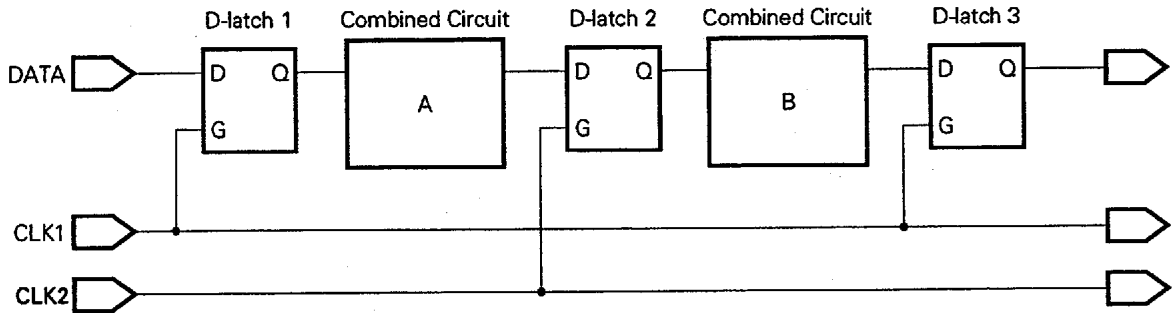
If the delay time of combined circuit A is too long to secure the set-up time of latch 2, then it may be necessary to break out combined circuit A into two parts, as shown in Fig. 5-3. By inserting another latch in between the separated circuit, it is possible to secure the setup time of latch 2. This same approach is also effective for securing the hold time.

Fig. 5-3 Example of Divided Circuit
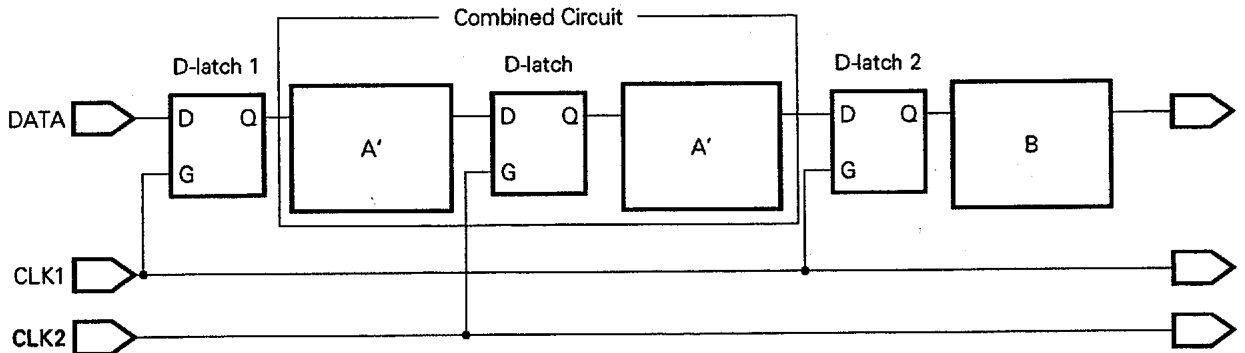
(b) When constructing a complicated circuit, it is possible to simplify the circuit by having each block share the timing tasks.

In a complex circuit, the number of gates can be reduced as compared with the use of a single-phase clock.

Fig. 5-4 shows the case where a 3-phase clock is used to compose a circuit which loads data serially from the ROM, and adds it to stored data sequentially.

Fig. 5-4 Adder Circuit (3-Phase Clock Design)
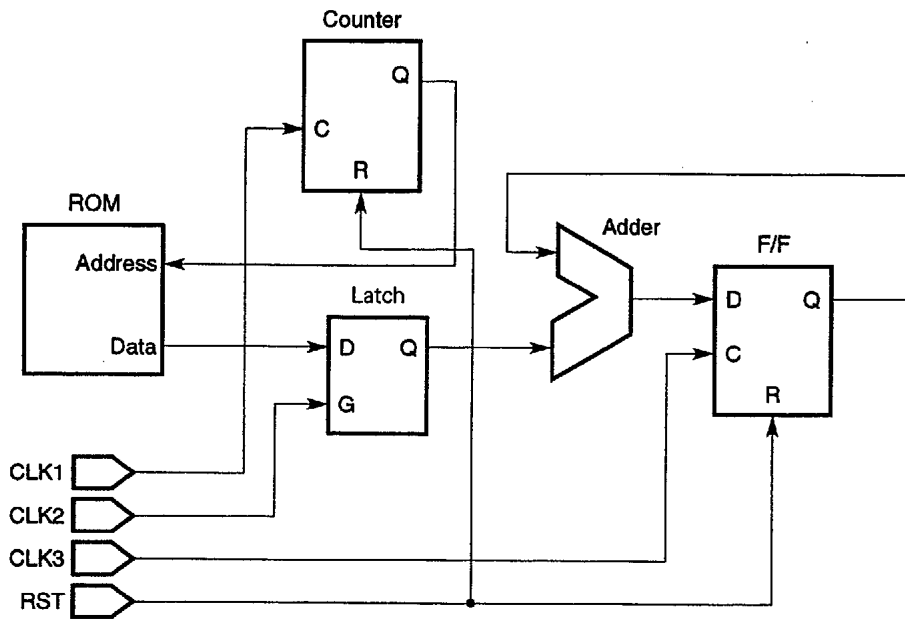
If one uses a single-phase clock to design the same function as above, the circuit will get more complicated as the number of gates increases, as shown in Fig. 5-5.

Fig. 5-5 Adder Circuit (Single-Phase Clock Design)
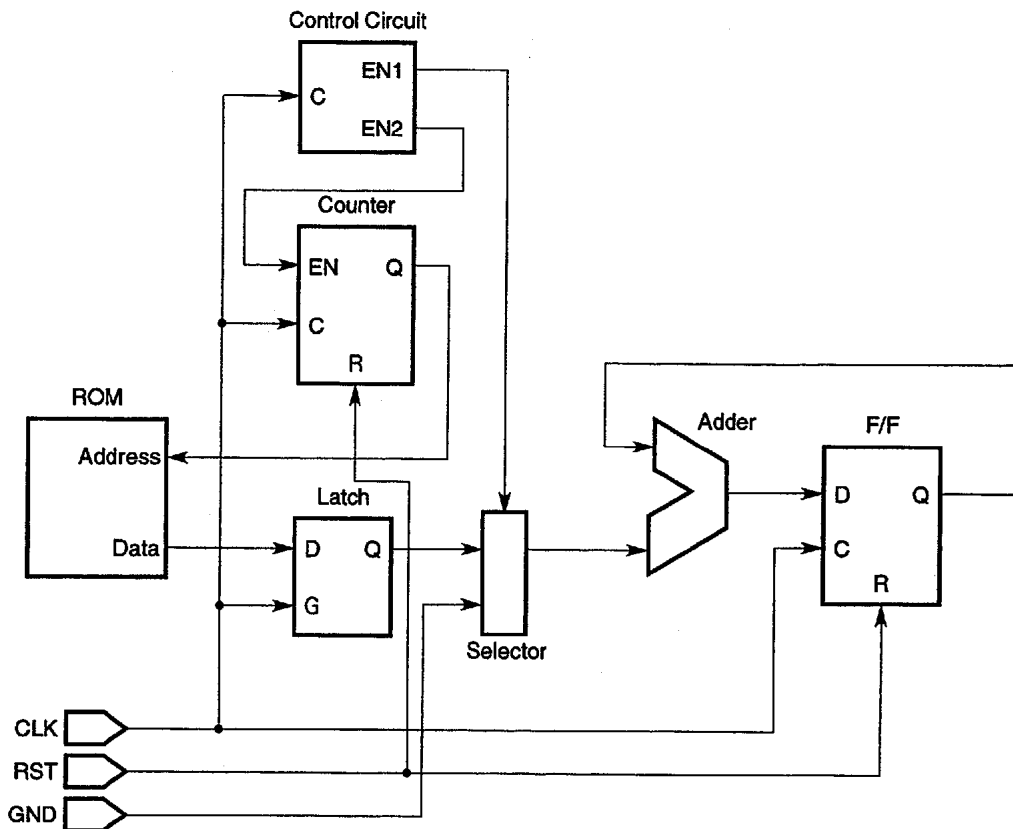
(c) Process (Technology) Independent Design Is Possible

When designing with synchronous circuit using multi-phase clock techniques, process technology affects only the highest clock frequency, because the set-up and hold times of a F/F are secured without the use of delay gates.

In the circuit shown in Fig. 5-6, which is often used in 74LS series designs with a single-phase clock, the hold-time of F/F (a) is ensured by delay gate (b). With a change of technology, the delay time at delay gate (b) is changed and the hold time of the F/F may not be secured.

Fig. 5-6   Circuit Used in the Design Using 74LS Series
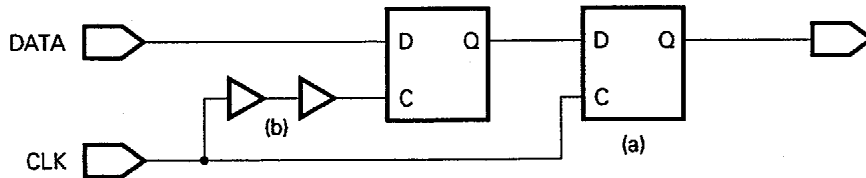
In the circuit shown in Fig. 5-7, which uses a multi-phase clock, the hold time of F/F(a) is independent of technology because it is secured at the "Rise of CLK2 Clock - Rise of CLK1 Clock".

Fig. 5-7   Circuit Using 2-Phase Clock
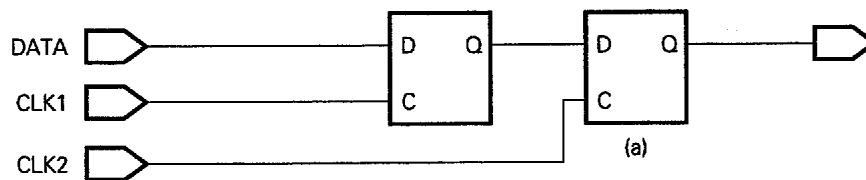
┌─ **Precautions in Using Multi-phase Clocks** ─────────────────────────
The greater the number of clock phases that can be introduced into a circuit, the easier the overall circuit design becomes. However, adding phases to a clock slows down the overall speed of a system. Therefore, a compromise is required. In general, it is best to implement a desired function with the least number of phases.
└──

(3) Single-phase clocked circuit

To reduce clock skew, clock tree synthesis techniques should be used in your CB-C8 design.

If clock tree synthesis is not used, it will take a long time to converge the simulation after placement and routing has been completed.

For details on clock tree synthesis, refer to **5.1.2 Clock tree synthesis**. The single-phase clocked circuit image is shown in Fig. 5-8.

Fig. 5-8 Single-phase Clocked Circuit Image
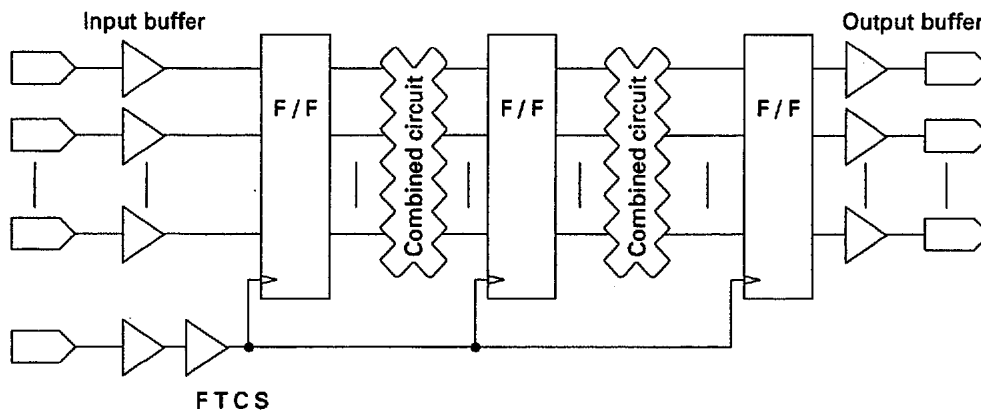
5.1.2 Clock tree synthesis

(1) Clock tree synthesis is a program to minimize the relative skew of clock inputs to each block, by making a clock line high-drive buffer tree structure as part of the chip layout. Clock tree synthesis (high-drive buffer tree) is synthesized at layout to the output net by using a virtual function block (fan-out = ∞) called "FCTS" on the circuit.

In principle, only one "FTCS" can be included in a circuit (for use of two or more "FCTSs", please contact NEC).

Fig. 5-9 shows an example of clock tree synthesis using a a clock line high-drive buffer tree structure.

Fig. 5-9 Clock Tree Synthesis Circuit
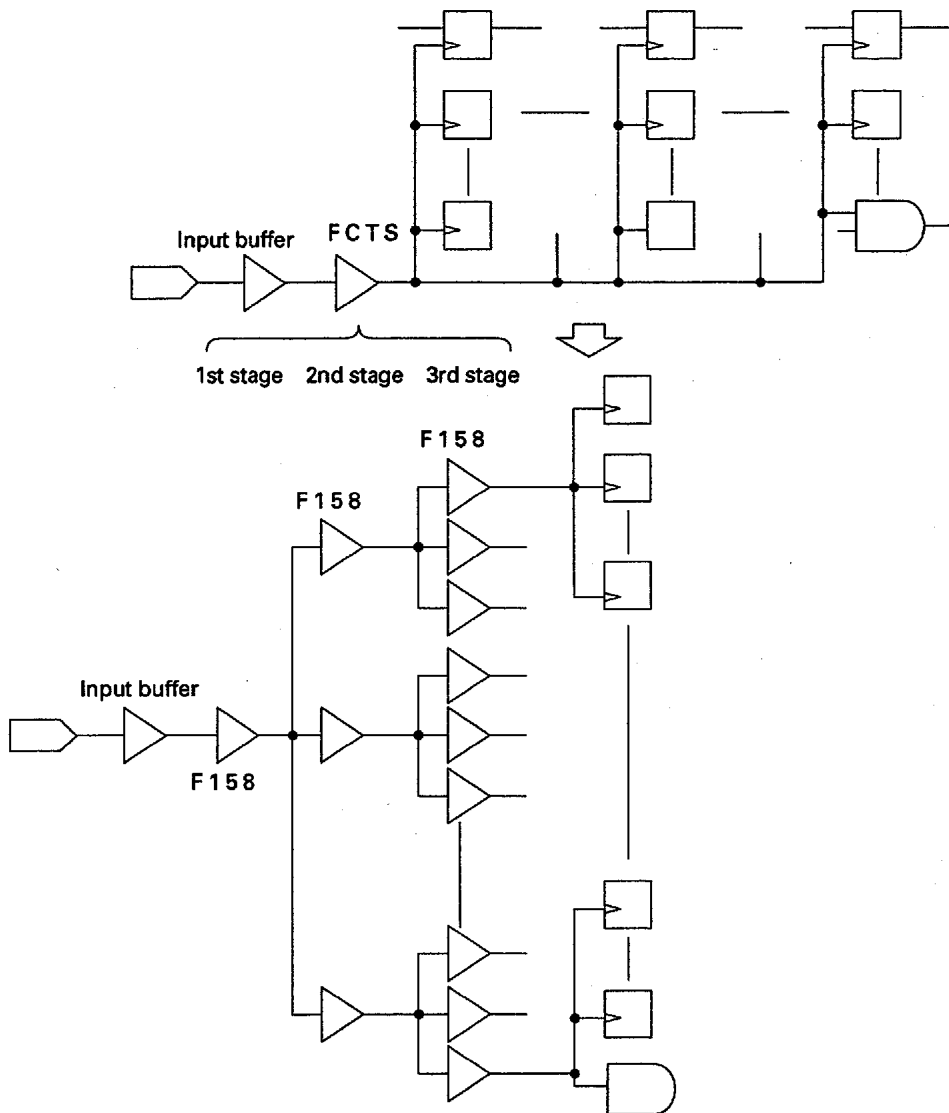
(2) The clock skew value and reference delay value when using clock tree synthesis
in a CB-C8 design is as follows:

±250 ps or less (V$_{DD}$ = 3.3 V ±0.3 V, T$_A$ = –40 °C to +85 °C)

The absolute delay time of a clock tree can be guaranteed when the circuit is simulated using actual wiring
lengths. Use the following table as a reference or standard for design.

Table 5-1 Delay Time Reference Value of FCTS Clock Tree (TYP.)

Number of blocks connected to FCTS output	B18~D16	D55~F34	F74~H33	H72~K90
~ 1280	1.75 ns	1.95 ns	2.15 ns	2.40 ns
1281 ~ 2560	1.80 ns	2.05 ns	2.25 ns	2.50 ns
2561 ~ 5120	1.90 ns	2.20 ns	2.35 ns	2.70 ns
5121 ~	2.15 ns	2.45 ns	2.70 ns	3.05 ns

These values are not guaranteed. Their distributions tend to be as follows:

MIN. value = TYP.value × 0.6

MAX. value = TYP.value × 1.8

| Caution! |

Be aware that during simulation with estimated wiring length, the above values are not used; rather use the following values for simulation purposes.

Table 5-2

Path	Intrinsic (ns)			Extrinsic (ns/pF)		
IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
(LL)	0.797	1.135	1.766	0.0014	0.0020	0.0034
(HH)	0.767	1.066	1.625	0.0016	0.0025	0.0043

(3) Notes on using clock tree synthesis

① Consideration of circuit overhead is necessary. Overhead can be estimated with the following formula. Confirm that there is sufficient margin with the number of grids required before using.

| Number of clock buffers : B = 1 + 8 + N/40 |

N ··· Number of blocks connected to FCTS

Number of grids can be calculated by the following formula: (from F158 = 23 grids)

| Number of overhead grids = 23 × B [grids] |

② When estimating power consumption, take into consideration that the above buffers operate at the clock frequency.

③ In the layout process, as NEC synthesizes the clock tree, there is a possibility that an additional week will be required. This represents the period of time required to get data of the complete simulation with estimated wiring length to data output using the actual wiring delay.

④ In principle, the number of FCTS that can be used is one.

⑤ When simulating actual wiring length, the delay value of the F158 clock tree is distributed at each branch delay of the FCTS block. Therefore, when simulating actual wiring length, the simulation is executed using the same (using FCTS block) netlist.

⑥ Clock tree synthesis controls the relative delay of the clock line, but not the absolute delay. The absolute delay may differ significantly from the expected delay (the above reference value and estimated wiring length delay) depending on the circuit configuration and chip size. When creating the test pattern, to avoid test pattern contention, be careful not to change the valid edge of the clock tree input signal and other signals so they occur at the same time.

5.1.3 Set and reset of latch and F/F

Basically, set and reset of a latch and F/F can not be used for any other signal but initialization (except for RS-latch). The reasons are:

(1) ATGs (Automatic test generators) such as scan path, cannot be used effectively.
    (Remark in the existing CB-C8, the scan bus presently cannot be used.)

(2) If a signal path becomes complicated, circuit verification becomes considerably more difficult and can cause improper verification. In designing a large scale circuit, to reduce the verification process and avoid bogus verification, the above method for initialization is recommended.

(3) A circuit depending on process technology (such as delay gate to assure the minimum pulse width of a reset) is likely to be configured.

A circuit, such as the typical 74LS circuit as shown in Fig. 5-10, should not be used in a cell-based design. In general, the circuit shown in Fig. 5-11 is preferred.

Fig. 5-10 5-Bit Counter (Poor Example)
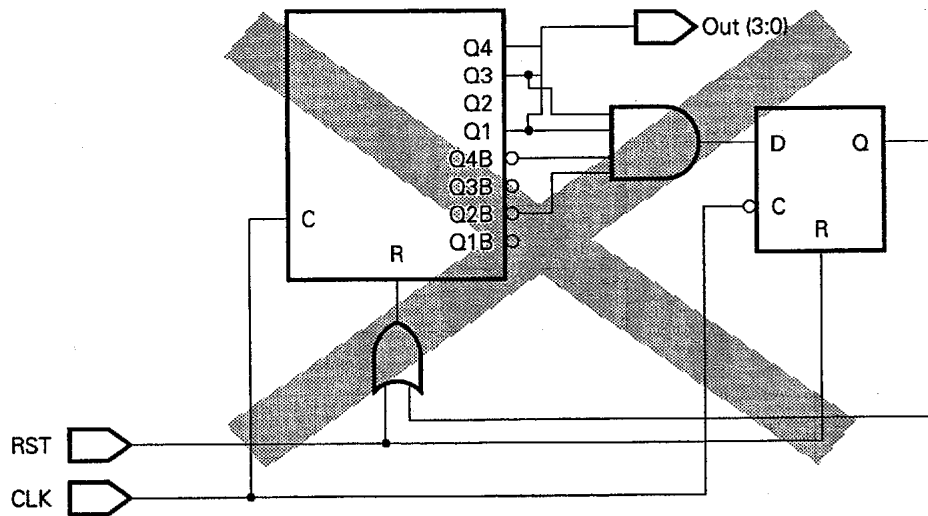
Fig. 5-11 5-Bit Counter (Good Example)
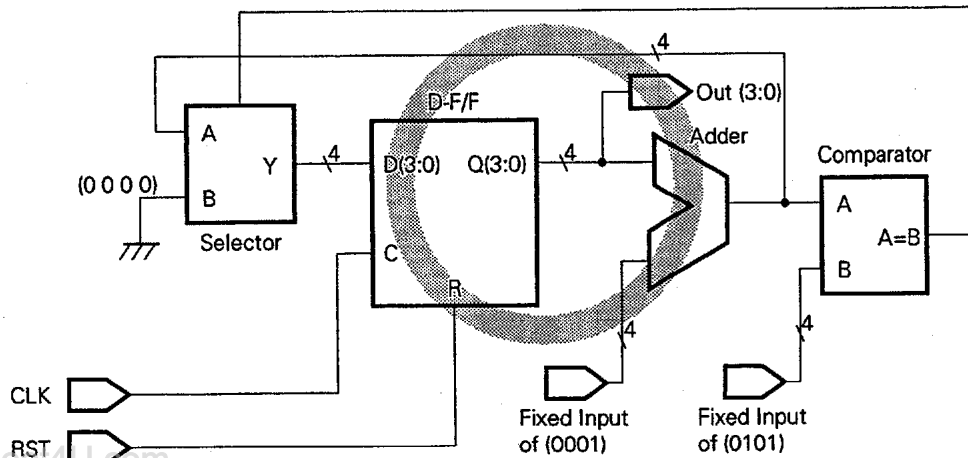
5.1.4 Modular design

When designing an LSI circuit, it is preferable to make the design modular for efficiency. This section describes precautions that should be observed when designing in a modular fashion.

Interface Standardization Between Macros

The most serious problem encountered in a modular design is dealing with the mismatches that result with separately developed macros, as they are combined to form larger building blocks. To solve this problem, it may be necessary to apply standardized interfaces between the macros.

In Fig. 5-12, transmitting "out" data is therefore completed only after latching with CLK2. Similarly, receiving any "in" data occurs only after latching with CLK1. Therefore, potential bus contention exists when transferring data between macros. This is avoided when the interface for transmitting data between macros is standardized.

Fig. 5-12 Standardization of Interface between Macros
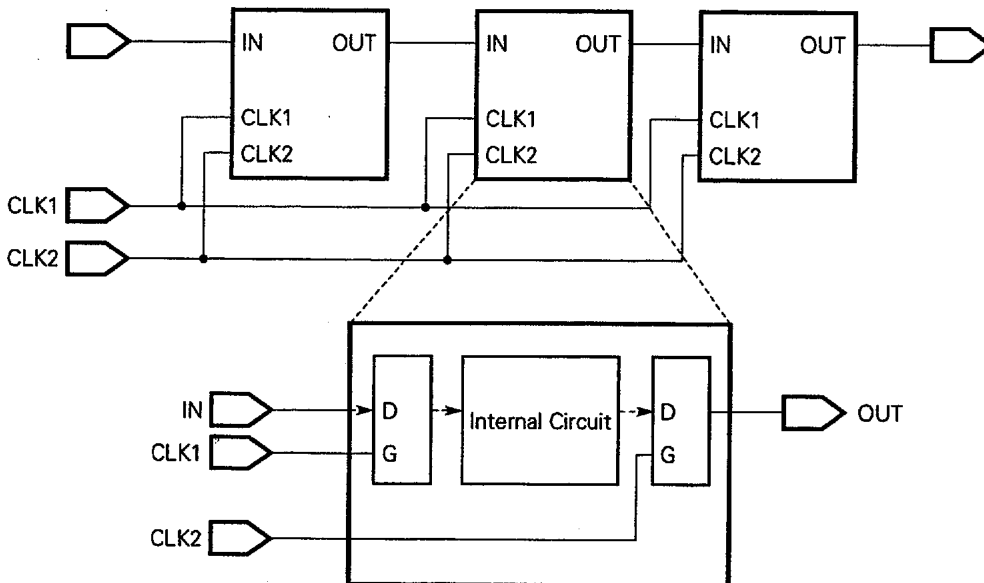
In the example shown in Fig. 5-12, only the control bus of CLK1 and CLK2 has been standardized upon. An example standardizing all buses is shown in Table 5-3.

Table 5-3 Standard Bus Interface for Single-Chip

Pin name	Active level	Pin function
CLK1		Internal system clock 1
CLK2		Internal system clock 2
UA (15:0)		Address bus
UD (7:0)		Data bus
URDB	L	Read signal
UWRB	L	Write signal
URST	H	Reset signal
URDY	L	Ready signal of other macro
UALE	H	Address strobe signal

Modular design also calls for each bus to follow a standard. When standard bus interfaces are defined for all buses, it is possible to reuse macros because all the bus interfaces are standardized.

Fig. 5-13 Modular Design

Sequence controller macro   Serial interface macro   Numerical data processor macro
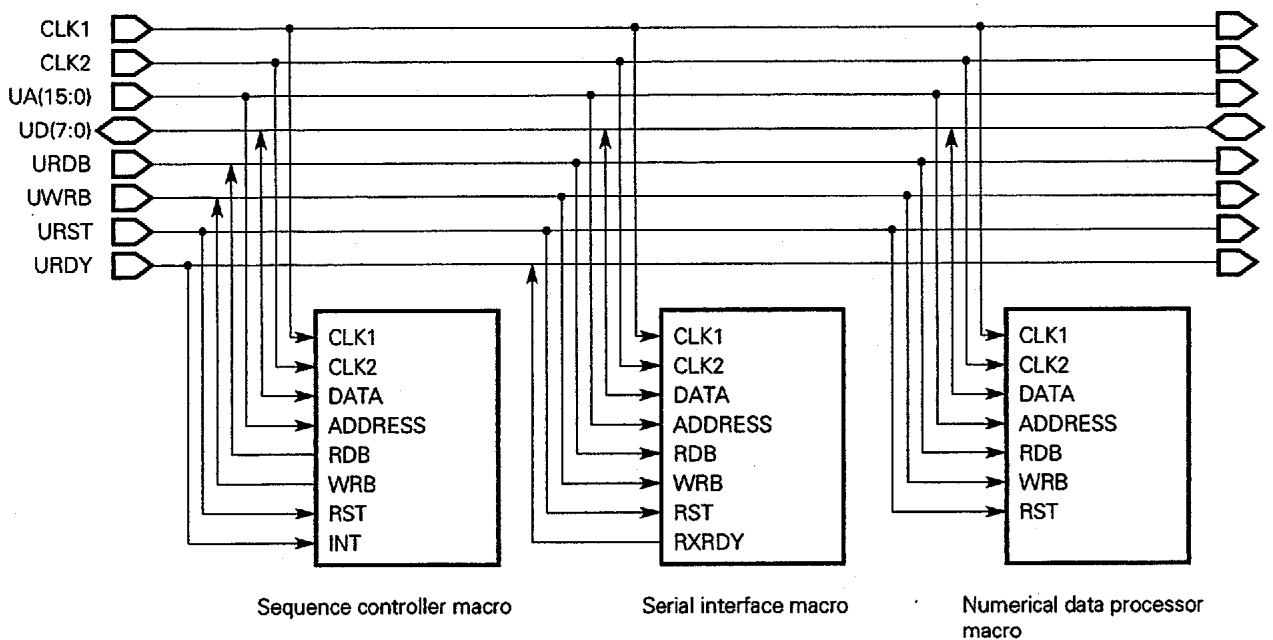
5.2   Notes for Developing High-Speed Circuits

An N-channel transistor can generally carry a larger current than a P-channel transistor. A NOR gate, composed of P-channel transistors in series, has a load drive capability that is lowered for rising outputs. A NOR block in a CB-C8, for example, is slower and has less fan-out capability than a NAND block.

When designing a high-speed circuit, the following rules should be observed:

(1)   Use NAND type normal blocks whenever possible.
(2)   Reduce the load capacitance whenever possible. Use 1/3 to 1/2 of the upper limit of load capacitance as a standard.
(3)   Convert complex gates and multi-input gates to simple gates wherever possible. (A complex gate or a multi-input gate has a transfer delay time that tends to vary depending on the input logic state.)

5.3   Notes on Creating an Asynchronous Circuit

In principle, NEC does not recommend the creation of asynchronous circuits. However, if the design of an asynchronous circuit is unavoidable, due to an external asynchronous input, etc., pay attention to the following items:

5.3.1   Minimum pulse width
5.3.2   Metastable state
5.3.3   Spike noise

5.3.1   Minimum pulse width

A malfunction may occur if the pulse width input to the chip or a pulse generated within the chip is too narrow.

When data is read at the active edge of a clock, the clock pulse may return to the original level and no expected logic operation is performed before data is completely read. The minimum pulse width necessary to read data, therefore, needs to be specified.

In the CB-C8 family, the minimum pulse width for clock, set and reset is described in **CB-C8 Family User's Manual Block Library**.

Naturally, the data pulse width must exceed the flip-flop's specific set-up time or hold time. Use caution when working with a combination of asynchronous and synchronous circuits.

5.3.2   Metastable state

When the outputs of flip-flops and latches, etc., are unstable in either a high or a low state, they are in what is called a metastable state.

To ensure operational stability of flip-flops and other blocks having clock pins, the critical timing parameters are restricted, such as the set-up time, hold time, release time and removal time.

If a clock and data signal or reset signal change at exactly the same time, it goes into a metastable state.

Once in a metastable state, the output level is indeterminate (low or high) even after recovery. To protect against these metastable conditions, the timing for each block must be set to meet all of the set-up, hold, release and removal times defined for the block. If the defined times cannot be satisfied, refer to **(2) Prevention against metastable state.**

(1) Occurence of metastable state and recovery

Fig. 5-14 Occurence of Metastable State and Recovery
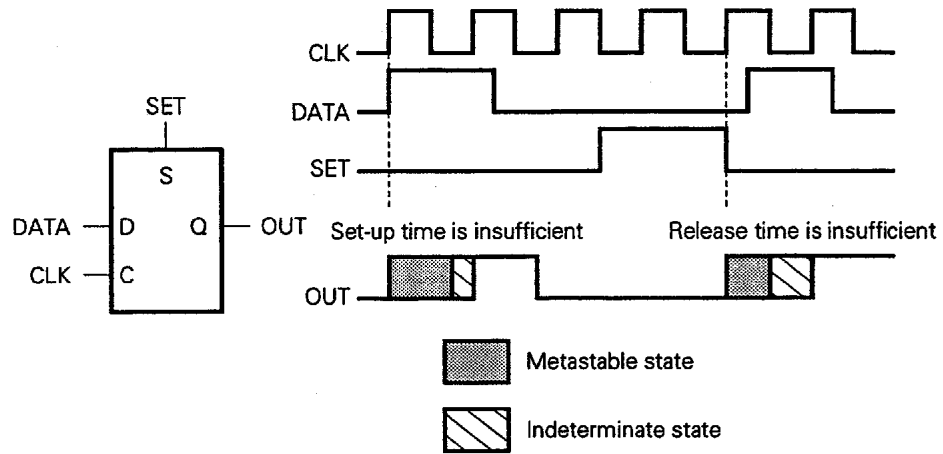
Recovery time from metastable state to a normal state is roughly estimated by the following formula:

> Recovery time = Metastable + Indeterminate
> Metastable time =tpd(MAX.) x 6

tpd(MAX.):   Maximum delay from a clock input change to a clock output change.
            (When requirement for set-up/hold time is violated)
            Or release/removal time
            (When requirement for release/removal time is violated)

(2) Prevention against metastable state

When each provided time is not satisfied, the circuit configuration should not negatively effect the circuit of the remaining stages.

Generally, as shown in Fig. 5-15, the asynchronous data is read twice and accepted after matching.

Fig. 5-15 Improved Circuit Configuration
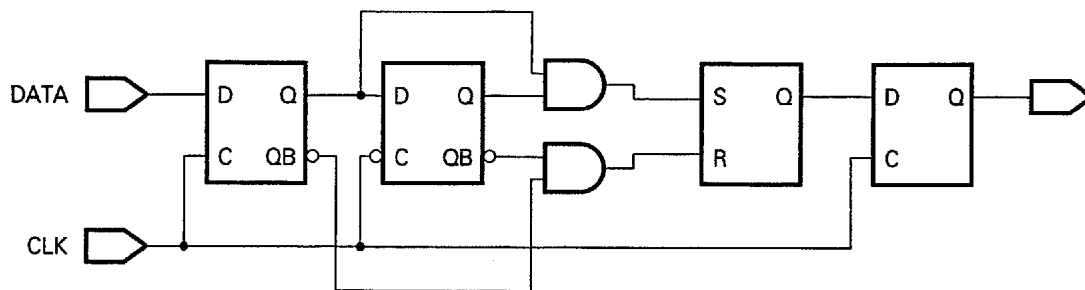
5.3.3 Spike noise

Spike noise is generated by a deviation in the timings of two or more input signals (also generated during multiplexer switching, etc.). Circuits that are prone to this condition are those that use a single gate for multiple input signals, such as a clock followed by a flip-flop. If this spike noise is input to the clock, the set, or reset conditions of the flip-flop in the next stage are affected, and a malfunction may occur in the output signal path of the flip-flop.

If in a design, a single gate for two or more inputs is used, check to see if spike occurs when these inputs vary simultaneously. The gate in the next stage may malfunction and a spurious output signal may be generated. If this spike noise cannot be ignored in the later stages, the test pattern or circuit must be altered so that the noise does not affect these subsequent circuits.

CHAPTER 6   TOTAL CHIP SIMULATION

6.1   General Description

Total chip simulation is the process of exercising an entire chip design under conditions that approximate actual operating conditions.

Since the mode without the CPU core is usually the same as the customer specified function block simulation, this section will only describe total chip simulation with the CPU core included.

If no megafunction (except for memory) is included, the total chip simulation can be substituted by the customer specified logic simulation.

In the following example, a CB-C8 circuit incorporating NA70008H, NA71051H, NA71059H and customer specified logic macros, is used for explanation. The actual operation of this circuit has not been tested and is for explanation purposes only.

6.2   Total Chip Simulation Flowchart

Total chip simulation flow consists of a simple, system level simulation and the process to create the test pattern from the results. The flowchart of total chip simulation is as follows:

Fig. 6-1 Total Chip Simulation Flow
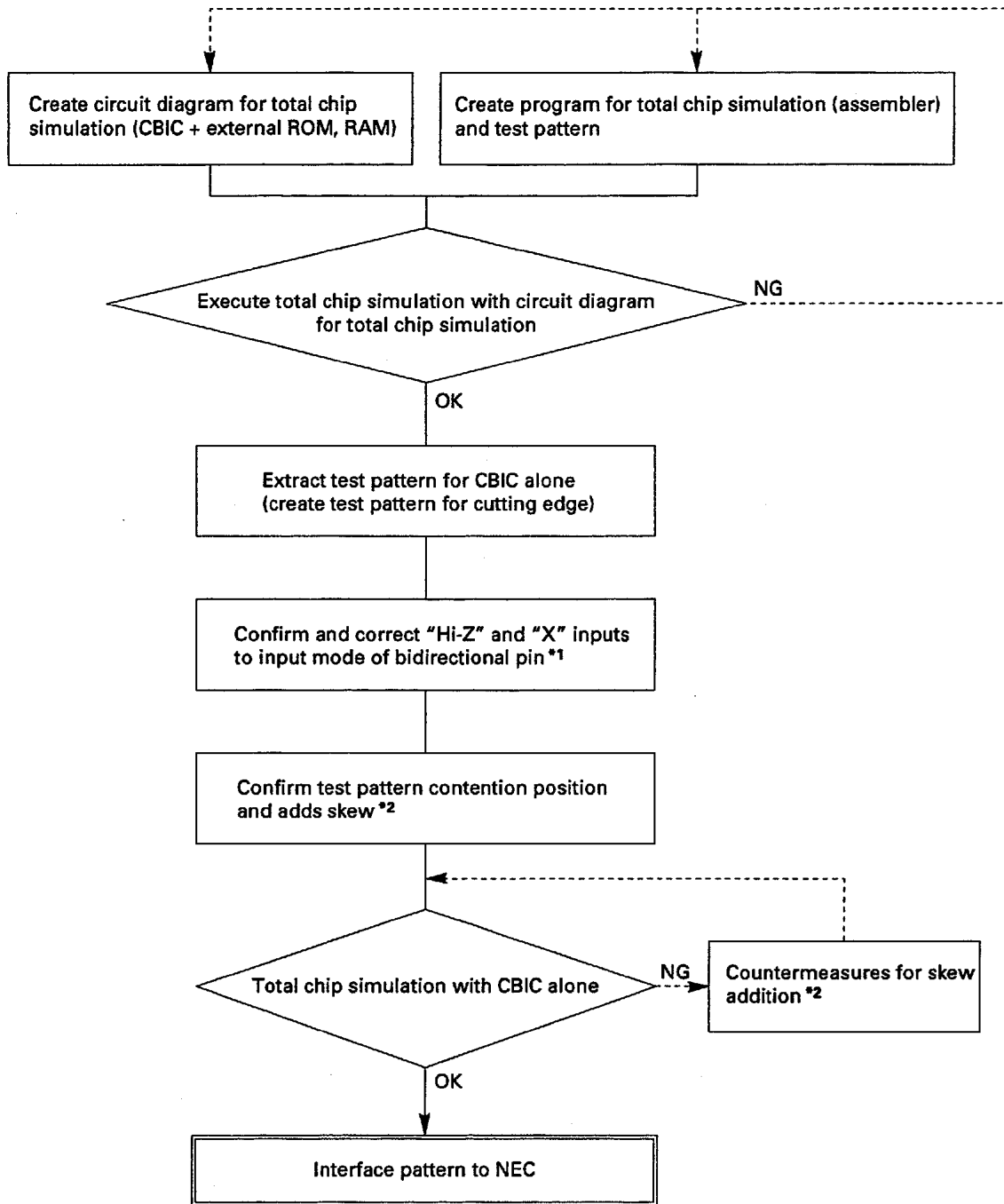
*1 If a "Hi-Z" or "X" condition exists immediately after a mode change, i.e. from output mode to input mode, then input the same output pattern value ("1" or "0") that occured just previous to the mode change.

*2 Some restrictions must be observed in setting the skew. Refer to **CHAPTER 7   TEST PATTERN DESIGN** for the restrictions.

(1) **Creation of a circuit diagram for total chip simulation**

Add circuits (external program ROM, data RAM, etc.) to execute total chip simulation. Refer to **6.3 Circuit Diagram for Total Chip Simulation.**

(2) **Creation of a test pattern and a program for total chip simulation**

Create a test pattern and a program for CPU macro to execute total chip simulation. Refer to **6.4 Program for Total Chip Simulation and Test Pattern.**

(3) **Execution of simulation with total chip simulation**

Execute total chip simulation with an external ROM program. Refer to **6.5 Execution of Total Chip Simulation.**

(4) **Extraction of test pattern for CBIC alone**

Dump and extract the test pattern of the CBIC chip cutting edge to create the test pattern for a separate CBIC. Refer to **6.6 Extraction of Test Pattern for CBIC Alone.**

(5) **Confirmation and correction of "Hi-Z", "X" inputs to input mode of bidirectional pin**

Check if a "Hi-Z" or "X" has been input to the input mode of an input or bidirectional pin. If it has, extract the test pattern and execute a correction. The correction of a pin attribute may be necessary at this stage, in order to extract it as an output pin while extracting the test pattern from the simulation run. If this is done, it is also necessary to confirm the operation of the new bidirectional pin for proper input/output mode switching and to confirm overall timing as a result of the total chip simulation with CBIC (described later). Refer to **6.7 Confirmation and Correction of "Hi-Z", "X" Inputs to Input Mode of Bidirectional Pin.**

(6) **Confirmation of test pattern contention position and adding skew**

If the test pattern for CBIC is kept intact, input contention of test pattern will occur and the test pattern may not operate normally. This occurs because input timing of the signal is normalized to the basic timing when extracting. To avoid this test pattern contention, it may be necessary to add some skew at this stage. Pay attention to the setting types and conditions (for details, refer to **CHAPTER 7 TEST PATTERN DESIGN**) The addition of skew also can cause signal reflections at the tester interface. Refer to **6.8 Confirmation of Test Pattern Contention Position and Adding Skew.**

(7) **Total chip simulation with CBIC alone**

Execute the simulation with dumped and corrected test pattern to the CBIC circuit and check the test pattern. Refer to **6.9 Execution of Total Chip Simulation with CBIC Alone.**

6.3   Circuit Diagram for Total Chip Simulation

If a CPU macro is incorporated, separate software to operate the CPU macro is required to execute total chip simulation. It is possible to prepare software to serve as a test pattern, similiar to the software created for the user logic. However, this is a very difficult approach because you must input the required instruction patterns in synchronously with the read timing of the CPU.

NEC recommends the following method:

Add a program ROM and data RAM to the external memory of the CB-C8 system circuit, and then store the created program to this ROM or RAM. Execute simulation with the ROM or RAM. After the simulation is completed, dump the pattern generated at the joint of system circuit and external circuit. The result can be used as the test pattern for total chip simulation.

An example of a system circuit is shown in the Fig. 6-2. The circuit diagram of the CB-C8 chip is called the

system circuit diagram. Sample circuit diagrams for total chip simulation, a system circuit, and the block diagrams corresponding to the other required circuits are shown in Figs. 6-6, 6-7, 6-3, and 6-4, respectively.

In Fig. 6-6, a NMI input on the CPU can be made by controlling port to reduce the burden against the test pattern. READY input can be input when accessing memory.

Fig. 6-2   Example of a System Circuit
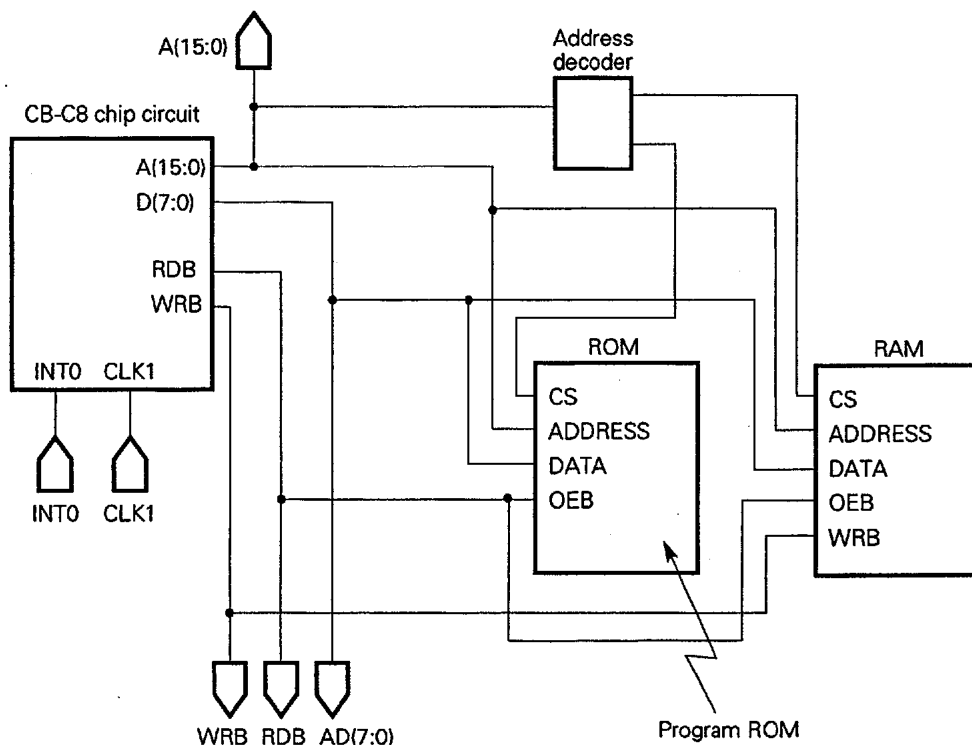
When creating a circuit diagram for total chip simulation, note the following items:

(1) A system circuit diagram must be defined as a macro.

(2) A system circuit diagram symbol should be located on top of the hierarchy.

(3) The CPU macro of a system circuit diagram must be able to access an external ROM/RAM.

(4) RAM is not necessary unless used to store a test program for total chip simulation.

(5) Connect any pins of a system circuit diagram symbol to external pins. At this time, the signals connected to the external ROM/RAM, address line, etc. should be connected to output pins.

   (This item may not be necessary according to the simulator used. Contact NEC for more details.)

(6) The blocks which are currently available for external memory are SRAM and masked ROM only. Contact your local ASIC Design Center for more details.

6.4   Program for Total Chip Simulation and Test Pattern

6.4.1   Program for total chip simulation and test pattern

Two types of test patterns are available for system simulation of a CB-C8 ASIC which incorporates a CPU macro.

(1) Test pattern (see Fig. 6-5)

   Test pattern data, such as clock or reset input.

(2) Test program (see Figs. 6-8 and 6-9)

The program should be created in the assembler language of the CPU macro incorporated. The program operates a CPU core after the reset input from a test pattern. The program converts to read format of each simulator through the extended Intel HEX format at simulation.

6.4.2 Precautions for creating test pattern and program

(1) All a test pattern has to do is to check connections between each macro. Inspecting each macro can be easily performed by using the simplified test pattern supplied by NEC, the same one used for the separate simulation of the macro.

(2) Submit the test program in extended Intel HEX format for each simulator.

(3) Make sure that the appropriate command (i.e. HALT, in the case of the NA70008H) to stop the program is given at the end of the test program.

(4) The test program size must be less than 4 kB. In this regard, it is not recommended that you use a subroutine command in the test program. For example, even though the volume of a program which includes CALL instructions may be less than 4 kB, the actual program size may be equivalent to more than 4 kB.

(5) Test program space used at simulation must be less than 4 kB.

6.4.3 Example of creating test pattern and test program

The test program and test pattern to check the connection between the CPU macro (NA70008H), other megafunctions, and any customer specified macros are described in this section.

Since considerable difficulty may be encountered in giving an expected value for the output pattern of a total chip simulation, it is suggested that the value be left undefined for an output buffer and be left as a high-impedance for an I/O buffer.

The final interface data is created after dumping the signals from the circuit. Therefore, the original signal input represents the expected data.

Fig. 6-3 Block Diagram of Circuit for Total Chip Simulation
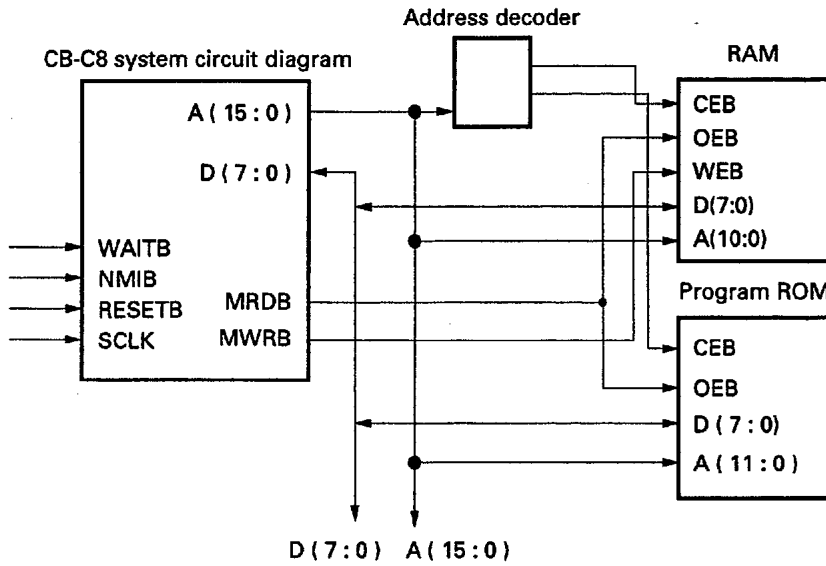
Fig. 6-4 CB-C8 Block Diagram
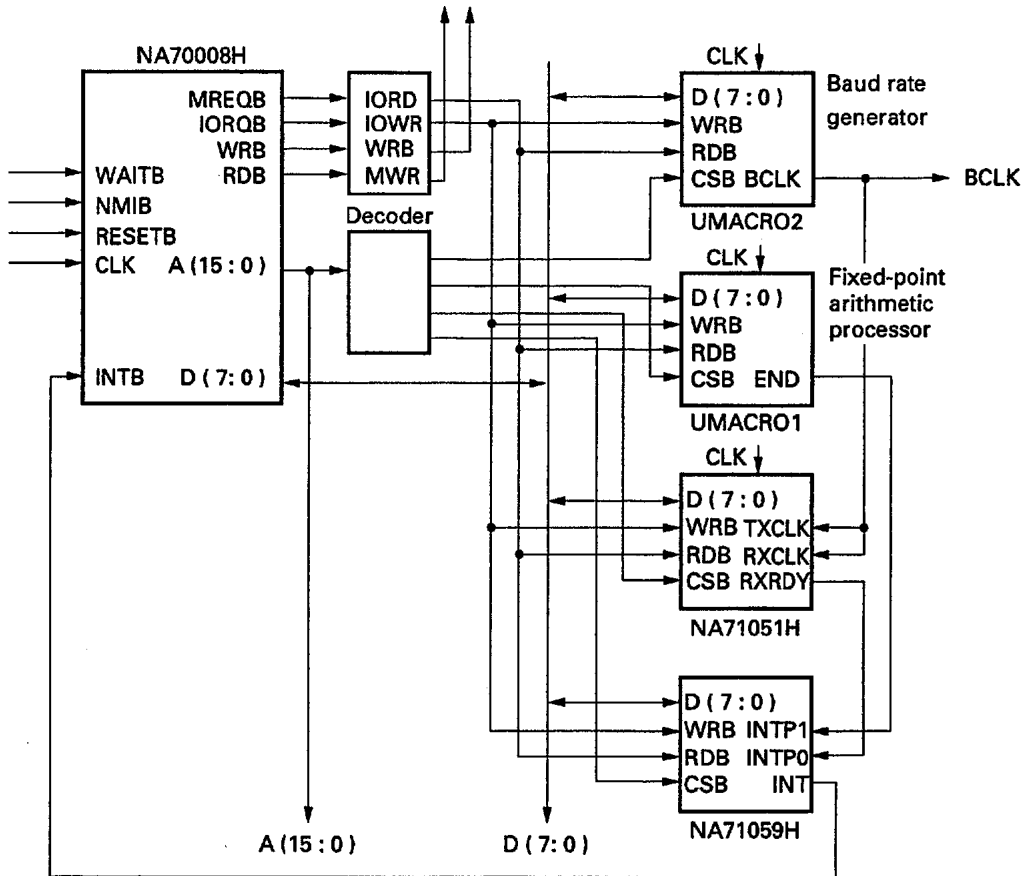
Fig. 6-5 Example of Test Pattern for Total Chip Simulation (External ROM Added)
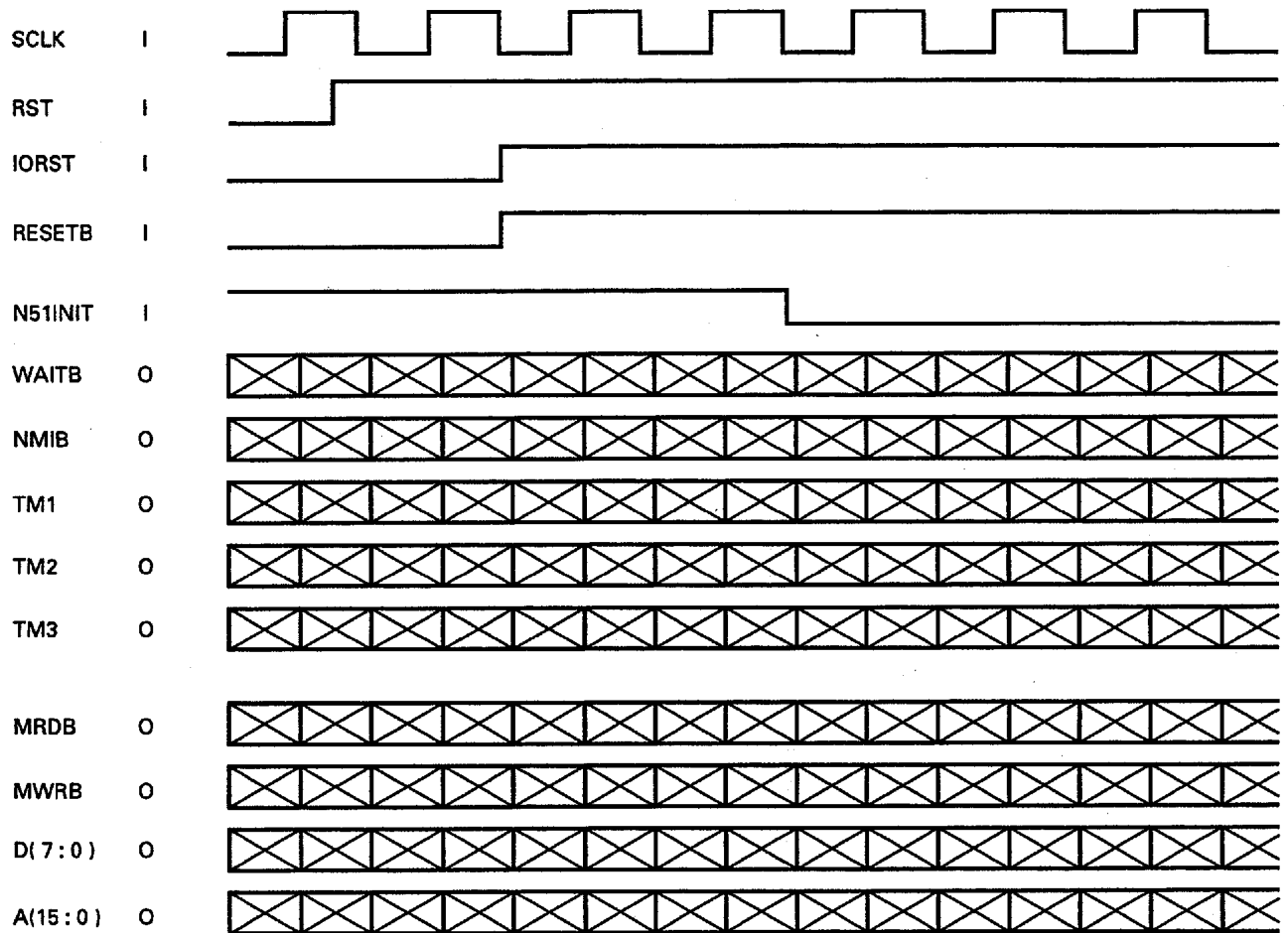
The test pattern above is an example of a test pattern suitable for performing total chip simulation of the circuit shown in Fig. 6-6.

As shown in Fig. 6-6, the test mode setting is executed in this circuit. The NMI input can be input as a port output from the program. A READY signal can be input while accessing memory. Any signals necessary for initialization, such as a system clock (CLK) and the reset signal of the CPU (RESETB) are to be considered as inputs. Other pins are defined as output pins for purposes of dumping the pattern data for test.

If READY, NMI, and mode setting pins are input from the test pattern, it is important to pay attention to their active levels and the conditions of the set mode.

Fig. 6-6 Circuit for Total Chip Simulation (Added ROM and RAM for Simulation)

Fig. 6-7 CB-C8 System Circuit Diagram
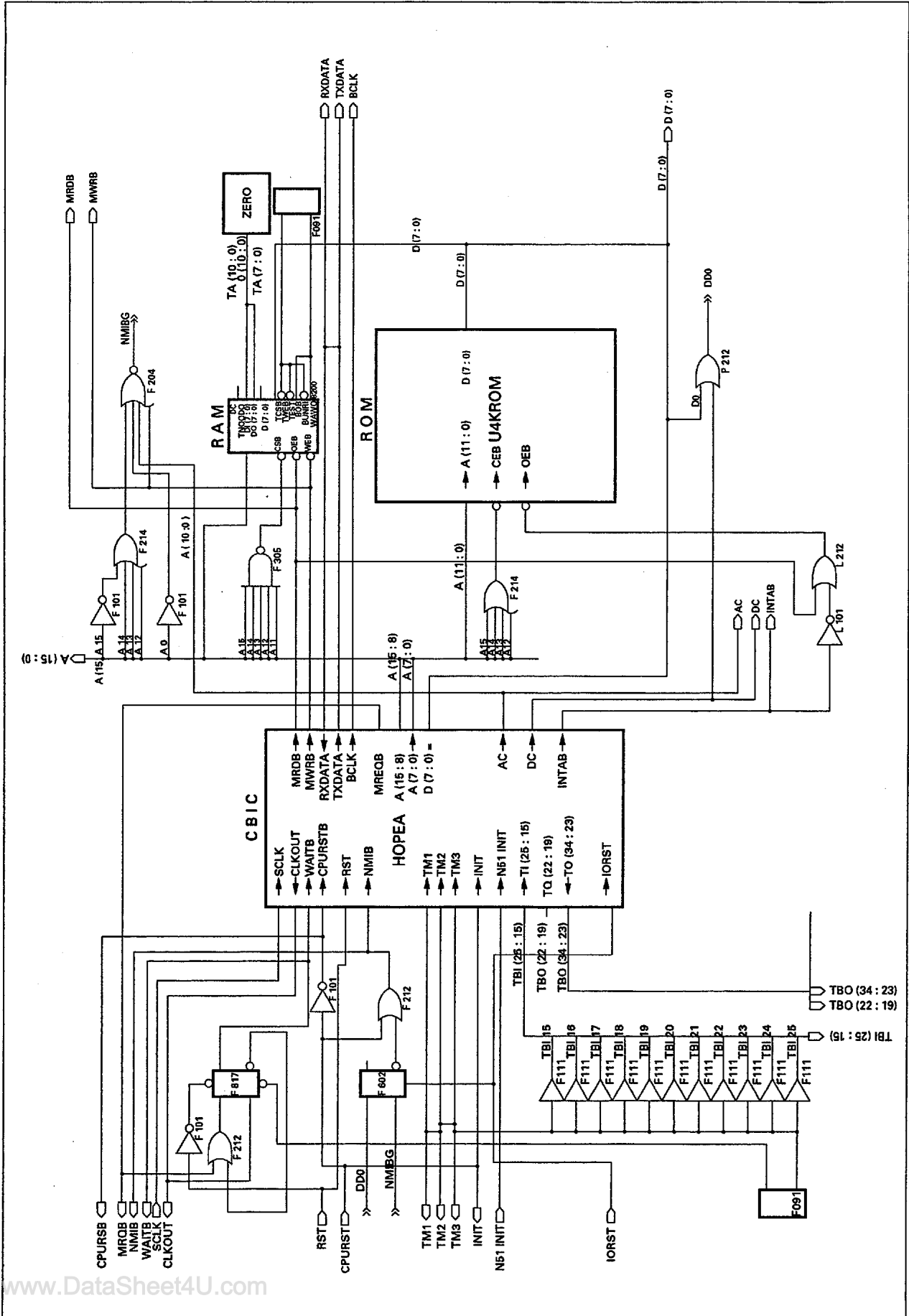
Fig. 6-8 Example of Program for Total Chip Simulation

Fig. 6-9 Example of assembler source list

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;        System simulation demonstration      ;
;        create          :1992/12/15          ;
;        update          :1993/03/10*         ;
;                 :typing :1993/04/15         ;
;                        :1992/06/15**        ;
;                        :1992/06/22+         ;
;        CPU             :NA70008H            ;
;        Version         :                    ;
;        Assembler       :AZ80                ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;        define I/O address               ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
scudat  equ     00h                     ;MSCU  Data address**
scucom  equ     02h                     :MSCU  Command address**
;
icur0   equ     20h                     ;MICU  Register (A0 = 0)*,**
icur1   equ     22h                     ;MICU  Register (A0 = 1)*,**
;
bgcnt   equ     60h                     ;Baud  rate  generator  reload  register*,**
bgpre   equ     62h                     ;Baud  rate  generator  prescaler*,**
;
calcmd  equ     40h                     ;Fixed-point  arithmetic  processor  command**
calap   equ     42h                     ;Fixed-point  arithmetic  processor  port  A**
calcpl  equ     42h                     ;Fixed-point  arithmetic  processor  port  C  lower  byte**
calbp   equ     44h                     ;Fixed-point  arithmetic  processor  port  B**
calcpu  equ     44h                     ;Fixed-point  arithmetic  processor  port  C  upper  byte**
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;        Definition  of  constants        ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
;;;;;;; MSCU initial data ;;;;;
;
scudmmy equ     00000000b               ;MSCU  Dummy command
scurst  equ     40h                     ;MSCU  Software  reset  command
scumd   equ     01001101b               ;MSCU  Mode word
scucmd  equ     00110111b               ;MSCU  Command word
;
;;;;;;;; baud  rate  generator  initial  data
;
bprec   equ     000b                    ;Prescaler  setting  data  (1/1)
bcnt    equ     14                      ;Reload  register  setting  data  (1/16)
;
;;;;;;; MICU  initial  data  ;;;;;
;
icuiw1  equ     01010010b       •       ;MICU  IW1  Register  setting  data
icuiw2  equ     00h                     ;MICU  IW2  Register  setting  data
icuimw  equ     11111100b               ;MICU  IMW  Register  setting  data
icupfcw equ     11000111b               ;MICU  PPCW  Register  setting  data
icumcw  equ     00001011b               ;MICU  MCW  Register  setting  data
;
;
```

```
;;;;;; output data
;
serout    equ    0a5h                    ;Serial output data
;
nmion     equ    0ffh                    ;NMI ON setting data
nmioff    equ    00h                     ;NMI OFF setting data
;
cdata     equ    55h                     ;Arithmetic processor port A setting data
cdatb     equ    0aah                    ;Arithmetic processor port B setting data
;
;;;;;;; MICU command
;
ficmd     equ    00100000b               ;MICU interrupt processing finish command (FI command)
;
;;;;;;; calculator command
;
addcmd    equ    00h                     ;Arithmetic processor add command
;
;;;;;;; CHECK DATA
;
txrdy     equ    00000001b               ;MSCU TXRDY Data for check
fscu      equ    00000001b
fcal      equ    00000010b
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;         Program                        ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
          org  0h
start:
          ld     sp,1111111111111111b    ;Stack  pointer  initial  setting
          jp  inis                       ;Start  address  setting
;
          org  40h                       ;Address  setting  for  serial  input  interrupt
          jp  intp0
;
          org  48h                       ;Address  setting  for  arithmetic  processor  interrupt
          jp  intp1
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;     NMI  interrupt  processing          ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
          org  66h
nmi:
          push   af                      ;Register  saving
;
          ld     a,nmioff                ;NMI  signal  release
          ld     (8001h),a
;
          halt                           ;Halt
          pop    af
          reti
;


;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; Serial input interrupt processing        ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
intp0:
          push af                        ;Register  saving
;
          in     a,(scudat)              ;Serial data input
```

```
        ld      (wrtes),a               ;Store into memory*
        in      a,(scucom)              ;MSCU status input
        ld      (wrtes+1),a             ;Store into memory*
        ld      a,(intflag)
        or      fscu
        ld      (intflag),a
        ld      a,ficmd
        out     (icur0),a
        pop     af
        reti
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; Address setting for arithmetic processor interrupt;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
intp1:
        push    af                      ;Register  saving
;
        in      a,(calcp1)              ;Serial data  input
        ld      (wrtes+2),a             ;Store into memory*
        in      a,(calcpu)              ;MSCU status input
        ld      (wrtes+3),a             ;Store into memory*
        ld      a,(intflag)
        or      fcal
        ld      (intflag),a
        ld      a,ficmd
        out     (icur0),a
        pop     af
        reti
;
inis:
        di                              ;Interrupt   disabled
;
;Baud  rate  generator  initial  setting+
        ld      a,bcnt                  ;Reload register setting (1/15)
        out     (bgcnt),a               ;*
        ld      a,bprec                 ;Prescaler  setting  (1/1)
        out     (bgpre),a
;
;
;MSCU initial setting
        ld      a,scudmmy               ;Dummy command
        out     (scucom),a              ;Dummy  command  first  output
        nop
        nop
        nop
        nop
        nop
        out     (scucom),a              ;Dummy  command  second  output
        nop
        nop
        nop
        nop
        nop
        out     (scucom),a              ;Dummy  command  third  output
        nop
        nop
        nop
        nop
        nop
        ld      a,scurst                ;Software  reset  command
```

```
                out     (scucom),a
                nop                             ;wait >=  3+4+4
                nop
                ld      a,scumd                 ;
                out     (scucom),a              ;Mode  word  setting
                nop
                nop
                ld      a,scucmd                ;
                out     (scucom),a              ;Command  word  setting
;
;MICU  initial  setting
                ld      a,icuiw1                ;IW1  Initial  setting  data
                out     (icur0),a               ;IW1  Initial  setting  data  output
                ld      a,icuiw2                ;IW2  Initial  setting  data
                out     (icur1),a
                ld      a,icuimw                ;IMW  Initial  setting  data
                out     (icur1),a
                ld      a,icupfcw               ;PPCW  Initial  setting  data
                out     (icur0),a
                ld      a,icumcw                ;MCW  Initial  setting  data
                out     (icur0),a
;
                ld      a,0
                ld      (intflag),a             ;Flag  area  0  clear
;
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;       main program                     ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                ei                              ;Interrupt enabled
;
                im      0                       ;
wittrdy:
                in      a,(scucom)              ;MSCU  Status  read
                bit     0,a                     ;TXRDY = 1?
                jr      z,wittrdy               ;WAIT until TXRDY = 1
;
                ld      a,serout                ;Serial  data  setting
                out     (scudat),a              ;Serial  data  output
;
                ld      a,cdata
                out     (calap),a               ;Arithmetic  processor  port  A  setting
                ld      a,cdatb
                out     (calbp),a               ;Arithmetic  processor  port  B  setting
                ld      a,addcmd
                out     (calcmd),a              ;Add  command  output
;
                ei                              ;Interrupt  enabled
wtint:
                ld      a,(intflag)             ;Flag area read
                bit     1,a                     ;Arithmetic  processor  interrupt  finished?
                jr      z,wtint
                bit     0,a                     ;Serial  input/output  interrupt  finished?
                jr      z,wtint
;
                ld      a,nmion                     ;NMI ON*
                ld      (8001h),a                       ;
;
endlp:
                jp      endlp
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;         RAM area definition           ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
        org    1111111000000000b
wrtes   defs   10                      ;Memory read/write test area*
intflag defs   1                       ;Flag area
;
        end    start
```

6.5 Execution of Total Chip Simulation

When megafunctions are included in a design, except for memory macros, it is difficult to create an expected value in total chip simulation. Therefore, total chip simulation is performed by an input test pattern and test program.

The total chip simulation is executed after the total chip circuit diagram, test pattern and test program are completed. At this time, be sure to read-in the ROM code to program the ROM.

If a CPU is incorporated, its operation should be checked by comparing it with an assembler program list. This is done by dumping the address output of the CPU or by referring to the address of program ROM.

6.6 Extraction of Test Pattern for CBIC Alone

Extracting method differs according to the simulator used.

When a Verilog™*1 simulator is used, recognize the CBIC chip cutting edge in the interface block. Set the test pattern to be automatically dump-extracted while executing simulation. Then, execute the simulation using the entire circuit for total chip simulation.

When an OpenCAD™*2 simulator is used, execute the total chip simulation using all signals of the CBIC chip (all symbol signals of system circuit diagram) and have them output at the external output pins, as described in 6.3 Circuit Diagram for Total Chip Simulation. In this case, the dump-extracted test patterns becomes the output pins, so correct the pin attribute as a next step.

*1   Verilog is a trademark of Cadence Design Systems, Inc.
*2   OpenCAD is a trademark of NEC Corporation.

6.7 Confirmation and Correction of "Hi-Z", "X" Inputs to Input Mode of Bidirectional Pin

In the extracted test pattern, a "Hi-Z" or "X" might be input to the input mode. This situation can be avoided by altering the external circuit, but be sure to check to confirm. If a "Hi-Z" or "X" is input to the input mode of an input or bidirectional pin, change the value to a "1" or "0".

When using a VISTASLIII simulator, set the attribute of extracted test pattern to the attribute of each pin of the CBIC chip (including the name). At this time, the attributes of a bidirectional pin should be set once to the attributes of an input pin, and then changed back to be a bidirectional pin. (This insures the test pattern is in the input mode).

6.8 Confirmation of Test Pattern Contention Position and Adding Skew

In the extracted test pattern, the skew originally required might be deleted because the input timing of the signal is normalized to the basic timing (i.e with no delay) when extracting. Add the skews back in again to correct the timing of each input signal at this stage. Note that there are some corresponding restrictions with the tester for adding the skews. Mainly, skews are necessary for the data bus. For details, refer to CHAPTER 7 TEST PATTERN DESIGN.

6.9 Execution of Total Chip Simulation with CBIC Alone

Execute the simulation to the CBIC chip circuit, not to the circuit diagram for total chip simulation, by using the dump-extracted and corrected test pattern. At this time, check that the simulation operates normally.

Fig.6-10 Execution Procedure Example When Using OpenCAD™

```
                                    ┌──────────────┐
                                    │    START     │
                                    └──────┬───────┘
         ┌─────────────────────────────────┼──────────────────────────────┐
┌────────────────────────────┐                    ┌────────────────────────────┐
│      Total chip  PWC        │                    │     CPU program + pattern   │
└────────────────────────────┘                    └────────────────────────────┘
                                    ┌──────────────────────────┐
                                    │   Total chip simulation   │
                                    └────────────┬─────────────┘
                                    ┌──────────────────────────┐
                                    │       Dump pattern         │         ┌──────────┐
                                    └────────────┬─────────────┘         │          │  Processing
                                    ┌──────────────────────────┐         └──────────┘
                                    │ Compare pattern and program│        ┌──────────┐
                                    └────────────┬─────────────┘         │          │  Data
                                                 │                        └──────────┘
                           n        ◇ Normal operation ? ◇
                                                 │ y
                                    ┌──────────────────────────┐
                                    │     Pattern correction     │
                                    │ (Correct pin attribute,    │
                                    │        add skew)           │
                                    └────────────┬─────────────┘
                                    ┌──────────────────────────┐
                                    │    Pattern for CBIC chip    │
                                    └────────────┬─────────────┘
                                    ┌──────────────────────────┐
                                    │  Execute CBIC chip simulation│
                                    └────────────┬─────────────┘
                                    ┌──────────────────────────┐
                                    │  Simulation result pattern  │
                                    └────────────┬─────────────┘
                           n        ◇ System normal operation ? ◇
                                                 │ y
                                    ┌──────────────────────────────────┐
                                    │ Result pattern -> Expected value pattern│
                                    └────────────┬─────────────┘
                                    ┌──────────────────────────┐
                                    │  Add information "Don't care"│
                                    │ (Initialize period, mode    │
                                    │     switching period, etc.) │
                                    └────────────┬─────────────┘
                                    ┌──────────────────────────┐
                                    │    Expected value pattern   │
                                    └────────────┬─────────────┘
                                    ┌──────────────────────────┐
                                    │  Execute CBIC chip simulation│
                                    └────────────┬─────────────┘
                                    ┌──────────────────────────┐
                                    │       Result pattern        │
                                    └────────────┬─────────────┘
                           n        ◇        No error ?        ◇
                                                 │ y
                                    ┌──────────────────────────┐   ┌───────────────────────────────────────────┐
                                    │    Result pattern (TRC)     │   │ Pattern for checking after placement and routing│
                                    └──────────────────────────┘   └───────────────────────────────────────────┘
```

As all test patterns of bidirectional pin are input mode, non-match signal generates to control signal. Check if operation is executed normally to the simulation result.

This process creates the expected value for simulation after placement and routing . At the simulation after placement and routing, operation can be checked only by checking the expected value with adding the information "Don't care", etc.

CHAPTER 7   TEST PATTERN DESIGN

7.1 Purpose of Creating Test Patterns

A test pattern is used for the following two purposes:

- **To verify and simulate the functionality of a designed circuit**
  Timing conditions, etc., can be set within the allowable range of the simulator to be used, and relatively fine settings can be made.
- **To used for an LSI tester for shipping inspection of the LSI part**
  The number of test patterns and the given timing conditions must be developed carefully so that the final test pattern has the contents and ability to efficiently and thoroughly test out the final circuit.

NEC prepares the test pattern for the LSI tester once the LSI has been completed.

This chapter describes how to create a test pattern for efficient shipping inspection, and describes other important points and limitations concerning test patterns. If there is a defect in an LSI and the test pattern does not test for it, then this defect can go undetected during the shipping test which may cause a malfunction in a future application. It is therefore essential that you very carefully and thoroughly develop your test pattern and observe any restrictions that may apply.

7.2 Types of Test Patterns

(1) Classification by test items

Test patterns are classified according to the test items required for shipping inspection:

Type of test pattern	Purpose of test
① Test pattern for DC test	To check DC characteristic parameters • Output current (I_{OL}, I_{OH}) • Input leakage current (I_I) • Off-state leakage current (I_{OZ}) • Static current dissipation (I_{DDS}) • Input voltage level (V_{IL}, V_{IH}) • DC test of oscillation circuit
② Test pattern for function test	To check logic function To detect internal failure To check AC characteristics

If there are common restrictions for both DC and function test, these items may be satisfied by sharing a common test pattern.

(2) Classification by CB-C8 design procedure

Test patterns are also classified according to the parameters of the design procedure:

Test pattern classification	Test pattern type/test purpose
① Test pattern for user logic separation simulation	● Test pattern for checking user logic operation (necessary if user logic function is integrated with CPU and CPU peripheral macro)
	Test pattern for checking operation with user logic separated from other CPU macros and CPU peripheral macros. This test pattern is used for shipping inspection.
② Test pattern for checking megafunction separation test circuit	● Test pattern for reading ROM macro code data (necessary only when integrating ROM macro)
	Test pattern to check ROM contents by directly reading all ROM codes with ROM macro in separation test mode. This test pattern is used for shipping inspection.
	● Test pattern for checking RAM macro separation test circuit (necessary only when integrating RAM macro)
	Test pattern to check separation test circuit by setting RAM macro in separation test mode and accessing specific address for read/write. Shipping inspection is conducted by using test pattern to check access to all addresses by checker board[1] and marching[1] methods (prepared by NEC in principle). [1] .... Standard RAM testing methods
	● Test pattern for checking CPU or CPU peripheral macro separation test circuit (necessary when integrating CPU or CPU peripheral macro)
	Dummy model[2] of CPU or CPU peripheral macro is selected for simulation (dummy model or full function model can be selected for simulation), each macro is set in separation test mode, and simulation is performed with separation test circuit checking test pattern prepared by NEC for occurrence of error. For shipping inspection, function test pattern equivalent to standard model is used for testing. [2] .... Simple model, not operation model peculiar to macro, created for checking connections of input/output. Usually, this model is used for purposes other than total chip simulation.

Test pattern classification	Test pattern type/test purpose
③ Test pattern for total chip simulation	● Test pattern for total chip simulation (when CPU is not included or when simulation in which CPU is not operated with assembler program is not performed)
	Test pattern to energize entire chip (actual operation mode) to verify functions. If CPU peripheral macro is included, this test pattern is created to check mutual connection between megafunction and user logic. This test pattern is used for shipping inspection.
	● Test pattern for total chip simulation (when simulation in which CPU is operated with assembler program is performed)
	Total chip simulation including CPU must be performed to check functions, but whether test result is to reflect upon LSI tester should be determined by customer because completely preventing contention of input pattern is difficult due to test pattern creating procedure. When reflecting on test results of LSI tester, application period may delay from reasons such that pattern contention can not be prevented completely, and therefore, timing adjustment is necessary on the tester. During this period, please cooperate with NEC when contacted. [Test pattern when reflecting result on tester] Test pattern to check only connections between macros and connections between macro and user logic with entire chip energized. First, extract test pattern at cutting edge of CB-C8 pins from simulation using assembler program, adjust skew, and provide NEC with test pattern with which CB-C8 pins are simulated. [When using test pattern only for function checking simulation (not for shipping inspection)] Test pattern to check functions with entire chip energized (actual operation mode). Simulation is performed with assembler program. Since result is not reflected on tester, it is not necessary to check input pattern contention through simulation of CB-C8 alone.

(3) Allotment of test pattern creation

Prepare the test pattern for DC test as a test for either user logic separation simulation or for total chip simulation. The following table shows who is responsible for creating each test pattern.

Details of each test pattern are described in **7.8 Notes on Creating Each Type of Test Pattern.**

Target test pattern			Created by:
Test pattern for user logic separation simulation			User
Test pattern for checking megafunction separation test circuit			As follows:
	Test pattern for reading ROM macro data		User
	Test pattern for checking RAM macro separation test circuit	Simple access pattern for checking test circuit	User
		For shipping test	NEC*1
	Test pattern for checking CPU or CPU peripheral macro separation test circuit	Simple access checking for test circuit checking	NEC
		For shipping test	NEC*1
Test pattern for total chip simulation			User

*1 ...... If a test circuit using the test bus method recommended by NEC is not configured, the test pattern must be prepared by the user.

7.3 Limits to Number of Test Patterns

The number of test patterns in developing a CB-C8 circuit is limited as follows:

(1) Limits to number of test patterns

Limits to number of test patterns per line			Limits to total number of test patterns
Target test pattern	MIN.	MAX.	MAX.
Test pattern for function test	0 pattern[*1]	32,000 patterns	256,000 patterns[*3]
Test pattern for DC test	150 patterns	32,000 patterns	
* Test pattern for megafunction only[*2] (Test pattern other than that for ROM macro only are prepared by NEC)			
Test pattern for ROM macro only	Number of addresses	32,768 patterns	

[*1] ....When used with test pattern for DC test.

[*2] ....The number of test patterns for each megafunction is as follows:

⎧   Number of test patterns for CPU and

⎪   CPU peripheral function macros ....Refer to **User's Manual – CB-C8 Megafunction Design**.

⎩   Number of test patterns for RAM macro ....Number of test patterns = Number of words × 13

[*3] ....If the total number of test patterns exceeds 256,000, consult NEC as early as possible.

(2) Limits to number of test pattern lines

Keep the number of test pattern lines to within the following ranges:

Target test pattern	MIN.	MAX.
Test pattern for function test	0 line[*1]	9 lines
Test pattern for DC test	1 line	1 line
ROM macro test pattern	1 line	Number of integrated ROM macros[*2]

[*1] ....When used with test pattern for DC test.

[*2] ....Keep the number of ROM macro test patterns to within 32,768 patterns by merging in macro units when two or more ROM macros are integrated.

[Example]

When integrating ROM1; (1024w × 8b) × 1 + ROM2; (512w × 16b) × 2

1024 patterns + 512 patterns × 2 = 2048 patterns < 32,768 patterns → merge to one ROM macro test pattern.

[Merging test patterns]

Test patterns can be merged (connected) except when a RZ[*1] clock is used, in which the input skew (delay) conditions or the edge timing and strobe setting conditions are different.
[Test patterns can be easily merged by using the waveform editor of the VISTASL3 (PJOINT command).]

[*1] ...... RZ: Return to Zero. A signal changing its status from 0 to 1 and then to 0 again, or from 1 to 0 and then to 1 again in one pattern (test rate).
In contrast, a NRZ (Non-Return to Zero) signal changes its status to 0 only once in one pattern (test rate) (normal test pattern).

(3) Notes on creating more than one test pattern
In preparing more than one test pattern, use an initialize pattern for each pattern to make sure that coincidence occurs in simulation even with a single test pattern.

7.4   Notes on Creating More Than One Function Test Pattern

(1) Pattern cycle

The pattern cycle must have values within that result in changes on all output pins which can readily be determined. Usually, the following values are recommended as the pattern cycle for the test pattern for simulation. This pattern is to be provided to NEC (Note: these values are independent of the tester cycle):

V$_{DD}$	Recommended pattern cycle
3.3 V	200ns

To insure that the simulation output changes occur within the same cycle, after placement and routing, make sure the maximum delay path time, is 10 ns or less than the pattern cycle, before placement and routing.

(2) Limit concerning input signal of test pattern

① Type of signal waveform that can be input

An NRZ signal without input skew (shift) is recommended, but the following types of signal waveforms can also be specified as inputs by the tester.

Note: RZ signals cannot be specified for bidirectional pins.

● NRZ signal (Non-Return to Zero) .... Signal that changes its status only once or less in one pattern cycle

    ├── NRZ signal without skew .... NRZ signal that changes its status only when the pattern cycle changes

    └── NRZ signal with skew .... NRZ signal that changes its status with specific skew or timing shift when the pattern cycle changes

● RZ signal (Return to Zero) .... Signal that changes its status two times ("0 → 1 → 0" or "1 → 0 → 1" in one pattern cycle) (pulse signal specification)

    ├── Positive pulse .... Pulse specification signal changing "0 → 1 → 0"

    └── Negative pulse .... Pulse specification signal changing "1 → 0 → 1"

② Limits to timing specification of input signal

    (a) At present, the number of timing phases that can be set is up to six phases (six groups), including basic timing, for one test pattern.

    Notes: NRZ and RZ signals are in different phases (different groups).

             If the change timing of the positive pulse and negative pulse of an RZ signal is identical, it is regarded as the same phase (same group).

[Example]   In the following example, three phases (groups) are used.

T: pattern cycle
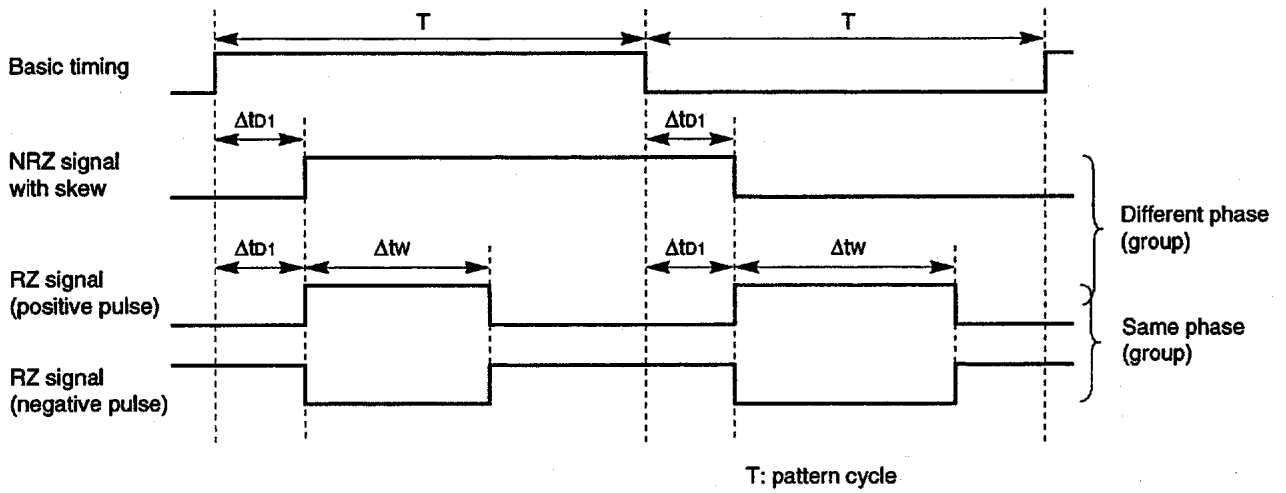
(b)   For the absolute value of the timing limit of each signal, refer to the table below. <u>Keep the time differential interval of each phase (group)</u> to within <u>10 ns or more</u> in consideration of inter-pin skew of the LSI tester.

Timing limit / Type of signal	Input delay (Δt_D)		Input pulse width (Δt_w)	
	MIN.	MAX.	MIN.	MAX.
Basic timing (NRZ)	0 ns		–	
NRZ signal with skew	10 ns	T-15 ns	–	
RZ signal (clock mode)	10 ns	T-15 ns	20ns	T-Δt_D 15ns

T: pattern cycle
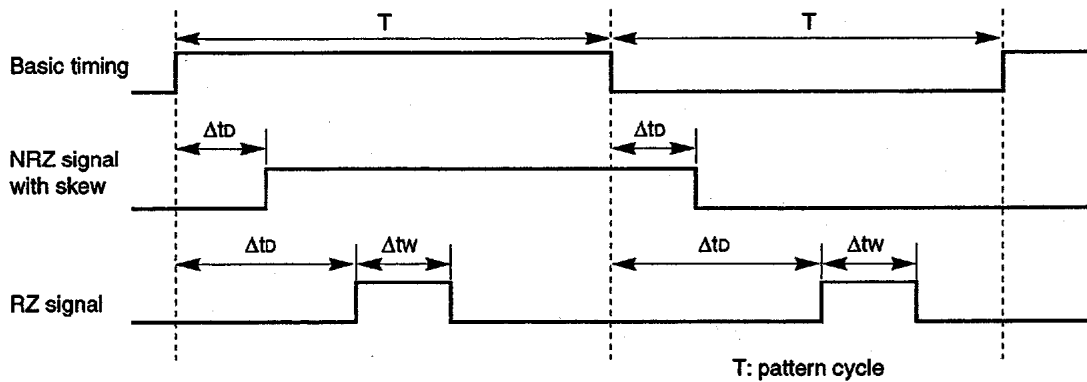
(c)   Skew variations of ±5 ns between pins are unavoidable with an LSI tester. Design test patterns and specify timing so that these variations in skew do not affect the operations of the circuit. To do this, avoid a signal change in the same pattern between input pins[*1] that can interfere with the circuit. Also set the skew value so that it does not affect operation, even if the input skew on external pins varies up to ±5 ns.

*1 ....Indicates between external signal pins such as pin setting the input timing to FF clock and data, and pin setting the input timing to FF clock and reset (or set).

③   Limits of input signal
In one test pattern, the following limits apply:

(a)   The NRZ signal, RZ signal (positive), and RZ signal (negative) must not mix on one pin.
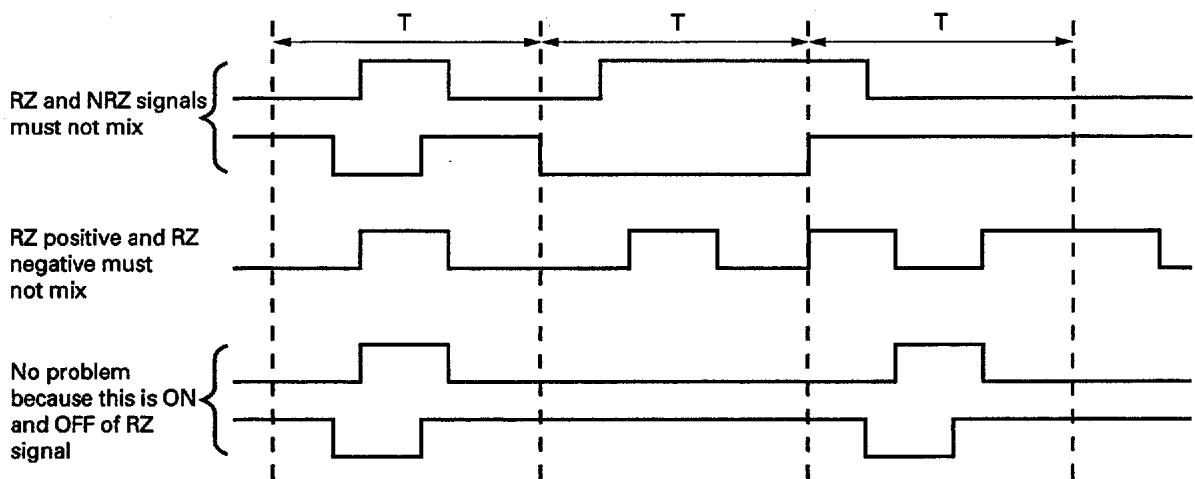
(b)   The signal change (shift) timing of one NRZ signal with skew must be constant (the timing change must not be changed in the middle of the test pattern).
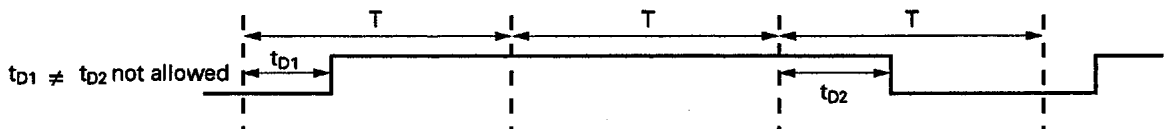
(c)   The change in timing of one RZ signal must be constant (the timing change must not occur in the middle of the test pattern).
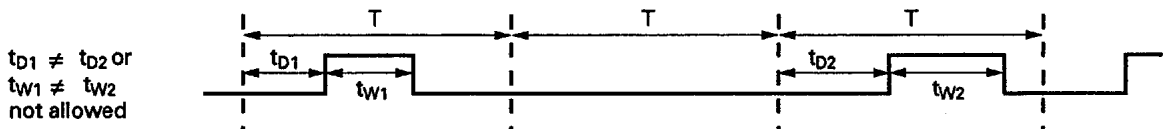
④   Handling first pattern of NRZ signal with skew

Consider that "X" is input during the skew period of the first pattern of an NRZ signal with skew (the test pattern must pass regardless of whether the signal is "0" or "1").

Design the test pattern to achieve operation of an edge trigger block, such as a FF, so that data is not fetched during this period.

First pattern
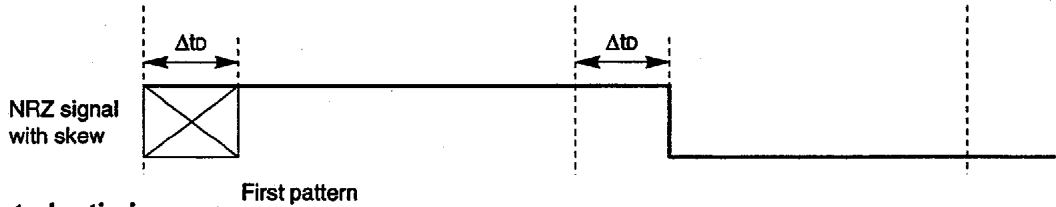
(3) Output strobe timing

① In principle, set the output strobe position at a time when the circuit has been stabilized (i.e. a change in the internal event has been completed) and all the changes in the output pins have been completed.

Usually, it is recommended that the last pattern cycle (pattern cycle – 1 ns) be set for simulation.

In this case, the strobe position at shipping test is automatically set to an optimum value, based on earlier results of delay simulation after placement and routing.

If setting the strobe position is required to other than the last time pattern cycle, consult NEC.

② Only one type of output strobe can be set in one test pattern. The strobe position cannot be changed for each pin, and two or more strobes cannot be set in one pattern cycle.

③ In principle, do not employ configurations in which the RZ signal is output to an output pin unaltered. If this is likely to occur, prepare another test pattern that can monitor the pulse output.

(4) Notes on creating test patterns for bidirectional pin

① The input/output mode of a bidirectional pin cannot be changed by the RZ signal.

② When creating a test pattern, take into consideration the following signal simulation and switching conditions with the tester:

Δt_1 ... Undefined period due to floating
Δt_2 ... Undefined period due to fighting
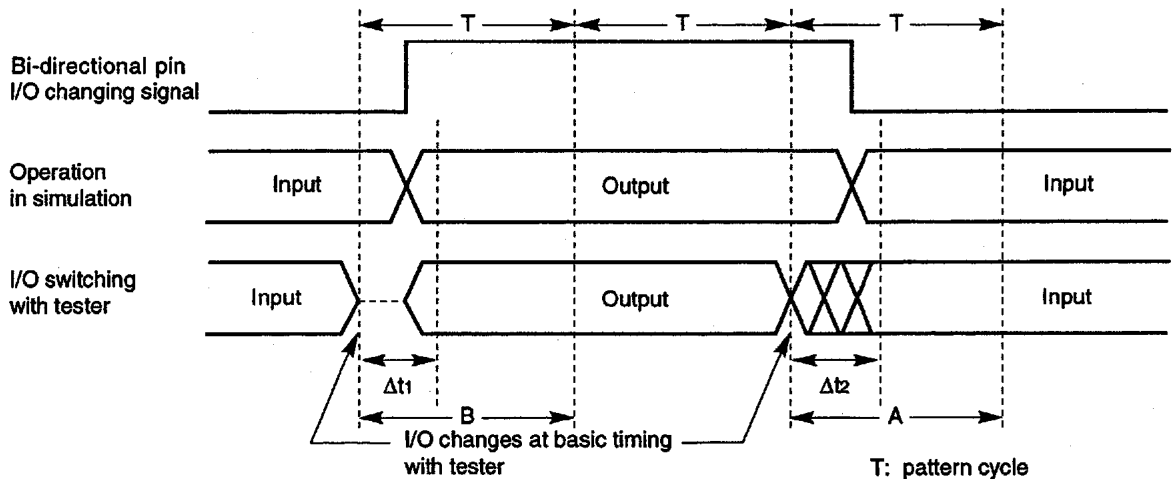
(a) An undefined period in a cycle exists immediately after the I/O mode has been changed. Design the test pattern so that data is not fetched to the internal latch of the FF during this period. It is recommended that the input logic value of one pattern (such as shown above insection A) be matched, immediately after changing from output to input, with the output pattern that occured immediately before. Otherwise this can cause of the tester to be unstable.

(b) An undefined period exists in a cycle immediately after the I/O mode has been changed. Make sure that the strobe is not set during this period. If there is a possibility of setting the strobe during this period, be sure to set the expected value of one pattern (section B as shown above) to "X" (Don't care), immediately after changing from input to output. Create a test pattern in which a valid value can be confirmed in the next pattern.

7.5 Consideration for DC Test

A function test and a DC test are conducted as shipping tests. The DC test pattern can be shared with the function test pattern, but in creating a common test pattern, keep the following points in mind:

(1) Number of DC test pattern lines

Only one test pattern is used for the DC test.

If you do prepare two or more test patterns, specify which one is the test pattern for DC test when providing NEC with the test patterns.

(2) Test pattern cycle and strobe timing

Set a pattern cycle sufficiently longer than the delay time of the circuit.

The internal status and output status must not change until the status of the circuit has been completely stabilized and a new input signal changes. This is because the test pattern is stopped at a targeted test time to measure each parameter of the DC test.

(3) Limits to test pattern input signal

Basically, the limits to the input signal described in (2) in **7.4 Notes on Creating More Than One Function Test Pattern** also apply. In addition, keep in mind the following points:

① The input pattern of RZ (Return to Zero) can be used, but the strobe position must be set when a sufficiently long time has elapsed, after change of the RZ signal has been completed and the circuit has been stabilized. (The strobe position must not be set before the RZ signal changes or while the signal is changing (during pulse period).)
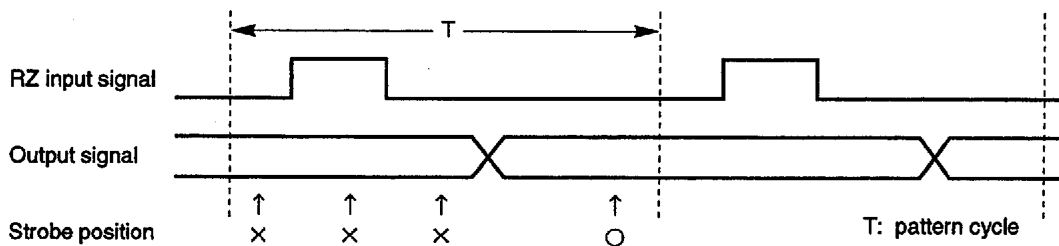
② Make sure that the input RZ signal is not output "as-is" or inverted and output to an output pin. If the test pattern allows an output like this, only one of the "H" or "L" output currents of the target output pin can be measured.

(4) Status setting necessary for DC test

Set the following in the test pattern:

① Status of I/O pin

All input pins	: "0", "1"
All output pins	: "0", "1"
All three-state output pins :	"0", "1", "Hi-Z"
All bidirectional pins	: input mode → "0", "1"
	output mode → "0", "1"

② Setting conditions to measure complete static current dissipation is recommended. In CB-C8, static current dissipation is measured in a test mode where the pull-up or pull-down resistor is cut off. However, to correctly measure complete static current dissipation(I_{LS}), consisting of only the leakage current of the integrated transistor, it is recommended that the test pattern be prepared satisfying the following conditions.

It is known that measurement of the complete static current dissipation (I_{LS}), is fairly effective for failure detection of LSIs with a very large scale of integration. It is recommended that one pattern or more of the conditions of this test be employed.

[Condition for measurement of complete static current dissipation]

Provide a stop pattern for measurement the current that satisfies the following conditions for one pattern or more. When providing this data to NEC, please specify the (I_{LS}) measuring pattern.

Target	Set condition
Internal bus status	Bus fight and bus floating must not occur.
CPU that can be stopped and CPU peripheral macro	Set STOP mode in accordance with STOP mode setting conditions. (Refer to **CB-C8 Family User's Manual – Megafunction.**)
Internal oscillation circuit	Set to "H" level input at enable status, or set to "L" level input status at disable status.

③   Limits when oscillation blocks are used:
     If an oscillation block is integrated, the DC test pattern should include the following status:

Status	Circuit configuration and specification
Enable (oscillation) status of oscillation circuit	Always necessary when oscillation circuit is used*1
Disable (stop) status of oscillation circuit	Always necessary only when STOP status of oscillation circuit is used in actual operation mode*2

*1 ...... Test pattern in enable (oscillation) status
          Input a pattern equivalent to the normal clock pattern to the input pin, and use the inverted clock pattern
          as the expected output value.

*2 ...... Test pattern in disable (stop) status
          Input the low level to the input pin when the oscillation circuit is stopped, and the expected output value
          is the high level.

7.6 Considerations for High-Speed Function Test

The means and techniques for performing high-speed function test are now under discussion. Please contact NEC for details.

7.7   Common Notes on Creating Test Patterns

(1)   Initialization of circuit (initialize)

The initial values of the sequential circuits, such as flip-flops and counters, differ between the actual LSI and simulation results as follows:

[With actual LSI]

Although the output status of the sequential circuit is defined to be either "1" or "0" on power application, which circuit is output is not known.

[Simulation result]

The initial output value of the sequential circuit is "X (undefined)".

Therefore, a circuit that includes a sequential circuit must always be initialized.

Design the circuit using the reset pin so that the circuit can be easily initialized. In addition, initialize the circuit at the beginning of a test pattern if the test pattern is to be created.

If megafunctions are integrated, some require particular initialization. Take this into consideration in creating the test pattern (for details, refer to **User's Manual CB-C8 Megafunction Design**).

* When executing simulation be careful and thorough in initializing, as substantial problems may occur due to non-initializing or inadequate initializing at simulation.

(2)   Consideration for test pattern contention (skew)

During simulation, signals are applied to all the input pins at the same time. With an LSI tester, however, it is impossible to apply the signals to all the pins completely simultaneously. Consequently, even if there is no problem during simulation, a skew of ±5 ns takes place between pins with the LSI tester, and the pattern fails in the LSI test. Therefore, create the test pattern so that it can operate even if a skew of ±5 ns exists, taking the following points into consideration:

[Countermeasures]

Do not change the data of a F/F and a clock, and the reset (set) of the clock.
- Provide one pattern or more between the two.
- Use the clock of RZ[*1].
- Set a skew of 10 ns or longer between the data of a F/F and a clock[*1].

[*1] ...... Keep in mind the timing setting conditions. Refer to **1.4 Notes on Creating More Than One Function Test Pattern**.

(3)   Considerations for testability

Because the test pattern is used as-is for the LSI shipping test, create a test pattern that checks not only the functions of an LSI, but also one that tests all the internal circuits. If the testability (failure detection rate) is low, then the LSI cannot be tested thoroughly. It is quite possible then that defective products are shipped as acceptable products.

(4) Prohibiting "X" and "Hi-Z" input

Do not input an "X" or "Hi-Z" to the input test pattern (including the pattern in the input mode of a bidirectional pin).

Do not use "Hi-Z" as an input pattern except for initial verification when performing total chip simulation on an LSI that includes a CPU. Inputting "Hi-Z" and "X" as an LSI test pattern is also prohibited when the main pattern is provided to NEC.

(5) Input pattern of buffer with pull-up/pull-down resistor

The CB-C8 provides a buffer with pull-up/pull-down resistor, but "Hi-Z" must not be used as an input pattern. Be sure to input "1" or "0". This is because the rise/fall time is very long with pull-up/down resistors, and consequently, the test cannot be conducted at high speeds with an LSI tester.

(6) Test of oscillation circuit

① When an oscillation circuit is integrated, make sure that the DC test pattern has the enable (oscillation) status of the oscillation circuit. To use the stop mode of the oscillation circuit in the actual operation mode, the DC test pattern must also have the disable (oscillation stop) status.
(Refer to **7.5 Consideration for DC Test.**)

② Test pattern of external pins of oscillation blocks. At enable (oscillation), input the pattern equivalent to the normal clock, and the expected output value should be the inverted value of the normal clock. At disable (stop), input a low level to the input pin, and the expected output value should be a high level.

(7) Consideration for AC specification (critical path)

If a critical path exists, where speed or input-output propagation delay time is important, it needs to be clearly known at the early stages of the system design. A critical path should be taken into consideration during the layout and wiring design stage. Specify the path as a critical path.

In addition, be sure to provide a pattern to the test pattern that can confirm this critical pattern, and confirm that the pattern satisfies given conditions by means of simulation with actual wiring.

7.8 Notes on Creating Each Type of Test Pattern

This section describes test pattern information that needs to be applied at various stages of the design procedure, in a CB-C8 design. Test patterns need to be created for each of the following design situations:

(1) Test pattern for user logic separation test

● This step is necessary when a user logic function block is used along with a CPU macro or a CPU peripheral macro; and are all integrated on a single chip.

● The test pattern is needed to separate the user logic block from the other megafunctions (CPU and CPU peripherals) to check the operations.

● If ROM macro or RAM macro is integrated, it is recommended that another test pattern that is accessed through this test pattern be included.

Note that access cannot be executed when a dummy model[*1] is used during user logic separate simulation.

*1 .....Dummy model and full function model may be selected for simulation. When user macro simulation is specified, dummy macro is selected. The dummy model is a simple model that just confirms the connections of the input/output of a macro. It is not an intrinsic operational model of the macro.

● This test pattern is used for shipping inspection.

(2) Test pattern for confirmation of megafunction separation test circuit

(a) Test pattern for reading ROM macro code data

● Necessary only when ROM macro is integrated.

● This test pattern is to set the ROM macro in the separation test mode and to check the ROM contents by directly reading all the ROM codes.

● This test pattern is used for shipping inspection.

(b) Test pattern for checking RAM macro separation test circuit

● Necessary only when RAM macro is integrated.

● This test pattern is to set the RAM macro in the separation test mode, and to check the separation test circuit by accessing the RAM macro for read/write with the following contents:

Provide NEC with the test mode setting conditions and information about the megafunction pins and the external pins in the test mode. It also provides NEC with a simple access pattern for checking.

① Least significant address (address 0)	:	Writes 010101...........01 (repetitive pattern of 01)
② Least significant address (address 0)	:	Reads above data (①) for coincidence confirmation
③ Least significant address (address 0)	:	Writes 101010...........10 (repetitive pattern of 10)
④ Least significant address (address 0)	:	Reads above data ③ for coincidence confirmation
⑤ Most significant address (number of words – 1 address)	:	Writes 010101...........01 (repetitive pattern of 01)
⑥ Most significant address (number of words – 1 address)	:	Reads above data (⑤) for coincidence confirmation
⑦ Most significant address (number of words – 1 address)	:	Writes 101010...........10 (repetitive pattern of 10)
⑧ Most significant address (number of words – 1 address)	:	Reads above data (⑦) for coincidence confirmation
⑨ Address (address wx[*1])	:	Writes yz[*2]
⑩ Address (address wx[*1])	:	Reads above data (⑨) for coincidence confirmation
*1 ....wx: Address that takes a different value if MSB and LSB are reversed		
*2 ....yz: Data that takes a different value if MSB and LSB are reversed		

● The shipping inspection is conducted by using a test pattern (prepared by NEC in principle*2) that accesses and confirms all the addresses with the checker board*1 and matching*1 board methods.

*1 ...... Standard RAM test methods

*2 ...... If a test circuit technique other than the test bus method recommended by NEC is used, the user must prepare the test pattern of the RAM macro (in this case also, use of both the matching and checker board methods is recommended in principle).

(c) Test pattern for confirming CPU or CPU peripheral macro separation test circuit

● Necessary when integrating a CPU or CPU peripheral macros

● This test pattern is used to select the dummy model*1 of the CPU or the CPU peripheral macro during simulation. It sets each macro in the separation test mode, and confirms that no errors exist during simulation. A test pattern prepared by NEC is used for confirming the separation test. Provide NEC with the test mode setting conditions and information on correspondence between the megafunction pins and external pins in the test mode.

*1 ...... Dummy model and full function model are selectable for simulation.

A simple model prepared for confirming the connections of input/output of a macro, not intrinsic operation model of the macro.

Usually, this model is used for purposes other than total chip simulation.

● This test pattern is to efficiently connect and confirm the separation circuit for megafunction test. The shipping inspection is conducted with a function test pattern equivalent to NEC's standard model.

[Megafunctions for which dummy function model is available]

```
NA70008H, NAV30MX
NA71037H, NA71051H, NA71054H,
NA71055H, NA71059H
```

(3) Test pattern for total chip simulation

(a) If CPU is not included or if simulation that operates the CPU with an assembler program is not performed

● This test pattern is used to energize the entire chip (actual operation mode) to verify functionality. If a CPU peripheral macro is included, this test pattern also confirms the mutual connections between the megafunction and the user logic.

● This test pattern is used for the shipping inspection.

(b) To perform total chip simulation that operates the CPU with an assembler program

Total chip simulation that includes the CPU must be performed to check full functionality. Whether the test results are compatible with the LSI tester must be determined by the customer. Completely eliminating contention of input pattern with the tester is difficult due to the unique procedures used in developing the test pattern.

When reflecting test results on an LSI tester, the test application period may be delayed for this test pattern due to pattern contention. This contention cannot be prevented completely. Therefore, timing adjustment are necessary for the tester. During this period, keep in contact with NEC.

* The operation of the megafunction is guaranteed by testing the megafunction with a test pattern prepared by NEC. The user logic can be verified by means of user logic simulation. If sufficient testability is secured by the simulation and this test, the tester is not always necessary.

[Test pattern when reflecting result on tester]

● Test pattern to check only connections between macros and user logic with entire chip energized (actual operation mode).

● Create the test pattern in the following procedure:

① Perform simulation with an assembler program by using the supplied ROM and RAM in addition to the chip circuit diagram of the CBIC.

② Extract the test pattern at the cutting edge of the chip circuit diagram of the CBIC, and change the test pattern so that any input pattern contention is avoided. Perform simulation again with just the CBIC. Eliminate the pattern contention that cannot be sampled, and provide that test pattern to NEC.

A flowchart illustrating creation of the total chip simulation pattern for interfacing is shown on the next page.

● Cause for inclusion of pattern contention and counter-measures:

When the test pattern of the chip cutting edge of the CBIC is extracted, detailed skew timing is normalized, giving rise to a high possibility of pattern contention. To prevent this, a skew for setting limits with the tester must be set.

For the setting limit of the input skew at this time, refer to 7.4 **Notes on Creating More Than One Function Test Pattern.**

<<Reference>>

① Signals that probably will result in pattern contention are indicated below. These result when the test pattern for the cutting edge of the CBIC are used for total chip simulation with an external memory.

● Memory address for memory read, CSB, OEB signal, and read data input.

↓

A skew can be given to the read data as a counter-measure.

(This is because the access time is too short since the same models are used for the external memory and internal memory.)

● Contention with the clock frequently occurs. Therfore use a RZ signal with the clock to avoid any possible contention. Note, however, that some CPU macros may require that the clock be fixed to a "H" level to set the stop mode.

[When using for function verification simulation only]

This is a test pattern to verify the function by energizing the entire chip (actual operation mode).

Simulation is performed by using an assembler program. Since the result of simulation is not reflected on a tester, it is not necessary to confirm input pattern contention through simulation of the CBIC alone.

Total Chip Simulation Pattern Creation Flow

```
                 ┌───────────────────────────┐              ┌───────────────────────────┐
                 │ Create circuit diagram for │              │ Create program for total   │
                 │ total chip simulation      │              │ chip simulation (assembler)│
                 │ (CBIC + external ROM, RAM) │              │ and test pattern           │
                 └───────────────────────────┘              └───────────────────────────┘

                    ╱─────────────────────────────────────────╲        NG
                   ╱   Execute total chip simulation with       ╲───────────
                   ╲   circuit diagram for total chip simulation ╱
                    ╲─────────────────────────────────────────╱
                                      │ OK

                    ┌───────────────────────────────────────┐
                    │ Extract test pattern for CBIC alone     │
                    │ (create test pattern for cutting edge)   │
                    └───────────────────────────────────────┘

                    ┌───────────────────────────────────────┐
                    │ Confirm and correct "Hi-Z" and "X"      │
                    │ inputs to input mode of bidirectional    │
                    │ pin *1                                   │
                    └───────────────────────────────────────┘

                    ┌───────────────────────────────────────┐
                    │ Confirm test pattern contention         │
                    │ position and adds skew *2                │
                    └───────────────────────────────────────┘

                    ╱──────────────────────────────╲    NG    ┌──────────────────────┐
                   ╱  Total chip simulation with     ╲─ ─ ─ ─→│ Countermeasures for  │
                   ╲  CBIC alone                     ╱         │ skew addition *2      │
                    ╲──────────────────────────────╱          └──────────────────────┘
                                      │ OK

                    ┌───────────────────────────────────────┐
                    │ Interface pattern to NEC                │
                    └───────────────────────────────────────┘
```

*1 .... If "Hi-Z" or "X" exists immediately after the mode has been changed from the output mode to the input mode, use the same output pattern as the pattern immediately after the mode change ("1" or "0").

*2 .... Some restrictions must be observed in setting the skew. Refer to **7.4 Notes on Creating More Than One Function Test Pattern.**

7.9 Interface Format of Test Pattern

The following test pattern data should be provided to NEC:

(1) Test pattern data
(a) If "V.SIM" is used as sign off simulator
   ● TRC (simulation result)[*1] : trc format or tcp format
   ● Timing file   : alb format[*2]
   *1 ... Specify the information of strobe position at simulation.
   *2 ... NEC original format. Only when input skew (shift) is set or a RZ signal is used.

(b) If "Verilog" is used as sign off simulator
<If expected value is not "Don't care">
   ● TSSI (simulation result)[*1] : TSSI format
   ● Timing file   : TPIV format[*3]

<If expected value is "Don't care">
   ● NELPAT (expected value)[*1, *2] : NELPAT format
   ● Timing file   : TPIV format[*3]
   *1 ... Specify the information of strobe position at simulation.
   *2 ... With expected value
   *3 ... NEC original format

(2) ROM code data format
   ● Extended Intel HEX format
      or
   ● nincf format[*1]
   *1 ... NEC original format
   Be sure to <u>specify the corresponding information of ROM code data, ROM type and instance name</u>.

(3) Information on setting each megafunction separation test mode and information on pin for separation test
   This information is always necessary when megafunctions are integrated.
   Prepare a test pattern condition for the separation test. Also provide information for each megafunction on the access between the megafunction pins to be tested and the external pins. Please contact NEC for examples on entry format and other entry information.

(4) List of test pattern interface data/information
① Data/information for DC test
   ● Test pattern data (one)
   ● Strobe position at simulation
   ● Timing file (only when RZ signal and NRZ signal with skew are used)
   ● Measurement request pattern when the test pattern is satisfying static current dissipation measuring conditions; two or more positions required.
   ● Oscillation circuit DC characteristics measuring target pattern (only when oscillator circuit is integrated; one pattern or more)

② Data/information for function test
  ● Test pattern data (nine or less; none is available when used with test pattern for DC test)
  ● Strobe position at simulation (corresponds to each test pattern)
  ● Timing file (only when RZ signal and NRZ signal with skew are used. Specify the correspondence to each test pattern)

③ Critical path specification (when specified)

④ ROM code data (when ROM is integrated)
  ● ROM code data (corresponds to integrated ROM)
  ● Corresponding information of ROM code and ROM macro instance name

⑤ Each megafunction separation test information
  ● Separation mode specification information of each megafunction (decode information)
  ● External pin corresponding information in separation mode of each megafunction

CHAPTER 8   CREATING DEBUGGER

This chapter describes the emulation procedure required when a CPU macro is incorporated in the CB-C8 LSI circuit. In the case where the CPU macro (NA70008H) is part of the CB-C8, the customer needs to create an emulator, one that combines a general-purpose emulator and an adapter.

If the macro NAV30MX is used, this corresponds to a ROM emulator. In this case, consult NEC.

8.1   Using Standard LSI Chips

Fig. 8-1 shows an example of a debug environment for the CB-C8. Here a breadboard for CB-C8 emulation is configured by using a general-purpose in-circuit emulator which serves as the CPU and an adapter board built up of standard LSI circuits. This board and emulator is then extended to the target system.

Fig. 8-1   Example of Debug Environment of Adapter Board Using Standard LSIs

General-purpose in-circuit emulator for built-in CPU

Breadboard for emulation

Target system

To PC

Built with standard LSIs, FPGA, PLD, G/A, etc.
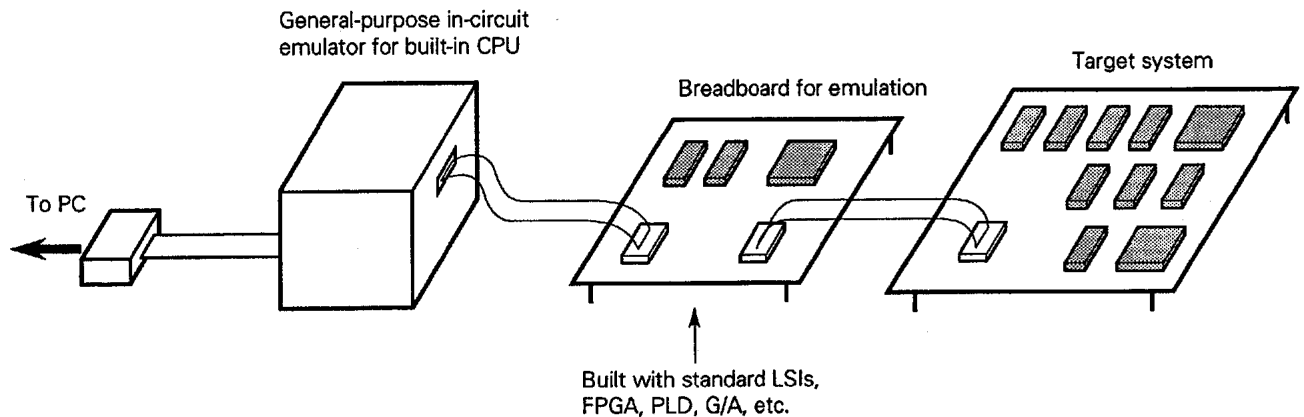
8.2   Using the CB-C8

If it is possible to finish creating the emulator after an engineering sample of the CB-C8 ASIC chip has been shipped, it is recommended that you replace the peripheral function part of the board that forms the CB-C8 functions with the actual CB-C8 sample.

When you design a CB-C8 circuit, it is very important to be able to isolate the CPU macro from the other circuits on the board in emulation mode. The CPU macro must also be accessible from external pins for test purposes.

Fig. 8-2 Example of Using the CB-C8 as an Emulation Chip

(Circuit diagram)
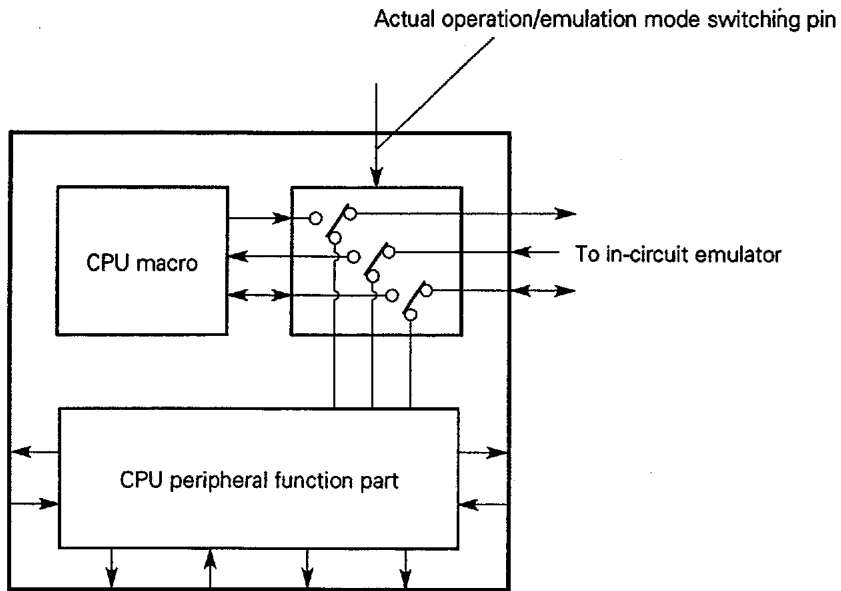
(Example of debugging environment)
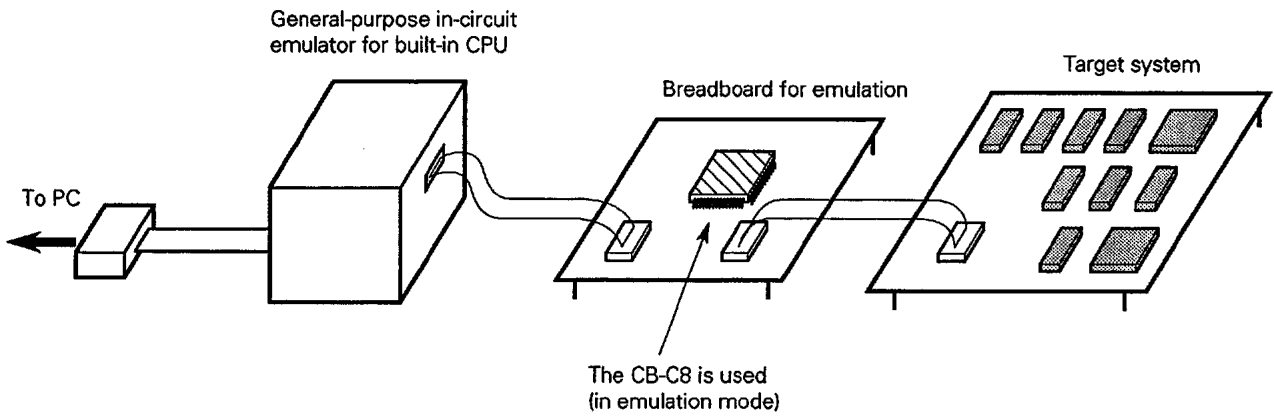
CHAPTER 9   RESTRICTIONS ON CB-C8 DESIGN

9.1   Restrictions on Creation of Circuit

9.1.1   Restrictions on naming

When creating a CB-C8 circuit, there are some restrictions on the naming of the circuit by the customer. This is due to limitations on certain development tools, such as the placement and routing program.

(1) Use only alphanumeric characters ($ added by the system is allowed).

(2) Characters used for names should not exceed eight characters. Up to twelve characters can be used for net names.

(3) The first character of a name should be alphabetic.

(4) Component names (F111, etc.) of megafunctions, functional cells, and interface blocks should not be used for naming other circuits.

(5) A name which contains GND or Vᴅᴅ should not be used as a block name or net name (reserved word).

(6) An array description, like a bus name, for example, D(7:0) is extracted into D7 through D0. The characters just before ( ) which indicates bus width should be alphabetic. Note that D[0] and D0 are recognized to be the same.

(7) In principle, the expression of bus names should begin from the bigger number (D(7:0), etc.). Note that when ascending and descending order expressions are mixed, the wiring may be twisted with some CAD tools.

9.1.2   Restrictions on circuit design

(1) Handling of unused pins

An output pin of a functional block must be connected to the input of another functional cell, megafunction, or interface block. However, if the block has two or more output pins such as a flip-flop and latch, at least one output pin must be connected.

When a dummy gate is used, it may generate an output pin which is not connected anywhere. In this case, the instance name of the dummy gate should be grasped in advance and then it should be checked against the error list of DRC result to confirm that there is no unconnected output pin.

(2) Limit of load capacitance

As shown in the illustration on the next page, the sum of the fan-ins of functional cells b, c, and d connected to the output of a functional cell a plus 0.17pF per pin as wiring capacitance should not exceed the maximum allowable output load capacitance of functional cell a.
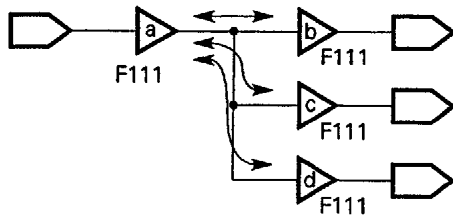
Functional cell type	F111
Fan-in load	0.060 pF
Number of pin-pairs	3
Maximum allowable output load capacitance	3.074 pF

(fan-in of buffer b, c, and d) = 0.060 × 3 + 0.17 × 3 = 0.69 pF < 3.074 pF : OK

(3) Unused input pin

Be sure to clamp all unused input pins of functionall cells to low or high by using the level generator block F091 (This rule should be observed even when a dummy gate is integrated).

(4) Bus configuration in customer specified logic

If configuring buses in the customer specified logic area, use 3-state buffers (F531, etc.) for the connection. Note that only one functional cell should be enabled on one bus line. Two or more cells must not be enabled at the same time.

When switching buses, the lines temporarily float. Therefore, design the bus switch timing so that the duration of the floating state is less than 20 ns.

(5) Differential circuit

Be sure not to design in a differential circuit such as shown below.
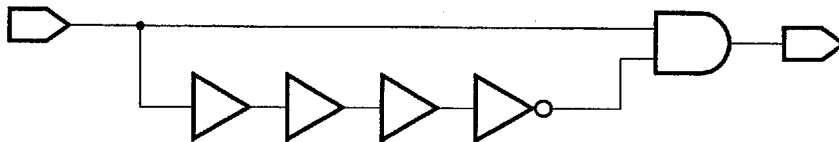
(6) Interface block

An interface block for a CB-C8 consists of a main buffer and a prebuffer. The main buffer is the part connected directly to the external pin and prebuffer is the logical part that interfaces with the internal circuits.

Items forbidden for the interface block are as follows:

• The main buffer should be connected to the specific prebuffer in strict accordance to the combinations described in the Block Library. Alternative combinations are not allowed.

• Be sure not to directly correct the main buffer of an input buffer to the main buffer of an output buffer.

(7) Restrictions on wired logic

Except for a 3-state buffer, wired logic technique prohibit connecting the output pins of a functional cell together in a CB-C8 design.

(8) Restrictions on high impedance input

Be sure not to input a high impedance to the pins of a functional block or a megafunction (except for the input pins which accept high impedance input according to the **CB-C8 Family User's Manual Block Library, the CB-C8 Family User's Manual Megafunction,** or this manual).

(9) Minimum pulse width

When a pulse width is input externally from an LSI circuit or generated within the LSI, it may be too narrow to be read and a malfunction may occur. For example, when reading data at the active edge of the clock, the expected logic operation cannot be executed because the clock pulse will return to the original level before reading the data completely. Therefore, the minimum pulse width required for data reading is defined.

For specifics on the minimum pulse width for a clock and for set/reset conditions concerning a CB-C8 design, refer to the **CB-C8 Family User's Manual Block Library.**

(10) Asynchronous circuit

In general, when creating customer specified logic, asynchronous circuit should not be used.

NEC cannot assure correct operation. When creating the single-phase clock synchronous circuit, be sure to use clock tree synthesis.

(11) Prohibited circuits

    (a) Shift register

A circuit such as shown below should not be created.
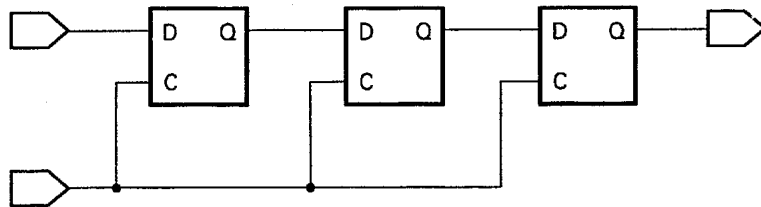
If you need the same function as shown above, use a configuration as shown below.
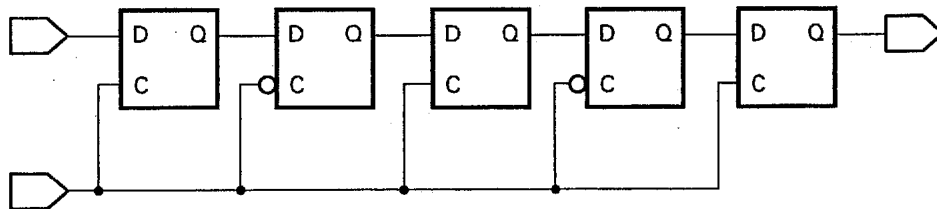
(b) Toggle circuit using D-F/F

In principle, the following circuit should not be created:
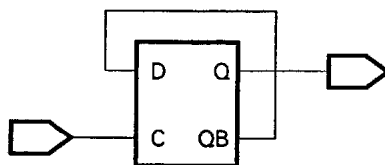
If you need the same function as above, use the dedicated toggle block.

(c) RS-latch using NAND or NOR gate

The following circuit should not be created:
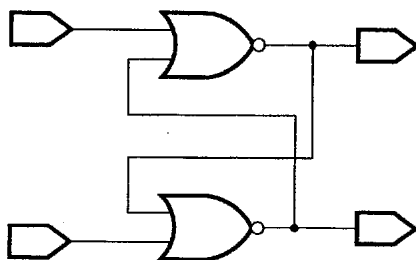
If you need the same function as above, use the dedicated RS-latch block.

9.1.3 Notes on creating circuit diagrams

(1) Through-path in circuit diagram

In principle, your circuit diagram should contain no through-path, that is the route where input and output buffers are connected only with wiring. Be sure to remove any from the diagram or to connect these pins via a function block, such as the F111.
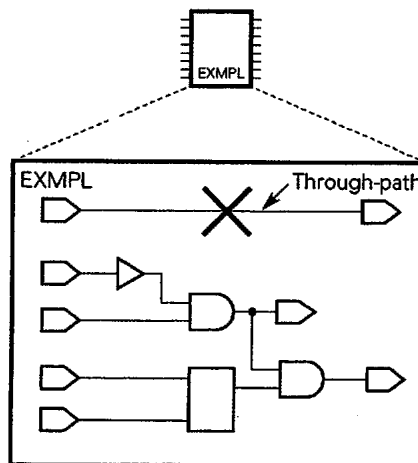
(2) Bus naming

Avoid such bus naming as shown below. It causes shorting because the expression will be recognized as follows.

A1 (7:0), A(15:0) → shorts with A10 to A15

With some CAD tools, the following may also create a short:

AD (07:00), AD (7:0) → recognized as AD7 to AD0

Therefore,

① The character just before the ( ) of bus width should be alphabetic.

② If two or more buses exist, do not use the same name for different buses, except for the characters between parenthesis ( ), which indicate the bus width.

9.2 Power Supply Pin Location and Oscillator Allocatable Pins

Location of power supply pins and oscillator allocatable pins are listed below.
This list includes packages under development. Before using them, contact NEC to confirm availability.

At present, the following three major material types are offered for QFP packages.
① Alloy .... Use ordinary lead frame material.
② Copper .... Use lead frame material of low thermal resistance.
③ Copper + HSP ..... Use lead frame material of low thermal resistance and heat spreader.

Power dissipation is a type of function used, as shown below:
① Alloy < ② Copper < ③ Copper + HSP
Select your package carefully. Packages with better heat dissipation are more expensive. Select a package that best suits your circuit needs.

[Power supply pin location and oscillator allocatable pins]
(Alloy)

(1/2)

Package type		GND pin	V_{DD} pin	Oscillator allocatable pins Note 1, 2	Number of signals	Noncon-nected pin Note 2
QFP	44-pin	17	39	(18, 19), (37, 38)	42	–
	52-pin	7, 33	34	(8, 9), (31, 32)	48	14
	64-pin	26, 58	27	(24, 25), (59, 60)	61	–
	80-pin	3, 22, 33, 43, 62	2, 23, 42, 63	(4, 5), (19, 20), (45, 46), (60, 61)	71	–
	100-pin	1, 28, 40, 53, 80	2, 29, 52, 79	(25, 26), (55, 56), (82, 83), (98, 99)	91	–
	120-pin	15, 31, 60, 75, 91, 120	1, 30, 61, 90	(33, 34), (57, 58) (93, 94), (117, 118)	110	–
	136-pin	35, 36, 67, 68, 103, 104, 135, 136	1, 34, 69, 102	(37, 38), (65, 66) (105, 106), (133, 134)	124	–
	160-pin	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	1, 20, 40, 81, 100, 120	(43, 44), (77, 78) (123, 124), (157, 158)	144	–
	208-pin	1, 2, 26, 51, 52, 79, 105, 106, 131, 155, 156, 182	27, 53, 78, 104, 130, 157, 183, 208	(3, 4), (49, 50), (107, 108), (153, 154)	188	–
TQFP	80-pin	1, 20, 41, 60	21, 40, 61, 80	(3, 4), (17, 18), (43, 44), (57, 58)	72	–
QFP(FP)	100-pin	26, 50, 76, 100	1, 25, 51, 75	(28, 29), (47, 48), (78, 79), (97, 98)	92	–
	120-pin	15, 31, 60, 75, 91, 120	1, 30, 61, 90	(33, 34), (57, 58), (93, 94), (117, 118)	110	–
	144-pin	37, 38, 71, 72, 109, 110, 143, 144	1, 36, 73, 108	(39, 40), (69, 70), (111, 112), (141, 142)	132	–
	160-pin	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	1, 20, 40, 81, 100, 120	(43, 44), (77, 78) (123, 124), (157, 158)	144	–
	176-pin	23, 45, 46, 87, 88, 111, 133, 134, 175, 176	1, 22, 44, 89, 110, 132	(47, 48), (85, 86), (135, 136), (173, 174)	160	–
	208-pin	1, 2, 26, 51, 52, 79, 105, 106, 131, 155, 156, 182	27, 53, 78, 104, 130, 157, 183, 208	(3, 4), (49, 50), (107, 108), (153, 154)	188	–

Note 1. The input pin and output pin of the oscillator should be adjacent. If you want to design using an allocation other than what is shown in the table, contact NEC.

   2. Note that in the combination of packages and step sizes, the pin adjacent to an oscillator allocatable pin is a non-connected pin. The number of available signal pins might decrease. Table 9-1 shows the combinations in which the oscillator location position is special or the adjacent pin becomes a non-connected pin.

(2/2)

Package type		GND pin	V_{DD} pin	Oscillator allocatable pins Note 1, 2	Number of signals	Nonconnected pin Note 2
PLCC	68-pin	1, 35	18, 52	(2, 3), (36, 37)	64	–
	84-pin	1, 43	22, 64	(2, 3), (44, 45)	80	–
PGA	72-pin	42, 48, 58, 64	41, 49, 57, 65	T.B.D.	64	–
	132-pin	53, 75, 97, 105, 106, 115, 123, 124	64, 86, 114, 132		120	–
	176-pin	57, 69, 81, 93, 105, 115, 120, 125, 135, 140	145, 153, 157, 161, 169, 173		160	–
	208-pin	65, 79, 93, 107, 121, 133, 139, 145, 157, 163, 174, 194	127, 151, 169, 179, 184, 189, 199, 204		188	–
	280-pin	137, 151, 165, 179, 193, 205, 217, 229, 244, 246, 254, 256, 264, 266, 274, 276	197, 199, 209, 211, 221, 223, 233, 235, 241, 251, 261, 271		252	–
	364-pin	293, 302, 315, 324, 329, 330, 331, 336, 337, 338, 339, 340, 341, 342, 343, 344, 349, 350, 351, 356, 357, 358, 359, 360, 361, 362, 363, 364	292, 314, 325, 326, 327, 328, 332, 333, 334, 335, 345, 346, 347, 348, 352, 353, 354, 355		T.B.D.	T.B.D.

Note 1. The input pin and output pin of the oscillator should be adjacent. If you want to design using an allocation other than what is shown in the table, contact NEC.

2. Note that in the combination of packages and step sizes, the pin adjacent to an oscillator allocatable pin is a non-connected pin. The number of available signal pins might decrease. Table 9-1 shows the combinations in which the oscillator location position is special or the adjacent pin becomes a non-connected pin.

[Power supply pin location and oscillator allocatable pins]
(Copper)

(1/2)

Package type		GND pin	V$_{DD}$ pin	Oscillator allocatable pins Note 2, 3	Number of signals	Noncon- nected pin Note 3
QFP	160-pin	21, 41, 42, 79, 80 101,121, 122, 159 160	1, 20, 40, 81, 100 120	(43, 44), (77, 78) (123, 124), (157, 158)	144	–
	184-pin	1, 24, 47, 70, 93 116, 139, 162	23, 46, 69, 92, 115, 138, 161, 184	(3, 4), (49, 50) (95, 96), (141, 142)	168	–
QFP (FP)	176-pin	23, 45, 56, 87, 88 111, 133, 134, 175 176	1, 22, 44, 89, 110 132	(47, 48), (85, 86) (135, 136), (173, 174)	160	–
	208-pin	1, 2, 26, 51, 52, 79 105, 106, 131, 155 156, 182	27, 53, 78, 104, 130 157, 183, 208	(3, 4), (49, 50) (107, 108), (153, 154)	188	–
	240-pin	1, 2, 20, 41, 59, 60 80, 101, 121, 122 139, 161, 179, 180 200, 221	21, 40, 61, 81, 100 120, 140, 160, 181 201, 220, 240	T.B.D	212	–
	256-pin Note 1	1, 2, 21, 44, 63, 64 85, 108, 129, 130 149, 172, 191, 192 213, 236	22, 43, 65, 86, 107 128, 150, 171, 193 214, 235, 256	(3, 4), (61, 62) (131, 132), (189, 190)	228	–
	272-pin Note 1	1, 2, 17, 34, 52, 67 68, 85, 102, 120 137, 138, 153, 170 188, 203, 204, 221 238, 256	18, 35, 51, 69, 86 103, 119, 136, 154 171, 187, 205, 222 239, 255, 272	T.B.D	236	–
	304-pin	1, 2, 20, 39, 40, 58 75, 76, 95, 96, 115 116, 133, 134, 153 154, 172, 191, 192 210, 227, 228, 247 248, 267, 268, 285 286	19, 37, 38, 57, 77 78, 113, 114, 151 152, 171, 189, 190 209, 229, 230, 265 266, 303, 304	(3, 4), (73, 74) (155, 156), (225, 226)	T.B.D.	T.B.D.

Note 1. This product is under development or under study.

   2. The input pin and output pin of the oscillator should be adjacent. When you attempt to design in an allocation other than what is shown in the table, contact NEC.

   3. Note that in the combination of packages and step sizes, the pin adjacent to an oscillator allocatable pin is a non-connected pin. The number of available signal pins might decrease. Table 9-1 shows the combinations in which oscillator location position is special or the adjacent pin becomes non-connected pin.

(2/2)

Package type		GND pin	V_{DD} pin	Oscillator allocatable pins Note 2, 3	Number of signals	Noncon- nected pin Note 3
TQFP	64-pin	9, 41	10	T.B.D.	T.B.D.	–
	100-pin	26, 50, 76, 100	1, 25, 51, 75	(28, 29), (47, 48) (78, 79), (97, 98)	92	–
	120-pin Note 1	15, 31, 60, 75, 91 120	1, 30, 61, 90	(33, 34), (57, 58) (93, 94), (117, 118)	110	–
LQFP	144-pin Note 1	37, 38, 71, 72, 109 110, 143, 144	1, 36, 73, 108	(39, 40), (69, 70) (111, 112), (141, 142)	132	–
	160-pin Note 1	21, 41, 42, 79, 80 101, 121, 122, 159 160	1, 20, 40, 81, 100 120	(43, 44), (77, 78) (123, 124), (157, 158)	144	–
	176-pin Note 1	23, 45, 46, 87, 88 111, 133, 134, 175 176	1, 22, 44, 89, 110 132	(47, 48), (85, 86) (135, 136), (173, 174)	160	–
	208-pin Note 1	1, 2, 26, 51, 52, 79 105, 106, 131, 155 156, 182	27, 53, 78, 104, 130 157, 183, 208	(3, 4), (49, 50) (107, 108), (153, 154)	188	–

Note 1. This product is under development or under study.

2. The input pin and output pin of the oscillator should be adjacent. When you attempt to design in an allocation other than what is shown in the table, contact NEC.

3. Note that in the combination of packages and step sizes, the pin adjacent to an oscillator allocatable pin is a non-connected pin. The number of available signal pins might decrease. Table 9-1 shows the combinations in which oscillator location position is special or the adjacent pin becomes non-connected pin.

[Power supply pin location and oscillator allocatable pins]
(Copper + HSP)

Package type		GND pin	V_{DD} pin	Oscillator allocatable pins Note 1, 2	Number of signals	Noncon-nected pin Note 2
QFP	160-pin	21, 41, 42, 79, 80 101,121, 122, 159 160	1, 20, 40, 81, 100 120	(43, 44), (77, 78) (123, 124), (157, 158)	144	–
QFP (FP)	160-pin	21, 41, 42, 79, 80 101, 121, 122, 159 160	1, 20, 40, 81, 100 120	(43, 44), (77, 78) (123, 124), (157, 158)	144	–
	176-pin	23, 45, 46, 87, 88 111, 133, 134, 175 176	1, 22, 44, 89, 110 132	(47, 48), (85, 86) (135, 136), (173, 174)	160	–
	208-pin	1, 2, 26, 51, 52, 79 105, 106, 131, 155 156, 182	27, 53, 78, 104, 130 157, 183, 208	(3, 4), (49, 50) (107, 108), (153, 154)	188	–
	304-pin	1, 2, 20, 39, 40, 58 75, 76, 95, 96, 115 116, 133, 134, 153 154, 172, 191, 192 210, 227, 228, 247 248, 267, 268, 285 286	19, 37, 38, 57, 77 78, 113, 114, 151 152, 171, 189, 190 209, 229, 230, 265 266, 303, 304	(3, 4), (73, 74) (155, 156), (225, 226)	T.B.D.	T.B.D.

Note 1. The input pin and output pin of the oscillator should be adjacent. If you want to design using an allocation other than what is shown in the table, contact NEC.

   2. Note that in the combination of packages and step sizes, the pin adjacent to an oscillator allocatable pin is a non-connected pin. The number of available signal pins might decrease. Table 9-1 shows the combinations in which the oscillator location position is special or the adjacent pin becomes a non-connected pin.

[Combinations in which oscillator location position is special or the adjacent pin becomes a non-connected pin]

In the combination of package and step size, when an oscillator is placed at the standard position, the adjacent pin becomes a non-connected pin. This means the number of available pins decreases by one. Changing the position of an oscillator can possibly avoid creation of a no-connect condition. The number of signals pins will not be reduced. Contact NEC for details on how to change the position of an oscillator.

Table 9-1 shows the various combinations where an oscillator cannot be integrated or where the oscillator location is a special case.

Table 9-1

(1/2)

	Package		Adjacent pin becomes a non-connected pin	Oscillator location position is special
Alloy	QFP	44-pin	T.B.D.	T.B.D.
		52-pin		
		64-pin		
		80-pin		B18, B57, D55, E54, E94
		100-pin	B57	C76
		120-pin	B97	–
		136-pin	B97, C37	D76, D16
		160-pin	–	–
		208-pin	–	T.B.D.
	TQFP	80-pin	T.B.D.	T.B.D.
	QFP (FP)	100-pin	B57	–
		120-pin	B97	T.B.D.
		144-pin	C37, C76	–
		160-pin	D16	–
		176-pin	D16	T.B.D
		208-pin	–	E54, E94
	PLCC	68-pin	T.B.D.	T.B.D.
		84-pin		
	PGA	72-pin	T.B.D.	T.B.D.
		132-pin		
		176-pin		
		208-pin		
		280-pin		
		364-pin		

(2/2)

Package			Adjacent pin becomes a non-connected pin	Oscillator location position is special
Copper	QFP	160-pin	T.B.D.	T.B.D.
		184-pin		
	QFP (FP)	176-pin		
		208-pin		
		240-pin		
		256-pin		
		272-pin		
		304-pin		
	TQFP	64-pin		
		100-pin		
		120-pin		
	LQFP	144-pin		
		160-pin		
		176-pin		
		208-pin		
Copper + HSP	QFP	160-pin		
	QFP (FP)	160-pin		
		176-pin		
		208-pin		
		304-pin		

9.3   Restriction on Simultaneous Output Buffer Operation

When an output buffer switches, charging or discharging of a capacitive load occurs as current flows between the load and the LSI chip. If the charging or discharging current is too high, noise may be generated in the power supply lines, causing malfunctions. Therefore, the number of output buffers operating simultaneously is limited by the following items:

① Number of power supply lines and GND pins
② Load capacitance (C_L)
③ Load driving capability of output buffer (I_{OL})
④ Input/output interface level

The following table shows the relationship of ① through ④ using a conversion multiplier, and the number of output buffers that can operated simultaneously.

To calculate the limit value of the buffers that can operate simultaneously, first, calculate the limit value from Table 9-2, and multiply the value obtained by the conversion multiplier shown in Table 9-3. There is no problem if the value is smaller than the actual number of output buffers operating simultaneously.

If the actual number of output buffers operating simultaneously exceeds the limit value, it is necessary to change the operation timing of the output buffer to avoid simultaneous operation. Alternately, it may be necessary to add power supply lines and GND pins.

Table 9-2   Limit Number of Output Buffers Operating Simultaneously

Number of V_{DD} pins	Number of GND pins	Load capacitance C_L (pF)					
		15	30	50	100	150	200
1	1	9	5	3.5	2.5	2.5	2
1~2	2	12	6.5	5	3.5	3.5	3
1~2	3	15	8.5	6	4.5	4	4
2~4	4	18	10	7.5	5.5	5	4.5
3~4	5	21	11	8.5	6.5	6	5.5
3~4	6	24	13	10	7.5	6.5	6.5
4~6	8	31	17	12	9.5	8.5	8
5~6	10	37	20	14	11	10	9.5
8~12	12	43	23	17	13	12	11
12	16	50	29	23	17	16	14
18	28	95	53	39	30	27	25

Table 9-3   Conversion Multiplier of Limit Number of Output Buffers Operating Simultaneously

Output level	Interface level	Driving capability	Conversion multiplier	Output level	Interface level	Driving capability	Conversion multiplier
CMOS	3 V	3.0 mA	× 2.99	CMOS	5 V	1.0 mA	× 2.50
		6.0 mA	× 1.48			2.0 mA	× 1.22
		9.0 mA	× 1.15			3.0 mA	× 0.94
		12.0 mA	× 1.00			6.0 mA	× 0.76
		18.0 mA	× 0.64			9.0 mA	× 0.56
		24.0 mA	× 0.72				

9.4 Limitations of Circuit Complexity

The CB-C8 offers 22 steps of its standardized master slices. The step size suitable for customer's circuit is determined by examination and selection of the following items:

(1) Wiring method (2-layer or 3-layer)
(2) Type and number of megafunctions
(3) Scale of customer specified logic (when clock tree synthesis is used, take its overhead into consideration.)
(4) Floor plan (megafunction placement)
(5) Package
(6) Number of required signals

When many megafunctions are used or when the customer specified logic part is small, a larger step size with more grids than the total number called for by macros may be required because unused spacing areas will automatically be generated on the chip during floor planning.

A method to find an adequate step size is described below. Note that this method should not be used for cost analysis, etc. It is just an initial approximation to come up with a suitable step size. The final step size required may be different depending on the routing of the wiring.

[Example when Σ (number of grids of megafunction) $\leq \Sigma$ (number of grids of customer specified logic)]

$$M + \frac{U + B}{\gamma} \leq L$$

M: Σ (number of grids of each megafunction including wiring field)
U : Σ (number of grids customer specified logic)
B : Σ (number of grids in interface block part)
L : Total number of grids in the step to be used
γ : Utilization of grids

Total number of grids by each step (for examining circuit scale) is shown in Table 9-4

Utilization of grids ····· Rate of usable grids to the number of incorporated
grids in customer specified logic part
2-layer: 0.5 (50 %)
3-layer: 0.7 (70 %)

Table 9-4 shows the maximum number of raw grids available for each step size.
To determine the number of gates available based on the number of grids depends on the routing and whether two or three-layer routing is used; and the types of functional blocks that will be used. A typical block selected for this conversion is the 2-input NAND which represents one gate.
The following "rule of thumb" reflects a typical value which is suitable for initial approximations:

1 gate ≈ 4.75 grid

For a more complete grid to gate conversion, information provided in the output list of the design rule check program or the exact grid value conversions as described in the CB-C8 block library should be used in the final analysis.

[Example: Σ (number of grids of megafunction) > Σ (number of grids of customers specified logic)]

A detailed study taking floor plans into consideration is required. Consult NEC for floor plans.

Table 9-4 Total Number of Grids for Examining Scale in Each Step

Step number	Maximum number of signal pins Note	Total number of grids for examining scale
B18	88	53400
B57	104	76700
B97	120	104000
C37	136	135700
C76	152	171600
D16	168	211300
D55	184	255500
D75	192	277800
E15	208	328800
E54	224	383500
E94	240	433200
F34	256	494400
F74	272	558200
G14	288	627400
G53	304	699800
G93	320	748900
H33	336	827000
H72	352	908100
J32	376	1038300
J71	392	1127000
K11	408	1221300
K90	440	1418100

Note   This value is further restricted depending on the package.
Be sure to examine the number of usable pins shown in tables **9.7 Step Size and Package Availability** and **9.2 Power Supply Pin Location and Oscillator Allocatable Pins.**

9.5 Maximum Allowable Power Consumption for Each Package

At an operating ambient temperature of 85°C and 70°C, the maximum allowable power consumption for each package type is shown on the following page. (Package information under development and under discussion is included. Be sure to check the availability/non-availability of packages and their schedules.

CB-C8 Maximum Allowable Power Consumption (Alloy) [W]

Package	Number of pins	Mold dimension (mm)	Lead pitch (mm)	Resin thickness (mm)	Ambient temperature (MAX.)	B18	B57	B97	C37	C76	D16	D55	D75	E15	E54	E94	F34	F74	G14	G53	G93	H33	H72	J32	J71	K11	K90
QFP	44	10x10	0.80	2.70	85°C	0.28	0.31	0.34	0.36	0.39																	
					70°C	0.39	0.42	0.46	0.50	0.54																	
	52	14x14	1.00	2.70	85°C	0.45	0.36	0.38	0.40	0.43	0.45	0.47	0.48	0.50	0.53	0.54	0.56										
					70°C		0.49	0.52	0.56	0.59	0.62	0.65	0.66	0.69	0.72	0.74	0.76										
	64	14x20	1.00	2.70	85°C	0.33	0.36	0.38	0.40	0.43	0.45	0.47	0.48	0.50	0.53	0.54	0.56										
					70°C	0.45	0.49	0.52	0.56	0.59	0.62	0.65	0.66	0.69	0.72	0.74	0.76										
	80	14x20	0.80	2.70	85°C	0.33	0.36	0.38	0.40	0.43	0.45	0.47	0.48	0.50	0.53	0.54	0.56										
					70°C	0.45	0.49	0.52	0.56	0.59	0.62	0.65	0.66	0.69	0.72	0.74	0.76										
	100	14x20	0.65	2.70	85°C				0.43	0.45	0.49	0.52	0.53	0.56	0.58	0.62	0.65	0.67	0.69	0.73	0.75	0.77	0.80	0.83			
					70°C				0.59	0.63	0.67	0.71	0.72	0.76	0.80	0.85	0.89	0.92	0.95	1.00	1.04	1.06	1.10	1.15			
	120	28x28	0.80	3.70	85°C													0.67	0.69	0.73	0.75	0.77	0.80	0.83	0.87	0.91	0.95
					70°C													0.92	0.95	1.00	1.04	1.06	1.10	1.15	1.20	1.25	1.31
	136	28x28	0.65	3.70	85°C				0.43	0.45	0.49	0.52	0.53	0.56	0.58	0.62	0.65	0.67	0.69	0.73	0.75	0.77	0.80	0.83	0.87	0.91	0.98
					70°C				0.59	0.63	0.67	0.71	0.72	0.76	0.80	0.85	0.89	0.92	0.95	1.00	1.04	1.06	1.10	1.15	1.20	1.25	1.31
	160	28x28	0.65	3.70	85°C																				0.85	0.89	0.91	0.98
					70°C																				1.17	1.20	1.25	1.34
	208	40x40	0.65	4.20	85°C																	1.06	1.10	1.17	1.20	1.25	1.34
					70°C																						
TQFP	80	12x12	0.50	1.05	85°C	0.28	0.29	0.30	0.32																		
					70°C	0.39	0.40	0.42	0.44																		
QFP	100	14x14	0.50	1.45	85°C		0.32	0.34	0.36	0.38	0.39	0.41	0.42	0.43	0.44	0.46	0.48	0.49									
					70°C		0.44	0.47	0.50	0.52	0.54	0.56	0.57	0.59	0.61	0.63	0.65	0.68									
	120	20x20	0.50	2.70	85°C			0.36	0.38	0.40	0.41	0.43	0.44	0.45	0.47	0.49	0.50	0.51	0.53	0.54	0.56	0.58	0.59				
					70°C			0.49	0.52	0.54	0.57	0.59	0.60	0.63	0.65	0.67	0.69	0.71	0.72	0.74	0.77	0.80	0.81				
(FP)	144	20x20	0.50	2.70	85°C				0.38	0.40	0.41	0.43	0.44	0.45	0.47	0.49	0.50	0.51	0.53	0.54	0.56	0.58	0.59	0.63			
					70°C				0.52	0.54	0.57	0.59	0.60	0.63	0.65	0.67	0.69	0.71	0.72	0.74	0.77	0.80	0.81	0.86			
	160	24x24	0.50	2.70	85°C						0.41	0.43	0.44	0.45	0.47	0.49	0.50	0.51	0.53	0.54	0.56	0.58	0.59	0.63	0.66		
					70°C						0.57	0.59	0.60	0.63	0.65	0.67	0.69	0.71	0.72	0.74	0.77	0.80	0.81	0.86	0.90		
	176	24x24	0.50	2.70	85°C						0.41	0.43	0.45	0.48	0.49	0.51	0.53	0.54	0.56	0.58	0.59	0.61	0.63	0.65	0.66	0.68	0.70
					70°C						0.57	0.59	0.60	0.63	0.67	0.67	0.72	0.71	0.72	0.74	0.77	0.80	0.81	0.86	0.88	0.90	0.93
	208	28x28	0.50	3.70	85°C						0.57	0.59	0.60	0.63	0.60	0.63	0.66	0.68	0.71	0.73	0.75	0.78	0.82	0.85	0.89	0.90	0.98
					70°C						0.81	0.83	0.86	0.87	0.82	0.86	0.90	0.93	0.98	1.00	1.04	1.08	1.12	1.17	1.22	1.25	1.34
PLCC	68	24.20	1.27	3.40	85°C				0.56	0.57	0.59	0.61	0.63	0.63	0.65												
					70°C				0.76	0.79	0.81	0.83	0.86	0.87	0.89												
	84	29.28	1.27	3.40	85°C				0.56	0.57	0.59	0.61	0.63	0.63	0.65												
					70°C				0.76	0.79	0.81	0.83	0.86	0.87	0.89												

CB-C8 Maximum Allowable Power Consumption [W]

Package	Number of pins	Mold dimension (mm)	Lead pitch (mm)	Resin thickness (mm)	Ambient temperature (MAX.)	B18	B57	B97	C37	C76	D16	D55	D75	E15	E54	E94	F34	F74	G14	G53	G93	H33	H72	J32	J71	K11	K90
PGA	72	27.94	2.54	2.50	85°C	0.87	0.89	0.91	0.93	0.93	0.95	0.95	0.95	0.98	0.98	0.98	0.98	1.00	1.00	1.00	1.00	1.00	1.33	1.33	1.33	1.33	1.33
					70°C	1.20	1.22	1.25	1.28	1.28	1.31	1.31	1.31	1.34	1.34	1.34	1.34	1.38	1.38	1.38	1.38	1.38	1.83	1.83	1.83	1.83	1.83
	132	35.56	2.54	2.90	85°C			1.03	1.05	1.11	1.14	1.18	1.18	1.21	1.25	1.25	1.29	1.29	1.29	1.29	1.33	1.33	1.33	1.33	1.33	1.33	1.33
					70°C			1.41	1.45	1.53	1.57	1.62	1.62	1.67	1.72	1.72	1.77	1.77	1.77	1.77	1.83	1.83	1.83	1.83	1.83	1.83	1.83
	176	38.10	2.54	2.81	85°C								1.43	1.48	1.48	1.54	1.54	1.54	1.54	1.54	1.60	1.60	1.60	1.60	1.60	1.60	1.60
					70°C								1.96	2.04	2.04	2.12	2.12	2.12	2.12	2.12	2.20	2.20	2.20	2.20	2.20	2.20	2.20
	208	43.18	2.54	3.20	85°C								1.38	1.43	1.48	1.54		1.60	1.60	1.60	1.67	1.67	1.67	1.67	1.67	1.67	1.67
					70°C								1.90	1.96	2.04	2.16		2.20	2.20	2.20	2.29	2.29	2.29	2.29	2.29	2.29	2.29
	280	48.26	2.54	2.90	85°C											2.16	2.16		1.54	1.67	1.74	1.82	1.82	1.90	1.90	2.00	2.00
					70°C														2.12	2.29	2.39	2.50	2.50	2.62		2.75	
	364	43.18	2.54	3.17	85°C														2.12	2.39	2.39	2.50	2.50	2.62	2.62	2.75	2.75
					70°C																						

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CB-C8 Maximum Allowable Power Consumption (Copper) [W]

Package	Number of pins	Mold dimension (mm)	Lead pitch (mm)	Resin thickness (mm)	Ambient temperature (MAX)	B18	B57	B97	C37	C76	D16	D55	D75	E15	E54	E94	F34	F74	G14	G53	G93	H33	H72	J32	J71	K11	K90
QFP	160	28X28	0.65	3.20	85°C								0.74	0.78	0.83	0.87	0.91	0.95	1.00	1.05	1.08	1.11	1.14	1.18	1.21	1.25	1.33
					70°C								1.02	1.08	1.15	1.20	1.25	1.31	1.38	1.45	1.49	1.53	1.57	1.62	1.67	1.72	1.83
	184	32x32	0.65	3.20	85°C											0.87	0.91	0.95	1.00	1.05	1.08	1.11	1.14	1.18	1.21	1.25	1.33
					70°C											1.20	1.25	1.31	1.38	1.45	1.49	1.53	1.57	1.62	1.67	1.72	1.83
	176	24x24	0.50	2.70	85°C											0.87	0.91	0.95	1.00	1.05	1.08	1.11	1.14	1.18	1.21	1.25	1.33
					70°C											1.20	1.25	1.31	1.38	1.45	1.49	1.53	1.57	1.62	1.67	1.72	1.83
(FP)	208	28x28	0.50	3.20	85°C										0.82	0.87	0.91	0.95	1.00	1.03	1.05	1.11	1.14	1.18	1.21	1.25	1.33
					70°C										1.12	1.20	1.25	1.31	1.38	1.41	1.45	1.53	1.57	1.62	1.67	1.72	1.83
	240	32x32	0.50	3.20	85°C														1.00	1.03	1.05	1.11	1.14	1.18	1.21	1.25	1.33
					70°C														1.38	1.41	1.45	1.53	1.57	1.62	1.67	1.72	1.83
	256	28x28	0.40	3.20	85°C														1.00	1.03	1.05	1.11	1.14	1.18	1.21	1.25	1.33
					70°C														1.38	1.41	1.45	1.53	1.57	1.62	1.67	1.72	1.83
	272	36x36	0.50	3.20	85°C														1.03	1.05	1.08	1.11		1.21	1.25	1.29	1.38
					70°C														1.41	1.45	1.49	1.53		1.67	1.72	1.77	1.90
	304	40x40	0.50	3.70	85°C																			1.67	1.72	1.33	1.42
					70°C																					1.83	1.96
TQFP	64	10x10	0.50	1.00	85°C																						
					70°C																						
	100	14x14	0.50	1.00	85°C																						
					70°C																						
	120	14x14	0.40	1.00	85°C																						
					70°C																						
LQFP	144	20x20	0.50	1.40	85°C						0.66	0.68	0.69	0.71	0.73	0.75	0.77	0.78	0.82	0.83	0.85	0.87	0.89	0.91	0.93	0.95	0.98
					70°C						0.90	0.93	0.95	0.98	1.00	1.04	1.06	1.08	1.12	1.15	1.17	1.20	1.22	1.25	1.28	1.31	1.34
	160	24x24	0.50	1.40	85°C						0.66	0.68	0.69	0.71	0.73	0.75	0.77	0.78	0.82	0.83	0.85	0.87	0.89	0.91	0.93	0.95	0.98
					70°C						0.90	0.93	0.95	0.98	1.00	1.04	1.06	1.08	1.12	1.15	1.17	1.20	1.22	1.25	1.28	1.31	1.34
	176	24x24	0.50	1.40	85°C						0.66	0.68	0.69	0.71	0.73	0.75	0.77	0.78	0.82	0.83	0.85	0.87	0.89	0.91	0.93	0.95	0.98
					70°C						0.90	0.93	0.95	0.98	1.00	1.04	1.06	1.08	1.12	1.15	1.17	1.20	1.22	1.25	1.28	1.31	1.34
	208	28x28	0.50	1.40	85°C														0.89	0.91	0.93	0.95	0.98	1.00	1.03	1.05	1.08
					70°C														1.22	1.25	1.28	1.31	1.34	1.38	1.41	1.45	1.49

CB-C8 Maximum Allowable Power Consumption (Copper + HSP) [W]

Package	Number of pins	Mold dimension (mm)	Lead pitch (mm)	Resin thickness (mm)	Ambient temperature (MAX)	B18	B57	B97	C37	C76	D16	D55	D75	E15	E54	E94	F34	F74	G14	G53	G93	H33	H72	J32	J71	K11	K90
QFP	160	28X28	0.65	3.20	85°C									1.54	1.54	1.54	1.54	1.54	1.54	1.54	1.54	1.54	1.54	1.54	1.54	1.54	1.54
					70°C									2.12	2.12	2.12	2.12	2.12	2.12	2.12	2.12	2.12	2.12	2.12	2.12	2.12	2.12
QFP	160	24X24	0.50	2.70	85°C								1.33	1.33	1.33	1.33	1.33	1.33	1.33	1.33	1.33	1.33	1.33				
					70°C								1.83	1.83	1.83	1.83	1.83	1.83	1.83	1.83	1.83	1.83	1.83				
(FP)	176	24x24	0.50	2.70	85°C									1.33	1.33	1.33	1.33	1.33	1.33	1.33	1.33	1.33	1.33				
					70°C									1.83	1.83	1.83	1.83	1.83	1.83	1.83	1.83	1.83	1.83				
	208	28x28	0.50	3.20	85°C														1.54	1.54	1.54	1.54	1.54	1.54	1.54	1.54	1.54
					70°C														2.12	2.12	2.12	2.12	2.12	2.12	2.12	2.12	2.12
	304	40x40	0.50	3.70	85°C																			2.11	2.11	2.11	2.11
					70°C																			2.89	2.89	2.89	2.89

9.6 Limit on the Number of Test Patterns

Refer to **7.3 Limits to Number of Test Patterns.**

9.7 Step Size and Package Availability

The circuit scale that can be incorporated changes depending on the package type and the number of pins. Customer should check that the system environment and circuit scale are within the range of the following table.

In the following table, some require several months to prepare lead frames, etc. Be sure to contact NEC for details when examining the development.

	Package		Available Step Size	
			MIN.	MAX.
Alloy	QFP	44-pin	B18	C76
		52-pin	B18	D55
		64-pin	B18	F34
		80-pin	B18	F34
		100-pin	B57	F34
		120-pin	B97	J32
		136-pin	B97	J32
		160-pin	D16	K90
		208-pin	J32	K90
	TQFP	80-pin	B18	C37
	QFP(FP)	100-pin	B57	F74
		120-pin	B97	H72
		144-pin	C37	H72
		160-pin	D16	K90
		176-pin	D16	K90
		208-pin	E54	K90
	PLCC	68-pin	C37	E54
		84-pin	C37	E54
	PGA	72-pin	T.B.D.	T.B.D.
		132-pin	T.B.D.	T.B.D.
		176-pin	T.B.D.	T.B.D.
		208-pin	T.B.D.	T.B.D.
		280-pin	T.B.D.	T.B.D.
		364-pin	T.B.D.	T.B.D.

Remark: The products under development and under study are included.

	Package		Available Step Size	
			MIN.	MAX.
Copper	QFP	160-pin	D75	K90
		184-pin	F34	K90
	QFP(FP)	176-pin	E54	K90
		208-pin	E54	K90
		240-pin	G14	K90
		256-pin	G14	K90
		272-pin	J32	K90
		304-pin	K11	K90
	TQFP	64-pin	B18	C37
		100-pin	B57	E15
		120-pin	T.B.D.	T.B.D.
	LQFP	144-pin	T.B.D.	T.B.D.
		160-pin	T.B.D.	T.B.D.
		176-pin	T.B.D.	T.B.D.
		208-pin	T.B.D.	T.B.D.
Copper + HSP	QFP	160-pin	D75	K90
	QFP(FP)	160-pin	D75	H72
		176-pin	E54	H72
		208-pin	G14	K90
		304-pin	J32	K90

Remark: The products under development and under study are included.

9.8 Sign-off Conditions and Interface Data

9.8.1 Basic sign-off conditions

(1) No error should exist in design rule check. (However, pseudo errors that have been confirmed to have no problem in advance is an exception, i.e. output open error of dummy gate incorporating part, etc.)

(2) The following items should be checked with sign-off simulator.
① Mismatch should not be found in the actual wiring length simulation for MAX. and MIN.
(When including a CPU macro, mismatch should not be found in extract pattern of the total chip simulation executed to CBIC chip circuit.)
② No error should be found in the timing check of actual wiring length simulation for MAX. and MIN. conditions. When the expected value is undefined , i.e. during a reset period, the subsequent value will not change regardless of what the output value of the timing error generation is. A case when the expected value and the result do not match in the pattern unit by this type of error is not available.
[Check item]
  • Set-up/hold time
  • Release/removal time
  • Minimum pulse width
  • Bus fight and bus floating should not last more than 20 ns.

9.8.2 Required data for interface

(1) Netlist with sign-off condition satisfied (PWC [Note 1] or EDIF format)

(2) Test pattern with sign-off condition satisfied (either TRC file of MAX simulation[Note 1]/tssi file[Note 1] and tpiv file[Note 1]/NELPAT[Note 1] and timing file[Note 2])
[Types of test pattern]
  • Customer specified macro separation test pattern
  • Test pattern for total chip simulation[Note 3,4] (pattern for CBIC chip)
  • Test pattern for ROM macro read verification with ROM code (for cases that include a ROM macro)
Be sure to prepare one test pattern that satisfies DC test conditions. For DC test conditions, refer to **7.5 Consideration for DC test.**

(3) In the case of including a ROM macro
  • NINCE [Note 1] or extended intel HEX format
  • Information of ROM code file name and ROM code header name, ROM block name and instance name (C$00**** in PWC)

(4) Other materials
① Check list
② CBIC products request specification
(including pin allocation table, megafunction test mode setting information)
③ Critical path instruction [Note 5]
④ Glitch noise confirmation [Note 5]
⑤ Design rule check result
⑥ Simulation result confirmation (before placement and routing, after placement and routing)
⑦ Examination result when there is other special requirement [Note 5]

Notes: 1. NEC original format

2. NEC original format (albatros format)

3. DC characteristics test conditions should be included to either customer specified macro separate test pattern or total chip simulation test pattern. (For details, refer to **CHAPTER 7 TEST PATTERN DESIGN.**)

4. Total chip simulation test pattern is not always necessary when operation is confirmed sufficiently with other test patterns.
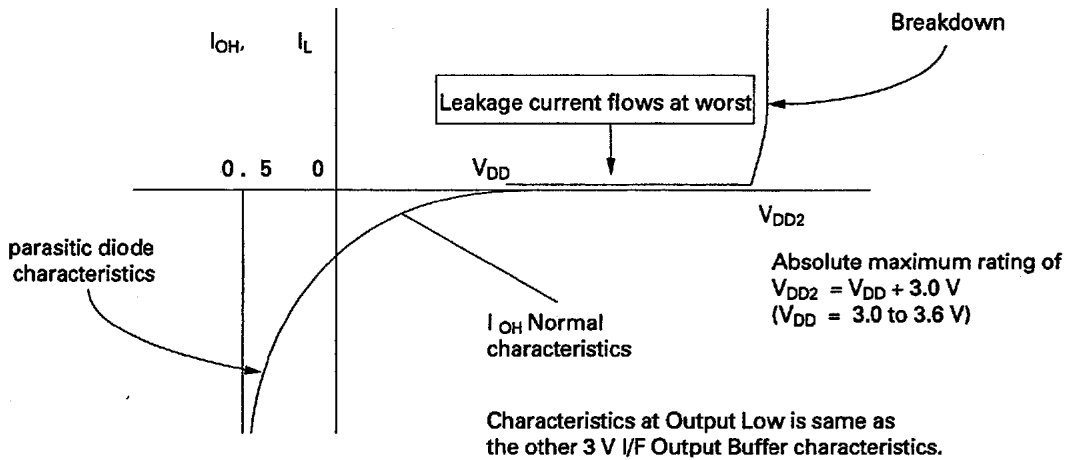
5. To be utilized as needed.

9.9 Notes on Using Interface Block

In the CB-C8 5 V I/F buffer, protection circuit exists as shown below. When interfacing with 5 V-system bus, note the following characteristics.

V_{DD}

V_{DD2}

I_L

Rpull-up

Protection Circuit

PAD

GND
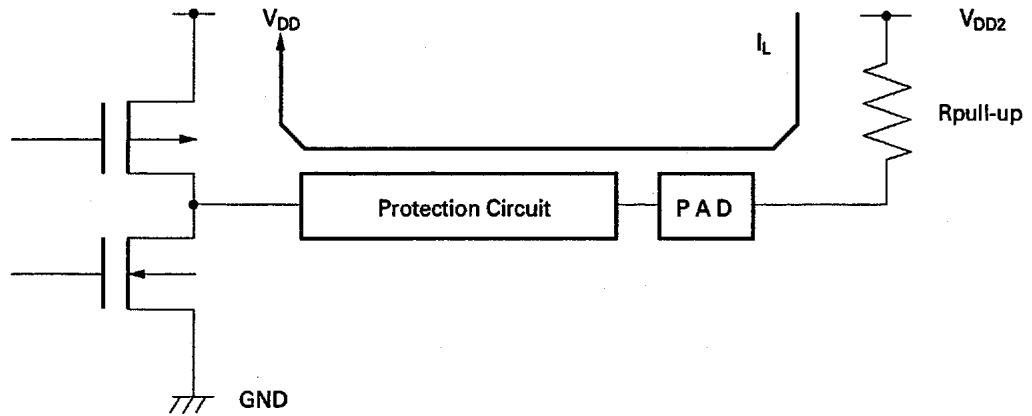
[Characteristics]

CASE : 1) Typical output buffer characteristics   Rpull-up
            OUTPUT : HIGH

$I_{OH},$ I_L

Breakdown

Leakage current flows at worst

0.5   0 V_{DD}

V_{DD2}

parasitic diode characteristics

I_{OH} Normal characteristics

Absolute maximum rating of
$V_{DD2} = V_{DD} + 3.0$ V
($V_{DD} = 3.0$ to 3.6 V)

Characteristics at Output Low is same as
the other 3 V I/F Output Buffer characteristics.

CASE : 2) 3-state BUFFER, I/O BUFFER
            3-state Hi-z, in I/O input mode

$I_{OH},$ I_L

Breakdown

0.5   0

V_{DD2}

parasitic diode characteristics

Absolute maximum rating of
$V_{DD2} = V_{DD} + 3.0$ V
($V_{DD} = 3.0$ to 3.6 V)

Characteristics at Output High is same as the 5V I/F
Output Buffer characteristics.   (CASE : 1)
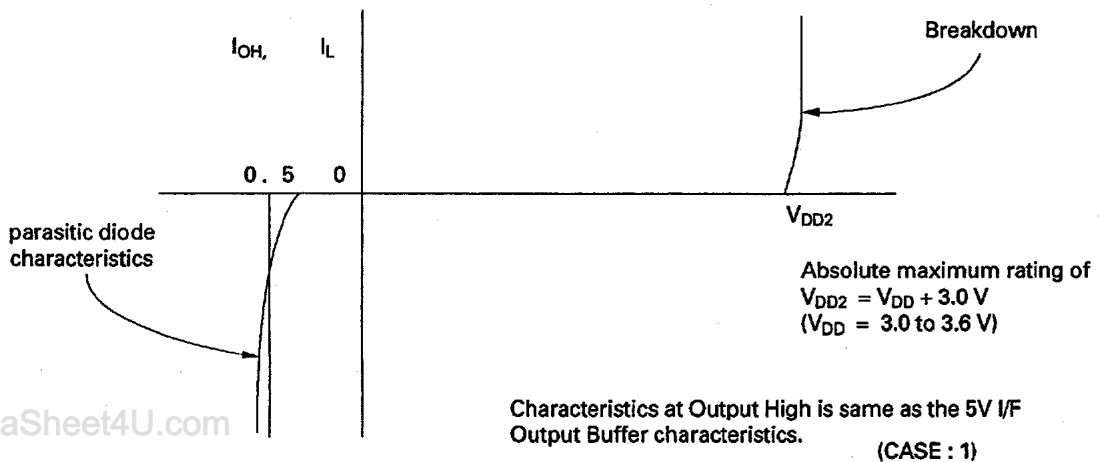
CHAPTER 10 ESTIMATING CHARACTERISTICS

10.1 Electrical Characteristics (Preliminary)

The DC and AC characteristics of the CB-C8 family are shown below.

10.1.1 Absolute maximum ratings (Preliminary)

Parameter	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		−0.5 to + 4.6	V
Input/Output Voltage 3 V Interface Block 5 V Interface Block	V_I/V_O		−0.5 to 4.6 V and $V_I/V_O < V_{DD} + 0.5$ V −0.5 to 6.6 V and $V_I/V_O < V_{DD} + 3.0$ V	V
Output Current	I_O	$I_{OL} = 3$ mA $I_{OL} = 6$ mA $I_{OL} = 9$ mA $I_{OL} = 12$ mA $I_{OL} = 18$ mA $I_{OL} = 24$ mA	10 20 30 40 60 80	mA
Operating Ambient Temperature	T_A		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

10.1.2   DC characteristics (Preliminary)

(V_{DD} = 3.3 V ± 0.3 V, T_A = −40 to +85 °C)

Parameter			Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Static Current Consumption [Note 1]			I_{DDS}	V_I = V_{DD} or GND	B18 to H33 [Note 2]			200	mA
					H72 to K90 [Note 2]			300	
Off-State Output Current			I_{OZ}	V_O = V_{DD} or GND				T.B.D.	mA
Input Clamp Voltage [Note 3]			V_{IC}			T.B.D.			V
Output Short-Circuit Current [Note 4]			I_{OS}			T.B.D.			mA
Input Leakage Current			I_I						
	Normal Input			V_I = V_{DD} or GND			10^{-5}	10	mA
	With Pull-Up Resistor (50 kΩ)			V_I = GND			−66		mA
	With Pull-Up Resistor (5 kΩ)			V_I = GND			−660		mA
	With Pull-Down Resistor (50 kΩ)			V_I = V_{DD}			66		mA
Low-Level Output Current			I_{OL}						
	Normal Output								
		3 mA		V_{OL} = 0.4 V		3			mA
		6 mA				6			mA
		9 mA				9			mA
		12 mA				12			mA
		18 mA				18			mA
		24 mA				24			mA
	5 V I/F BUFF								
		3 mA				3			mA
		6 mA				6			mA
		9 mA				9			mA
High-Level Output Current			I_{OH}						
	Normal Output								
		3 mA		V_{OH} = 2.4 V		−3			mA
		6 mA				−6			mA
		9 mA				−9			mA
		12 mA				−12			mA
		18 mA				−18			mA
		24 mA				−24			mA
	5V I/F BUFF								
		3 mA				−3			mA
		6 mA				−3			mA
		9 mA				−3			mA
Low-Level Output Voltage			V_{OL}						
	3 V Interface Block			I_{OL} = 0 mA				0.1	V
	5 V Interface Block							0.1	V
High-Level Output Voltage			V_{OH}						
	3 V Interface Block			I_{OH} = 0 mA		V_{DD}-0.1			V
	5 V Interface Block					V_{DD}-0.2			V

Note 1. When using interface blocks with pull-up/pull-down resistors or oscillation circuits, the static current consumption increases.

2. Step size

3. Input clamp voltage V_{IC} means the voltage is clamped when the input signal is negative. In the case of under-shooting or ringing of input signal, input signal is clamped at this voltage.

4. Output short-circuit current should be within 1 second, for one pin of LSI.

Remark In table 10.1.2, + and − added to current values indicate the direction of the current. The + is for the flow into the device and the − for the flow out of the device.

10.1.3 AC Characteristics (Preliminary)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Toggle Frequency	f_{tog}	Internal toggle F/F	175			MHz
Propagation Delay Time	t_{PD}	Internal gate F/O = 2, L = 2 mm		0.22		ns
		Input buffer F/O = 2, L= 2 mm		0.36		ns
		Output buffer C_L = 15 pF, I_{OL} = 9 mA		1.46		ns
Output Rise Time	t_r	C_L = 15 pF, I_{OL} = 9 mA		1.88		ns
Output Fall Time	t_f	C_L = 15 pF, I_{OH} = −9 mA		1.32		ns

10.1.4 Capacitance $(V_{DD} = V_I = 0)$ (Preliminary)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V		10	20	pF
Output Capacitance	C_{OUT}			10	20	pF
I/O Capacitance	$C_{I/O}$			10	20	pF

10.1.5 Recommended operating conditions (Preliminary)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	V_{DD}	3.3 V CMOS level	3.0	3.3	3.6	V
Negative Trigger Voltage	V_N		0.6		1.8	V
Positive Trigger Voltage	V_P		1.2		2.4	V
Hysteresis Voltage	V_H		0.3		1.5	V
Low-Level Input Voltage	V_{IL}	3 V interface block	0		0.3 V_{DD}	V
		5 V interface block	0		0.8	V
High-Level Input Voltage	V_{IH}	3 V interface block	0.7 V_{DD}		V_{DD}	V
		5 V interface block	2.2		5.5	V
Input Rise or Fall Time	t_r t_f		0 0		200 200	ns ns
Input Rise or Fall Time (Schmitt triggered)	t_r t_f		0 0		10 10	ms ms

Remark When incorporating a megafunction, the range of power supply voltage and ambient temperature may change depending on the megafunction. The value of rise or fall time, when using a schmitt triggered input buffer, changes depending on the operating environment of schmitt triggered input pins. Therefore, simultaneous operation of output buffer, etc. should be studied when using schmitt triggered types.

10.2 Delay Time of Functional Cells and Interface Blocks

The propagation delay time of an internal functional cell and interface block of CB-C8 cell-based IC depends heavily on the load capacitance.

To facilitate a rough estimate of the delay time, the equation below can be used. The equation is subject to increasing error as the load L, increases. It is best to confirm the actual delay, using the delay times generated from simulation.

First, calculate the load capacitance connected to output pin.

- Load capacitance : $C_L = \Sigma C_{IN} + L \times 0.17$ (pF)

1) $C_L < 0.5$ pF

$t_{PD} = t_{PD0A} + C_L \times K_A$ (ns)

2) $C_L \geq 0.5$ pF

$t_{PD} = t_{PD0B} + C_L \times K_B$ (ns)

C_{IN} : Input capacitance (pF) $[C_{IN}]$
L : Wiring length (mm)

t_{PD0A} : Gate delay (ns) [Intrinsic A]
K_A : Delay coefficient (ns/pF) [Extrinsic A]

t_{PD0B} : Gate delay (ns) [Intrinsic B]
K_B : Delay coefficient (ns/pF) [Extrinsic B]

Remark: [ ] are expressions in block library.

As for the values of C_{IN}, t_{PD0A}, K_A, t_{PD0B} and K_B, refer to **CB-C8 Family User's Manual Block library.**

Maximum/minimum value of propagation delay time can be calculated by using the maximum or minimum value described in block library as t_{PD0A}, K_A, t_{PD0B} and K_B in the above formula.

10.3 Power Consumption of Functional Cells and Interface Blocks (Preliminary)

The power consumption of an internal functional cell and interface block of CB-C8 cell-based IC also depends heavily on the load capacitance and operating frequency.

To facilitate a rough estimate of the delay time, the equation below can be used. The equation is subject to increasing error as the load L, increases. It is best to confirm the actual delay, using the delay times generated from simulation.

(1) Power consumption of functional cell (except for megafunction and memory macro)

Σ (K $\times$ 2.08 $\times$ f $\times$ number of gates) μW

or Σ (K $\times$ 0.42 $\times$ f $\times$ number of grids) μW (K: Operating ratio, f: Operating frequency (MHz),

2 input NAND (F302) = 1 gate)

Remark Operating ratio shows the ratio of transistors which are actually switching in the functional cells. For example, when data input for a D-F/F is fixed, all of the transitors of the D-F/F do not always switch at the clock frequency. Therefore, the operating ratio depends on the application of customer specified circuit. In general, the ratio is about 1/3 except for the special applications, such as high-speed data processing.

(2) Power consumption of interface block

(a) Power consumption of input buffer and bidirectional buffer input : ΣP_I

Power consumption of an input buffer and a bidirectional buffer input can be calculated by the following formula:

$$\Sigma P_I = \Sigma\ (12 \times f + P_A) \quad (\mu W)$$

f : Operating frequency (MHz)

P_A :   110 μW (with 50 kW pull-up/down resistor)

1100 μW (with 5 kW pull-up resistor)

(b) Power consumption of output buffer and bidirectional buffer output : ΣP_O

Power consumption of an output buffer and bidirectional buffer output can be calculated by the following formula:

$$\Sigma P_O = \Sigma P_{AC} + \Sigma P_{DC} \quad (\mu W)$$

P_{AC}: AC power consumption

P_{DC}: DC power consumption

AC power consumption is the power consumed when the output buffers switch.

DC power consumption is the power consumed when the output of output buffer, connected with resistive load, is fixed high or low.

When the load is capacitive, assume 0 as the DC power consumption.

$$P_{AC} = 80 + (25 + 12 \times (C_L + 15)) \times f + P_A \quad (\mu W)$$

f : Operating frequency (MHz) (*)

C_L: Load capacitance (pF)

P_A: 110 μW (with 50 kΩ pull-up/pull-down resistor)

1100 μW (with 5 kΩ pull-up resistor)

* ... Output buffer operates continuously or intermittently depending on the characteristics of the output signal. The power consumption can be estimated by using the formula for average operating frequency as shown below:

$$f_A = f_B \times T_B\ /\ T_C$$

f_A : Average operating frequency (MHz)

f_B : Operating frequency in normal operation (MHz)

T_B : Normal operating period (ns)

T_C : Intermittent operating cycle (ns)

$$P_{DC} = V_{OL} \times I_{OL} \times (1 - DUTY) + (V_{DD} - V_{OH}) \times I_{OH} \times DUTY$$

Remark DUTY means the rate of time during which output level is high.

DUTY = a/t
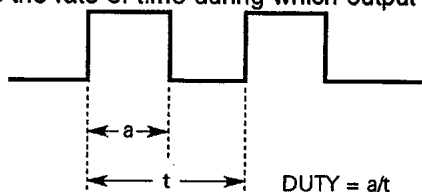
10.4   Current Consumption of Oscillation Block

Now under evaluation.

10.5   Current Consumption of Memory Block

Refer to **CB-C8 Family User's Manual Memory Macro Design.**

CHAPTER 11 SPECIAL CIRCUIT

11.1 Oscillation Circuit

11.1.1 Outline of oscillation block

There are six oscillation blocks offered in the CB-C8 library as shown in the following table. Each block has a recommended oscillation range. Be sure to select the block most suitable for your purposes.

All oscillation blocks have pins for stop control. For more information on the oscillator allocatable pins, refer to **9.2 Power Supply Pin Location and Oscillator Allocatable Pins.**

Block Name	Recommended Oscillating Frequency			Unit
	MIN.	TYP.	MAX.	
OSB1		32		kHz
OSB3		4		MHz
OSB4		8		MHz
OSB5		16		MHz
OSB6		32		MHz
OSB7		40		MHz

Remark MIN. value, MAX. value and using conditions are now under evaluation. When using overtone with a resonator of 24 MHz or more, a tank circuit composed of L and C should be used.

Operations of oscillation block and pin function are described below;

(Pin function)

(Symbol)

H01 — XT1   EN — H02
OSB1 to OSB7
N02 — XT2   OUT — N01
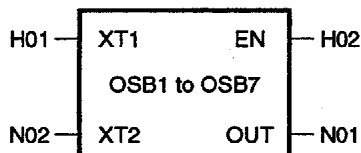
(Truth table) Common to OSB1 to OSB7

H01(XT1)	H02(EN)	N01(OUT)	N02(XT2)	
0	1	0	1	
1	1	1	0	
0	0	0	1	
1	0	0	x	← Prohibited

Pin name	Function name	Description
H01	XT1	External input pin connected to external resonator. External clock is input from this pin in external clock input mode.
N02	XT2	External input pin connected to the other side of external resonator. This pin is open in external clock input mode.
H02	EN	Oscillation enable pin. High level input enables starting oscillation and low level input stops oscillating.
N01	OUT	Internal clock signal output pin. The phase of this pin is the same with that of H01 (except for prohibited state).

Remark When an external clock input is required for an oscillation block, contact NEC. (In this case, it may not be possible to use a stop control on the oscillation block, and the output pin should be left open.)

11.1.2 Notes on using oscillation block

When using oscillation blocks, please note the following points:

(1) When a stop control is not used, the stop control signal should be clamped to attain the proper operational state. (EN=1)

(2) When using a stop control, be sure to add the stop mode in the test pattern for the DC customers test.

(3) During simulation, when set to the stop mode (EN=0), a low level should be given to the external input (XT1) and the expected value at the external output (XT2) should be high.

(4) When the stop control of the oscillation block is executed directly from a megafunction, be sure to check the active level of each block.

(5) When incorporating multiple oscillation circuits, contact NEC.

(6) Design the circuit taking into account the oscillation stabilization time after releasing the stop command. (The oscillation stabilization time for each frequency is now under evaluation.)

11.2 Interface Block with Pull-Up/Pull-Down Resistor

The interface block has the follwing pull-up/pull-down resistors for the CB-C8 family.

$(V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}, T_A = -40 \text{ to } +85 \text{ °C})$

Item	MIN.	TYP.	MAX.	Unit
Pull-up resistor		5		kΩ
		50		kΩ
Pull-down resistor		50		kΩ

Remark MIN. value and MAX. value are now under evaluation.

NEC ASIC DESIGN CENTERS

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  P.O. Box 7241
  Mountain View, CA 94039

  TEL   415-965-6533
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  FAX   305-428-5906

NEC
NEC Electronics Inc.

CORPORATE HEADQUARTERS

475 Ellis Street
P.O. Box 7241
Mountain View, CA 94039
TEL 415-960-6000

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