CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C383
CY7C384

Very High Speed 2K (6K) Gate CMOS FPGA

Features

- Very high speed
  - Loadable counter frequencies greater than 100 MHz
  - Chip-to-chip operating frequencies up to 85 MHz
  - Input + logic cell + output delays under 9 ns
- Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic
- High usable density
  - 12 x 16 array of 192 logic cells provides 6,000 total available gates
  - 2,000 typically usable "gate array" gates in 68- and 84-pin PLCC/CPGA packages
- Low power, high output drive
  - Standby current typically 2 mA
  - 16-bit counter operating at 100 MHz consumes 50 mA
  - Minimum I_{OL} and I_{OH} of 8 mA
- Flexible logic cell architecture
  - Wide fan-in (up to 14 input gates)
  - Multiple outputs in each cell
  - Very low cell propagation delay (3.4 ns)
- Low-cost, powerful design tools
  - Designs entered in VHDL, schematics, or both
  - Fast, fully automatic place and route
  - Waveform simulation with back annotated net delays
  - PC and workstation platforms
- Robust routing resources
  - Fully automatic place and route of designs using up to 100 percent of logic resources
  - No hand routing required
- 56 (CY7C383) to 68 (CY7C384) bidirectional input/output pins
- 6 dedicated input/high-drive pins
- 2 clock/dedicated input pins with fan-out-independent, low-skew nets
  - Clock skew <1 ns
- Input hysteresis provides high noise immunity
- Thorough testability
  - Built-in scan path permits 100 percent factory testing of logic and I/O cells
  - Automatic Test Vector Generation (ATVG) software supports user testing after programming
- CMOS process with ViaLink© programming technology
  - High-speed metal-to-metal link
  - Non-volatile antifuse technology
- 68-pin PLCC is compatible with CY7C382 footprint for easy upgrade
- 84-pin PLCC is compatible with ACT1020 power supply and ground pinouts

Functional Description

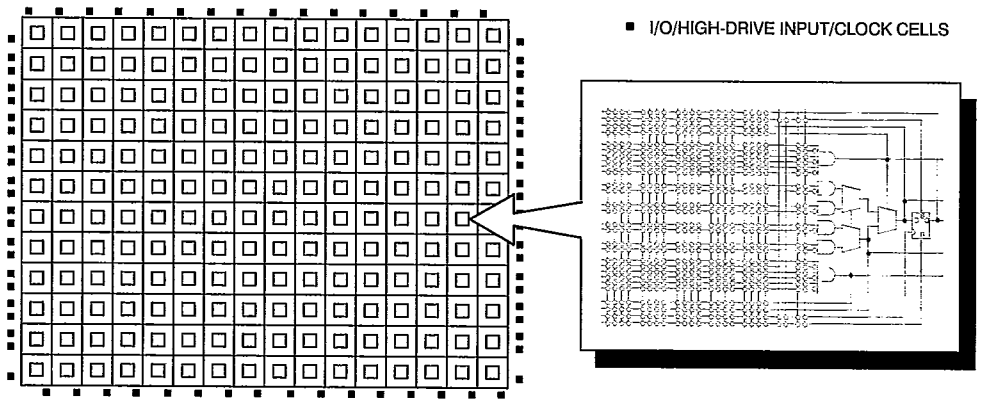
The CY7C383 and CY7C384 are members of the pASIC380 family of very high speed CMOS user-programmable ASIC (pASIC) devices. The 192 logic cell field-programmable gate array (FPGA) offers 2,000 typically usable "gate array" gates. This is equivalent to 6,000 EPLD or LCA gates. The CY7C383 is available in a 68-pin PLCC. The CY7C384 is available in an 84-pin PLCC and CPGA.

Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 100 MHz with input and output delays under 4 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C383 and CY7C384 using Cypress *Warp3* software or one of several third-party tools. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C383 and CY7C384 feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

Logic Block Diagram



68 or 84 PINS, INCLUDING 68 I/O CELLS, 6 INPUT HIGH-DRIVE CELLS, 2 INPUT/CLK (HIGH-DRIVE) CELLS c383-1

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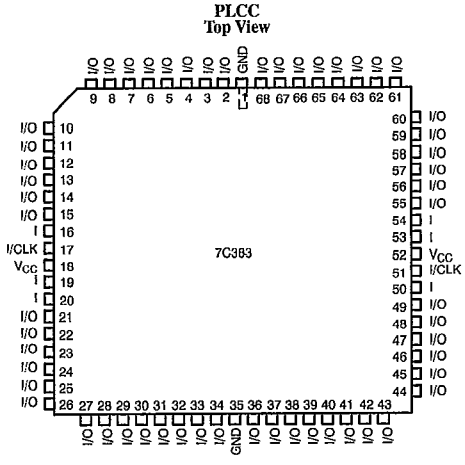
CYPRESS SEMICONDUCTOR

PRELIMINARY

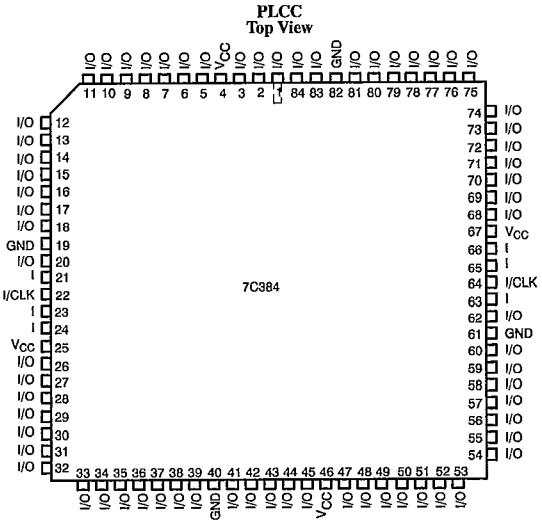
CY7C383
CY7C384

Pin Configurations

PLCC
Top View



PLCC
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature
Ceramic ..... −65°C to +150°C
Plastic ..... −40°C to +125°C
Lead Temperature ..... 300°C
Supply Voltage ..... −0.5V to +7.0V
Input Voltage ..... −0.5V to V_{CC} +0.5V
ESD Pad Protection ..... ±2000 V
DC Input Voltage ..... ±20 mA
Latch-Up Current ..... ±100 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40° to +85°C	5V ± 10%

Delay Factor (K)

Speed Grade	Industrial		Commercial	
	Min.	Max.	Min.	Max.
−0	0.4	1.67	0.46	1.55
−1	0.4	1.43	0.46	1.33
−2			0.46	1.25

Shaded area contains advanced information.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = − 4.0 mA	3.7		V
		I_{OH} = − 8.0 mA	2.4		V
		I_{OH} = − 10.0 µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
		I_{OL} = 10.0 µA		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	V_{IN} = V_{CC} or GND	−10	+10	µA
I_{OZ}	Output Leakage Current	V_{IN} = V_{CC} or GND	−10	+10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = GND	−10	−80	mA
		V_{OUT} = V_{CC}	30	140	mA
I_{CC1}	Standby Supply Current	V_{IN}, $V_{I/O}$ = V_{CC} or GND		10	mA
I_{CC2}	Supply Current[1, 2]	f = 1.0 MHz, V_I = V_{CC} or GND		25	mA

Capacitance

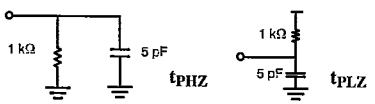
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance[3]	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 5.0V$	10	pF
C_{OUT}	Output Capacitance		20	pF

Switching Characteristics Over the Operating Range

Parameter	Description	Propagation Delays[4] with Fanout of 1	2	3	4	8	Unit
LOGIC CELLS							
t_{PD}	Combinatorial Delay[5]	3.4	3.8	4.2	4.8	8.1	ns
t_{SU}	Set-Up Time[5]	3.7	3.7	3.7	3.7	3.7	ns
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t_{CLK}	Clock to Q Delay	3.0	3.3	3.8	4.3	4.9	ns
t_{SET}	Set Delay	2.7	3.1	3.5	4.1	7.4	ns
t_{RESET}	Reset Delay	2.9	3.2	3.6	4.2	7.5	ns
t_{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t_{CWLO}	Clock LOW Time	3.6	3.6	3.6	3.6	3.6	ns
t_{SW}	Set Width	2.1	2.1	2.1	2.1	2.1	ns
t_{RW}	Reset Width	1.9	1.9	1.9	1.9	1.9	ns
INPUT CELLS							
t_{IN}	Input Delay (HIGH Drive)	3.7	3.8	4.2	4.6	6.4	ns
t_{INI}	Input, Inverting Delay (HIGH Drive)	3.5	3.6	4.0	4.4	6.2	ns
t_{IO}	Input Delay (Bidirectional Pad)	2.3	2.6	3.2	4.1	5.5	ns
t_{GCK}	Clock Buffer Delay [6]	4.4	4.5	4.6	4.6	5.0	ns
		Propagation Delays[4] with Output Load Capacitance (pF) of					
OUTPUT CELLS		**30**	**50**	**75**	**100**	**150**	
t_{OUTLH}	Output Delay LOW to HIGH	3.1	3.8	4.6	5.5	7.2	ns
t_{OUTHL}	Output Delay HIGH to LOW	3.1	3.9	5.0	6.1	8.3	ns
t_{PZH}	Output Delay Three-State to HIGH	4.4	5.3	6.5	7.7	10.1	ns
t_{PZL}	Output Delay Three-State to LOW	4.0	4.6	5.4	6.2	7.7	ns
t_{PHZ}	Output Delay HIGH to Three-State[7]	3.3	3.3	3.3	3.3	3.3	ns
t_{PLZ}	Output Delay LOW to Three-State[7]	3.7	3.7	3.7	3.7	3.7	ns

Notes:

1. Measured with twelve 16-bit counters configured internally and all outputs driving. To calculate power for your application, see the "pASIC380 Power vs. Operating Frequency" application note.
2. Guaranteed but not 100% tested.
3. C_I = 20 pF max. on pin 50 (7C383) or pin 63 (7C384.).
4. Worst-case propagation delay times over process variation at V_{CC} = 5.0V and $T_A = 25°C$. Mulitply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
5. These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
6. Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
7. The following loads are used for t_{PXZ}:

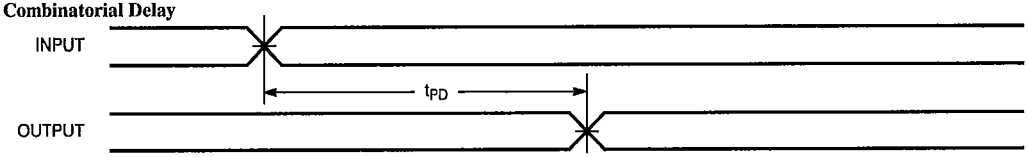


High Drive Buffer

Parameter	Description	# High Drives Wired Together	Propagation Delays[4] with Fanout of 12	24	48	72	96	Unit
t_{IN}	High Drive Input Delay	1	7.9	11.2				ns
		2		8.0	9.7			ns
		3			8.6	10.4	11.8	ns
		4				9.4	10.8	ns
t_{INI}	High Drive Input, Inverting Delay	1	7.5	10.8				ns
		2		7.5	9.3			ns
		3			8.2	10.0	11.8	ns
		4				9.0	10.8	ns

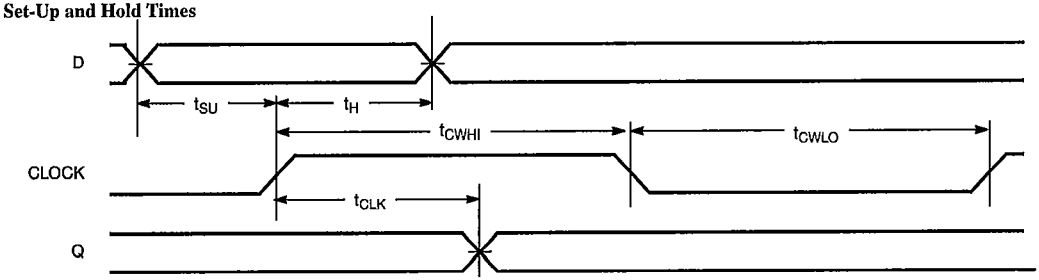
Switching Waveforms

Combinatorial Delay



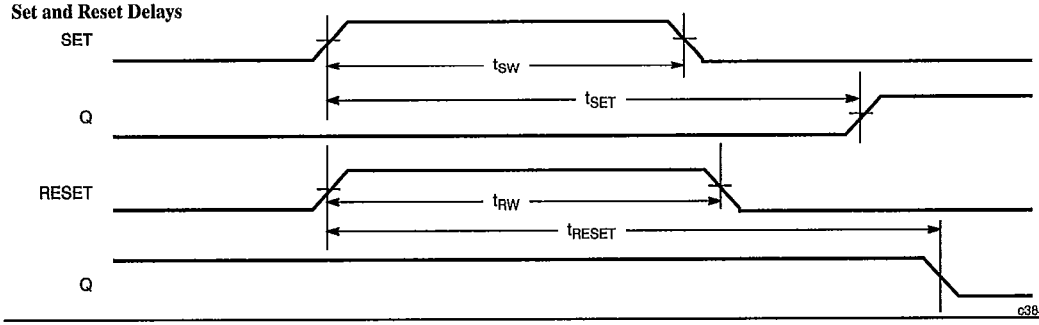
c383-2

Set-Up and Hold Times



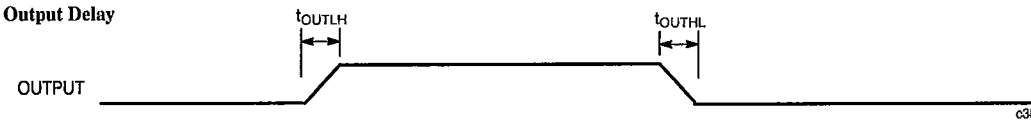
c383-3

Set and Reset Delays



c383-4

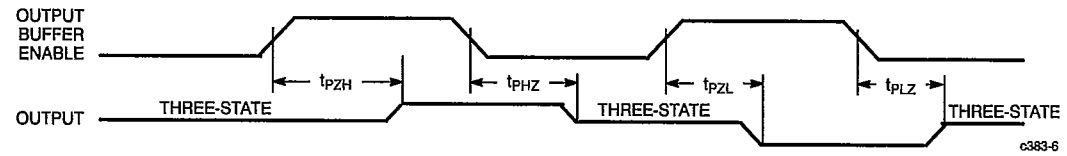
Output Delay



c383-5

Switching Waveforms (continued)

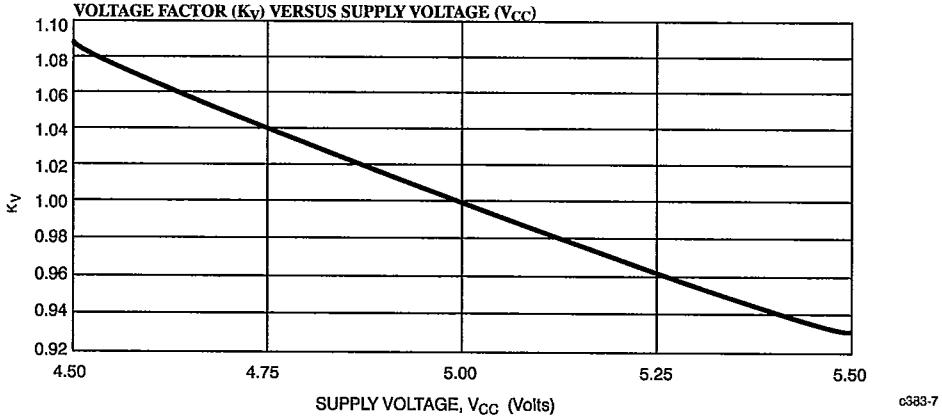
Three-State Delay

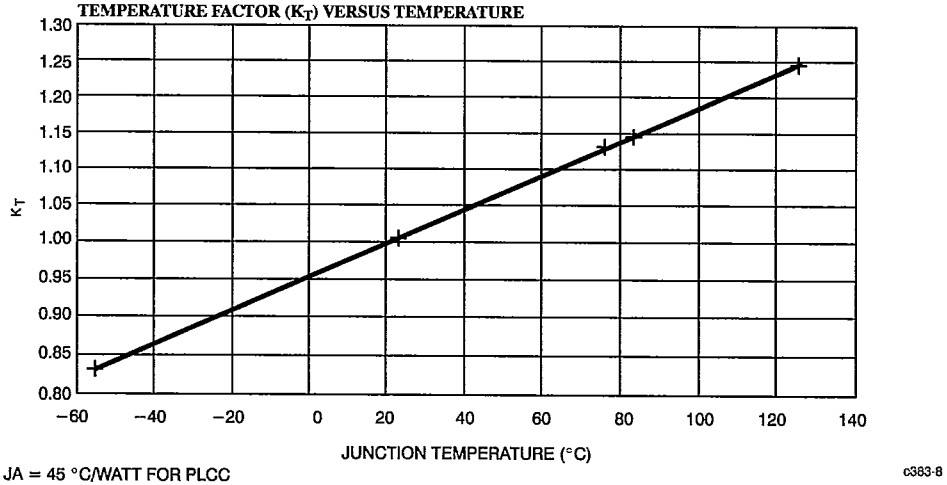


Typical AC Characteristics

Propagation delays depend on routing, fan-out, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. *Warp3* incorporates datasheet AC Characteristics into the design database for pre-place-and-route simulations. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.

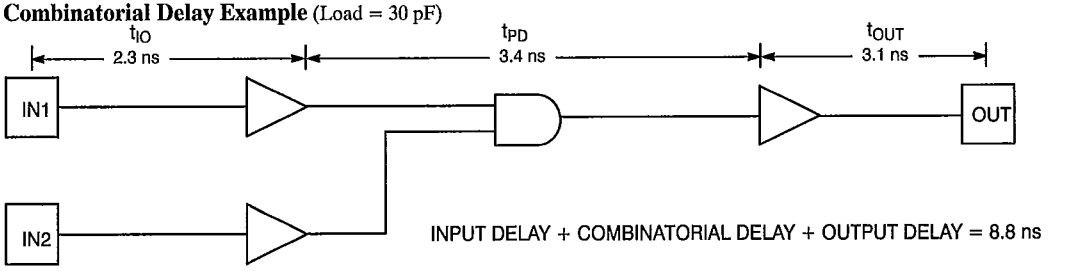
4 PLDs



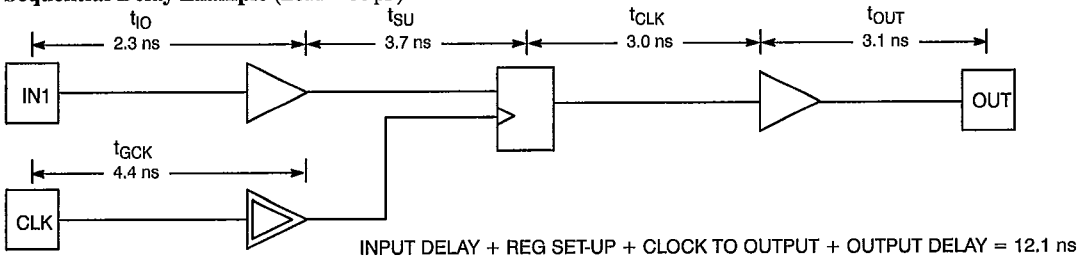


*THETA JA = 45 °C/WATT FOR PLCC

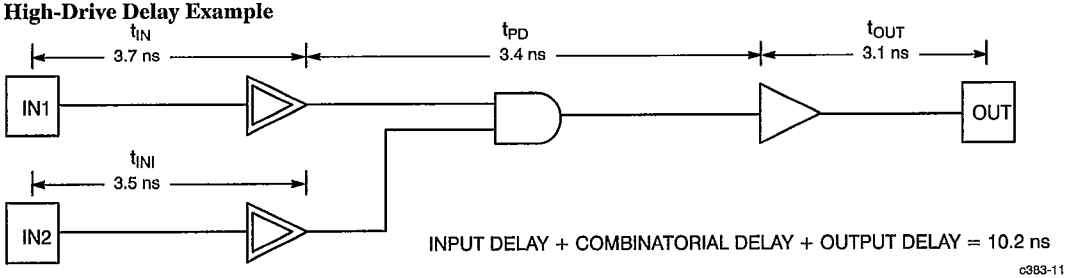
Combinatorial Delay Example (Load = 30 pF)



Sequential Delay Example (Load = 30 pF)



High-Drive Delay Example



Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C383–2GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7C383–2JC	J81	68-Lead Plastic Leaded Chip Carrier	
1	CY7C383–1GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7C383–1JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C383–1GI	G68	68-Pin Grid Array (Cavity Down)	Industrial
	CY7C383–1JI	J81	68-Lead Plastic Leaded Chip Carrier	
0	CY7C383–0GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7C383–0JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C383–0GI	G68	68-Pin Grid Array (Cavity Down)	Industrial
	CY7C383–0JI	J81	68-Lead Plastic Leaded Chip Carrier	

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C384–2GC	G84	84-Pin Grid Array (Cavity Up)	Commercial
	CY7C384–2JC	J83	84-Lead Plastic Leaded Chip Carrier	
1	CY7C384–1GC	G84	84-Pin Grid Array (Cavity Up)	Commercial
	CY7C384–1JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C384–1GI	G84	84-Pin Grid Array (Cavity Up)	Industrial
	CY7C384–1JI	J83	84-Lead Plastic Leaded Chip Carrier	
0	CY7C384–0GC	G84	84-Pin Grid Array (Cavity Up)	Commercial
	CY7C384–0JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C384–0GI	G84	84-Pin Grid Array (Cavity Up)	Industrial
	CY7C384–0JI	J83	84-Lead Plastic Leaded Chip Carrier	

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Document #: 38–00208–A

CYPRESS SEMICONDUCTOR

PLCC and CLCC Packaging for High-Speed Parts

The semiconductor industry is constantly searching for package options that enhance the capabilities of high-performance devices. For fast device performance with minimal ground bounce, electrical characteristics must include low inductance and capacitance from external pin to die bond-wire pad. A package should also furnish good thermal characteristics for reliability over extended temperature ranges.

Other major properties sought after are low cost, as well as standardized outline/pin configurations for compatibility, ease of manufacturing, and handling throughput. The package must also work with surface mount technology and have a small footprint to save board space.

The package that best meets all these requirements is the PLCC (plastic leaded chip carrier). In the past, utilization of PLCCs was not practical for high-power, bipolar devices. However, the advent of low-power bipolar and BiCMOS ECL-compatible SRAMs and PLDs now provides the opportunity for high-volume usage. As manufacturers switch from bipolar to BiCMOS, the lower power dissipation of high-density ECL SRAMs and complex PLDs promise to give PLCC packages a bright future. For military applications and extended temperature environments or for devices with higher power dissipation, you can substitute the CLCC (ceramic leaded chip carrier).

The PLCC has many desirable qualities:

- Suitable for surface mounting with J-type leads
- Small footprint to save board space
- Low inductance and capacitance for high speed with little ground-bounce
- Good thermal characteristics for reliability over temperature range
- Ease of manufacturing and handling for production throughput
- Low cost compared to CERDIP, flatpack, LCC
- Standard package outline and pin-configuration compatibility

The PLCC's J-type surface-mount leads have the advantage over gull-wing leads, which are susceptible to fatigue. J leads also enhance handling ease in test and burn-in fixtures. The PLCC's 1-pF capacitance compares favorably with the 3 and 6 pF for plastic DIPs and CERDIPs, and inductance is equally impressive: 2 nH versus 6 and 11 nH for plastic DIP and CERDIP. Unlike flatpacks, PLCCs are available in standard tooling. PLCCs come in a variety of pin configurations, from 18 to over 200 pins, versus a maximum of 40 pins for plastic DIPs.

The Ceramic Leaded Chip Carrier

For high-temperature environments and high-power devices, you can make use of the ceramic leaded chip carrier (CLCC, Y package), which can also be surface mounted. The Y package has the same footprint and J leads as the PLCC (*Figure 1*) and works well for the faster PLDs and SRAMs.

If you do not know system temperature in the early stages of a design, you can substitute the Y package for the PLCC and vice versa, so long as the device's die junction temperature does not exceed 150°C. The Y package is slightly more expensive than the PLCC, but with a thermal resistance from junction to ambient (Θ_{JA}) of 35°C/W at 500 LFPM, the Y package can dissipate heat more efficiently.

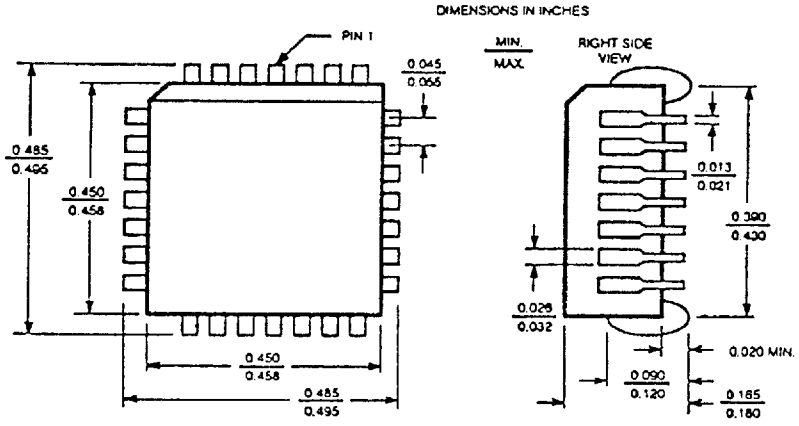
Reliability

Cypress's bipolar and BiCMOS products in PLCC and CLCC packages go through extensive burn-in and testing at elevated temperature to guarantee package integrity. Cypress strongly recommends 500-LFPM system forced air flow but guarantees reliability in systems with or without the flow if the ambient air does not cause the junction temperature (T_J) to exceed 150°C.

The PLCC's Θ_{JA} is approximately 45°C/W. The SRAMs have power dissipation that ranges from 780 mW max for the CY100E422L-5 up to 1097 mW max for the CY10E474L-5. This dissipation results in junction temperature rises from 35 to 49°C. The 16P4-type PLD (CY100E302L-6) has a temperature rise of 39°C, and the

T-90-20

28-Lead Plastic Leaded Chip Carrier J64



28-Pin Ceramic Leaded Chip Carrier Y64

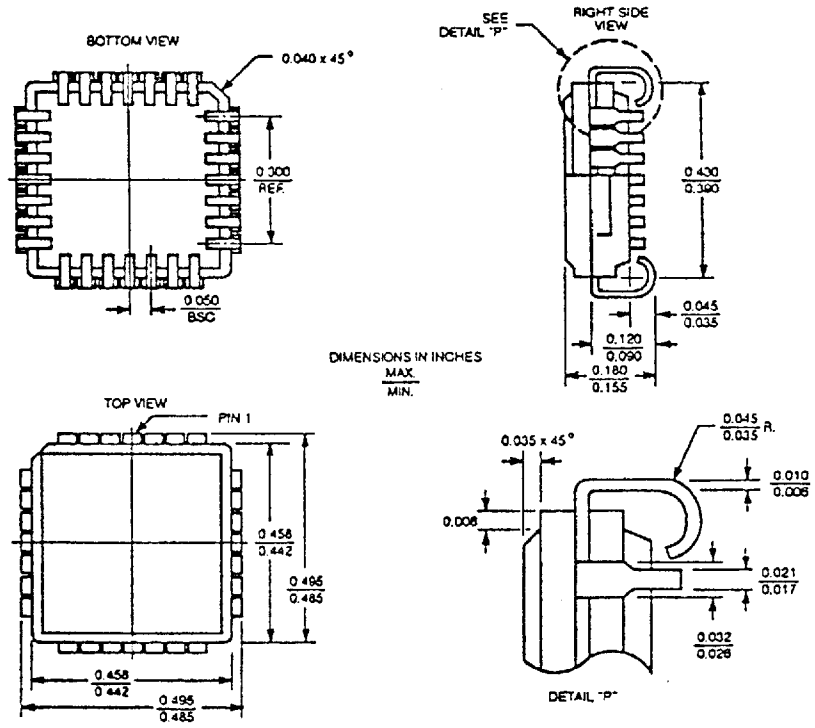


Figure 1. Diagrams of 28-Lead Chip Carriers

16P8-type PLD (CY10E301L-6) has a temperature rise of 47°C. The CLCC package's Θ_{JA} equals 35°C/W for temperature rises of up to 55°C (CY10E474-3).

Finding Chip-Level Junction Temperature

The following relationship determines chip-level junction temperature for the PLCC package:

$T_J = \Delta T + T_A$

where

$\Delta T = P_D \times \Theta_{JA}$

and

$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$

To calculate worst case junction temperature (T_J) use maximum supply V_{EE} and I_{EE} for power dissipation and maximum T_A for the temperature range of interest. For the 10K/10KH CY10E301L in a PLCC, for example, device I_{EE} = 170 mA max and V_{EE} = 5.46V max for P_D = 928 mW. Add 15 mW per output for a total output P_D = 120 mW. Therefore, the total P_D = 1048 mW.

For a PLCC, Θ_{JA} = 45°C/W at 500 LFPM, and Θ_{JA} = 64°C/W for still air.

For a CLCC, Θ_{JA} = 35°C/W at 500 LFPM, and Θ_{JA} = 54°C/W for still air.

Because

T_J = total $P_D \times \Theta_{JA} + T_A$

and

T_A = 75°C worst-case commercial temperature range, for the PLCC:

$T_J = (1.048\ W)(45°C/W) + 75°C = 122°C$ at 500 LFPM

$T_J = (1.048\ W)(64°C/W) + 75°C = 142°C$ in still air

This calculation is for absolute worst-case data sheet conditions. The burn-in temperature used by Cypress (T_J) is much higher than the device will ever see in a system. Note that *most systems will not run at worst case due to guard-banding*. For this reason, use V_{EENOM} = 5.2V or 4.5V and $I_{EENOM} = (I_{EEMAX})(85\%)$ for nominal-condition calculations.

Real-World Values

Obviously, most systems do not operate at the worst-case conditions. Therefore, *Figures 2* through *5* show graphs over different operating conditions to determine failures in time (FITs) and mean time between failure (MTBF) for a typical system or in a worst-case scenario.

The graphs are based on a linear method of interpreting the failures observed at burn-in and indicate the long-term reliability of Cypress devices. You can use the graphs to determine MTBF and FITs for any Cypress device in any package after calculating the appropriate ΔT.

The X-axis on the graphs indicates junction temperature. These values are determined by adding the ΔT to ambient temperature, as described earlier. As an example, *Figures 2* and *3* note the following critical points for a CY10E301L ECL PLD under three different operating conditions:

- Point A — 10K/10KH typical data sheet conditions: 25°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 64°C, FITs = 7, MTBF = 18,000 yrs.
- Point B — 10K/10KH typical operating conditions: 55°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 94°C, FITs = 45, MTBF = 2800 yrs.
- Point C — 10K/KH absolute worst-case conditions: 75°C ambient, 5.46 V max and 170 mA max, 50Ω loads, 500 LFPM air flow, T_J = 122°C, FITs = 225, MTBF = 525 yrs.

The activation energy used for the MTBF and FITs information is 0.7 eV. This is an average number for die-surface-related defects, such as metal and oxide pinholes, etc., but is very conservative for silicon defects or mechanical interfaces to packages. The number is usually 1.0 eV. A small change here results in a significant change in MTBF or FITs. A change to 0.8 eV equates to a 33% reduction in FITs rate or a 50% increase in MTBF.

The Packages of Choice

The PLCC and CLCC are accepted as the packages of choice by many manufacturers of high-speed devices. Motorola Semiconductor uses the PLCC as the only package for the company's very high speed ECL$_{INPS}$ ECL logic family, which stands for "ECL in picoseconds" and is pronounced "eclipse." This family has set-up times and propagation delays in the sub-nanosecond range, with power dissipation of over 1W. Fully compatible with Cypress SRAMs and PLDs, the ECL$_{INPS}$ family includes many 10K, 10KH, and 100K standard logic gates, building blocks, and transceivers.

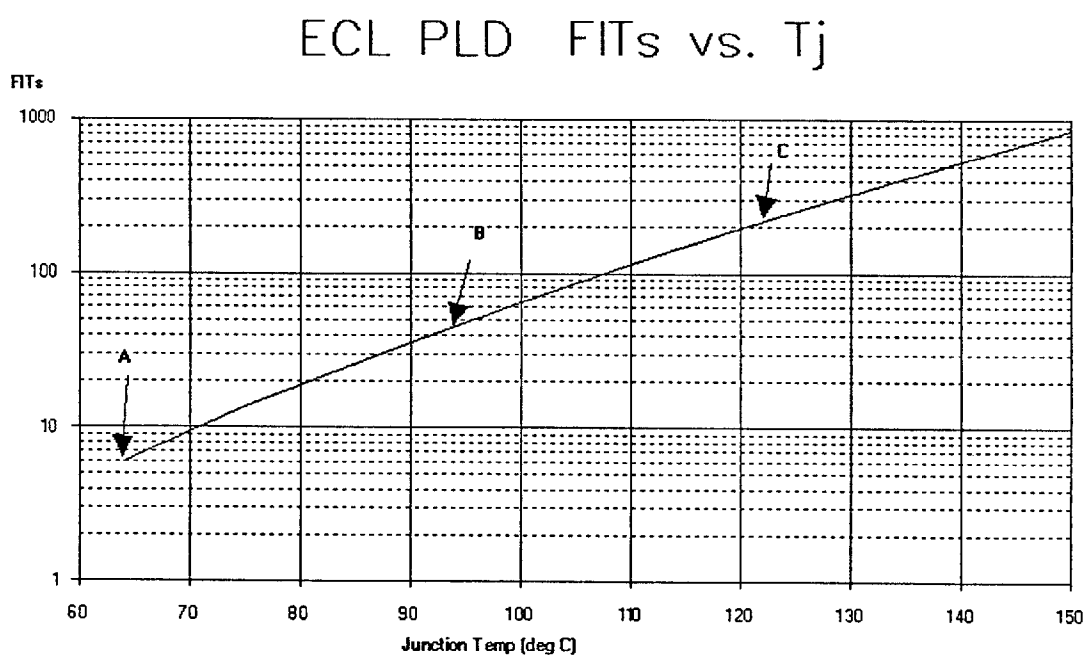


Figure 2. Failures in Time vs Junction Temperature

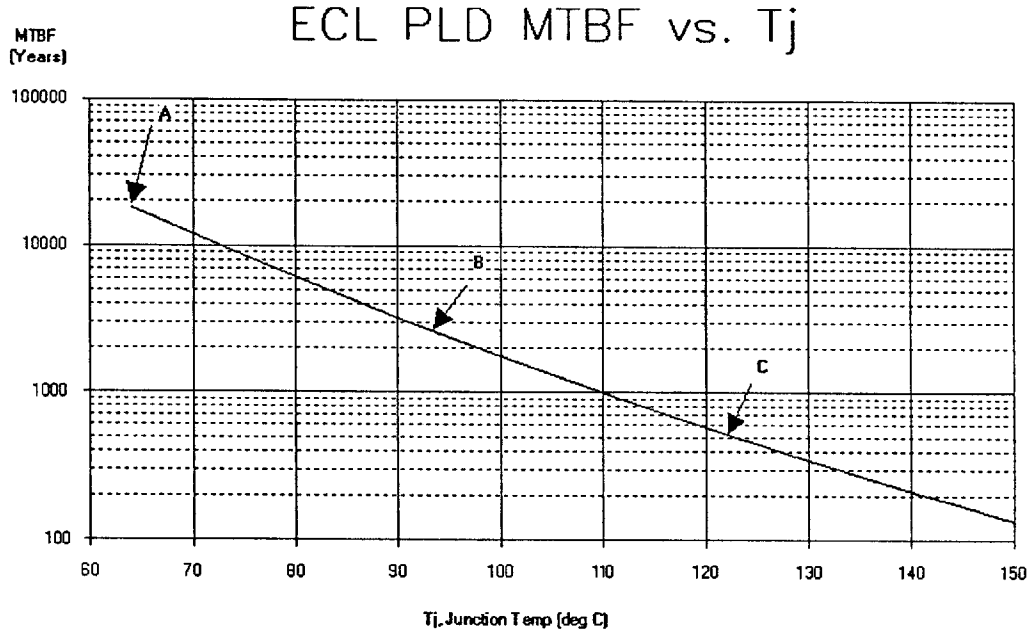


Figure 3. Mean Time Between Failures vs Junction Temp.

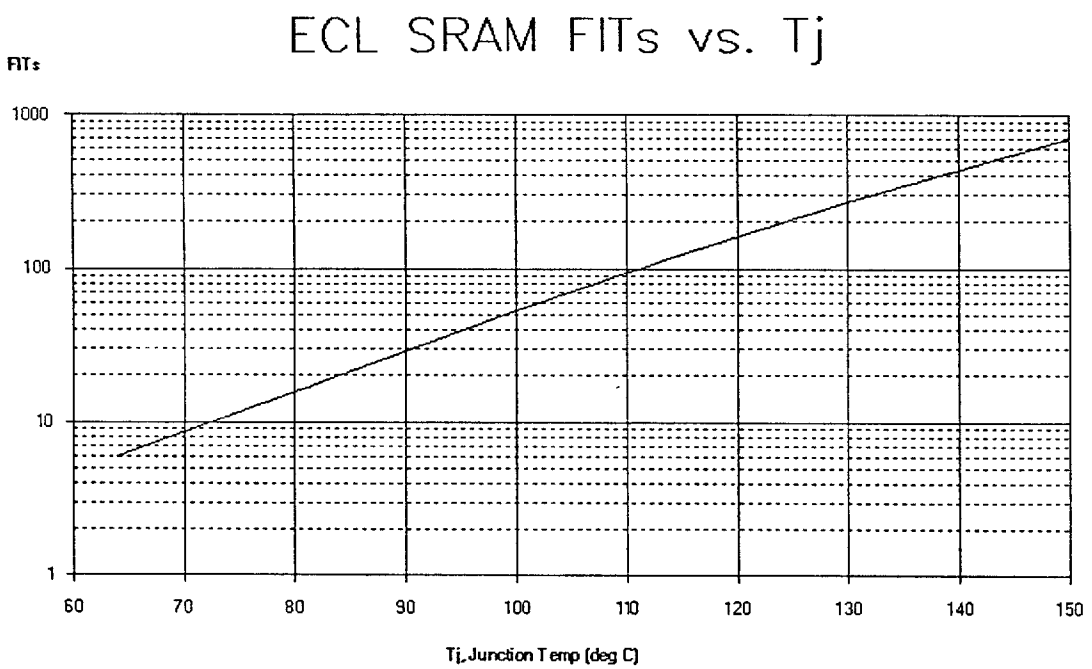


Figure 4. Failures in Time vs Junction Temperature

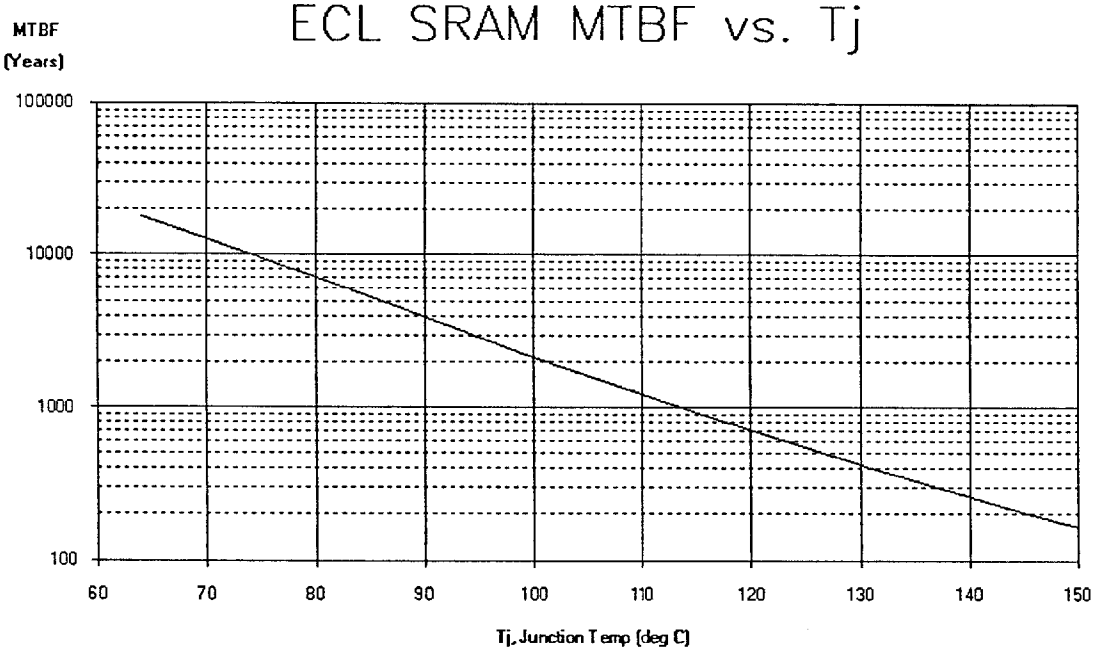


Figure 5. Mean Time Between Failure vs Junction Temp.