

SONY CXK58257ATM/AYM -70LLX/85LLX/10LLX/12LLX

32768-word × 8-bit High Speed CMOS Static RAM

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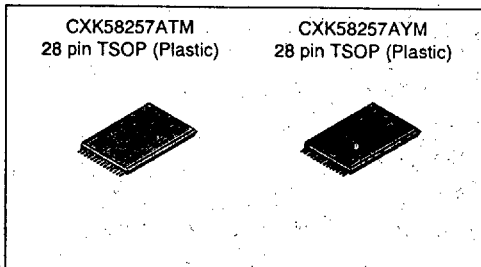
Description

CXK58257ATM/AYM is a 256K bits, 32,768 words by 8 bits, CMOS static RAM.

It is suitable for portable and battery back-up systems which require extremely small package and low stand-by current.

Features

- Extended operation temperature range: -25 to +85 °C
- Thin small-outline package:
 - CXK58257ATM: 8mm × 13.4mm 28 pin TSOP
 - CXK58257AYM: 8mm × 13.4mm 28 pin TSOP (Mirror image pinout)
- Low stand-by current:
 - 10 μA (Max.) @V_{cc}=5.5V, T_a=-25 to +85 °C
- Low voltage data retention: 2.0V (Min.)
- Fast access time: (Access time)
 - CXK58257ATM/AYM-70LLX 70ns (Max.)
 - CXK58257ATM/AYM-85LLX 85ns (Max.)
 - CXK58257ATM/AYM-10LLX 100ns (Max.)
 - CXK58257ATM/AYM-12LLX 120ns (Max.)
- Single +5V Supply: 5V ± 10%



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
V _{cc}	+5V power supply
GND	Ground

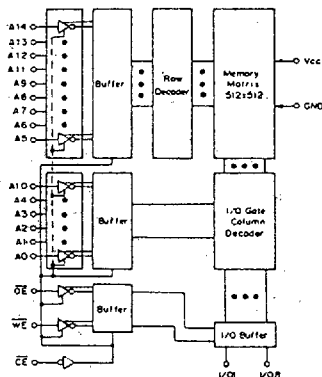
Function

32768-word × 8-bit static RAM

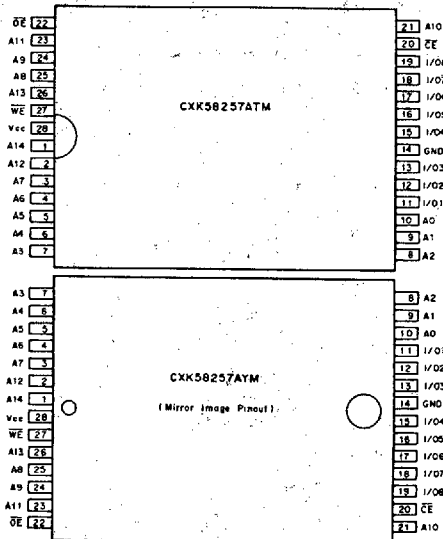
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



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Absolute Maximum Ratings

(Ta=25°C, GND=0V)

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Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	-25 to +85	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	235 • 10	°C • sec

* V_{IN}, V_{I/O}=-3.0V Min. for pulse width less than 50ns.

Truth Table

CE	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	×	×	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Not selected	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	×	L	Write	Data in	I _{CC1} , I _{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta=-25 to +85°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

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Electrical Characteristics

• DC and operating characteristics (Vcc=5V ± 10%, GND=0V, Ta=-25 to +85 °C)

Item	Symbol	Test conditions	-70LLX/85LLX/10LLX/12LLX			Unit	
			Min.	Typ.*	Max.		
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	-0.5	—	0.5	μA	
Output leakage current	I _{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ V _{I/O} =GND to V _{CC}	-0.5	—	0.5	μA	
Operating power supply current	I _{CC1}	$\overline{CE}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	—	3	10	mA	
		$\overline{CE} \leq 0.2V$ V _{IN} $\leq 0.2V$ or $\geq V_{CC}-0.2V$	—	1	5		
Average operating current	I _{CC2}	Cycle=Min, Duty=100% I _{OUT} =0mA	70LLX	—	30	60	mA
			85LLX	—	25	60	
			10LLX	—	23	60	
			12LLX	—	20	60	
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC}-0.2V$	-25 to +85 °C	—	—	10	μA
			-25 to +70 °C	—	—	5	
			-25 to +40 °C	—	—	1	
			+25 °C	—	0.2	0.5	
	I _{SB2}	$\overline{CE}=V_{IH}$	—	0.4	2	mA	
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	—	—	V	
Output low voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	V	

* Vcc=5V, Ta=25 °C

I/O Capacitance

(Ta=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

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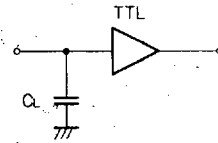
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AC Characteristics

● AC test conditions

(V_{CC}=5V ± 10%, T_a=-25 to +85°C)

Item	Conditions	
Input pulse high level	V _{IH} =2.4V	
Input pulse low level	V _{IL} =0.6V	
Input rise time	t _r =5ns	
Input fall time	t _f =5ns	
Input and output reference level	1.5V	
Output load conditions	85LLX/10LLX/12LLX	C _L *=100pF, 1TTL
	70LLX	C _L *=30pF, 1TTL

* C_L includes scope and jig capacitances.

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• Read cycle

Item	Symbol	-70LLX		-85LLX		-10LLX		-12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	trc	70	—	85	—	100	—	120	—	ns
Address access time	tAA	—	70	—	85	—	100	—	120	ns
Chip enable access time	tco	—	70	—	85	—	100	—	120	ns
Output enable to output valid	toE	—	35	—	45	—	50	—	60	ns
Output hold from address change	toH	5	—	10	—	10	—	10	—	ns
Chip enable to output in low Z (\overline{CE})	tlz	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	tolz	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z (\overline{CE})	thz*	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z (\overline{OE})	tohz*	0	30	0	30	0	30	0	30	ns

* thz and tohz are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write cycle

Item	Symbol	-70LLX		-85LLX		-10LLX		-12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	twc	70	—	85	—	100	—	120	—	ns
Address valid to end of write	taw	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	tcw	65	—	75	—	80	—	100	—	ns
Data to write time overlap	tdw	30	—	30	—	35	—	40	—	ns
Data hold from write time	tdH	0	—	0	—	0	—	0	—	ns
Write pulse width	tWP	50	—	50	—	60	—	70	—	ns
Address setup time	tas	0	—	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	tWR	5	—	5	—	5	—	5	—	ns
Write recovery time (\overline{CE})	tWR1	0	—	0	—	0	—	0	—	ns
Output active from end of write	tow	10	—	10	—	10	—	10	—	ns
Write to output in high Z	twhz*	0	25	0	25	0	25	0	25	ns

* twhz is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

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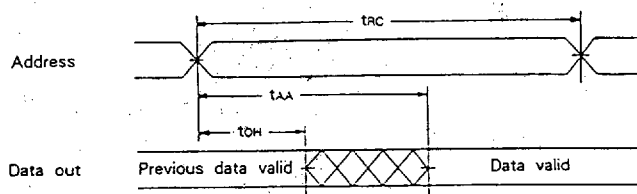
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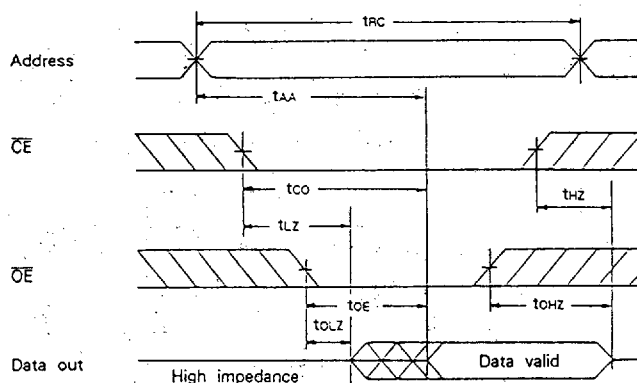
Timing Waveform

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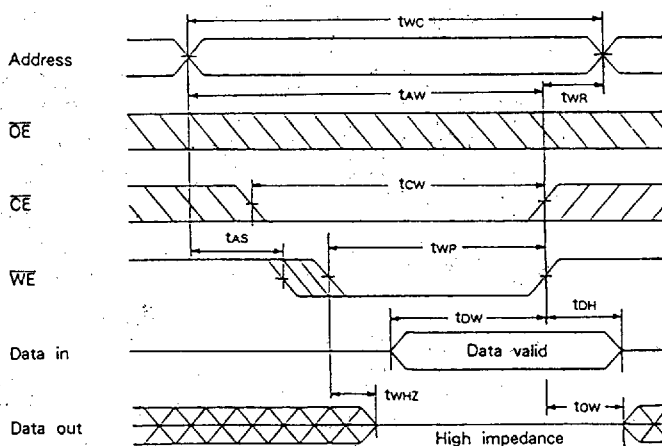
- Read cycle (1) : $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



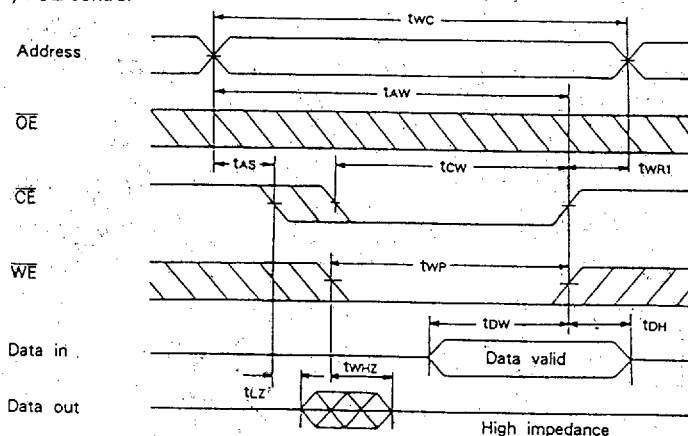
- Read cycle (2) : $\overline{WE}=V_{IH}$



- Write cycle (1) : \overline{WE} control



• Write cycle (2) : \overline{CE} control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

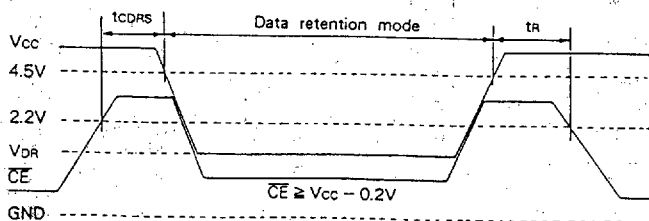
($T_a = -25$ to $+85^\circ\text{C}$)

Item	Symbol	Test conditions	-70LLX/85LLX/10LLX/12LLX			Unit	
			Min.	Typ.	Max.		
Data retention voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	—	5.5	V	
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V$ $\overline{CE} \geq 2.8V$	-25 to $+85^\circ\text{C}$	—	—	6	μA
			-25 to $+70^\circ\text{C}$	—	—	3	
			-25 to $+40^\circ\text{C}$	—	—	0.6	
			$+25^\circ\text{C}$	—	0.1	0.3	
	I_{CCDR2}	$V_{CC} = 2.0$ to $5.5V$ $\overline{CE} \geq V_{CC} - 0.2V$	—	0.2**	10	μA	
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns	
Recovery time	t_R		t_{RC}^*	—	—	ns	

* t_{RC} : Read cycle time

** $V_{CC} = 5V, T_a = 25^\circ\text{C}$

Data Retention Waveform

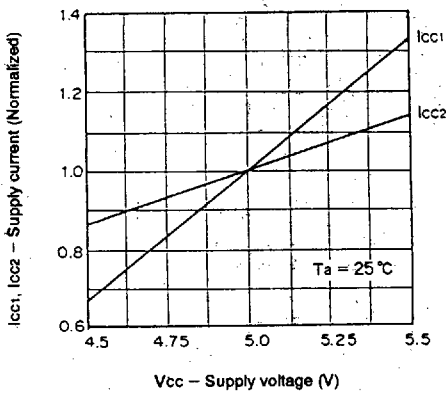


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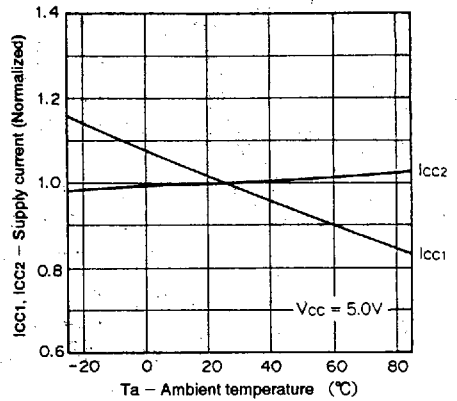
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Example of Representative Characteristics

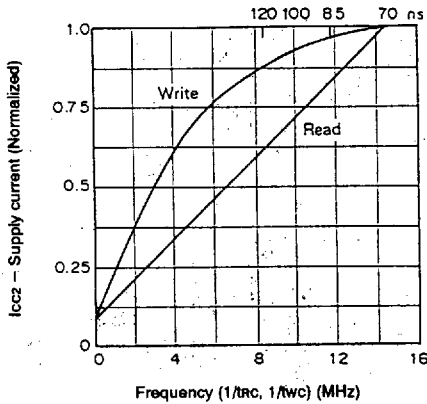
Supply current vs. Supply voltage



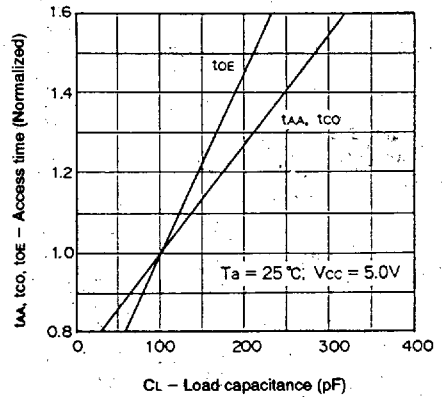
Supply current vs. Ambient temperature



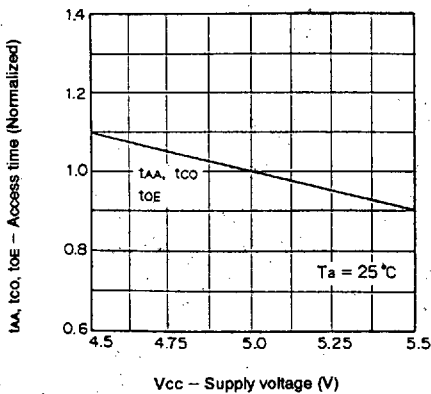
Supply current vs. Frequency



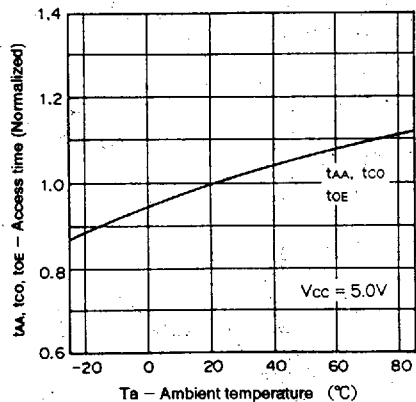
Access time vs. Load capacitance



Access time vs. Supply voltage

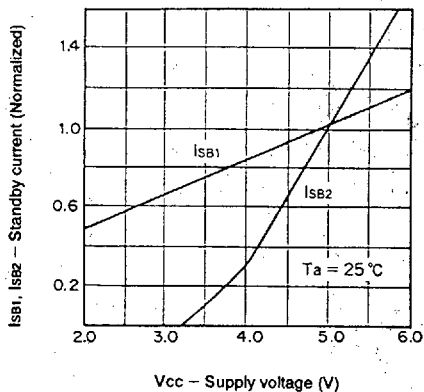


Access time vs. Ambient temperature

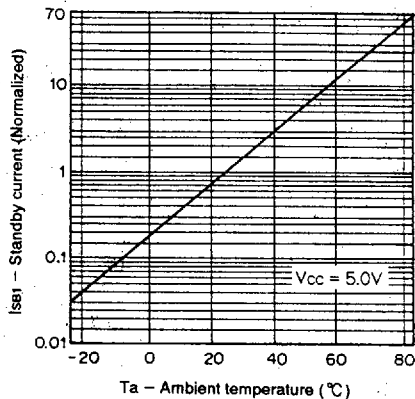


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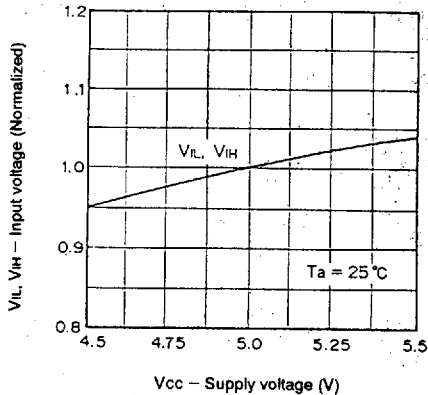
Standby current vs. Supply voltage



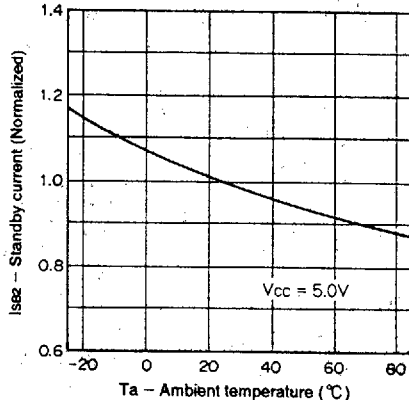
Standby current vs. Ambient temperature



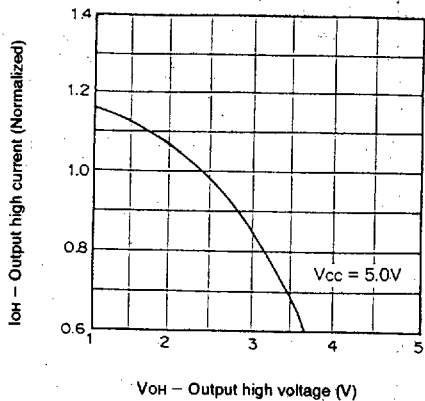
Input voltage level vs. Supply voltage



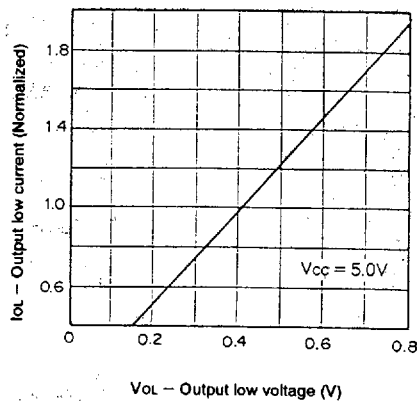
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



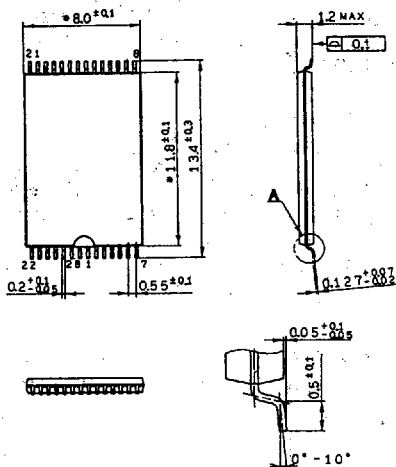
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Package Outline Unit: mm

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CXK58257ATM

28pin TSOP (Plastic)



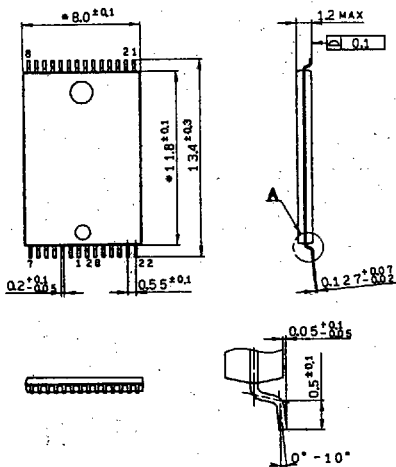
Detailed diagram of A

Note) Dimensions marked with * do not include resin residue.

SONY NAME	TSOP-28P-L01
EIAJ NAME	TSOPQ28-P-0000-A
JEDEC CODE	

CXK58257AYM

28pin TSOP (Plastic)



Detailed diagram of A

Note) Dimensions marked with * do not include resin residue.

SONY NAME	TSOP-28P-L01R
EIAJ NAME	TSOPQ28-P-0000-B
JEDEC CODE	