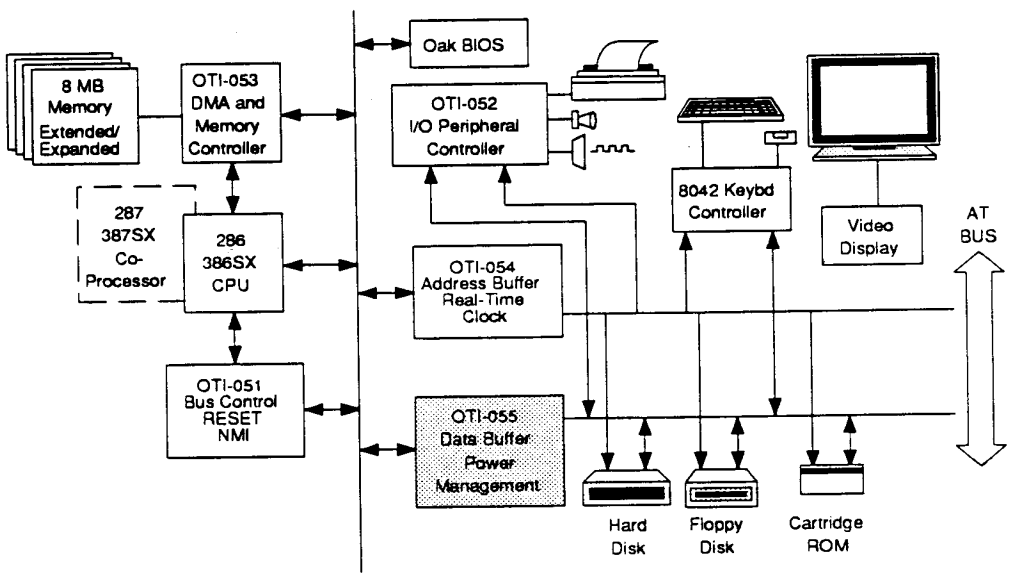
1.0 INTRODUCTION TO OTI-055 DATA BUFFER and POWER MANAGER

OTI-055 contains the data buffers for IBM AT or Model 30 - 286 compatible systems and replaces all the TTL data drivers that are normally required on the system board.

In addition to the data buffers on the chip, the OTI-055 also serves as a power manager in battery-powered systems. The OTI-055 has 16 general purpose bidirectional control/status lines available to the system manufacturer to control power distribution to various peripherals in the system. Besides the 16 signals, OTI-055 also has an internal timer/counter that allows the user to automatically turn on power to the whole system.

System Block Diagram



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2.0 PIN-OUT ASSIGNMENT

Table 1. OTI-055 Pin Description

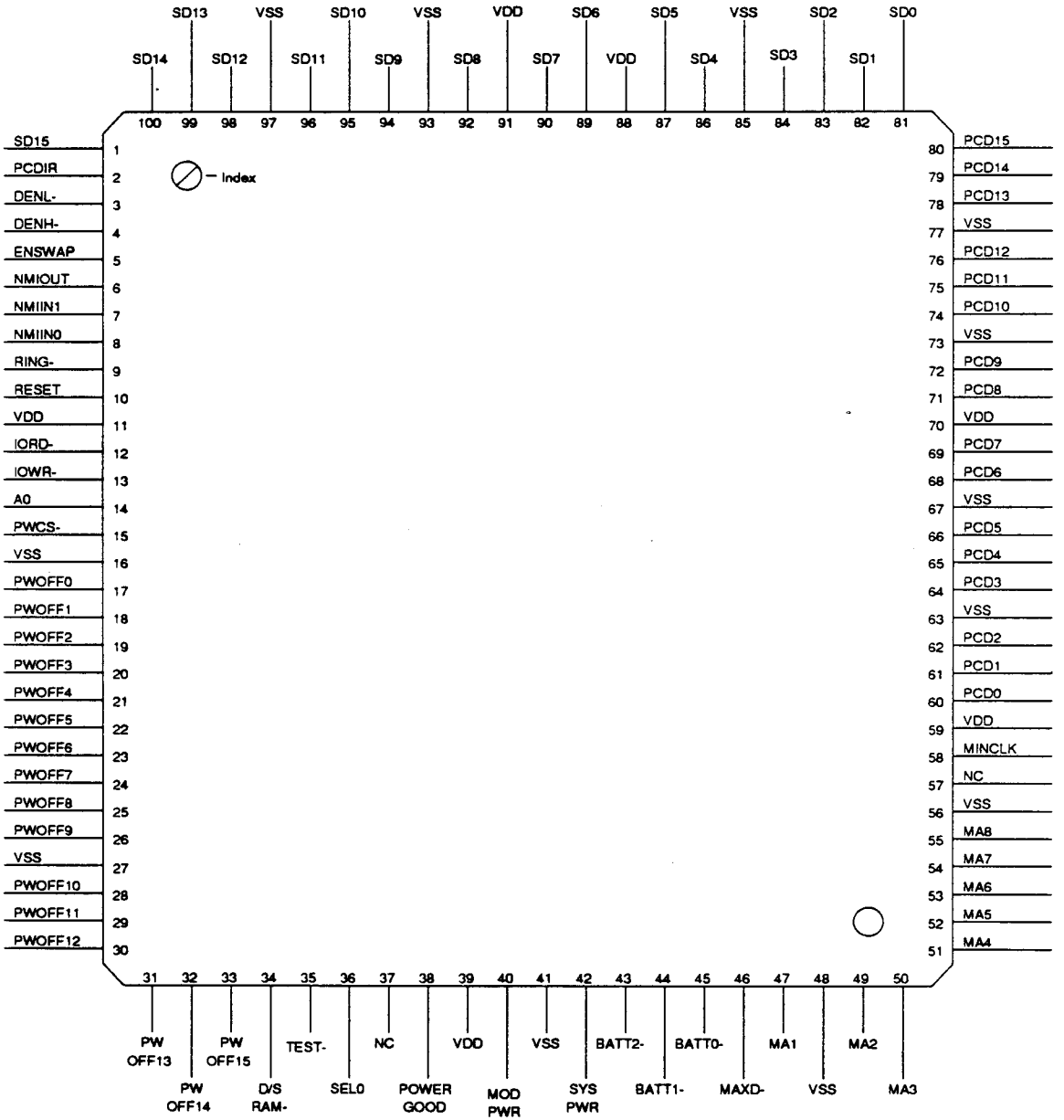
SYMBOL	PIN #	TYPE	NAME and FUNCTION
PWCS-	15	I	POWER MANAGEMENT CHIP SELECT: is an active low input used to select the internal registers of the chip.
A0	14	I	ADDRESS LINE 0: is the latched version of address 0. A0 together with PWCS- is used to program the power management chip OTI-055. When A0 is 0, the index register is accessed; when A0 is 1, the data register is accessed.
PCD(0-15)	60-62,64-66,68,69, 71,72,74-76,78-80	I/O	PC DATA BUS (0-15): is the PC data bus. There are 2 sets of data transceivers that are connected internally i.e. between SD(0-7) and PCD(0-7) and between SD(8-15) and PCD(8-15) to form a 16 bit PC data bus: PCD(0-15).
SD(0-15)	81-84,86,87,89,90, 92,94-96,98-100,1	I/O	SYSTEM DATA BUS (0-15): is the system data bus. There are 2 sets of data transceivers that are connected internally i.e. between SD(0-7) and PCD(0-7) and between SD(8- 15) and PCD(8-15) to form a 16 bit PC data bus: PCD(0-15).
MA8 - MA1	55-49,47	I/O	MEMORY ADDRESS BUS: bi-directional lines between the memory address lines and I/O chanell bus. OTI-053 multiplexes the MA lines with the PC data bus.
MAXD-	46	I	MA TO DATA BUS CONTROL: active low signal from OTI-054 enabling the data path between the MA lines and PC data bus.
SEL0	36	I	SELECT 0: is an active high signal from OTI-051 indicating an I/O cycle with address A15-A10 all zeroes.
DENL-	3	I	DATA LOW ENABLE: is an active low control signal to enable/disable the internal data transceiver between SD(0-7) and PCD(0-7).
DENH-	4	I	DATA HIGH ENABLE: is an active low control signal to enable/disable the internal data transceiver between SD(8-15) and PCD(8-15).
PCDIR	2	I	PC DATA DIRECTION: is the direction control signal for the data transceivers between PCD(0-15) and SD(0-15): PCDIR = 0 ==>SD follows PCD bus. =1 ==>PCD follows SD bus.
ENSWAP	5	I	ENABLE DATA SWAP: is an input signal used for enabling the data buffer for data swap.
IORD-	12	I	I/O READ COMMAND: active low command to instruct the I/O device to drive its data onto the data bus.
IOWR-	13	I	I/O WRITE COMMAND: active low command to instruct the I/O device to read the data present on the data bus.
RESET	10	I	RESET: is an active high signal synchronized to the system clock to reset the system.
NMIOUT	6	O	NMI: active high output to the CPU for non-maskable interrupt.
NMIIN0	8	I	NMI input 0: active high input ORed internally with other NMI generating sources to generate NMIOUT to the CPU.
NMIIN1	7	I	NMI input 1: active high input ORed internally with other NMI generating sources to generate NMIOUT to the CPU.

Table 1. OTI-055 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
D/SRAM-	34	I	DRAM OR SRAM SELECT: is an input signal to tell the chip the memory type used in the system: D/SRAM- =low ==>pseudo-static RAM D/SRAM- =high==>Dynamic RAM
TEST-	35	I	INTERNAL TEST: active low input signal to invoke the internal test circuitry.
			***** POWER MANAGEMENT*****
MINCLK	58	I	MINUTE CLOCK: input signal from the minute count from the Real Time Clock inside OTI-054.
RING-	9	I	RING SIGNAL: active low input indicating that there is ring signal detected from the modem.
POWERGOOD	38	I	POWER GOOD SIGNAL: active high signal indicating the system power is in the desired range +/- 5%.
BATT0-	45	I	BATTERY LEVEL 0: active low signal to indicate that battery low level 0 is reached. NMI might be generated to invoke the power saving routine.
BATT1-	44	I	BATTERY LEVEL 1: active low signal to indicate that battery low level 1 is reached. NMI might be generated to invoke the power saving routine.
BATT2-	43	I	BATTERY LEVEL 2: active low signal to indicate that battery level is getting low, and it should be recharged. This is just a warning signal.
SYSPWR	42	O	SYSTEM POWER: active high output controlling the regulator to turn on the system power.
MODPWR	40	O	MODEM POWER: active high output controlling the regulator to turn on the power to the modem.
PWOFF0	17	I/O	POWER OFF CONTROL 0: e.g. HARD DISK POWER CONTROL: active low signal to turn off power to hard disk. Output current is 4 mA.
PWOFF1	18	I/O	POWER OFF CONTROL 1: e.g. FLOPPY DISK POWER CONTROL: active low signal to turn off power to the floppy disk controller. Output current is 4 mA.
PWOFF2	19	I/O	POWER OFF CONTROL 2: e.g. DISPLAY POWER CONTROL: active low signal to turn off the display. Output current is 4 mA.
PWOFF3	20	I/O	POWER OFF CONTROL 3: e.g. DISPLAY POWER CONTROL: active low signal to turn off display. Output current is 4 mA.
PWOFF4	21	I/O	POWER OFF CONTROL 4: e.g. TRANSCEIVER POWER CONTROL: active low signal to turn off power to the RS-232 transceivers. Output current is 4 mA.
PWOFF5	22	I/O	POWER OFF CONTROL 5: e.g. CO-PROCESSOR POWER CONTROL: active low signal to turn off the math co-processor. Output current is 4 mA.
PWOFF6	23	I/O	POWER OFF CONTROL 6: general purpose control signal, also programmable to be a status input. Output current is 4 mA.
PWOFF7	24	I/O	POWER OFF CONTROL 7: general purpose control signal, also programmable to be a status input. Output current is 4 mA.
PWOFF8-11	25,26,28,29	I/O	POWER OFF CONTROL 8 - 11: general purpose control signals, also programmable to be status inputs. Output current drive is 4 mA.

Table 1. OTI-055 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
PWOFF12-15	30-33	I/O	POWER OFF CONTROL 12 - 15: general purpose control signals, also programmable to be status inputs. The output drive for these 4 pins are 8 mA each.
NC	37,57		NO CONNECT: 2 pins
VSS	16,27,41,48,56,63, 67,73,77,85,93,97	I	GROUND: 12 pins 0V
VDD	11,39,59,70,88,91	I	POWER: 6 pins 5V



3.0 OTI-055 FUNCTIONAL DESCRIPTION

OTI-055 functions can be categorized as follows:

1. Data Buffers
2. NMI Logic
3. Power Manager

3.1 Data Buffers

OTI-055 integrates all the data buffers necessary for the PC data bus, the CPU data bus and the X-Bus. It also contains the logic for byte swap. All data buffers have a propagation delay of 35ns. The PC data bus loading is designed for 200 pF and 20 mA IOL. The capacitive loading on the system bus is 100 pF.

3.2 NMI Logic

Two external NMI inputs are provided so that the NMI output from OTI-051 can be gated together with another external NMI input to generate an NMI signal to the CPU. Internal NMI logic also allows other internal circuitry to generate NMI to invoke the power management routines. The NMI sources can be programmed through a control port.

3.3 Power Manager

OTI-055 provides system designers with the capability to manage power distribution to the various peripheral devices on the computer system. The key features include automatic power-on, programmable I/O control/status lines and NMI generation logic for invoking software control.

3.3.1 Automatic Power-ON

OTI-055 supports two modes of automatic power on:

- Self-timed Power-On: an internal counter allows the user to program the system to power on automatically in up to 11 days.
- Modem Power-On: internal circuitry to detect the RING signal coming from the modem to turn on the system automatically if the RING count exceeds the value programmed by the user.

3.3.2 Programmable Control/Status Lines

OTI-055 provides 16 programmable bidirectional control/status lines for the system designers. Each of the lines can be programmed to be an input or an output. Four of the outputs have 8 mA IOL current drive, while all the others have an output current drive of 4 mA. These programmable I/O lines allow the system designer to power ON or power OFF different devices on the system as well as monitor the status of the system. Three of the status inputs can be programmed to generate NMI.

Below are the control registers and program definitions for each of the 16 programmable pins:

Pins PWOFF7-0
(program bit 7 for pin PWOFF7,...bit 0 for pin PWOFF0)

Direction Control Register 0
PWRIOL I/O PORT 48(Hex) READ/WRITE

Programmable Value	Definition
0	Input (default)
1	Output

At Power-on Reset, indexed port 48(Hex) reads as 00.

Output Control Register 0
PWROTL I/O PORT Index 49(Hex) READ/WRITE

Programmable Value	Definition
0	output is "0" (default)
1	output is "1"

At Power-on Reset, indexed port 49(Hex) reads as 00.

Input Status Register 0
PWRINL I/O PORT Index 4A(Hex) READ

Programmable Value	Definition
0	input is "0"
1	input is "1"

Pins PWOFF15-8
(program bit 7 for pin PWOFF15,...bit 0 for pin PWOFF8)

Direction Control Register 1
PWRIOH I/O PORT Index 4B(Hex) READ/WRITE

Programmable Value	Definition
0	input (default)
1	output

At Power-on Reset, indexed port 4B(Hex) reads as 00.

Output Control Register 1
PWROTH I/O PORT Index 4C(Hex) READ/WRITE

Programmable Value	Definition
0	output is "0" (default)
1	output is "1"

At Power-on Reset, indexed port 4C(Hex) reads as 00.

Input Status Register 1
PWRINH I/O PORT Index 4D(Hex) READ

Programmable Value	Definition
0	input is "0"
1	input is "1"

4.0 ELECTRICAL CHARACTERISTICS

4.1 A.C. Characteristics

Table 2. A.C. Characteristics of OTI-055

A.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	LOADING CAPACITANCE
t1	PCD,MA from SD		35	ns	CL=200 pF
t2	SD from PCD, MA		35	ns	CL=100 pF
t3	Address Valid Before IOWRN	40		ns	
t4	SEL0 Valid Before IOWRN	40		ns	
t5	WRITE Data SETUP Time	100		ns	
t6	WRITE Data HOLD Time	20		ns	
t7	READ Data Valid from IORDN		100	ns	
t8	READ Data Float from IORDN	5		ns	
t9	POFFx Delay from IOWRN		50	ns	

4.2 D.C. Characteristics

Table 3. D.C. Characteristics of OTI-055

D.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
VOH	Output HIGH Voltage	2.4		V	IOH=400 µA
VOL1	Output LOW Voltage		0.45	V	IOL=24 mA, Note 1
VOL2	Output LOW Voltage		0.45	V	IOL=14 mA, Note 1
VOL3	Output LOW Voltage		0.45	V	IOL= 4 mA, Note 1
VIH	Input HIGH Voltage	2.0	VDD+0.5	V	TTL
VIL	Input LOW Voltage	- 0.5	0.8	V	TTL
ILI	Input Leakage Current	- 10	10	µA	
OLI	Output Leakage Current	- 10	10	µA	
ICC	Operating Supply Current		30	mA	Input=VDD or VSS No Output Load
CI	Input Capacitance		8	pF	
CO	Output Capacitance		8	pF	
CIO	I/O Capacitance		16	pF	

1. Output Current (IOL) Capabilities:

24 mA :	PCD0-15
14 mA :	SD0-15, POFF12-15,MA1-8
4 mA :	NMIOUT, POFF0-11, MODPWR, SYSPWR

5.0 OTI-055 TIMING DIAGRAM

FIGURE 5-1.