

DESCRIPTION

The HY51V17400B is the new generation and fast dynamic RAM organized 4,194,304 x 4-bit. The HY 51V17400B utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY51V17400B to be packaged in standard 24/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of $3.3V \pm 10\%$ tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
- Max. battery back-up 1.8mW (SL-part)
Max. CMOS standby 0.72mW (SL-part)
1.8mW
- Max. TTL standby 3.6mW
- Max. operating

Speed	Power
60	432mW
70	360mW
80	324mW

- Single power supply of $3.3V \pm 10\%$
- TTL compatible inputs and outputs
- Fast access and cycle time

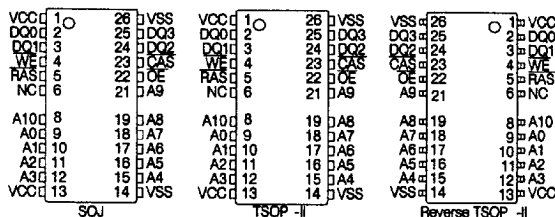
Speed	t _{RAC}	t _{CAC}	t _{PC}
60	60ns	15ns	40ns
70	70ns	18ns	45ns
80	80ns	20ns	50ns

- Fast page mode operation
- Multi-bit test capability
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self refresh capability
- 2048 refresh cycles /256ms (SL-part)
2048 refresh cycles /32ms

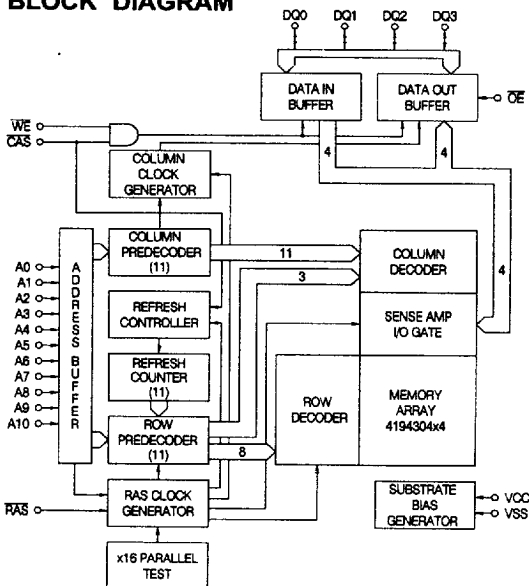
PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0 - A10	Address Input
DQ0 - DQ3	Data Input/Output
Vcc	Power (+3.3V)
Vss	Ground

PIN CONNECTION



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-0.5 to 4.6	V
VCC	Voltage on Vcc Relative to Vss	-0.5 to 4.6	V
Ios	Short Circuit Output Current	20	mA
PD	Power Dissipation	1	W
TSOLDER	Soldering Temperature • Time	260 • 10	°C • sec

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	3.0	3.3	3.6	V
VIH	Input High Voltage	2.0	-	Vcc+0.3	V
VIL	Input Low Voltage	-0.3	-	0.8	V

NOTE: All Voltage are referenced to Vss.

DC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=3.3V±10%, Vss=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	Vss ≤ VIN ≤ Vcc+1.0, All other pins not under test = Vss		-10	10	μA	
ILO	Output Leakage Current (High impedance State)	Vss ≤ VOUT ≤ Vcc RAS & CAS at VIH		-10	10	μA	
ICC1	Vcc Supply Current, Operating	trc = trc (min.)	60 70 80	- - -	120 100 90	mA	1,2,3
ICC2	Vcc Supply Current, TTL Standby	RAS & CAS at VIH (min.), other inputs ≥ Vss		-	1	mA	
ICC3	Vcc Supply Current, RAS-only refresh	trc = trc (min.)	60 70 80	- - -	120 100 90	mA	1,3
ICC4	Vcc Supply Current, Fast Page mode	tPC = tPC (min.)	60 70 80	- - -	80 70 60	mA	1,2,3
ICC5	Vcc Supply Current, CMOS Standby	RAS & CAS ≥ Vcc-0.2V	SL-part	-	0.5 0.2	mA	5
ICC6	Vcc Supply Current, CAS-before- RAS refresh	trc = trc (min.)	60 70 80	- - -	120 100 90	mA	1,3
ICC7	Vcc Supply Current, Battery Back Up (L-part Only)	trc = 125μs, CAS = CBR cycling or 0.2V, WE = Vcc-0.2V, A0-A10 = Vcc-0.2V or 0.2V, DQ0-DQ3 = Vcc-0.2V, 0.2V or open	tRAS ≤ 300ns tRAS ≤ 1μs	- -	300 500	μA	1, 4, 5
ICC8	Vcc Supply Current, Self Refresh (SL-part only)	RAS & CAS ≤ 0.2V, OE & WE & A0-A10=Vcc-0.2V or 0.2V, DQ0-DQ3=Vcc-0.2V, 0.2V or open		-	300	μA	5
VOL	Output Low Voltage	IOL = 2.0mA		-	0.4	V	
VOH	Output High Voltage	IOH = -2.0mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rates.
2. ICC1, ICC3, ICC4 and ICC6 dependent on output loading. Specified values are obtained with the output open.
3. ICC is specified as average current. ICC1, ICC3, ICC6, Address can be changed maximum two times while RAS =VIL. ICC4, Address can be changed maximum once while CAS=VIH.
4. tRAS(max.) =1μs is only6 applied to refresh of battery backup but tRAS(max.) =10μs is applied to normal functional operationsg.
5. ICC5(max.) =0.2mA, ICC7 and ICC8 are applied to SL-part only.

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AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=3.3V ± 10%, Vss=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER		HY51V17400BJT/R/SLJ/SLT/SLR						UNIT	NOTE
				-60		-70		-80			
				MIN	MAX	MIN	MAX	MIN	MAX		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns		
2	tRWC	Read-Modify-Write Cycle Time	160	-	180	-	200	-	ns		
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns		
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	85	-	90	-	100	-	ns		
5	tRAC	Access Time form RAS	-	60	-	70	-	80	ns	4,9,10	
6	tCAC	Access Time from CAS	-	15	-	18	-	20	ns	4,9	
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10	
8	tCPA	Access Time from CAS Precharge	-	35	-	40	-	45	ns	4	
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns		
10	tOFF	Output Buffer Turn-off Delay	0	15	0	18	0	20	ns		
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3	
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns		
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns		
14	tRASP	RAS Pulse Width (Fast Page Mode)	60	200K	70	200K	80	200K	ns		
15	tRSH	RAS Hold Time	15	-	18	-	20	-	ns		
16	tCSH	CAS Hold Time	60	-	70	-	80	-	ns		
17	tCAS	CAS Pulse width	15	10K	18	10K	20	10K	ns		
18	tRCD	RAS to CAS Delay	20	45	20	52	20	60	ns	9	
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10	
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns		
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns		
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns		
23	tRAH	Row Address Hold time	10	-	10	-	12	-	ns		
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns		
25	tCAH	Column Address Hold Time	10	-	10	-	15	-	ns		
26	tAR	Column Address Hold Time from RAS	50	-	50	-	55	-	ns		
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns		
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns		
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6	
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6	
31	tWCH	Write Command Hold Time	10	-	10	-	15	-	ns		
32	tWCR	Write Command Hold Time from RAS	45	-	55	-	60	-	ns		
33	tWP	Write Command Pulse Width	10	-	10	-	15	-	ns		
34	tRWL	Write Command to RAS Lead Time	15	-	18	-	20	-	ns		
35	tCWL	Write Command to CAS Lead Time	15	-	18	-	20	-	ns		
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7	
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	7	
38	tDHR	Data-In Hold Time Referenced to RAS	50	-	50	-	55	-	ns		
39	tREF	Refresh Period (2048)	-	32 256	-	32 256	-	32 256	ms ms	12 11	
40	tWCS	Write Command Set up Time	0	-	0	-	0	-	ns	8	

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AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY51V17400BJ/T/R/SLJ/SLT/SLR						UNIT	NOTE
			-60		-70		-80			
			MIN	MAX	MIN	MAX	MIN	MAX		
41	tCWD	CAS to WE Delay Time	38	-	43	-	45	-	ns	8
42	tRWD	RAS to WE Delay Time	83	-	95	-	105	-	ns	8
43	tAWD	Column Address to WE Delay Time	53	-	60	-	65	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
48	tROH	RAS Hold Time Referenced to OE	0	-	0	-	0	-	ns	
49	tOEA	OE Access Time	-	15	-	18	-	20	ns	
50	tOED	OE to Data Delay	15	-	15	-	15	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time	0	13	0	15	0	15	ns	
52	tOEH	OE Command Hold Time	10	-	10	-	10	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	35	-	40	-	45	-	ns	
54	tRHCP	RAS Hold Time from CAS Precharge	35	-	40	-	45	-	ns	8
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
58	tWTH	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
59	tRASS	RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	μs	
60	tRPS	RAS Precharge Time (Self Refresh)	90	-	110	-	130	-	ns	
61	tCHS	CAS Hold Time (Self Refresh)	- 50	-	- 50	-	- 50	-	ns	

AC CHARACTERISTICS IN TEST MODE

NOTE 13

#	SYMBOL	PARAMETER	HY51V17400BJ/T/R/SLJ/SLT/SLR						UNIT	NOTE
			- 60		- 70		- 80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	105	-	135	-	155	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	165	-	185	-	205	-	ns	
3	tPC	Fast Page Mode Cycle Time	45	-	50	-	55	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	90	-	95	-	105	-	ns	
5	tRAC	Access Time from RAS	-	65	-	75	-	85	ns	4,9,10
6	tCAC	Access Time from CAS	-	20	-	23	-	25	ns	4,9
7	tAA	Access Time from Column Address	-	35	-	40	-	45	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	40	-	45	-	50	ns	4
13	tRAS	RAS Pulse Width	65	10K	75	10K	85	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	65	200K	75	200K	85	200K	ns	
15	tRSH	RAS Hold Time	20	-	23	-	25	-	ns	
16	tCSH	CAS Hold Time	65	-	75	-	85	-	ns	
17	tCAS	CAS Pulse width	20	10K	23	10K	25	10K	ns	
27	tRAL	Column Address to RAS Lead Time	35	-	40	-	45	-	ns	
41	tCWD	CAS to WE Delay Time	43	-	48	-	50	-	ns	8
42	tRWD	RAS to WE Delay Time	88	-	100	-	110	-	ns	8
43	tAWD	Column Address to WE Delay Time	58	-	65	-	70	-	ns	8
49	tOEA	OE Access Time	-	20	-	20	-	25	ns	
50	tOED	OE to Data Delay	20	-	20	-	25	-	ns	
52	tOEH	OE Command Hold Time	15	-	15	-	15	-	ns	

NOTE:

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles proper device operation is achieved.
2. If $\overline{\text{RAS}}=\text{Vss}$ during power-up, this device could begin an active cycle. These condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with Vcc during power-up or be held at a valid Vih in order to minimize the power-up current.
3. $\text{Vih}(\text{min.})$ and $\text{Vil}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $\text{Vih}(\text{min.})$ and $\text{Vil}(\text{max.})$, and are assumed to be 5ns for all inputs.
4. Measured with a load equivalent to 100pF and $\text{VOH}=2.0\text{V}$ ($\text{IOUT}=2\text{mA}$), $\text{VOL}=0.8\text{V}$ ($\text{IOUT}=2.0\text{mA}$).
5. $\text{tOFF}(\text{max.})$ and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either trCH or trRH must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and $\overline{\text{WE}}$ leading edge in Read-Modify-Write cycles.
8. twCS , trWD , tcWD , tAWD and tcpWD are not restrictive operating parameters. They are included in the data sheet as electrical parameters only. If $\text{twCS}\geq\text{twCS}(\text{min.})$, the cycle is an early write cycle and data output will remain open circuit (high impedance) through the entire cycle. If $\text{trWD}\geq\text{trWD}(\text{min.})$, $\text{tcWD}\geq\text{tcWD}(\text{min.})$, $\text{tAWD}\geq\text{tAWD}(\text{min.})$, and $\text{tcpWD}\geq\text{tcpWD}(\text{min.})$, the cycle is a Read-Modify-Write cycle and data will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the $\text{trCD}(\text{max.})$ limit insures that $\text{trAC}(\text{max.})$ can be met. $\text{trCD}(\text{max.})$ is specified point only. If trCD is greater than the specified $\text{trCD}(\text{max.})$ limit, then access time is controlled by tCAC .
10. Operation within the $\text{trAD}(\text{max.})$ limit insures that $\text{trAC}(\text{max.})$ can be met. $\text{trAD}(\text{max.})$ is specified as a reference point only. If trAD is greater than the specified $\text{trAD}(\text{max.})$ limit, then access time is controlled by tAA .
11. $\text{tREF}(\text{max.})=256\text{ms}$ is applied to SL-Parts.
12. A burst of 2048 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles must be executed within 32ms (256ms for SL-part) after exiting self refresh.
13. These specifications are applied to the Test Mode.

CAPACITANCE

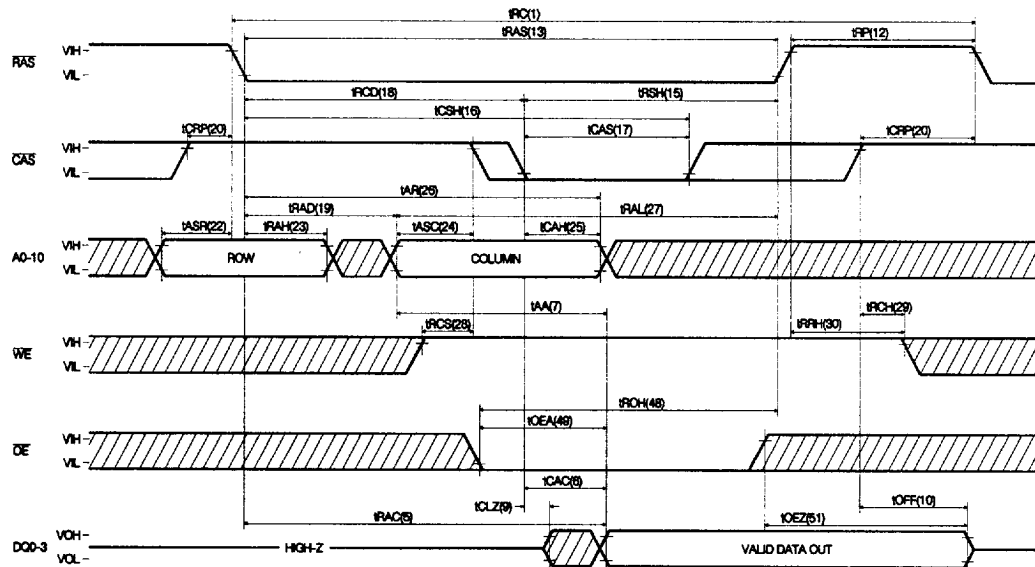
($\text{TA}=25^\circ\text{C}$, $\text{Vcc}=3.3\text{V}\pm 10\%$, $\text{Vss}=0\text{V}$, $\text{f}=1\text{MHz}$, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A10)	-	5	pF
CIN2	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	-	7	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ3)	-	7	pF

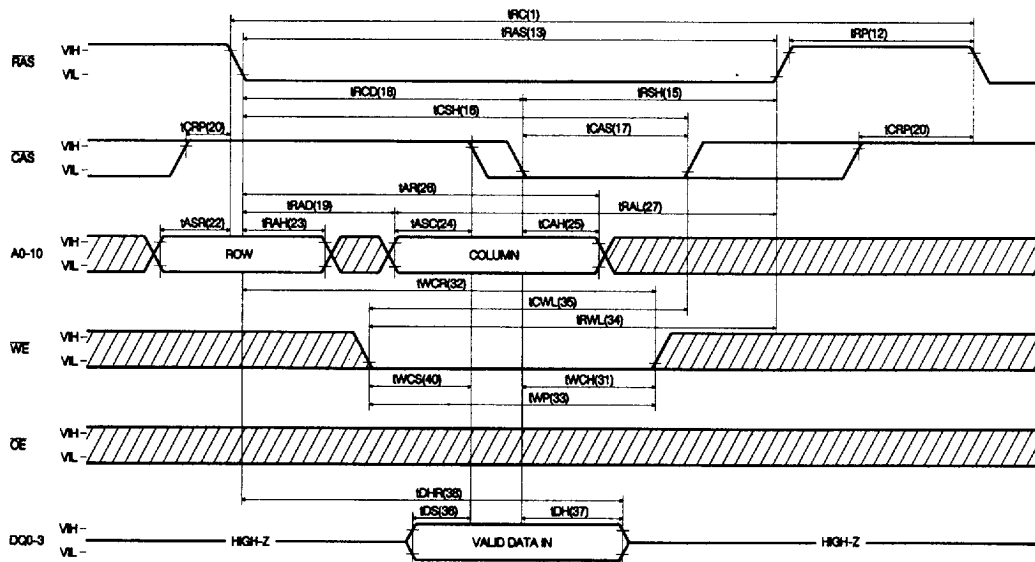
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TIMING DIAGRAM

READ CYCLE



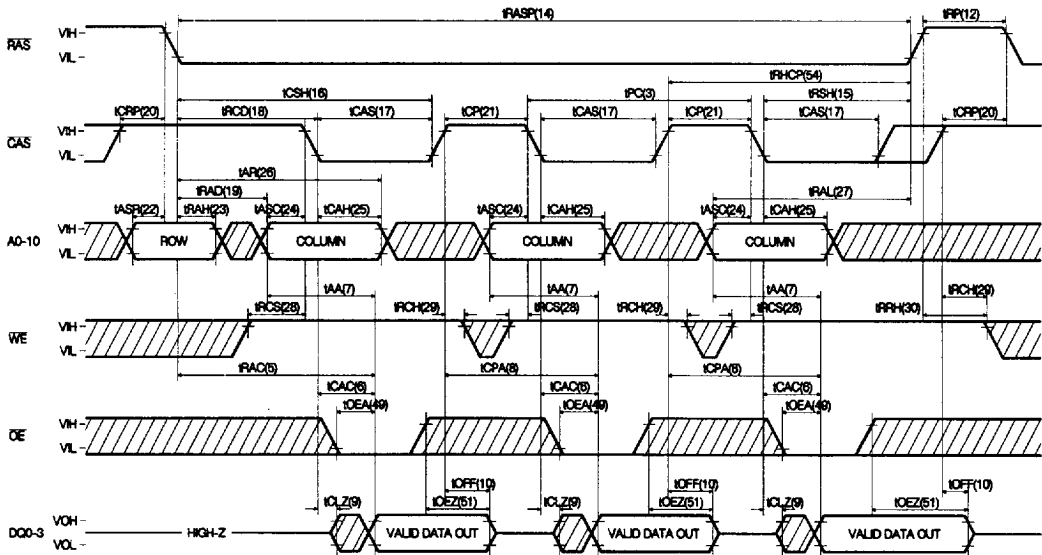
EARLY WRITE CYCLE



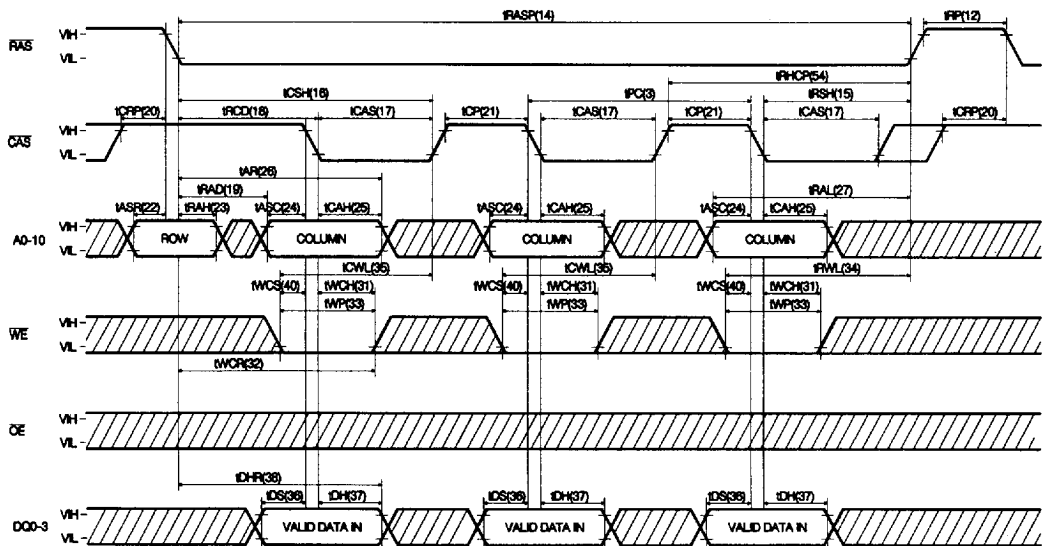
The timing diagram illustrates the relationship between several signals and their timing parameters:

- RAS:** RAS Enable signal. Timing parameters include $t_{RAS}(13)$, $t_{RCD}(18)$, $t_{RSH}(19)$, and $t_{RFP}(12)$.
- CAS:** CAS Enable signal. Timing parameters include $t_{ICP}(20)$, $t_{ICSH}(16)$, $t_{ICAS}(17)$, and $t_{ICRP}(20)$.
- A0-10:** Address bus. Timing parameters include $t_{ASR}(22)$, $t_{RAH}(23)$, $t_{ASC}(24)$, $t_{CAH}(25)$, and $t_{RAL}(27)$. The bus is divided into ROW and COLUMN phases.
- WE:** Write Enable signal. Timing parameters include $t_{CWL}(35)$ and $t_{RWL}(34)$.
- OE:** Output Enable signal. Timing parameters include $t_{MP}(33)$ and $t_{OEH}(32)$.
- DQ0-3:** Data bus. Timing parameters include $t_{OED}(50)$, $t_{DS}(38)$, $t_{DH}(37)$, and $t_{VDS}(36)$. The signal is shown in a HIGH-Z state during certain periods.

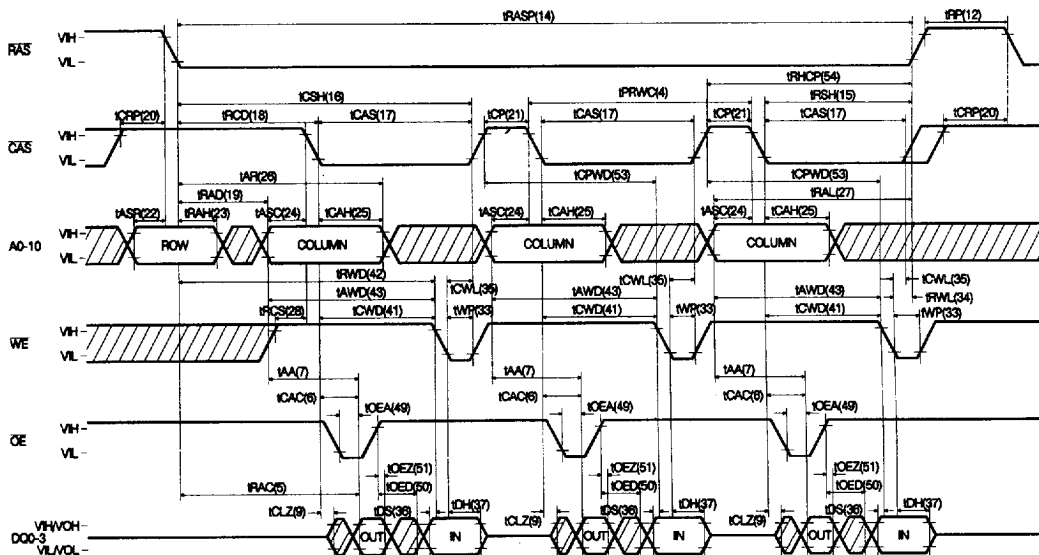
FAST PAGE MODE READ CYCLE



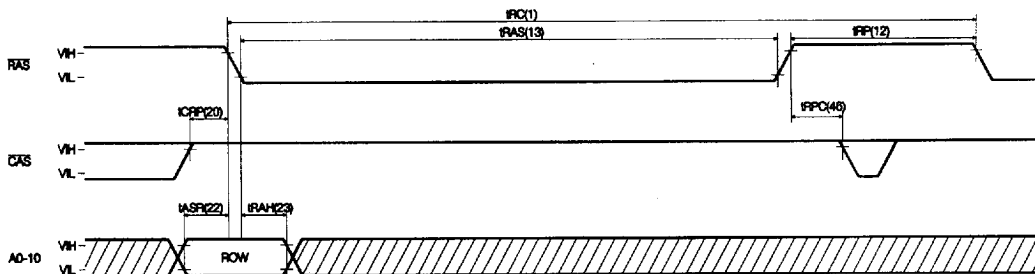
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

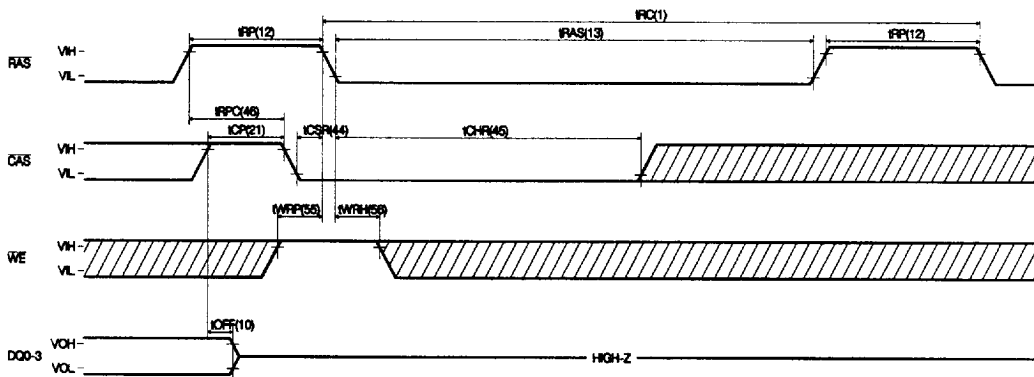


RAS-ONLY REFRESH CYCLE



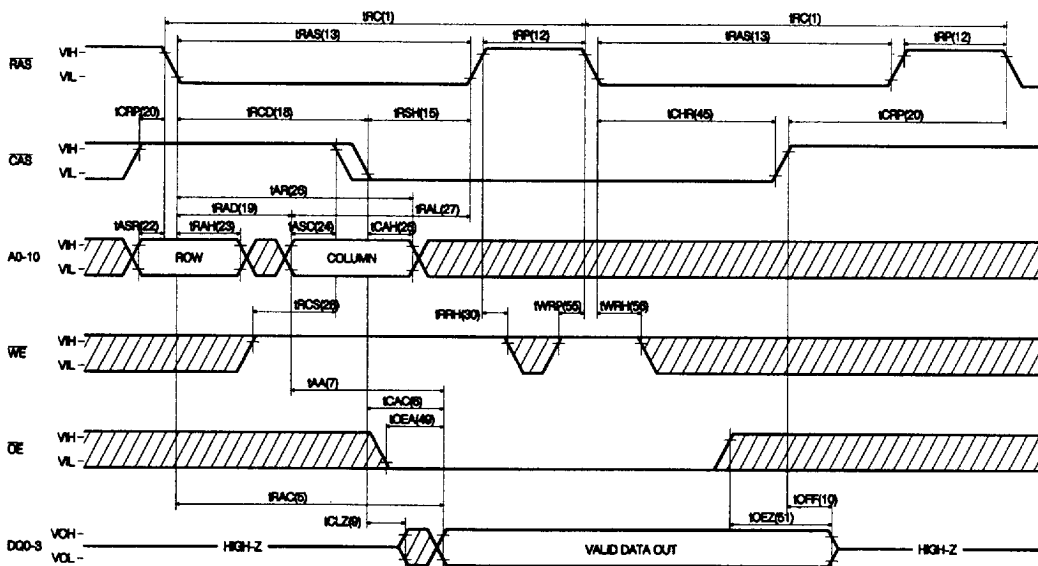
NOTE : OE and WE = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

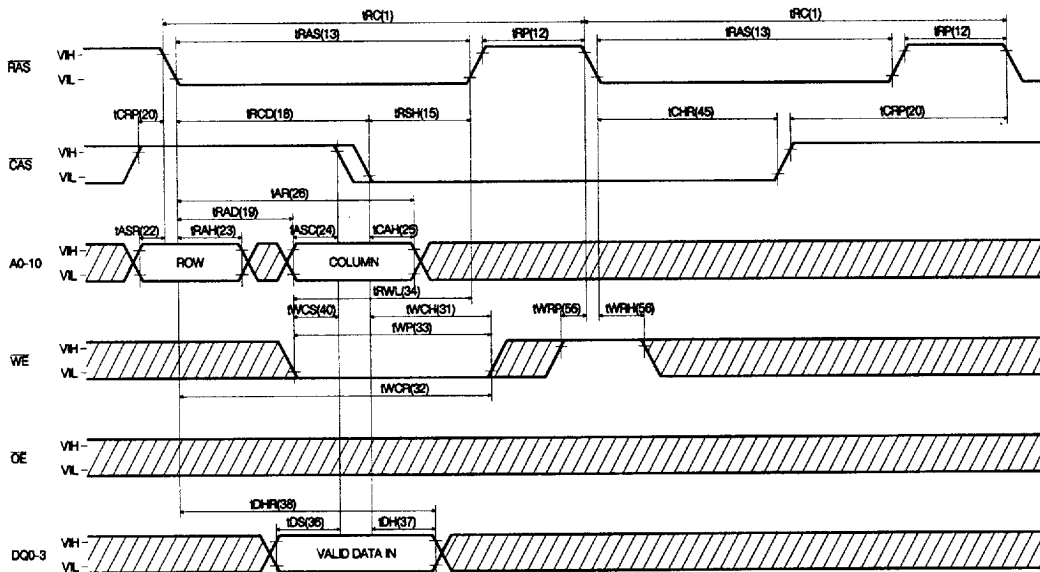


NOTE : A0-10 and $\overline{OE}$ = "H" or "L"

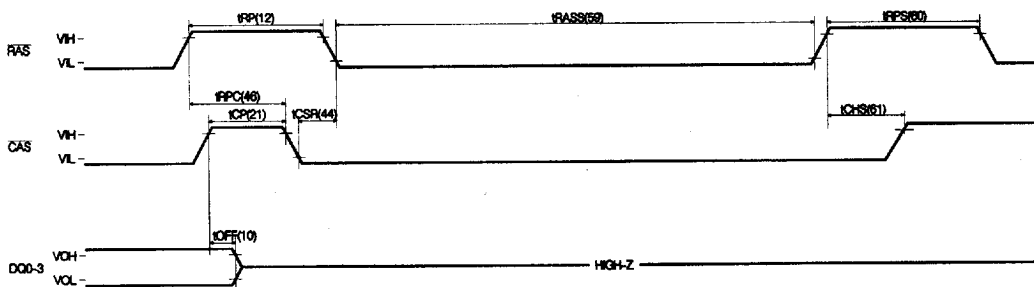
HIDDEN REFRESH CYCLE (FEAD)



HIDDEN REFRESH CYCLE (WRITE)

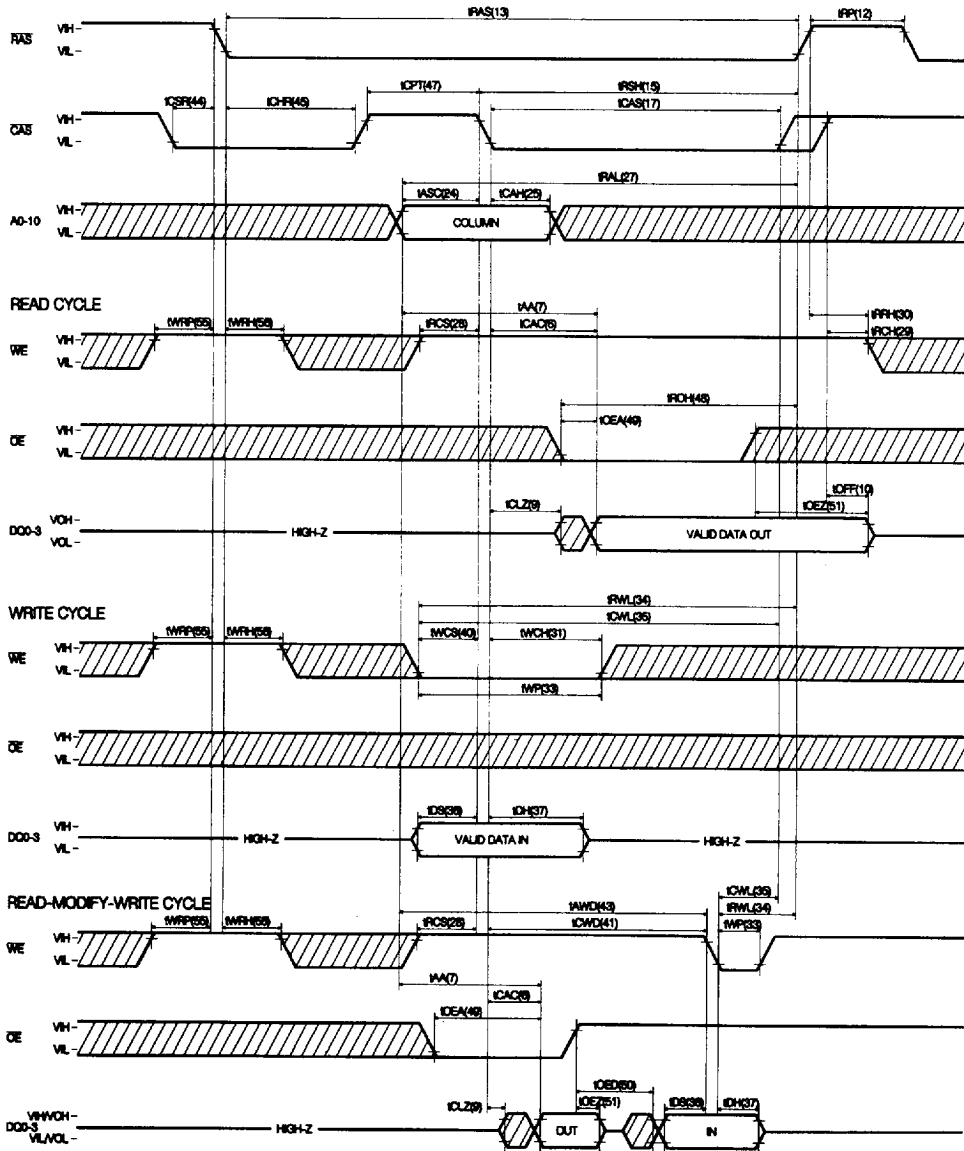


CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE : A0-10, OE and WE = "H" or "L"

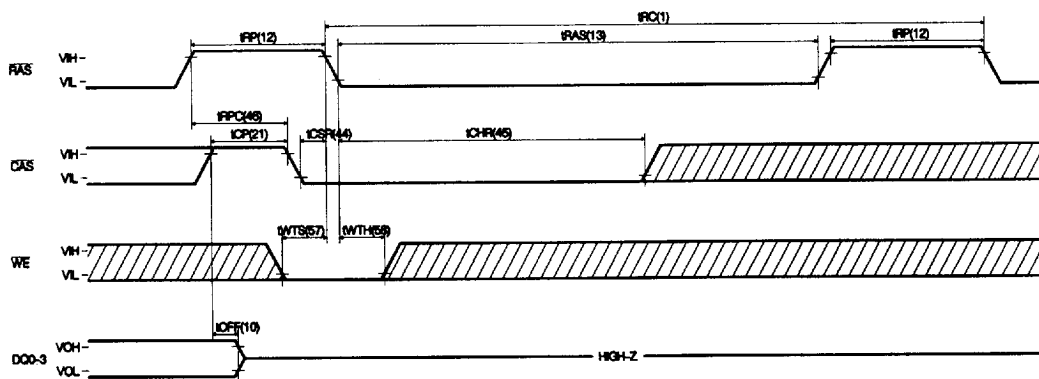
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



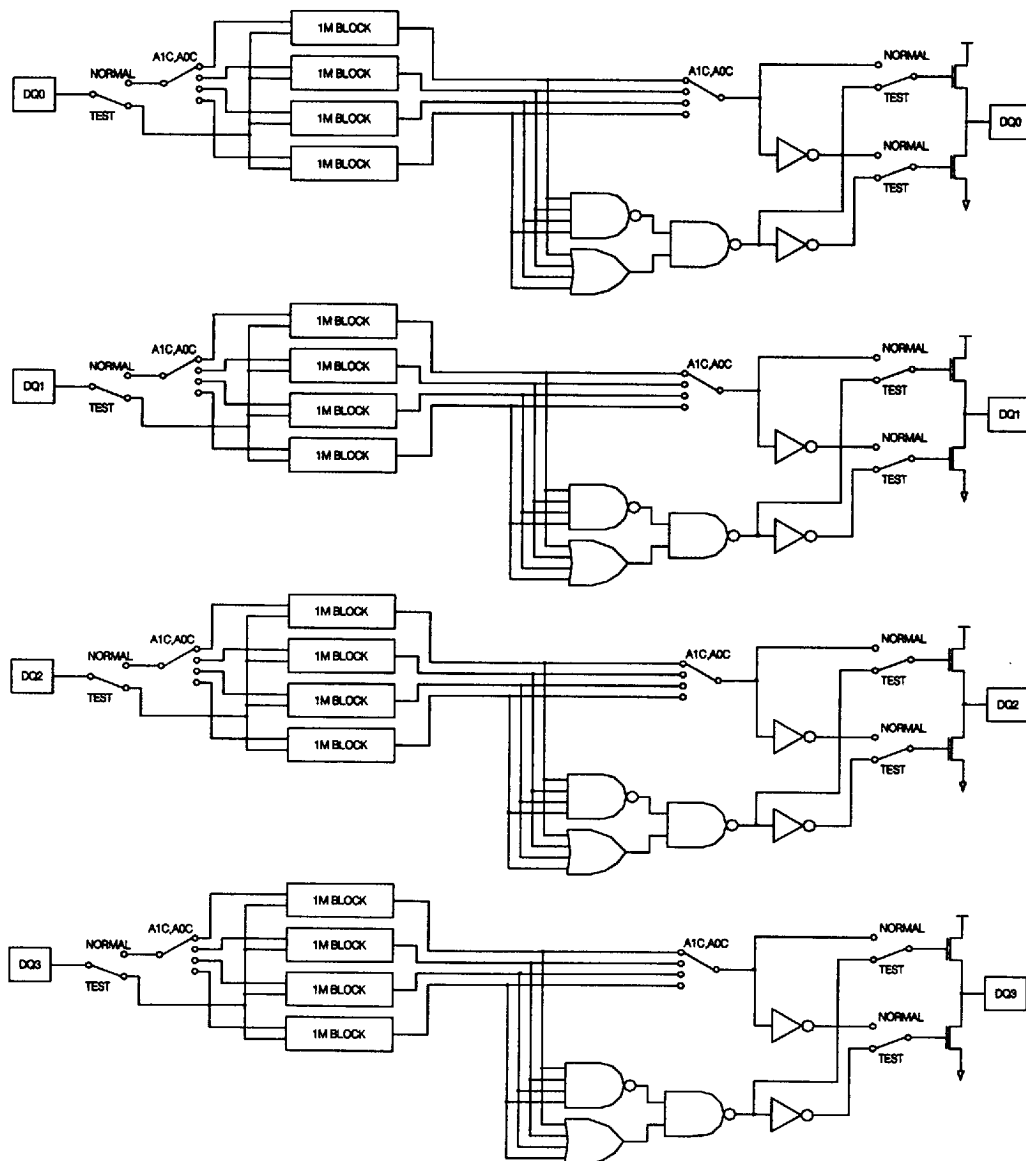
TEST MODE

The HY51V17400B is a DRAM organized $4,194,304 \times 4$ -bit. It is internally organized $1,048,576 \times 16$ -bit. In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrieved the same way. Column address A0 and A1 are not used. If, upon reading, 4-bit data from 4 sectors connected to one DQ pin are equal (all "1"s or "0"s), the DQ pin indicates a "1". If they are not equal, the DQ pin indicates a "0". Belowing shows the timing diagram of the HY51V17400B to enter Test Mode. In Test Mode, the 4M $\times$ 4 DRAM can be tested as if it were a 1M $\times$ 4 DRAM. WE, CAS-before-RAS cycle (Test Mode In Cycle) puts the HY51V17400B into Test Mode and CAS-before-RAS or RAS-only refresh cycle puts it back into Normal Mode. In Test Mode, WE, CAS-before-RAS cycle shall be used for the refresh operation. The Test Mode function reduces test time (1/4 in case of N test pattern).

TEST MODE IN CYCLE

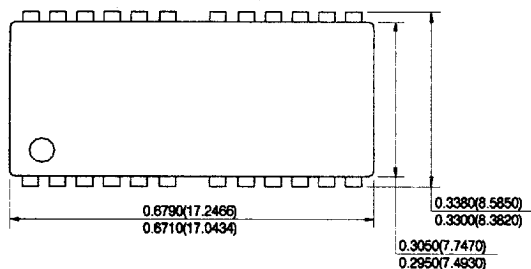


BLOCK DIAGRAMIN TEST MODE

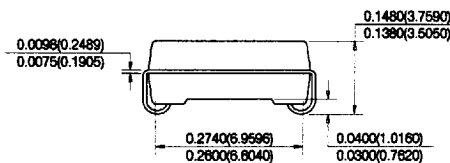
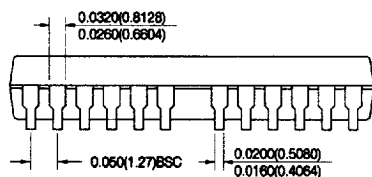


PACKAGE INFORMATION

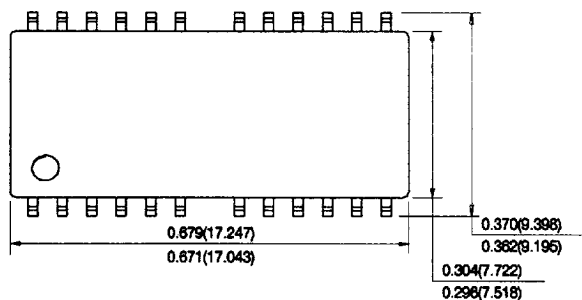
300 mil 24/26 pin Small Outline J-form Package (J)



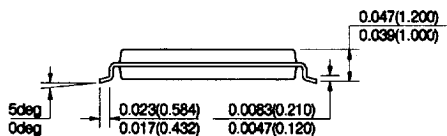
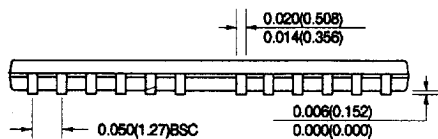
UNIT : INCH(mm)



300 mil 24/26 pin Thin Small Outline Package (T)(R)



UNIT : INCH(mm)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY51V17400BJ	60/70/80		SOJ
HY51V17400BSLJ	60/70/80	SL-part	SOJ
HY51V17400BT	60/70/80		TSOP-II
HY51V17400SLT	60/70/80	SL-part	TSOP-II
HY51V17400BR	60/70/80		TSOP-II(R)
HY51V17400BSLR	60/70/80	SL-part	TSOP-II(R)