

INTRODUCTION

The EB9021 is an evaluation and reference design platform for the **GENLINX™ II** GS9021 EDH Coprocessor. The EB9021 is a parallel ECL input, parallel ECL output board that fully supports Error Detection and Handling (EDH) according to SMPTE RP165. The board operates to 54MHz and supports the following standards:

- 4:2:2 Component with 13.5 MHz Y sampling (NTSC & PAL)
- 4:2:2 Component with 18.0 MHz Y sampling (NTSC & PAL)
- 4fsc Composite (NTSC & PAL)
- 4:4:4:4 Component Single Link with 13.5 MHz Y sampling (NTSC & PAL)

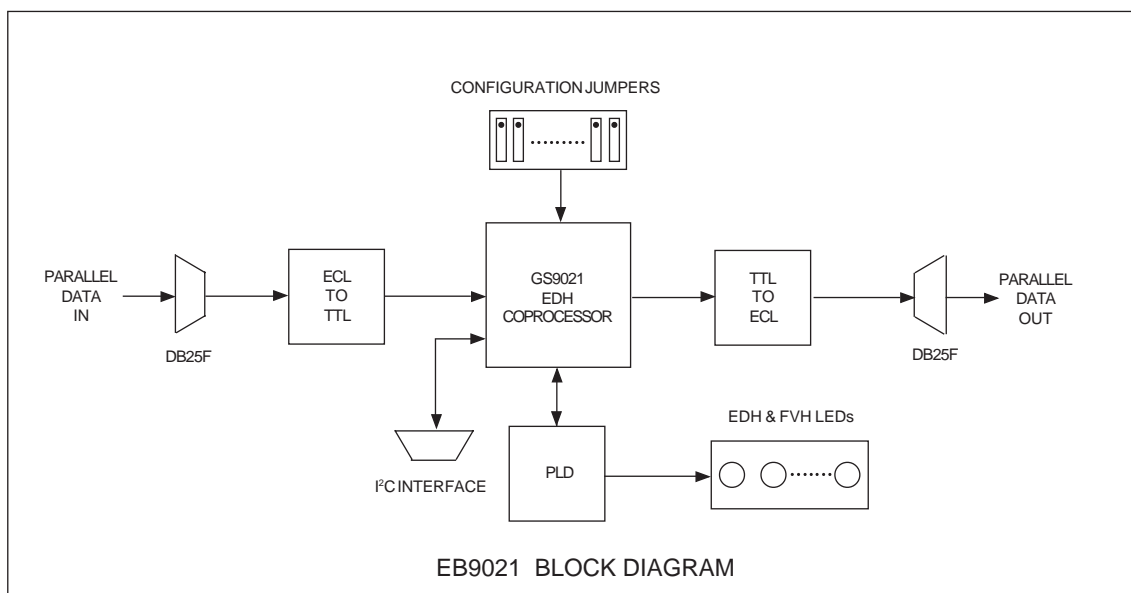
CIRCUIT DESCRIPTION

A block diagram of the board is shown below and illustrates the primary circuit functions. A full schematic is also included.

Bit parallel data is connected to the board through a DB25F connector with a pin configuration in accordance with SMPTE 125 and SMPTE 244M. Three 10125 ECL to TTL converter ICs are used to shift the logic levels of the bit parallel data to directly interface with the GS9021 EDH Coprocessor. The resulting CMOS (TTL compatible) outputs of the GS9021 are supplied to three 10124 TTL to ECL converter ICs. These ECL outputs are then available at the output DB25F connector.

A PLD is provided primarily to interface to the Flag Port of the GS9021 and extract the Ancillary, Full Field, and Active Picture error flags. The PLD is designed to cycle the S[1:0] inputs of the GS9021, read and demultiplex the output error flags, and drive the EDH LEDs providing visual indication of the type of EDH errors present. The PLD is also designed to control which error flags are read from the GS9021 Flag Port — incoming or outgoing. Upon power-up or RESET, the board is configured to display the outgoing EDH error flags. When the INC. FLAGS push-button is depressed, the PLD writes to the GS9021 flag port instructing it to output the incoming EDH error flags instead. To return to the outgoing error flags, the system must be RESET. Finally, the PLD is used to buffer the GS9021 field, vertical, and horizontal output signals and drive the respective LEDs.

A DB9F connector is provided for access to the I²C interface of the GS9021. I²C slave address bits are set via configuration jumpers. For a detailed description of the GS9021 I²C interface refer to the GS9021 data sheet.



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Finally, configuration jumpers are provided for further configuration of the GS9021. A detailed description of the input and output pins of the GS9021 can be found in the GS9021 data sheet.

BOARD SET-UP AND TEST

Upon power-up or RESET, the GS9021 is configured for auto standards detection of any of the supported video standards. The GS9021 can also be configured for manual standards detection by setting the STD[3:0], STD_SEL, and S bits of the HOSTIF write table appropriately via the I²C interface.

To verify operation of the EB9021, a source of parallel digital video should be applied to the input DB25F connector. The output data stream available at the DB25F output connector can be supplied to a D to A converter for verification via a monitor. Note that the following configuration signals must be set as shown for an output to be present:

BLANK_EN = HIGH (blanking disabled)
LSB_TOP = LOW (output data bus is not reversed)

The power supply requirements for the EB9021 are +5V for VCC at a current rating of 300mA and -5V for VEE at a current rating of 415mA (nominally).

PCB DETAILS

The EB9021 is a four layer printed circuit board constructed of standard FR-4 material and measures approximately 6.5" by 4.5". Ground and power plane layers are internal to the board with signal layers on the top and bottom of the board. Components are mounted on the top side. The silk-screen (top) and the top and bottom layers are shown on the following pages.

APPLICATIONS

The EB9021 evaluation board is designed to allow evaluation and testing of the GS9021 EDH Coprocessor. The board can also be used in stand alone applications where it is necessary to test the performance of a system. In this application, the EB9021 provides visual indication of system errors as well as detailed error reporting via the I²C interface.

