National Semiconductor Corporation

DS1644/DS3644/DS1674/DS3674 Quad TTL to MOS Clock Drivers

General Description

The DS1644/DS3644 and DS1674/DS3674 are quad bipolar-to-MOS clock drivers with TTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features two common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transisitors are used on all inputs thereby minimizing input loading.

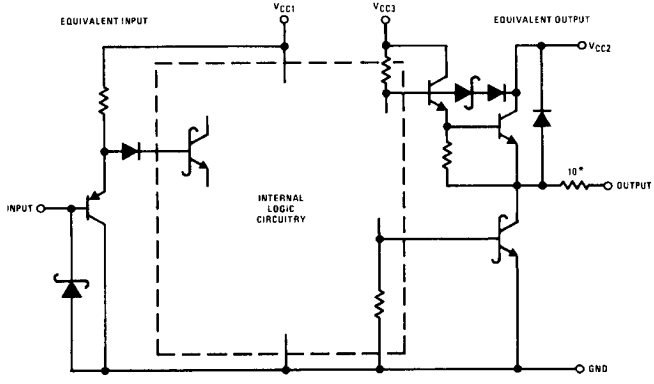
The circuit may be connected to provide a 12V clock output amplitude as required by 4k RAMs or a 5V clock output amplitude as required by 16k RAMs.

The DS1644/DS3644 contains a 10Ω resistor in series with each output to dampen the transients caused by the fast-switching output, while the DS1674/DS3674 has a direct, low impedance output for use with or without an external damping resistor.

Features

- TTL compatible inputs
- 12V clock or 5V clock driver
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function compatible with MC3460 and 3235
- Built-in damping resistors (DS1644/DS3644)

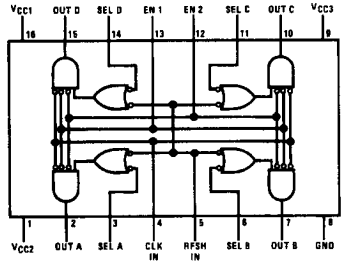
Schematic and Connection Diagrams



*DS1644/DS3644 only

TL/F/5876-1

Dual-In-Line Package



TL/F/5876-2

Top View
Order Number DS3644J, DS3674J, DS3644N or DS3674N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	
V_{CC1}	7V
V_{CC2}	13.5V
V_{CC3}	16V
Input Voltage	−1.0V to +7V
Output Voltage	−1.0V to +16V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 sec.)	300°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
V_{CC1}			
DS1644, DS1674	4.5	5.5	V
DS3644, DS3674	4.75	5.25	V
V_{CC2}			
DS1644, DS1674	4.5	13.2	V
DS3644, DS3674	4.75	12.6	V
V_{CC3}			
DS1644, DS1674	V_{CC2}	16.5	V
DS3644, DS3674	V_{CC2}	15.75	V
Temperature, T_A			
DS1644, DS1674	−55	+125	°C
DS3644, DS3674	0	+70	°C

Electrical Characteristics

5V operation, (V_{CC1} = V_{CC2} = 5V, V_{CC3} = 12V); 12V operation, (V_{CC1} = 5V, V_{CC2} = 12V, V_{CC3} = V_{CC2} + (3V ±10%)); DS1644, DS1674, ±10% power supply tolerances; DS3644, DS3674, ±5% power supply tolerances, unless otherwise noted. (Notes 2, 3 and 4).

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = 5.5V	Select Inputs		0.01	10	μA
			All Other Inputs		0.04	40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V	Select Inputs		−40	−250	μA
			All Other Inputs		−0.16	−1.0	mA
V_{CD}	Input Clamp Voltage	I_I = −12 mA			−0.8	−1.5	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −1 mA, V_{IL} = 0.8V		V_{CC2} −0.5	V_{CC2} −0.2		V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 5 mA, V_{IH} = 2.0V			0.3	0.5	V
V_{OC}	Output Clamp Voltage	I_{OC} = 5 mA, V_{IL} = 0.8V			V_{CC2} +0.8	V_{CC2} +1.5	V
I_{CCH}	Supply Current Output High	All Inputs V_{IN} = 0V Outputs Open					
	I_{CC1}		V_{CC1} = Max		18	27	mA
	I_{CC2}		12V Operation		−2	−4	mA
	I_{CC3}				2	4	mA
	I_{CC2}		5V Operation		−8	−16	mA
	I_{CC3}				8	16	mA
I_{CCL}	Supply Currents Outputs Low	All Inputs V_{IN} = 5V Outputs Open					
	I_{CC1}		V_{CC1} = 5.25V		25	40	mA
	I_{CC2}		V_{CC2} = 12.6V			3	mA
	I_{CC3}		V_{CC3} = 15.75V		16	25	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1644, DS1674 and across the 0°C to +70°C range for the DS3644, DS3674. All typicals are given for T_A = 25°C.

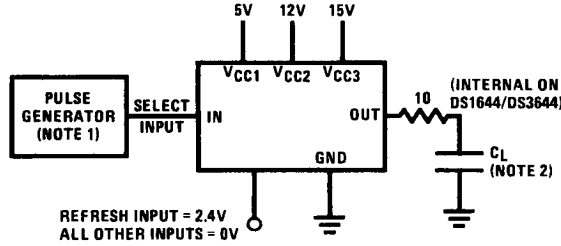
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: For AC measurements, a 10Ω resistor must be placed in series with the output of the DS1674/DS3674. This resistor is internal to the DS1644/DS3644 and need not be added.

Switching Characteristics T_A = 25°C unless otherwise noted, (Note 4), (*Figures 1, 2, 3 and 4*)

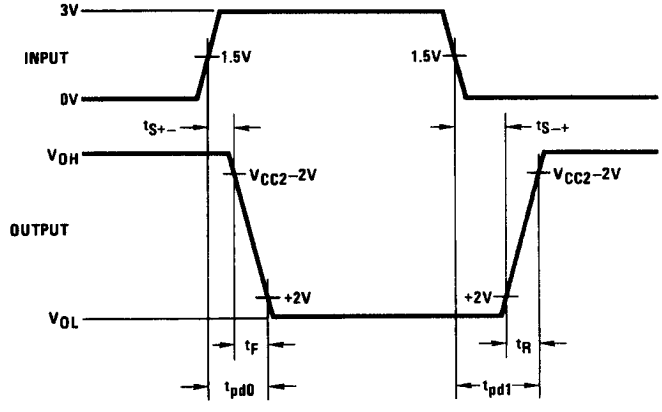
Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{s+-}	Storage Delay Negative Edge	R_D = 10Ω	C_L = 100 pF		8	11	ns
			C_L = 400 pF		12	16	ns
t_{s-+}	Storage Delay Positive Edge	R_D = 10Ω	C_L = 100 pF		10	13	ns
			C_L = 400 pF		13	16	ns
t_F	Fall Time	R_D = 10Ω	C_L = 100 pF		9	16	ns
			C_L = 400 pF		17	24	ns
t_R	Rise Time	R_D = 10Ω	C_L = 100 pF		8	12	ns
			C_L = 400 pF		13	19	ns
t_{pd0}	Propagation Delay to a Logical "0"	R_D = 10Ω	C_L = 100 pF		17	27	ns
			C_L = 400 pF		29	40	ns
t_{pd1}	Propagation Delay to a Logical "1"	R_D = 10Ω	C_L = 100 pF		18	25	ns
			C_L = 400 pF		26	35	ns

AC Test Circuits and Switching Time Waveforms



TL/F/5876–3

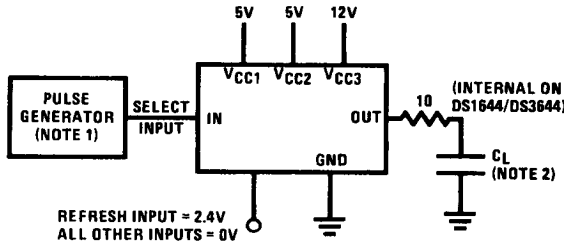
FIGURE 1. 12V Operation



TL/F/5876–4

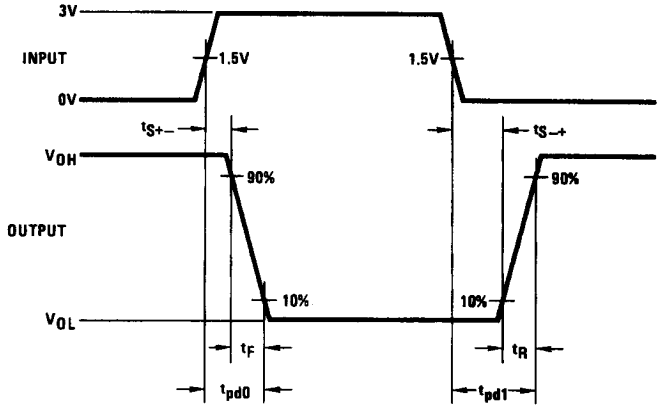
FIGURE 2. 12V Operation

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5876–5

FIGURE 3. 5V Operation



TL/F/5876–6

FIGURE 4. 5V Operation

Note 1: The pulse generator has the following characteristics. PPR = 1 MHz, $t_R \leq 10$ ns, $Z_{OUT} = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

Truth Table

Input					Output
Enable 1	Enable 2	Select Input	Clock Input	Refresh Input	
1	X	X	X	X	0
X	1	X	X	X	0
X	X	X	1	X	0
X	X	1	X	1	0
0	0	0	0	X	1
0	0	X	0	0	1