MAXIMUM R **IGS** (Above which the useful life may be impaired)

Storage Temper.	
Temperature (Ambient) Under Bias	−65°C to +150°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−55°C to +125°C
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +7V
DC Input Voltage	−0.5V to + V_{CC} max.
DC Output Current, Into Outputs	−0.5V to +5.5V
DC Input Current	30 mA
	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74153 T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am54153 T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −800µA V_{IN} = V_{IH} or V_{IL}		2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −12mA				−1.5	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−1.6	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				40	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V	Am54	−20		−55	mA
			Am74	−18		−57	
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)	Am54		36	52	mA
			Am74		36	60	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Data to Output	V_{CC} = 5.0V, R_L = 400Ω, C_L = 30 pF		12	18	ns
t_{PHL}				15	23	
t_{PLH}	Select to Output			22	34	ns
t_{PHL}				22	34	
t_{PLH}	Strobe to Output			19	30	ns
t_{PHL}				15	23	

FUNCTION TABLE

INPUTS						OUTPUTS
Select		Data			Strobe	Output
B	A	C_0	C_1	C_2	C_3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH
L = LOW
X = Don't Care

Note: A & B are common to both 4 input multiplexers.

DEFINITION OF FUNCTIONAL TERMS

$1C_i$, $2C_i$ Data Inputs. The four data inputs to each multiplexer $i = 0, 1, 2,$ and 3.

1Y, 2Y Multiplexer Outputs. The output of each four-input multiplexer.

A, B Select Inputs. The inputs used to determine which of the four inputs are selected for the output.

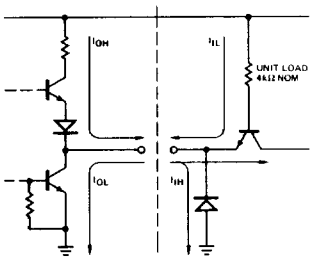
G Enable (Strobe). An active-LOW strobe used to enable the output. A HIGH level input forces the output LOW regardless of the other inputs.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Unit Load	Fan-out Output HIGH	Fan-out Output LOW
1G	1	1	–	–
B	2	1	–	–
1C3	3	1	–	–
1C2	4	1	–	–
1C1	5	1	–	–
1C0	6	1	–	–
1Y	7	–	20	10
GND	8	–	–	–
2Y	9	–	20	10
2C0	10	1	–	–
2C1	11	1	–	–
2C2	12	1	–	–
2C3	13	1	–	–
A	14	1	–	–
2G	15	1	–	–
V_{CC}	16	–	–	–

A TTL Unit Load is defined as +40μA measured at 2.4V HIGH and −1.6mA measured at 0.4V LOW.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

FUNCTION TABLE

INPUTS							OUTPUTS
Select		Data				Strobe	Output
B	A	C_0	C_1	C_2	C_3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH
L = LOW
X = Don't Care

Note: A & B are common to both 4 input multiplexers.

DEFINITION OF FUNCTIONAL TERMS

$1C_i$, $2C_i$ Data Inputs. The four data inputs to each multiplexer $i = 0, 1, 2$, and 3.

1Y, 2Y Multiplexer Outputs. The output of each four-input multiplexer.

A, B Select Inputs. The inputs used to determine which of the four inputs are selected for the output.

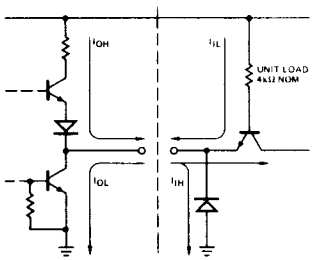
G Enable (Strobe). An active-LOW strobe used to enable the output. A HIGH level input forces the output LOW regardless of the other inputs.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Unit Load	Fan-out Output HIGH	Fan-out Output LOW
1G	1	1	–	–
B	2	1	–	–
1C3	3	1	–	–
1C2	4	1	–	–
1C1	5	1	–	–
1C0	6	1	–	–
1Y	7	–	20	10
GND	8	–	–	–
2Y	9	–	20	10
2C0	10	1	–	–
2C1	11	1	–	–
2C2	12	1	–	–
2C3	13	1	–	–
A	14	1	–	–
2G	15	1	–	–
V_{CC}	16	–	–	–

A TTL Unit Load is defined as +40μA measured at 2.4V HIGH and −1.6mA measured at 0.4V LOW.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

UNIT LOAD DEFINITIONS

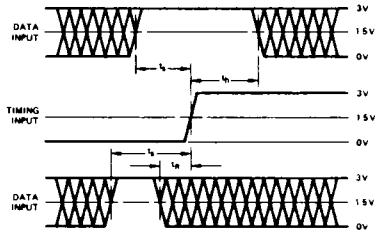
SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	-0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	-0.36mA	0.4V
Am54/74	40μA	2.4V	-1.6mA	0.4V
54H/74H	50μA	2.4V	-2.0mA	0.4V
Am54S/74S	50μA	2.7V	-2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	-0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	-0.36mA	0.4V
Am9300	40μA	2.4V	-1.6mA	0.4V
Am93L00	20μA	2.4V	-0.4mA	0.3V
Am93S00	50μA	2.7V	-2.0mA	0.5V
Am75/85	40μA	2.4V	-1.6mA	0.4V
Am8200	40μA	4.5V	-1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

PARAMETER MEASUREMENTS

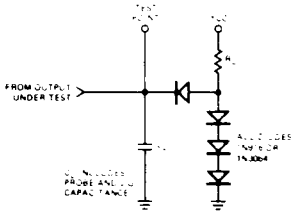
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

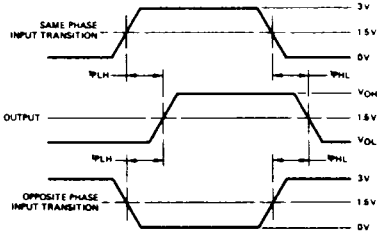


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

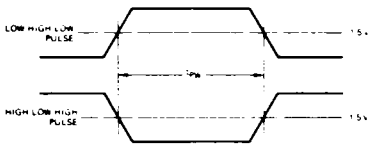
LOAD TEST CIRCUIT



PROPAGATION DELAY

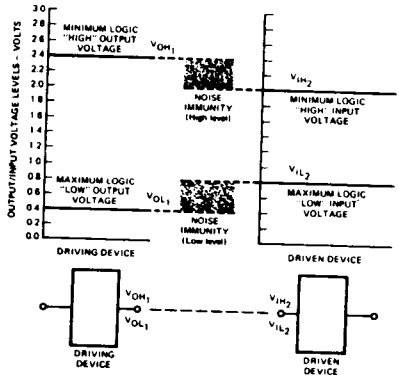


PULSE WIDTH



Notes: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz Z_o = 50Ω t_r ≤ 10ns t_f ≤ 10ns

IN OUTPUT VOLTAGE IN...RFACE CONDITIONS



Note: Refer to Electrical Characteristics for measure current.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

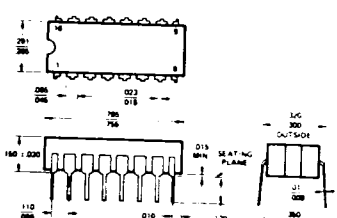
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

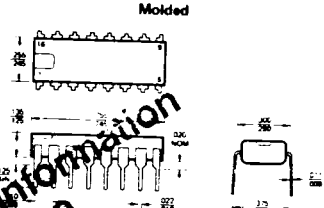
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

Ceramic

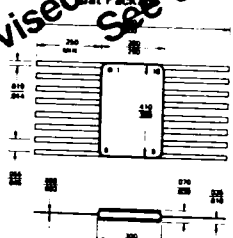


Molded



Revised Package Information
See Section 9

Flat Package



ADVANCED MICRO DEVICES INC.
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Am54/74160 • Am54/74161
Am54/74162 • Am54/74163

Synchronous Four-Bit Counters

Distinctive Characteristics

- 4-bit synchronous counters
- Synchronously programable
- Internal look-ahead counting
- Carry output for n-bit cascading
- Synchronous or asynchronous clear
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

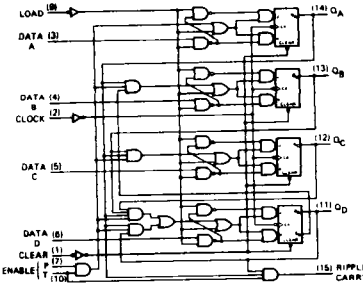
The Am54/74160, Am54/74161, Am54/74162 and Am54/74163 synchronous, presettable counters have internal look-ahead carry and ripple carry output for high-speed counting applications. The Am54/74160 and Am54/74162 are decade counters and the Am54/74161 and Am54/74163 are 4-bit binary counters. Counting or loading occurs on the positive transition of the clock pulse. A LOW level on the load input causes the data on the A, B, C and D inputs to be shifted to the appropriate Q outputs on the next positive clock transition. LOW-to-HIGH transitions of the load input should not occur when the clock is LOW if the enable inputs are HIGH at or before the transition.

The Am54/74160 and Am54/74161 feature an asynchronous clear. A LOW level at the clear input sets the Q outputs LOW regardless of the other inputs. The Am54/74162 and Am54/74163 have a synchronous clear. A LOW level at the clear input sets the Q outputs LOW after the next positive clock transition regardless of the enable inputs.

Both count-enable inputs P and T must be HIGH to count. Count enable T is included in the ripple carry output gate for cascading connection. HIGH-to-LOW level transitions on the enable P or T inputs should occur only when the clock is HIGH.

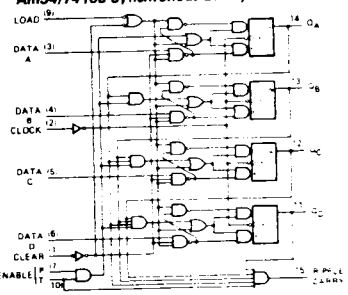
LOGIC DIAGRAMS

Am54/74160 Synchronous Decade Counter



Am54/74162 synchronous decade counters are similar; however, the clear is synchronous as shown for the Am54/74163 binary counters.

Am54/74163 Synchronous Binary Counter

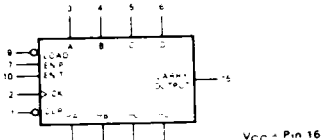


Am54/74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the Am54/74160 decade counters.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am54/74160	Molded DIP	0°C to +70°C	SN74160N
	Hermetic DIP	0°C to +70°C	SN74160J
	Dice	0°C to +70°C	SN74160X
	Hermetic DIP	−55°C to +125°C	SN54160J
	Hermetic Flat Pak	−55°C to +125°C	SN54160W
	Dice	−55°C to +125°C	SN54160X
Am54/74161	Molded DIP	0°C to +70°C	SN74161N
	Hermetic DIP	0°C to +70°C	SN74161J
	Dice	0°C to +70°C	SN74161X
	Hermetic DIP	−55°C to +125°C	SN54161J
	Hermetic Flat Pak	−55°C to +125°C	SN54161W
	Dice	−55°C to +125°C	SN54161X
Am54/74162	Molded DIP	0°C to +70°C	SN74162N
	Hermetic DIP	0°C to +70°C	SN74162J
	Dice	0°C to +70°C	SN74162X
	Hermetic DIP	−55°C to +125°C	SN54162J
	Hermetic Flat Pak	−55°C to +125°C	SN54162W
	Dice	−55°C to +125°C	SN54162X
Am54/74163	Molded DIP	0°C to +70°C	SN74163N
	Hermetic DIP	0°C to +70°C	SN74163J
	Dice	0°C to +70°C	SN74163X
	Hermetic DIP	−55°C to +125°C	SN54163J
	Hermetic Flat Pak	−55°C to +125°C	SN54163W
	Dice	−55°C to +125°C	SN54163X

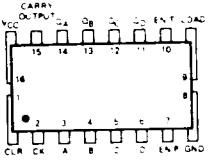
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

MAXIMUM 'INGS (Above which the useful life may be impaired)

Storage Temp	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} ma
DC Input Voltage	−0.5 V to +5.5
DC Output Current, Into Outputs	30 m
DC Input Current	−30 mA to +5.0 m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74160, Am74161, Am74162, Am74163 T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
Am54160, Am54161, Am54162, Am54163 T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −800 µA V_{IN} = V_{IH} or V_{IL}		2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −12 mA				−1.5	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V	CK or EN T			−3.2	mA
			Others			−1.6	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V	CK or EN T			80	µA
			Others			40	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0 V	54 Series	−20		−57	mA
			74 Series	−18		−57	
I_{CCH}	Power Supply Current All Outputs HIGH	V_{CC} = MAX. (Note 5)	54 Series		59	85	mA
			74 Series		59	94	
I_{CCL}	Power Supply Current All Outputs LOW	V_{CC} = MAX. (Note 6)	54 Series		63	91	mA
			74 Series		63	101	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CCH} is measured with the load input HIGH, then again with the load input LOW, with all other inputs HIGH and all outputs open.
6. I_{CCL} is measured with the clock input HIGH, then again with the clock input LOW, with all other inputs LOW and all outputs open.

Switching Characteristics (T_A = +25°C)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Carry Output		V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400 Ω		23	35	ns
t_{PHL}					23	35	
t_{PLH}	Clock to Q Output with Load Input HIGH				13	20	ns
t_{PHL}					15	23	
t_{PLH}	Enable T to Carry Output				10	14	ns
t_{PHL}					10	14	
t_{PLH}	Clock to Q Output with Load Input LOW				17	25	ns
t_{PHL}					19	29	
t_{PHL}	Clear to Q Output (Note 1)				20	30	ns
t_{pw}	Pulse Width	Clock		25			ns
		Clear		20			
t_s	Set-up Time	Data – A, B, C, D		15			ns
		Enable P		20			
		Load		25			
		Clear (Note 2)		20			
t_h	Hold Time – Any Input			0			ns
$f_{MAX.}$	Maximum Clock Frequency			25	32		MHz

Notes: 1. Measured from clear input on Am54/74160 and Am54/74161. Measured from clock input on Am54/74162 and Am54/74163.
2. Applies to Am54/74162 and Am54/74163 only.

DEFINITION OF FUNCTIONAL TERMS

CK Clock pulse. Enters data or counts on the positive-going edge.

CLR Clear. On the Am54/74160 and Am54/74161, the clear is asynchronous. A LOW on the clear sets all four flip-flops LOW. On the Am54/74162 and Am54/74163 the clear is synchronous. A LOW on the clear sets all four flip-flops LOW after the next positive-going clock edge.

LOAD Load. When the load is LOW, data on the A, B, C and D inputs is transferred to the output on the positive-going clock edge. When the load is HIGH, the counter is enabled.

EN P Enable P. Parallel count enable. Must be HIGH to count.

EN T Enable T. Serial trickle count enable. Must be HIGH to count.

A, B, C, D The four counter parallel inputs.

Q_A, Q_B, Q_C, Q_D The four counter outputs.

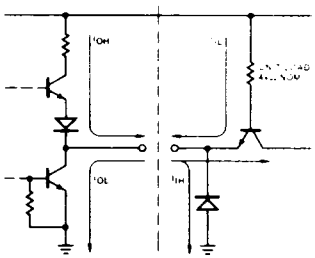
Carry Output Carry look-ahead circuitry for cascading. Will be HIGH when the four-bit counter is maximum (1001 for BCD and 1111 for binary).

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
Clear	1	1		
Clock	2	2		
A	3	1		
B	4	1		
C	5	1		
D	6	1		
Enable P	7	1		
GND	8			
Load	9	1		
Enable T	10	2		
Q_D	11		20	10
Q_C	12		20	10
Q_B	13		20	10
Q_A	14		20	10
Carry Out	15		20	10
V_{CC}	16			

A TTL unit load is defined as 40μA measured at 2.4V HIGH and −1.6mA measured at 0.4V LOW.

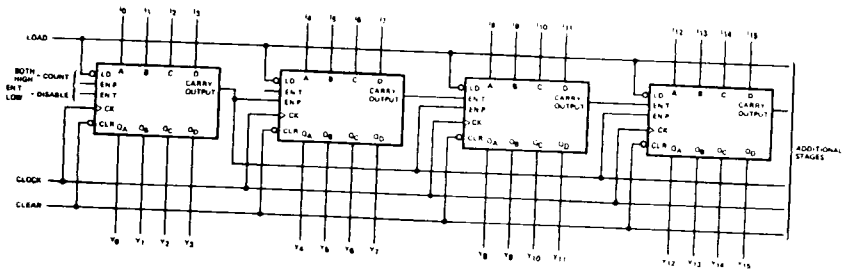
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown

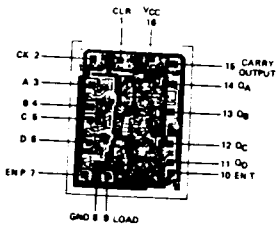
APPLICATIONS

Am54/74160 thru Am54/74163



High-speed, look-ahead carry counter for BCD (Am54/74160 or Am54/74162) or binary (Am54/74161 or Am54/74163). Can count modulo N, N_1-to-N_2, or N_1-to-N maximum.

Pad Layout



DIE SIZE 0.074" X 0.095"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5 V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

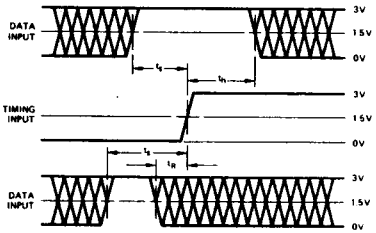
UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40 μA	2.4 V	−1.6 mA	0.4 V
Am25S/26S/27S	50 μA	2.7 V	−2.0 mA	0.5 V
Am25L/26L/27L	20 μA	2.4 V	−0.4 mA	0.3 V
Am25LS/26LS/27LS	20 μA	2.7 V	−0.36 mA	0.4 V
Am54/74	40 μA	2.4 V	−1.6 mA	0.4 V
54H/74H	50 μA	2.4 V	−2.0 mA	0.4 V
Am54S/74S	50 μA	2.7 V	−2.0 mA	0.5 V
54L/74L (Note 1)	20 μA	2.4 V	−0.8 mA	0.4 V
54L/74L (Note 1)	10 μA	2.4 V	−0.18 mA	0.3 V
Am54LS/74LS	20 μA	2.7 V	−0.36 mA	0.4 V
Am9300	40 μA	2.4 V	−1.6 mA	0.4 V
Am93L00	20 μA	2.4 V	−0.4 mA	0.3 V
Am93S00	50 μA	2.7 V	−2.0 mA	0.5 V
Am75/85	40 μA	2.4 V	−1.6 mA	0.4 V
Am8200	40 μA	4.5 V	−1.6 mA	0.4 V

Note: 1. 54L/74L has two different types of standard inputs.

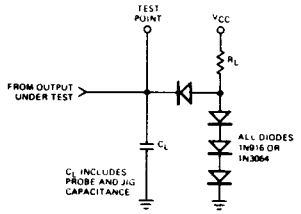
PARAMETER MEASUREMENTS
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

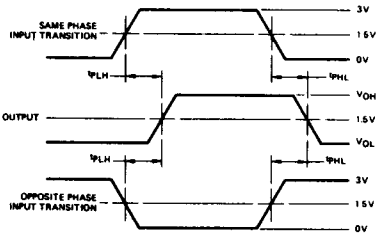


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

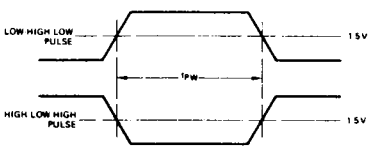
LOAD TEST CIRCUIT



PROPAGATION DELAY

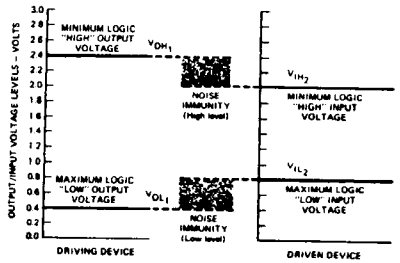


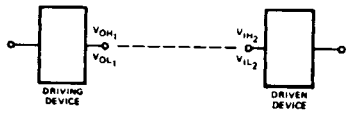
PULSE WIDTH



Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_O = 50\Omega$; $t_r \leq 10$ ns, $t_f \leq 10$ ns.

INPUT/OUTPUT VO. GE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

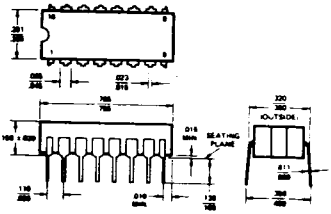
V_{IH} Logic HIGH input voltage.

V_{OL} Low-level output voltage with I_{OL} applied.

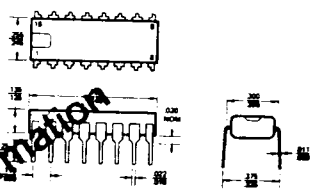
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

Ceramic

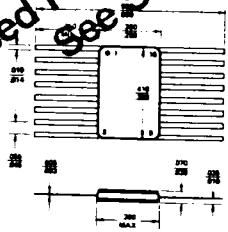


Molded



Revised Package Information
See Section 9

Package



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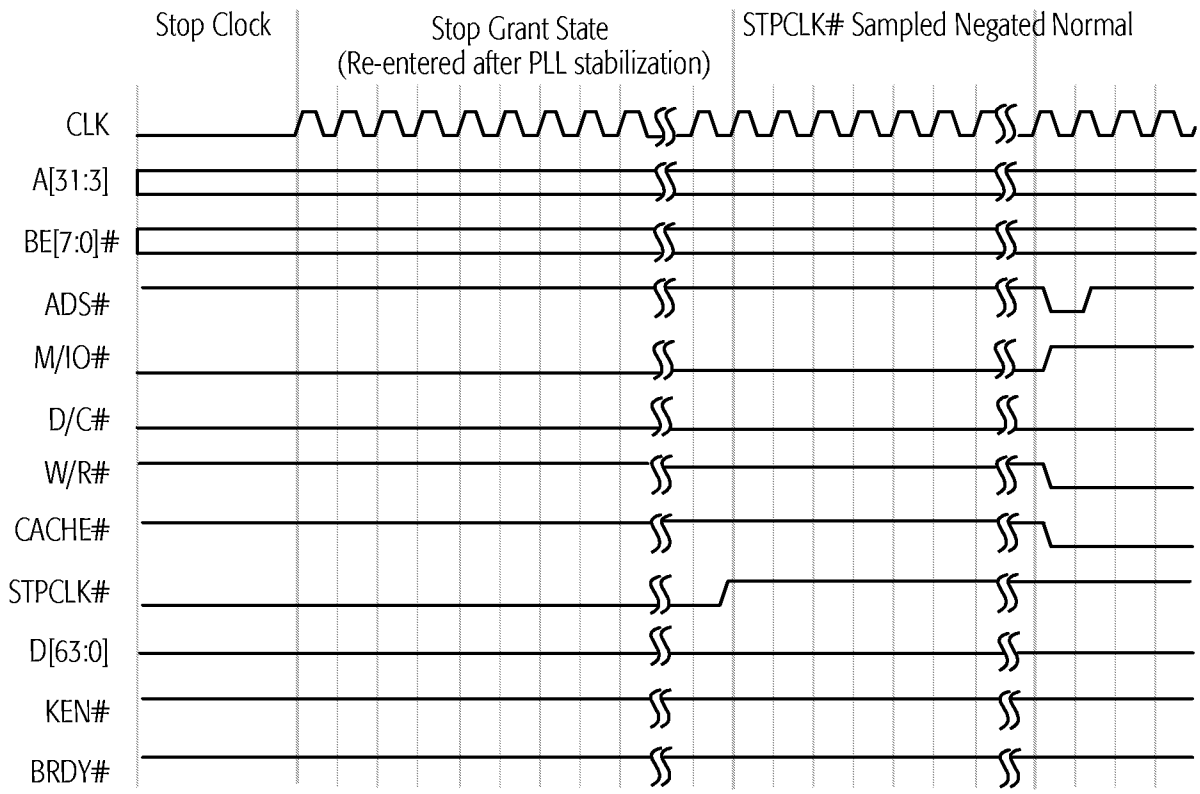

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

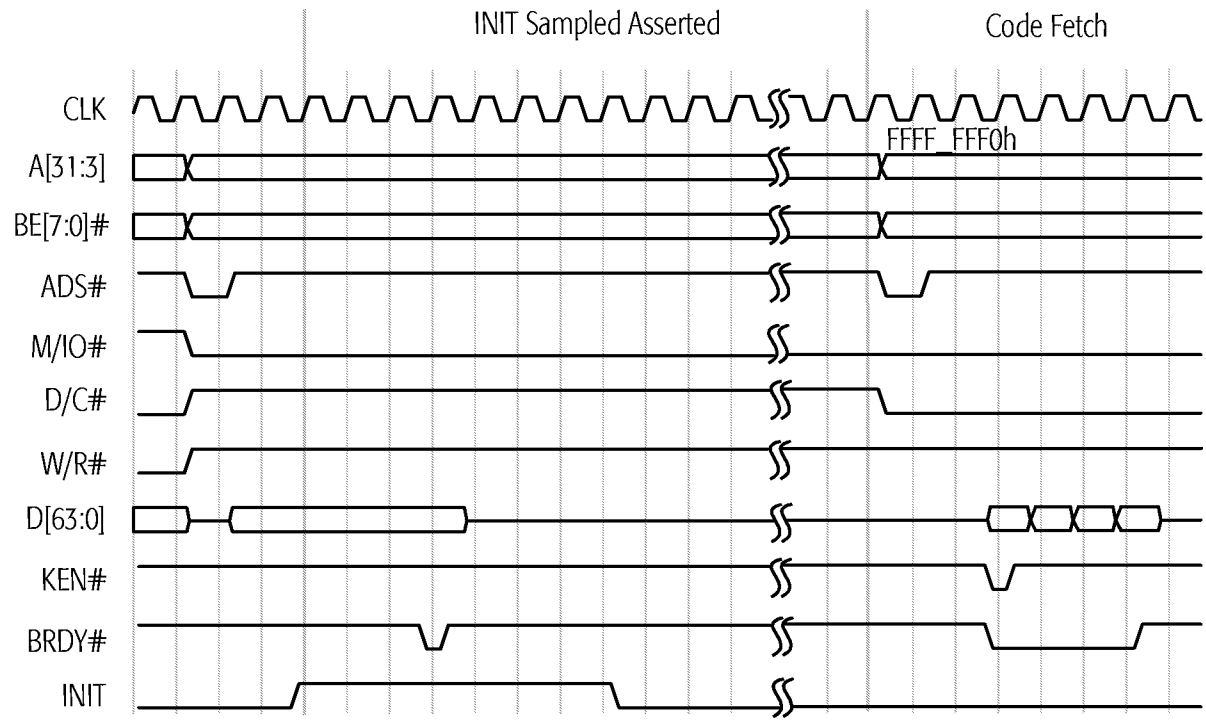

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.