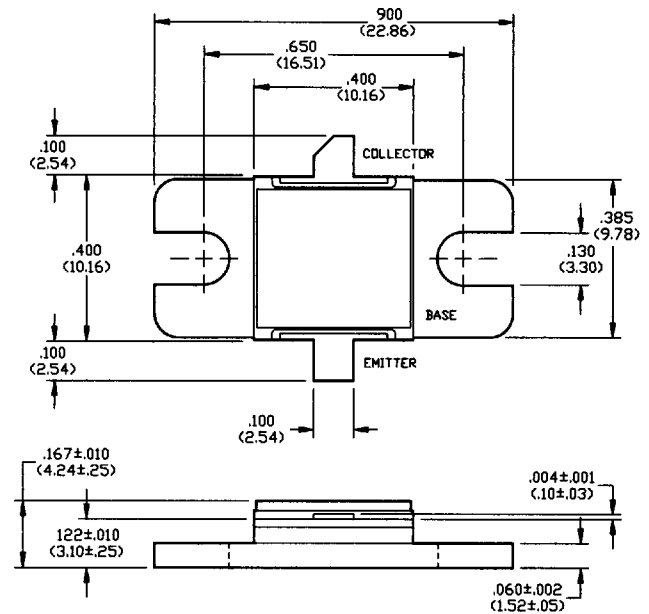


5 Watts, 2.70-2.90 GHz, 100 μ s Pulse, 10% Duty

Features

- NPN Silicon Microwave Power Transistor
- Common Base Configuration
- Broadband Class C Operation
- High Efficiency Interdigitated Geometry
- Diffused Emitter Ballasting Resistors
- Gold Metallization System
- Internal Input and Output Impedance Matching
- Hermetic Metal/Ceramic Package

Outline Drawing

UNLESS OTHERWISE NOTED, TOLERANCES ARE INCHES ± 0.005
(MILLIMETERS ± 0.13 MM)

Absolute Maximum Ratings at 25°C

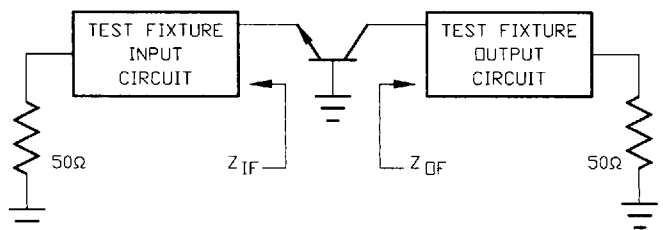
Parameter	Symbol	Rating	Units
Collector-Emitter Voltage	V_{CES}	63	V
Emitter-Base Voltage	V_{EBO}	3.0	V
Collector Current (Peak)	I_C	1.1	A
Power Dissipation	P_D	40	W
Junction Temperature	T_J	200	°C
Storage Temperature	T_{STG}	-65 to +200	°C

Electrical Characteristics at 25°C

Parameter	Symbol	Min	Max	Units	Test Conditions
Collector-Emitter Breakdown Voltage	BV_{CES}	63	-	V	$I_C=10$ mA
Collector-Emitter Leakage Current	I_{CES}	-	1.0	mA	$V_{CE}=40$ V
Thermal Resistance	$R_{TH(JC)}$	-	5.0	°C/W	$V_{CC}=36$ V, $P_{IN}=1.0$ W, $F=2.7, 2.8, 2.9$ GHz
Output Power	P_{OUT}	5.0	-	W	$V_{CC}=36$ V, $P_{IN}=1.0$ W, $F=2.7, 2.8, 2.9$ GHz
Input Return Loss	RL	6	-	dB	$V_{CC}=36$ V, $P_{IN}=1.0$ W, $F=2.7, 2.8, 2.9$ GHz
Power Gain	G_p	7.0	-	dB	$V_{CC}=36$ V, $P_{IN}=1.0$ W, $F=2.7, 2.8, 2.9$ GHz
Collector Efficiency	η_c	30	-	%	$V_{CC}=36$ V, $P_{IN}=1.0$ W, $F=2.7, 2.8, 2.9$ GHz
Load Mismatch Tolerance	VSWR-T	-	3:1	-	$V_{CC}=36$ V, $P_{IN}=1.0$ W, $F=2.7, 2.8, 2.9$ GHz
Load Mismatch Stability	VSWR-S	-	1.5:1	-	$V_{CC}=36$ V, $P_{IN}=1.0$ W, $F=2.7, 2.8, 2.9$ GHz

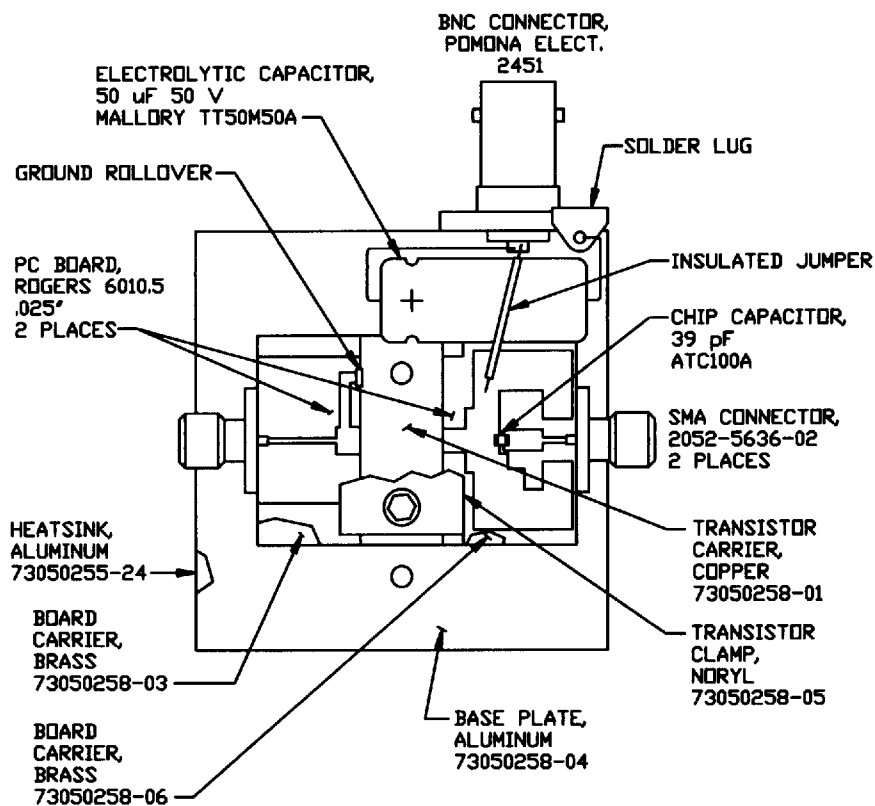
Broadband Test Fixture Impedances

F(GHz)	$Z_{IF}(\Omega)$	$Z_{OF}(\Omega)$
2.70	$40 - j12$	$25 + j3.5$
2.80	$38 - j14$	$20 + j2.0$
2.90	$35 - j16$	$16 + j2.4$



The figure consists of two diagrams illustrating the geometry of the test section. The left diagram is a cross-section showing a horizontal inlet pipe on the left, a vertical section in the middle, and a horizontal outlet pipe on the right. Dimensions are given in feet (') and degrees (°). The right diagram is a plan view showing the top-down layout of the test section, including the inlet, vertical section, and outlet, with dimensions in feet (') and degrees (°).

CIRCUIT DIMENSIONS



TOP VIEW