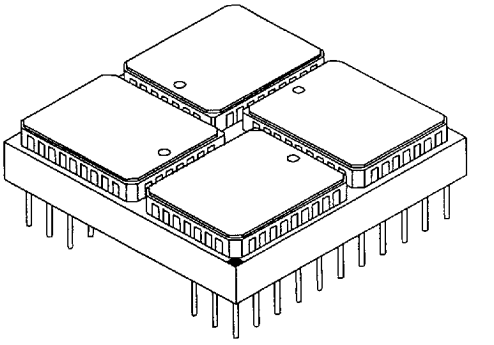
1 Megabit CMOS SRAM

DPS3232V



DESCRIPTION:

The DPS3232V is a 66-pin Pin Grid Array (PGA) consisting of four 32K x 8 SRAM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matching thermal coefficients. The LCCs are mounted in a rotary pattern resulting in the smallest possible module outline.

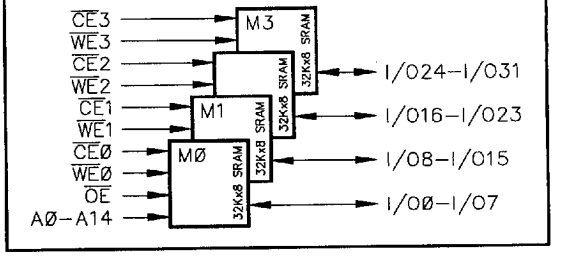
The pins have been arranged around a central 0.6" gap which can accomodate a heat rail. In this central gap is a cavity containing four 0.1µf decoupling capacitors.

Provisions have been made in the pinout for use of 1MB SRAMs, providing an upgrade path to 128Kx32 and 256Kx32, increasing the module density from four to eight times.

FEATURES:

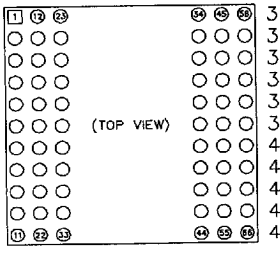
- Organizations Available:
  128K X 8, 64K X 16 or 32K X 32
- Access Times:
  25, 35, 45, 55, 70, 85, 100, 120, 150ns
- Low Data Retention: 2.0V min.
- Fully Static Operation - No clock or refresh required
- TTL-compatible
- 66-Pin PGA (Pin Grid Array) Package
- Same Package as other Versapac Versions (EEPROM, EPROM AND MIXED)
- Module Weight is 15 grams
- Module can be built with devices compliant to MIL-STD 883C

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0-A14	Address Inputs
I/O0-I/O31	Data In/Out
$\overline{CE0}$ - $\overline{CE3}$	Chip Enables
$\overline{WE0}$ - $\overline{WE3}$	Write Enables
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM



1	I/O8	12	$\overline{WE1}$	23	I/O15	34	I/O24	45	VDD	56	I/O31
2	I/O9	13	$\overline{CE1}$	24	I/O14	35	I/O25	46	$\overline{CE3}$	57	I/O3Ø
3	I/O1Ø	14	VSS	25	I/O13	36	I/O26	47	$\overline{WE3}$	58	I/O29
4	A13	15	I/O11	26	I/O12	37	A6	48	I/O27	59	I/O28
5	A14	16	A1Ø	27	$\overline{OE}$	38	A7	49	A3	6Ø	AØ
* 6	N.C.	17	A11	28	N.C.	39	N.C.	5Ø	A4	61	A1
* 7	N.C.	18	A12	29	$\overline{WEØ}$	4Ø	A8	51	A5	62	A2
8	N.C.	19	VDD	3Ø	I/O7	41	A9	52	$\overline{WE2}$	63	I/O23
9	I/OØ	2Ø	$\overline{CEØ}$	31	I/O6	42	I/O16	53	$\overline{CE2}$	64	I/O22
1Ø	I/O1	21	N.C.	32	I/O5	43	I/O17	54	VSS	65	I/O21
11	I/O2	22	I/O3	33	I/O4	44	I/O18	55	I/O19	66	I/O2Ø

* Designers should connect these pins to A15 and A16 for future upgrades.

25, 35, 45, 55, 70, 85, 100ns DC OPERATING CHARACTERISTICS: Over operating ranges

Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-10	+10	-10	+10	-10	+10	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-10	+10	-10	+10	-10	+10	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		400		400		400	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA		560		640		640	mA
I_{SB1}	Full Standby Supply Current (CMOS)	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ + 0.2V, $\overline{CE} \geq V_{DD}$ -0.2V		40		60		80	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}		160		160		160	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	2.4		2.4		2.4		V

25, 35, 45, 55, 70, 85, 100ns DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	TYP.	Max.	Unit
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2V, $\overline{CE} \geq V_{DD}$ -0.2V		0.4	4.0	mA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3V, $\overline{CE} \geq V_{DD}$ -0.2V		1.5	6.0	mA
t_{CDR}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	5			ms

120 and 150ns DC OPERATING CHARACTERISTICS: Over operating ranges

Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-10	+10	-10	+10	-10	+10	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-10	+10	-10	+10	-10	+10	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		180		180		180	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA		240		260		280	mA
I_{SB1}	Full Standby Supply Current (CMOS)	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ + 0.2V, $\overline{CE} \geq V_{DD}$ -0.2V		400		800		1200	µA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}		8		8		8	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	2.4		2.4		2.4		V

120 and 150 DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	TYP.	Max.	Unit
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2V, $\overline{CE} \geq V_{DD}$ -0.2V		6	800	µA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3V, $\overline{CE} \geq V_{DD}$ -0.2V		8	960	µA
t_{CDR}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	5			ms

RECOMMENDED OPERATING RANGE[1]						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage		-0.5[2]		0.8	V
T_A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	
		M/B	-55	+25	+125	

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	H*	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

* If $\overline{OE}$ is LOW during Write, t_{WHZ} must be observed before data is presented to the device.

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns**
Input and Output Timing Reference Levels	1.5V

** Transition between 0.8V and 2.2V.

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100 pF	except t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{OLZ}, t_{WLZ} and t_{WHZ}
2	5 pF	t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{OLZ}, t_{WLZ} and t_{WHZ}

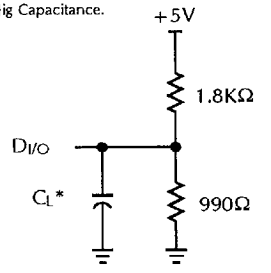
ABSOLUTE MAXIMUM RATINGS[3]		
Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} +0.5	V

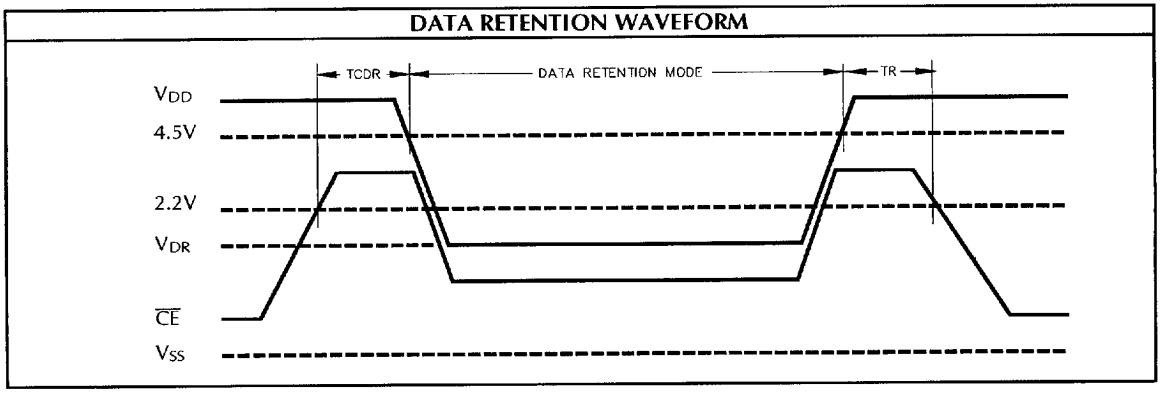
CAPACITANCE[4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	50	pF	V_{IN} = 0V
C_{CE}	Chip Enable	20		
C_{WE}	Write Enable	20		
C_{OE}	Output Enable	50		
$C_{I/O}$	Data Input/Output	20		

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -1.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL} = 2.1mA	-	0.4	V

Figure 1. Output Load

*** Including Probe and Jig Capacitance.





AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

No.	Symbol	Parameter	25ns		35ns		45ns		55ns		70ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	25		35		45		55		70		ns
2	t_{AA}	Address Access Time		25		35		45		55		70	ns
3	t_{CO}	Chip Enable to Output Valid		25		35		45		55		70	ns
4	t_{OV}	Output Enable to Output Valid		15		20		25		35		40	ns
5	t_{OH}	Output Hold from Address Change	3		3		3		3		3		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 6]	5		5		5		5		5		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	0		0		5		5		5		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 6]		15		15		20		25		30	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		15		15		20		25		30	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [7]

No.	Symbol	Parameter	25ns		35ns		45ns		55ns		70ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	25		35		45		55		70		ns
11	t_{AW}	Address Valid to End of Write	20		30		40		50		65		ns
12	t_{CW}	Chip Enable to End of Write	20		30		40		50		65		ns
13	t_{DW}	Data Valid to End of Write	15		20		25		25		30		ns
14	t_{DH}	Data Hold Time	3		3		3		3		3		ns
15	t_{WP}	Write Pulse Width	20		30		35		40		45		ns
16	t_{AS}	Address Set-up Time*	0		0		0		0		0		ns
17	t_{AH}	Address Hold Time	0		0		0		0		0		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		15		15		15		20		25	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4, 6]	5		5		5		5		5		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

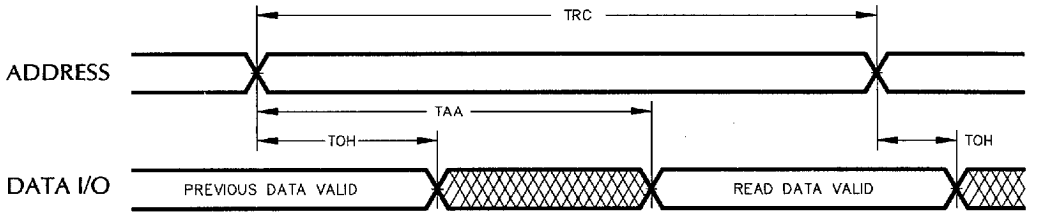
No.	Symbol	Parameter	85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	85		100		120		150		ns
2	t_{AA}	Address Access Time		85		100		120		150	ns
3	t_{CO}	Chip Enable to Output Valid		85		100		120		150	ns
4	t_{OV}	Output Enable to Output Valid		60		60		60		70	ns
5	t_{OH}	Output Hold from Address Change	5		10		10		10		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 6]	10		10		10		10		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	5		5		5		5		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 6]		30		35		40		50	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		30		35		40		50	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [7]

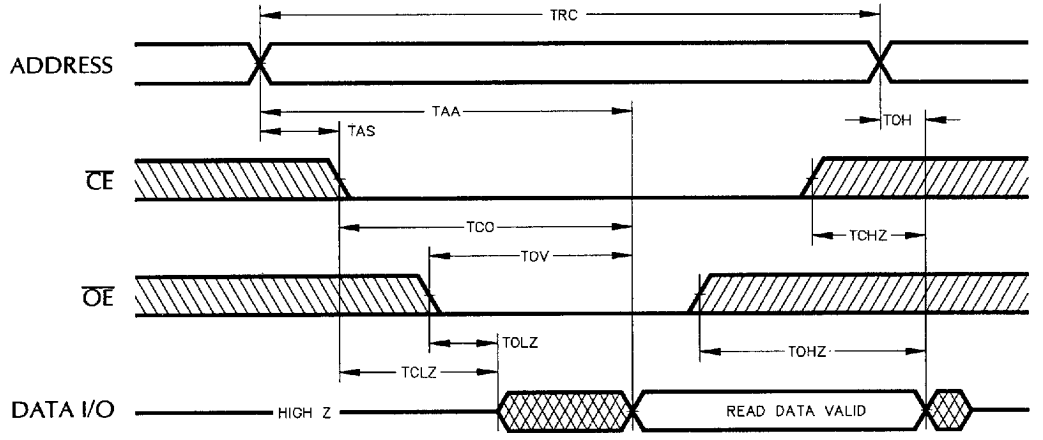
No.	Symbol	Parameter	85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	85		100		120		150		ns
11	t_{AW}	Address Valid to End of Write	75		90		100		120		ns
12	t_{CW}	Chip Enable to End of Write	75		90		100		120		ns
13	t_{DW}	Data Valid to End of Write	35		40		50		60		ns
14	t_{DH}	Data Hold Time	0		0		0		0		ns
15	t_{WP}	Write Pulse Width	65		75		90		100		ns
16	t_{AS}	Address Set-up Time*	0		0		0		0		ns
17	t_{AH}	Address Hold Time	0		0		0		0		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		30		35		40		50	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4, 6]	5		5		5		5		ns

* Valid for both Read and Write Cycles.

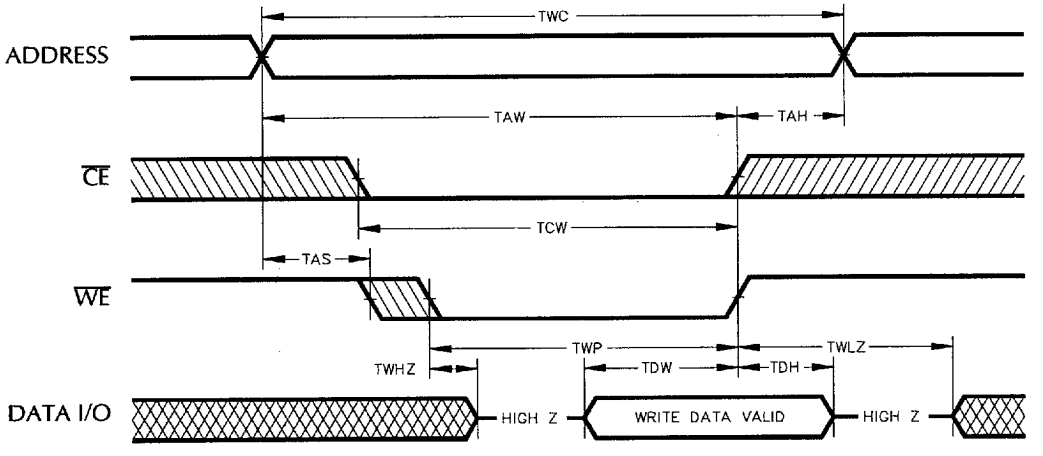
READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



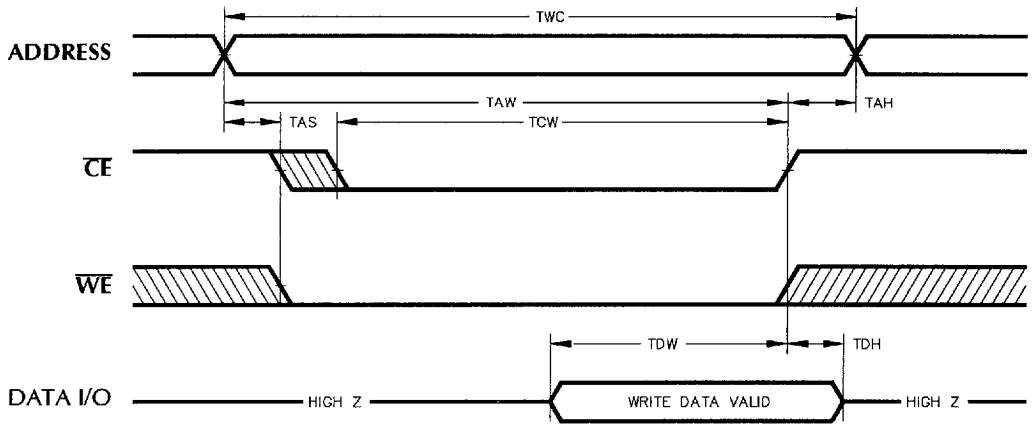
READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.



WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is HIGH.



NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

WAVEFORM KEY

Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

ORDERING INFORMATION

DP S3232 V – XXX X

PREFIX | DEVICE TYPE | PACKAGE | SPEED | GRADE

C	COMMERCIAL	Ø°C to +7Ø°C
I	INDUSTRIAL	–4Ø°C to +85°C
M	MILITARY	–55°C to +125°C
B *	MIL–PROCESSED	–55°C to +125°C

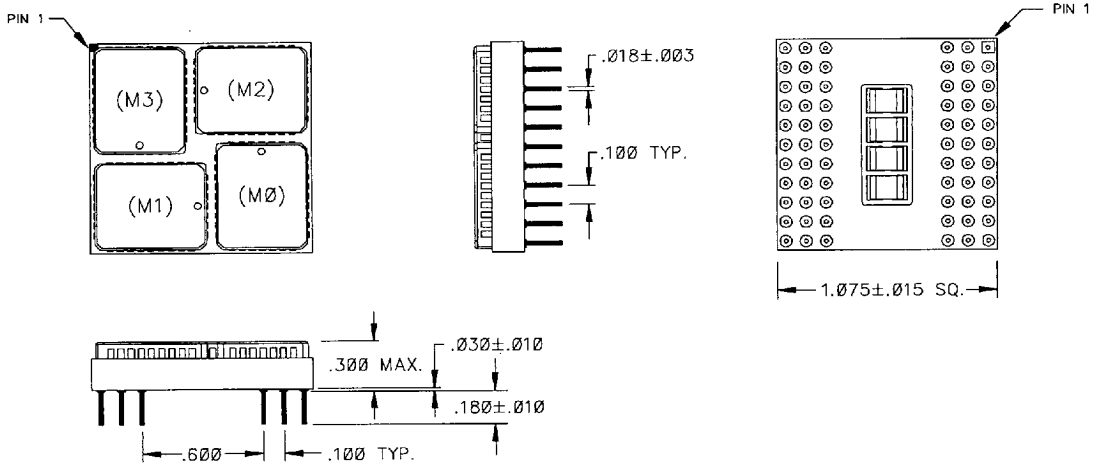
25	25ns
35	35ns
45	45ns
55	55ns
7Ø	7Ønns
85	85ns
1ØØ	1ØØns
12Ø	12Ønns
15Ø	15Ønns

V 66–PIN PGA VERSAPAC

CMOS SRAM 128KX8, 64KX16 OR 32KX32

* B grade modules can be constructed with 883 devices.

MECHANICAL DRAWING



Dense-Pac Microsystems, Inc.

7321 Lincoln Way ◆ Garden Grove, California 92641-1428

(714) 898-0007 ◆ (800) 642-4477 (Outside CA) ◆ FAX: (714) 897-1772

2759415 0001218 T36